



## 2°C Accurate Digital Temperature Sensor with SPI™ Interface

### FEATURES

- DIGITAL OUTPUT: SPI-Compatible Interface
- RESOLUTION: 10-Bit, 0.25°C
- ACCURACY:  
±2.0°C (max) from –25°C to +85°C  
±2.5°C (max) from –40°C to +125°C
- LOW QUIESCENT CURRENT: 50µA (max)
- WIDE SUPPLY RANGE: 2.7V to 5.5V
- TINY SOT23-6 PACKAGE
- OPERATION FROM –40°C to +125°C

### APPLICATIONS

- BASE STATION EQUIPMENT
- COMPUTER PERIPHERAL THERMAL PROTECTION
- NOTEBOOK COMPUTERS
- DATA ACQUISITION SYSTEMS
- TELECOM EQUIPMENT
- OFFICE MACHINES

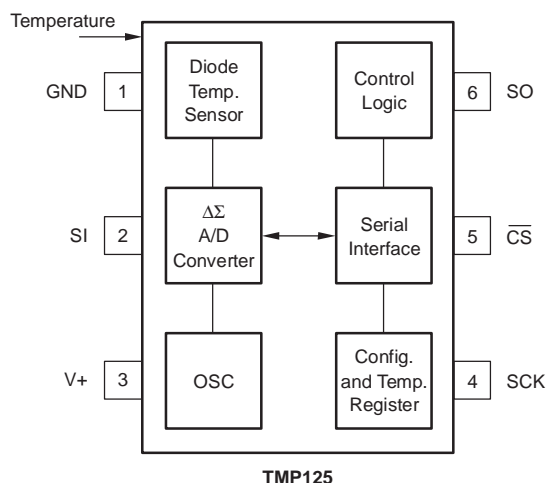
### TMP125 RELATED PRODUCTS

FEATURES	PRODUCT
2°C Digital Temp Sensors with Two-Wire Interface	TMP100/101
1.5°C Digital Temp Sensors with Two-Wire Interface	TMP75/175
1.5°C Digital Temp Sensors with SPI	TMP121/123
1.5°C Programmable Digital Temp Sensors with SPI	TMP122/124

### DESCRIPTION

The TMP125 is an SPI-compatible temperature sensor available in the tiny SOT23-6 package. Requiring no external components, the TMP125 is capable of measuring temperatures within 2°C of accuracy over a temperature range of –25°C to +85°C and 2.5°C of accuracy over –40°C to +125°C. Low supply current, and a supply range from 2.7V to 5.5V, make the TMP125 an excellent candidate for low-power applications.

The TMP125 is ideal for extended thermal measurement in a variety of communication, computer, consumer, environmental, industrial, and instrumentation applications.



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### ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	+7V
Input Voltage(2)	-0.3V to +7V
Input Current	±10mA
Output Short Circuit(3)	Continuous
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-60°C to +150°C
Junction Temperature (T <sub>J</sub> max)	+150°C
Lead Temperature (soldering)	+300°C
ESD Rating (Human Body Model)	4000V
(Charged Device Model)	1000V



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

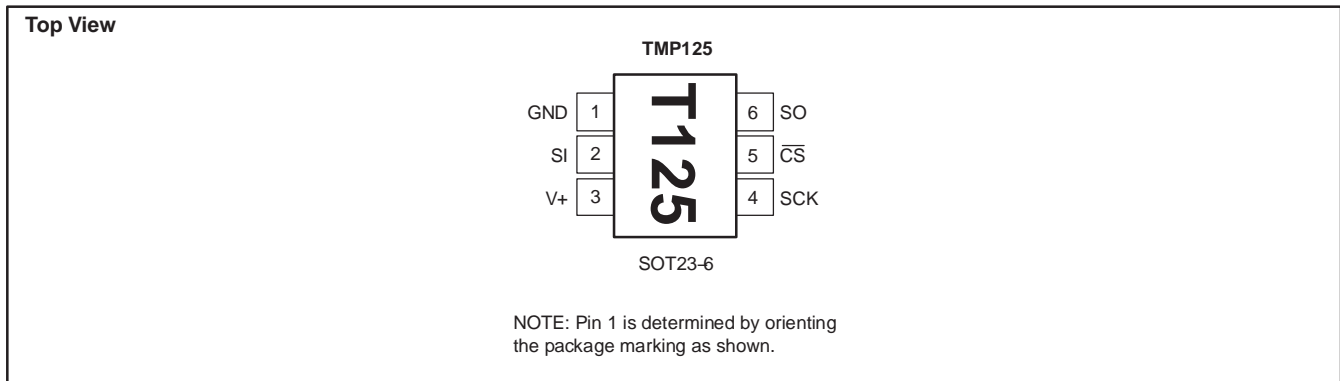
- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
- (3) Short-circuit to ground.

### ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
TMP125	SOT23-6	DBV	T125

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

### PIN CONFIGURATION



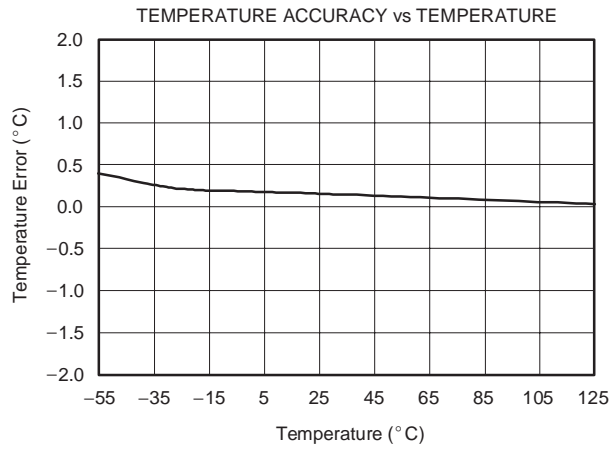
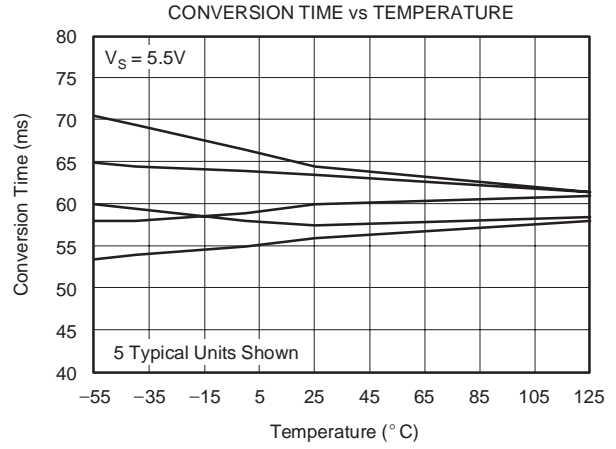
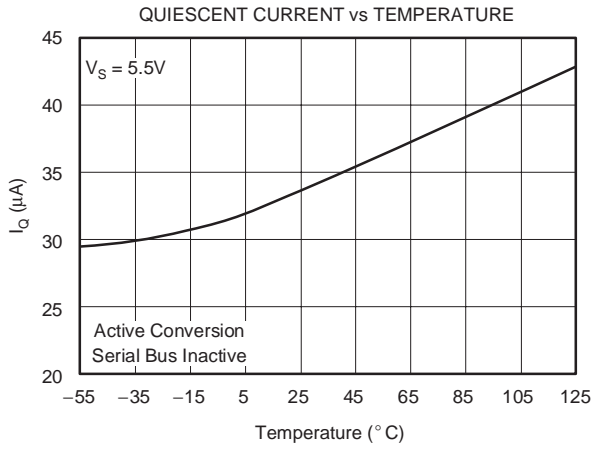
**ELECTRICAL CHARACTERISTICS**

 At  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  and  $V_S = +2.7\text{V}$  to  $5.5\text{V}$ , unless otherwise noted.

PARAMETER	CONDITIONS	TMP125			UNIT
		MIN	TYP	MAX	
<b>TEMPERATURE INPUT</b>					
Range		-40		+125	$^\circ\text{C}$
Accuracy (temperature error)	-25 $^\circ\text{C}$ to +85 $^\circ\text{C}$		$\pm 0.5$	$\pm 2.0$	$^\circ\text{C}$
	-40 $^\circ\text{C}$ to +125 $^\circ\text{C}$		$\pm 1.0$	$\pm 2.5$	$^\circ\text{C}$
Resolution			10		Bits
Temperature Measurement Noise			0.1		LSB
<b>DIGITAL INPUT/OUTPUT</b>					
Input Logic Levels:					
$V_{IH}$		0.7(V+)			V
$V_{IL}$				0.3(V+)	V
Input Current, SI, SCK, $\overline{\text{CS}}$	$I_{IN}$ 0V = $V_{IN} = V+$			$\pm 1$	$\mu\text{A}$
Output Logic Levels:					
$V_{OL\ SO}$	$I_{SINK} = 3\text{mA}$			0.4	V
$V_{OH\ SO}$	$I_{SOURCE} = 2\text{mA}$	(V+)-0.4			V
Input Capacitance, SI, SCK, $\overline{\text{CS}}$			2.5		pF
Conversion Time	10-Bit		60		ms
Update Rate			120		ms
<b>POWER SUPPLY</b>					
Operating Range		2.7		5.5	V
Quiescent Current, at $T_A = 25^\circ\text{C}$	$I_Q$ Serial Bus Inactive		36	50	$\mu\text{A}$
over Temperature	-40 $^\circ\text{C}$ to +125 $^\circ\text{C}$			60	$\mu\text{A}$
Shutdown Current			0.1	1	$\mu\text{A}$
over Temperature				1	$\mu\text{A}$
<b>TEMPERATURE RANGE</b>					
Specified Range		-40		+125	$^\circ\text{C}$
Operating Range		-55		+125	$^\circ\text{C}$
Storage Range		-60		+150	$^\circ\text{C}$
Thermal Resistance	$\theta_{JA}$ SOT23-6 Surface-Mount		200		$^\circ\text{C}/\text{W}$

### TYPICAL CHARACTERISTICS

At  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  and  $V_S = +2.7\text{V}$  to  $5.5\text{V}$ , unless otherwise noted.



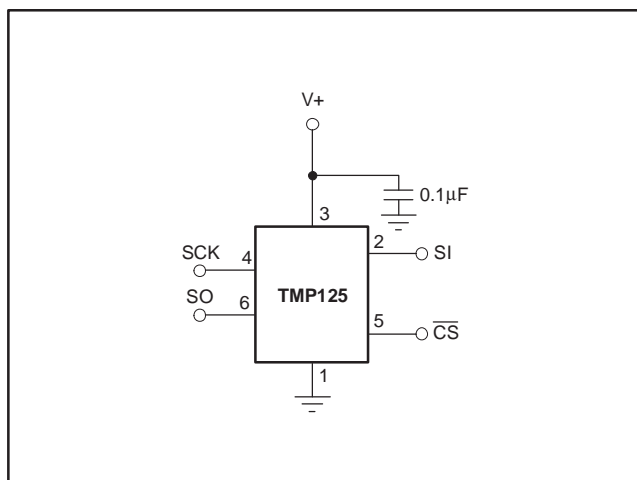
## APPLICATIONS

The TMP125 10-bit, read-only digital temperature sensor is optimal for thermal management and thermal protection applications. The TMP125 is specified for a temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , with operation extending down to  $-55^{\circ}\text{C}$ . It is specified for a supply voltage range of 2.7V to 5.5V, and also features a hardware shutdown to provide power savings. Quiescent current is reduced to  $1\mu\text{A}$  during analog shutdown.

The TMP125 communicates through a serial interface that is SPI-compatible. Temperature is converted to a 10-bit data word with  $0.25^{\circ}\text{C}$  resolution. The TMP125 is optimal for low-power applications, with a 120ms conversion period for reduced power consumption.

The sensing device of the TMP125 is the chip itself. Thermal paths run through the package leads as well as the plastic package, and the lower thermal resistance of metal causes the leads to provide the primary thermal path.

The TMP125 requires no external components for operation, though a  $0.1\mu\text{F}$  supply bypass capacitor is recommended. Figure 1 shows typical connection for the TMP125.



**Figure 1. Typical Connections for the TMP125**

### COMMUNICATING WITH THE TMP125

The TMP125 continuously converts temperatures to digital data. Temperature data is read by pulling  $\overline{\text{CS}}$  low. Once  $\overline{\text{CS}}$  is pulled low, temperature data from the last completed conversion prior to dropping  $\overline{\text{CS}}$  is latched into the shift register and clocked out at SO on the falling SCK edge. The 16-bit data word is clocked out sign bit first, followed by the MSB. The SI pin is used to put the device into shutdown mode. To enter shutdown mode, SI must be high on the rising edge of the third bit of SCK (see Figure 3). Also, all 16 bits must be clocked to allow shutdown on the TMP125. To bring the device out of

shutdown, perform a 16-clock communication with SI set to logic low. The 16-clock communication is the same as the Data Read shown in Figure 3, except that the data on SO will be the last conversion prior to putting the device into shutdown mode. Note that SO is only used to control the shutdown function; if not using this function, connect this pin to ground.

The one-shot command can be used to force a single conversion. When the command is issued, the part will perform a single conversion and then go into shutdown mode. After the conversion is complete, the conversion result should be read with the power-down bit high (see Figure 3) if you do not want to start a new conversion.

The TMP125 will go into idle mode for 60ms, requiring only  $20\mu\text{A}$  of current. A new conversion begins every 120ms. Figure 2 describes the conversion timing for the TMP125.

### TEMPERATURE REGISTER

The Temperature Register of the TMP125 is a 16-bit, read-only register that stores the output of the most recent conversion. However, temperature is represented by only 10-bits, which are in signed two's complement format. The first bit of the Temperature Register, D15, is a leading zero. Bits D14 and D5 are used to indicate temperature. Bits D4 to D0 are the same as D5 (see Table 1). Data format for temperature is summarized in Table 2. When calculating the signed two's complement temperature value, be sure to use only the 10 data bits.

Following power-up or reset, the Temperature Register will read  $0^{\circ}\text{C}$  until the first conversion is complete.

<b>D15</b>	<b>D14</b>	<b>D13</b>	<b>D12</b>	<b>D11</b>	<b>D10</b>	<b>D9</b>	<b>D8</b>
0	T9	T8	T7	T6	T5	T4	T3
<b>D7</b>	<b>D6</b>	<b>D5</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>
T2	T1	T0	T0	T0	T0	T0	T0

**Table 1. Temperature Register**

TEMPERATURE ( $^{\circ}\text{C}$ )	DIGITAL OUTPUT D14...D5
+127	01 1111 1100
+125	01 1111 0100
+100	01 1001 0000
+75	01 0010 1100
+50	00 1100 1000
+25	00 0110 0100
+10	00 0010 1000
+0.25	00 0000 0001
0	00 0000 0000
-0.25	11 1111 1111
-25	11 1001 1100
-50	11 0011 1000
-55	11 0010 0100

**Table 2. Temperature Data Format**

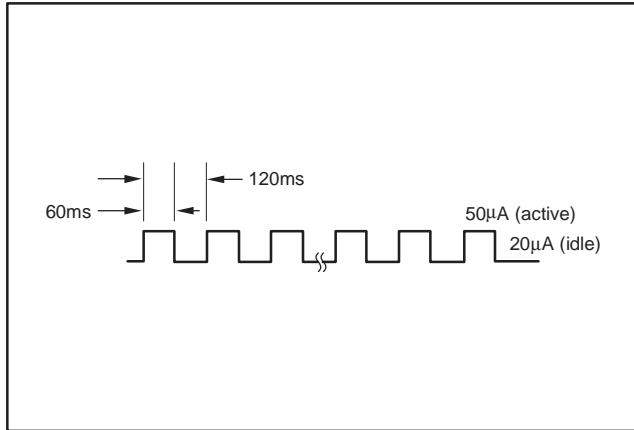


Figure 2. Conversion Time and Period

Timing Diagrams

The TMP125 is SPI-compatible. Figure 3 and Figure 4 describe the output data of the TMP125. Figure 5, Figure 6, and Figure 7 describe the various timing requirements, with parameters defined in Table 3.

PARAMETER	MIN	MAX	UNITS
SCK Period	$t_1$	100	ns
Data In to Rising Edge SCK Setup Time	$t_2$	20	ns
SCK Falling Edge to Output Data Delay	$t_3$	30	ns
SCK Rising Edge to Input Data Hold Time	$t_4$	20	ns
$\overline{CS}$ to Rising Edge SCK Set-Up Time	$t_5$	40	ns
$\overline{CS}$ to Output Data Delay	$t_6$	30	ns
$\overline{CS}$ Rising Edge to Output High Impedance	$t_7$	30	ns

Table 3. Timing Description

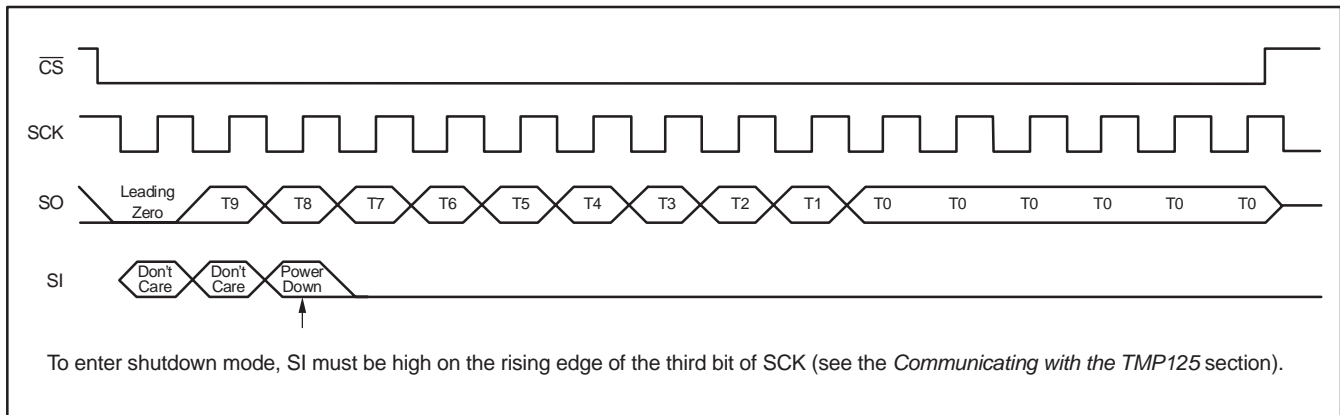


Figure 3. Data READ

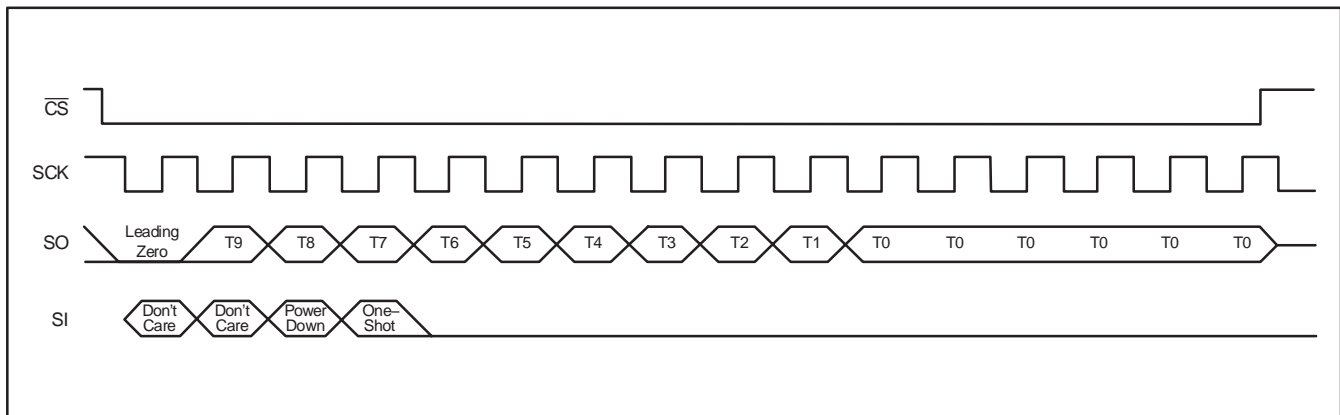
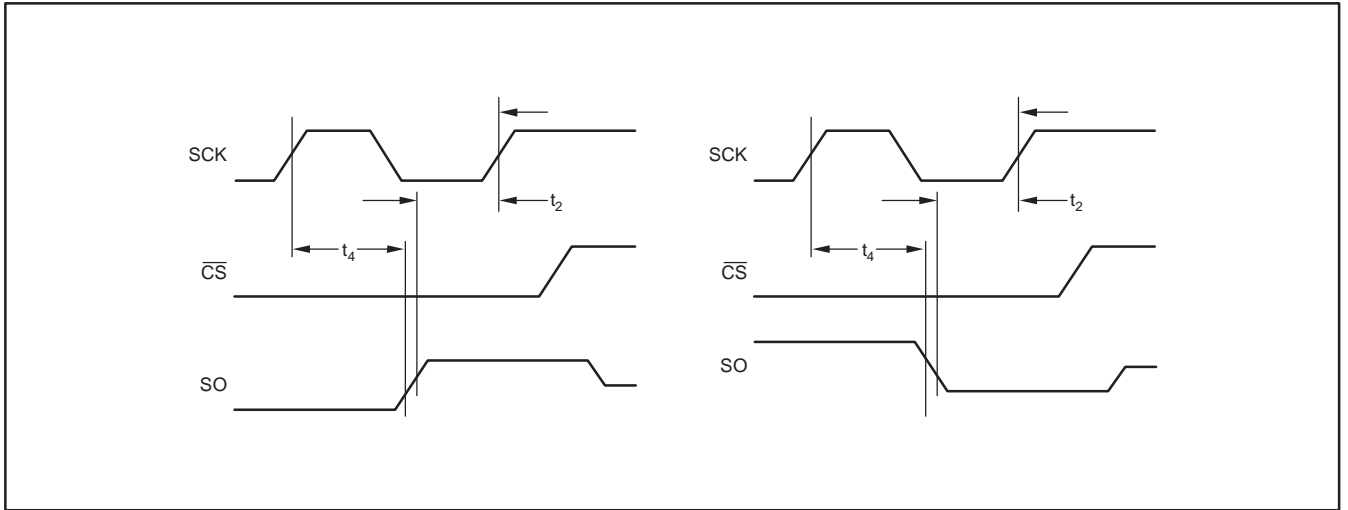
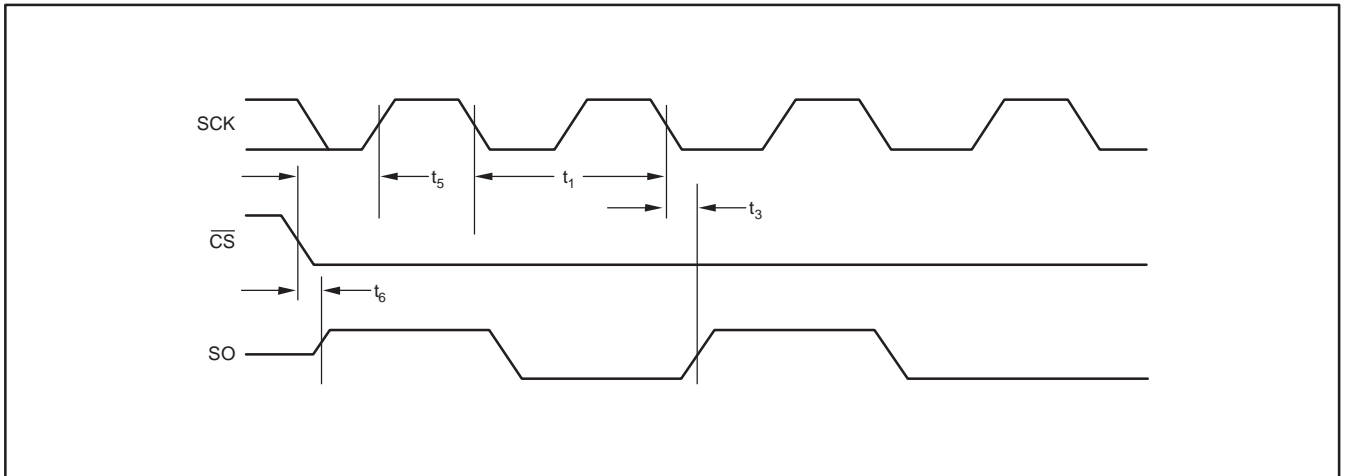


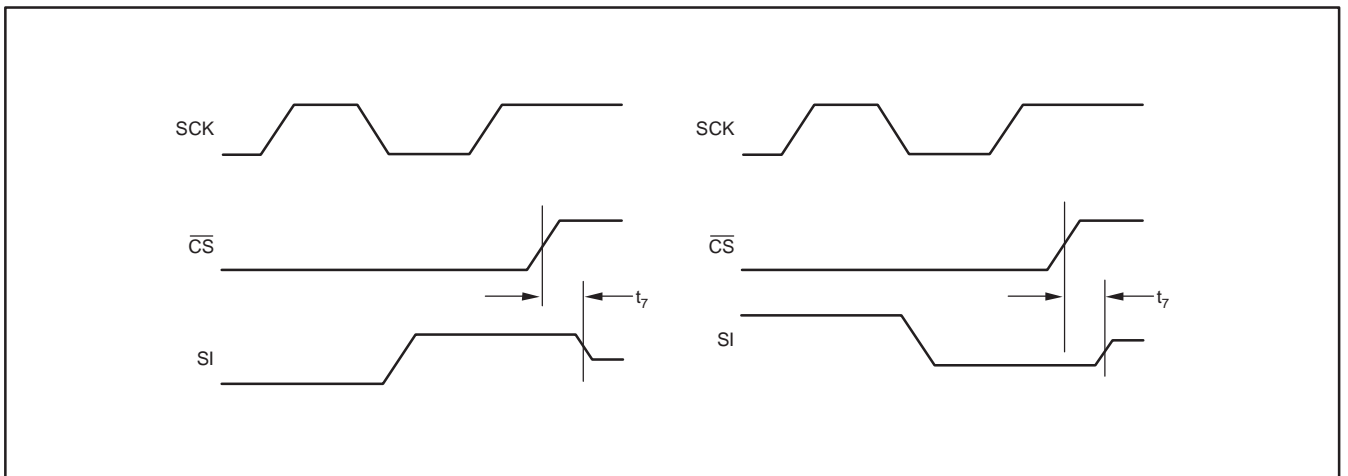
Figure 4. One-Shot Command



**Figure 5. Input Data Timing Diagram**



**Figure 6. Output Data Timing Diagram**



**Figure 7. High Impedance Output Timing Diagram**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA00444AIDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T125	<a href="#">Samples</a>
TMP125AIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T125	<a href="#">Samples</a>
TMP125AIDBVRG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T125	<a href="#">Samples</a>
TMP125AIDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T125	<a href="#">Samples</a>
TMP125AIDBVTG4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T125	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP125AIDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TMP125AIDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP125AIDBVR	SOT-23	DBV	6	3000	445.0	220.0	345.0
TMP125AIDBVT	SOT-23	DBV	6	250	445.0	220.0	345.0



# EXAMPLE BOARD LAYOUT

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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