

TMP300 1.8-V, Resistor-Programmable Temperature Switch and Analog Out Temperature Sensor in SC70

1 Features

- Accuracy: $\pm 1^\circ\text{C}$ (typical at $+25^\circ\text{C}$)
- Programmable trip point
- Programmable hysteresis: $5^\circ\text{C}/10^\circ\text{C}$
- Open-drain outputs
- Low power: $110\ \mu\text{A}$ (maximum)
- Wide voltage range: $+1.8\ \text{V}$ to $+18\ \text{V}$
- Temperature range: -40°C to $+125^\circ\text{C}$
- Analog out: $10\text{mV}/^\circ\text{C}$
- SC70-6 and SOT23-6 packages

2 Applications

- Power-supply systems
- DC-DC modules
- Thermal monitoring
- Electronic protection systems

3 Description

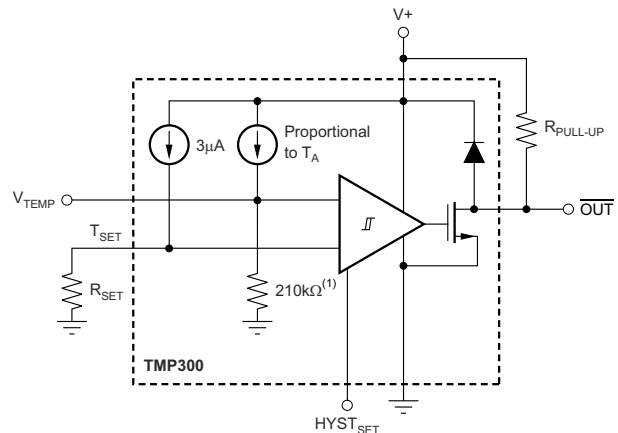
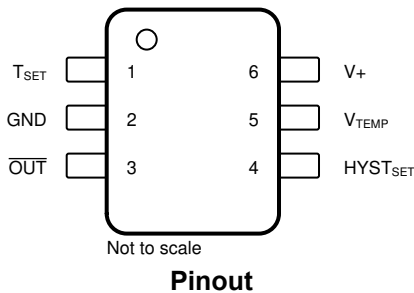
The TMP300 is a low-power, resistor-programmable, digital output temperature switch. The device allows a threshold point to be set by adding an external resistor. Two levels of hysteresis are available. The TMP300 has a V_{TEMP} analog output that can be used as a testing point or in temperature-compensation loops.

Available in two micropackages with proven thermal characteristics, low current consumption, and a supply voltage as low as $1.8\ \text{V}$, the TMP300 is designed for power-sensitive systems that require simple and reliable thermal management.

Package Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMP300	SOT-23 (6)	2.90 mm × 1.60 mm
	SC70 (6)	2.00 mm × 1.25 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



NOTE: Thin-film resistor with approximately 10% accuracy; however, this accuracy error is trimmed out at the factory.

Application Schematic



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4 Revision History

Changes from Revision E (December 2018) to Revision F (January 2023) Page

- Updated the numbering format for tables, figures, and cross-references throughout the document..... **1**
- Changed *Device Information* table to *Package Information* **1**
- Added parameter to the *Absolute Maximum Ratings* table: input current into any pin..... **4**

Changes from Revision D (January 2016) to Revision E (December 2018) Page

- Added *Pin Configuration and Functions* section **3**

Changes from Revision C (January 2011) to Revision D (January 2016) Page

- Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section..... **1**
- Changed *Temperature Range* Features bullet **1**
- Added package names to pinout **1**
- Deleted *Ordering Information* table **4**
- Changed Temperature Range, *TA*, *Functional Range* parameter name in *Electrical Characteristics* table..... **5**
- Added footnote 4 to *Electrical Characteristics* table **5**

Changes from Revision B (November 2008) to Revision C (January 2011) Page

- Deleted second sentence from *Description* section..... **1**
- Added TMP300B grade device specifications to *Electrical Characteristics* table..... **5**

5 Pin Configuration and Functions

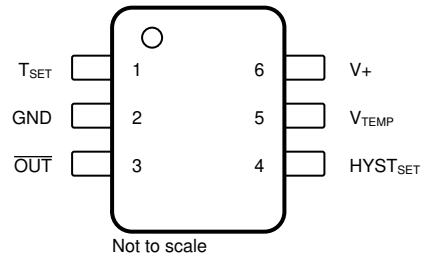


Figure 5-1. DCK and DBV Package 6-Pin SOT-23 and SC70 Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
T _{SET}	1	I	Temperature set pin. Connects to a resistor to set the trip point
GND	2	—	Ground
OUT	3	O	Trip output
HYST _{SET}	4	I	Hysteresis Set. Connect to Ground for 5°C hysteresis or connect to V+ for 10°C hysteresis
V _{TEMP}	5	I	Analog Temperature output
V+	6	O	Supply voltage: 1.8 V to 18 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V+	Supply voltage		+18	V
	Signal input pins, voltage ⁽²⁾	-0.5	(V+) + 0.5	V
	Signal input pins, current ⁽²⁾	-10	10	mA
	Input current into any pin		10	mA
I _{SC}	Output short-circuit ⁽³⁾	Continuous		
	Open-drain output		(V+) + 0.5	V
T _A	Functional temperature	-40	+150	°C
T _{stg}	Storage temperature	-55	+150	°C
T _J	Junction temperature		+150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
- (3) Short-circuit to ground.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM)	±4000
		Charged-device model (CDM)	±1000

6.3 Electrical Characteristics

At $V_S = 3.3\text{ V}$ and $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	TMP300			TMP300B			UNIT	
		MIN ⁽¹⁾	TYP ⁽¹⁾	MAX ⁽¹⁾	MIN	TYP	MAX		
TEMPERATURE MEASUREMENT									
Measurement range	$V_S = 2.35\text{ V}$ to 18 V	-40		+125	-40		+125	°C	
	$V_S = 1.8\text{ V}$ to 2.35 V	-40		$100 \times (V_S - 0.95)$	-40		$100 \times (V_S - 0.95)$		
TRIP POINT									
Total accuracy	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		± 2	± 4 ⁽³⁾		± 2	± 6	°C	
R _{SET} equation	T_C is in °C		$R_{SET} = 10(50 + T_C)/3$			$R_{SET} = 10(50 + T_C)/3$			kΩ
HYSTERESIS SET INPUT									
LOW threshold				0.4			0.4	V	
HIGH threshold		$V_S - 0.4$			$V_S - 0.4$			V	
Threshold hysteresis	HYST _{SET} = GND			5			5	°C	
	HYST _{SET} = V_S			10			10		
DIGITAL OUTPUT									
Logic family			CMOS			CMOS			
Open-drain leakage current	OUT = V_S			10			10	μA	
V _{OL} Logic levels	$V_S = 1.8\text{ V}$ to 18 V , I _{SINK} = 5 mA			0.3			0.3	V	
ANALOG OUTPUT									
Accuracy			± 2	± 3		± 2	± 5	°C	
Temperature sensitivity			10			10		mV/°C	
Output voltage	$T_A = +25^\circ\text{C}$	720	750	780	720	750	780	mV	
V _{TEMP} pin output resistance			210			210		kΩ	
POWER SUPPLY									
I _Q Quiescent current ⁽²⁾	$V_S = 1.8\text{ V}$ to 18 V , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			110			110	μA	
TEMPERATURE RANGE									
T _A	Specified range	$V_S = 2.35\text{ V}$ to 18 V	-40		+125	-40		+125	°C
		$V_S = 1.8\text{ V}$ to 2.35 V	-40		$100 \times (V_S - 0.95)$	-40		$100 \times (V_S - 0.95)$	
	Functional range ⁽⁴⁾	$V_S = 2.35\text{ V}$ to 18 V	-40		+150	-40		+150	
		$V_S = 1.8\text{ V}$ to 2.35 V	-50		$100 \times (V_S - 0.95)$	-50		$100 \times (V_S - 0.95)$	
θ _{JA} Thermal resistance	SC70			250			250	°C/W	
	SOT23-6			180			180		

- (1) 100% of production is tested at $T_A = +85^\circ\text{C}$. Specifications over temperature range are ensured by design.
- (2) See [Figure 6-1](#) for typical quiescent current.
- (3) Shaded cells indicate characteristic performance difference.
- (4) The TMP300 is functional over this range and no indication of performance is implied.

6.4 Typical Characteristics

At $V_S = 5\text{ V}$, unless otherwise noted.

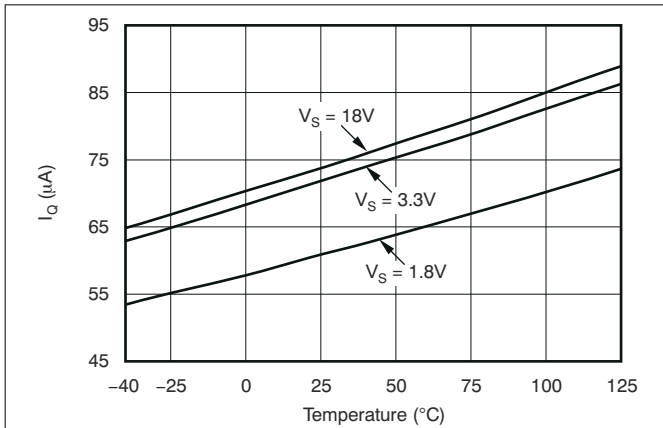


Figure 6-1. Quiescent Current Over Temperature and Supply

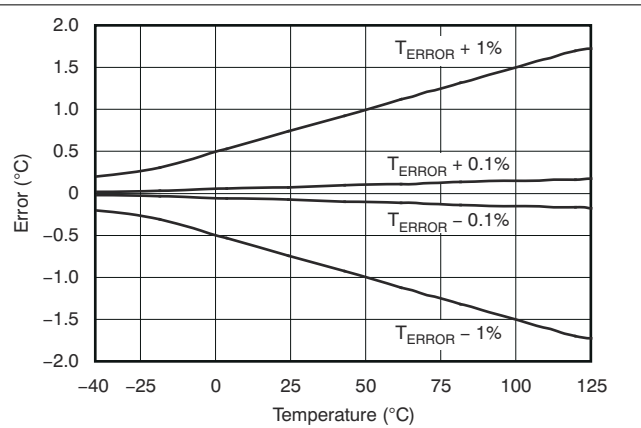


Figure 6-2. R_{SET} Shift Resulting From R_{SET} Tolerance

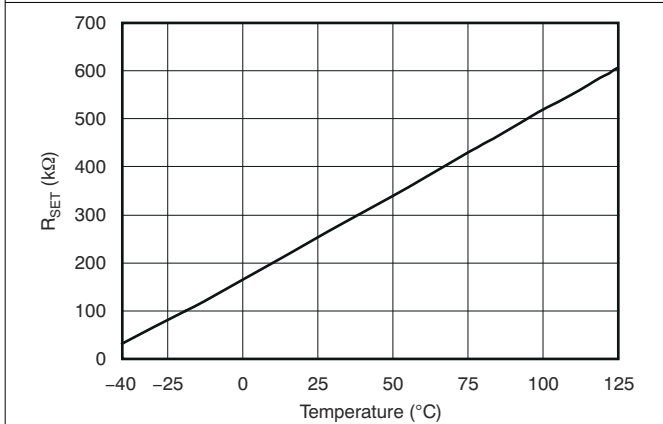


Figure 6-3. R_{SET} vs Temperature

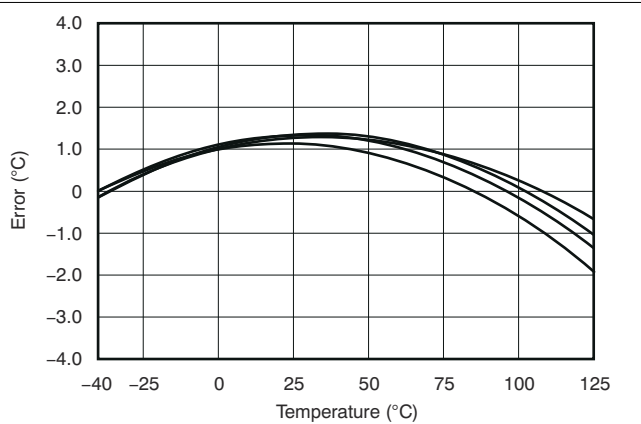


Figure 6-4. Typical Trip Error

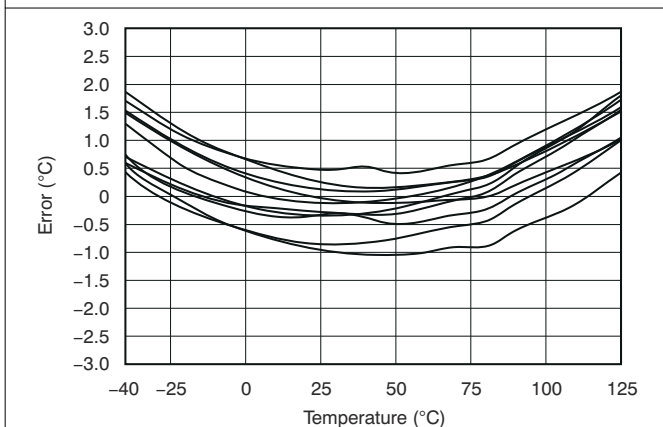


Figure 6-5. Typical Analog Output Error

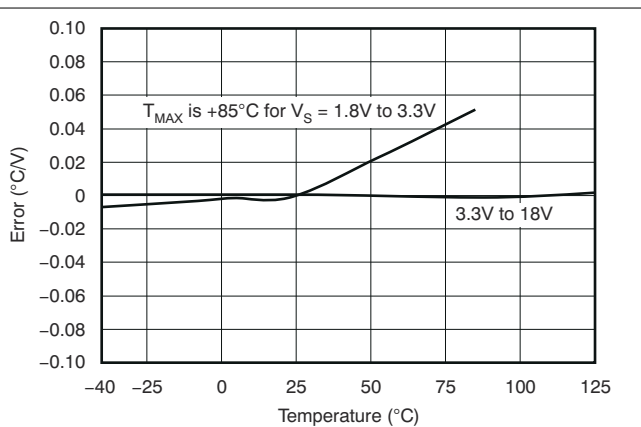


Figure 6-6. Analog PSR Over Temperature

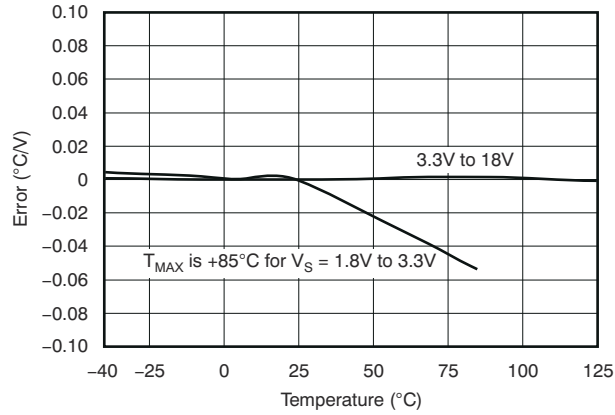


Figure 6-7. Trip PSR Over Temperature

7 Detailed Description

7.1 Overview

The TMP300 is a thermal sensor designed for overtemperature protection circuits in electronic systems. The TMP300 uses a set resistor to program the trip temperature of the digital output. An additional high-impedance (210 kΩ) analog voltage output provides the temperature reading.

7.2 Feature Description

7.2.1 Calculating R_{SET}

The set resistor (R_{SET}) provides a threshold voltage for the comparator input. The TMP300 trips when the V_{TEMP} pin exceeds the T_{SET} voltage. The value of the set resistor is determined by the analog output function and the 3-μA internal bias current.

To set the TMP300 to trip at a preset value, calculate the R_{SET} resistor value according to [Equation 1](#) or [Equation 2](#):

$$R_{SET} = \frac{(T_{SET} \times 0.01 + 0.5)}{3e^{-6}} \tag{1}$$

where

- T_{SET} is in °C; or

$$R_{SET} \text{ in k}\Omega = \frac{10(50 + T_{SET})}{3} \tag{2}$$

where

- T_{SET} is in °C.

7.2.2 Using V_{TEMP} to Trip the Digital Output

The analog voltage output can also serve as a voltage input that forces a trip of the digital output to simulate a thermal event. This simulation facilitates easy system design and test of thermal safety circuits, as shown in [Figure 7-1](#).

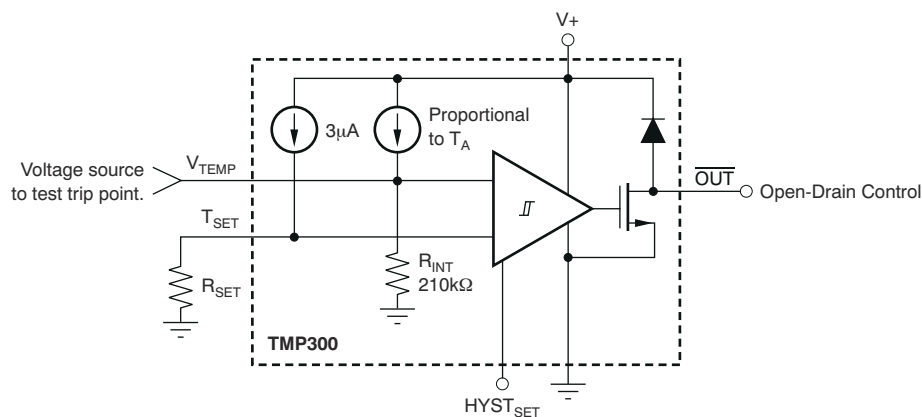


Figure 7-1. Applying Voltage to Trip Digital Output

7.2.3 Analog Temperature Output

The analog out or V_{TEMP} pin is high-impedance (210 k Ω). Avoid loading this pin to prevent degrading the analog out value or trip point. Buffer the output of this pin when used for direct thermal measurement. Figure 7-2 shows buffering of the analog output signal.

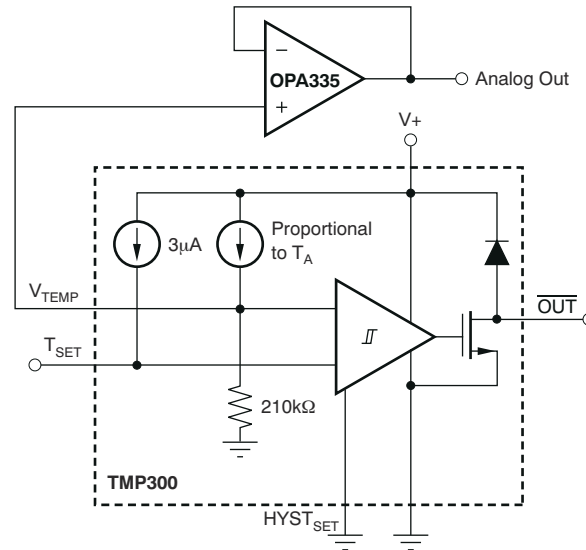


Figure 7-2. Buffering the Analog Output Signal

7.2.4 Using a DAC to Set the Trip Point

The trip point is easily converted by changing the digital-to-analog converter (DAC) code. This technique can be useful for control loops where a large thermal mass is being brought up to the set temperature and the \overline{OUT} pin is used to control the heating element. The analog output can be monitored in a control algorithm that adjusts the set temperature to prevent overshoot. Figure 7-3 shows the trip set voltage error versus temperature, which shows error in $^{\circ}\text{C}$ of the comparator input over temperature. Figure 7-4 shows an alternative method of setting the trip point by using a DAC.

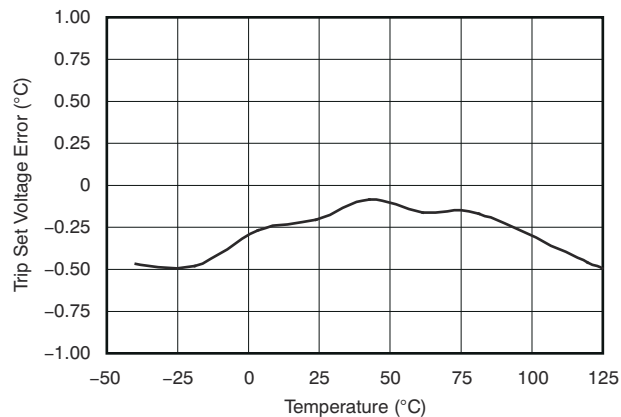


Figure 7-3. Trip Set Voltage Error vs Temperature

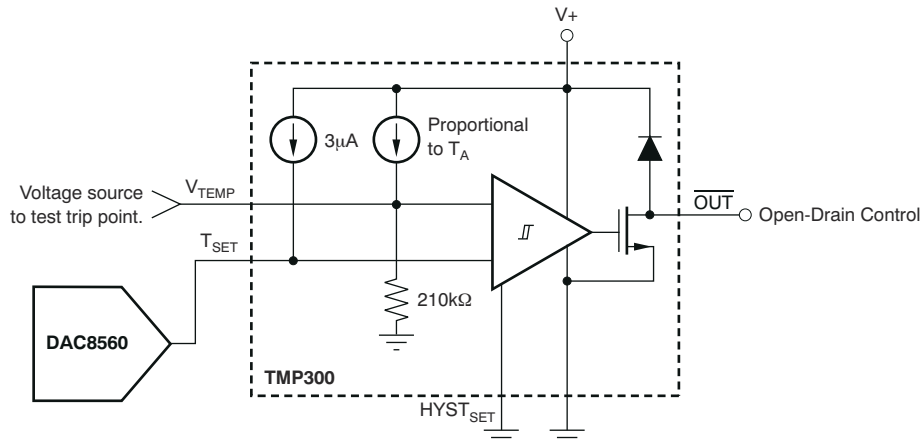


Figure 7-4. DAC Generates the Voltage-Driving T_{SET} Pin

7.2.5 Hysteresis

The hysteresis pin has two settings. Grounding HYST_{SET} results in 5°C of hysteresis. Connecting HYST_{SET} to V_S results in 10°C of hysteresis. [Figure 7-5](#) and [Figure 7-6](#) show the hysteresis error variation over temperature.

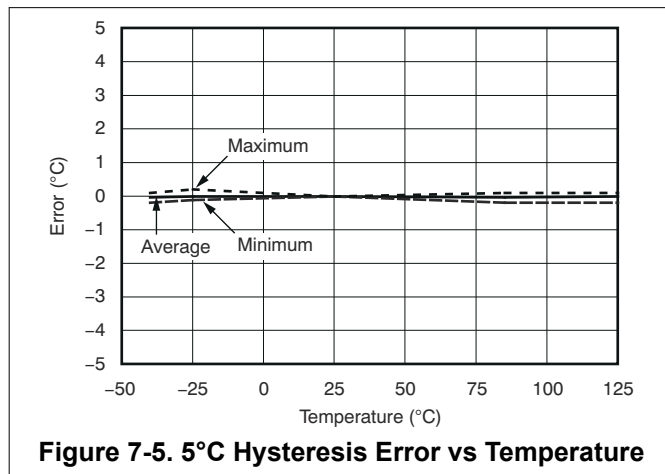


Figure 7-5. 5°C Hysteresis Error vs Temperature

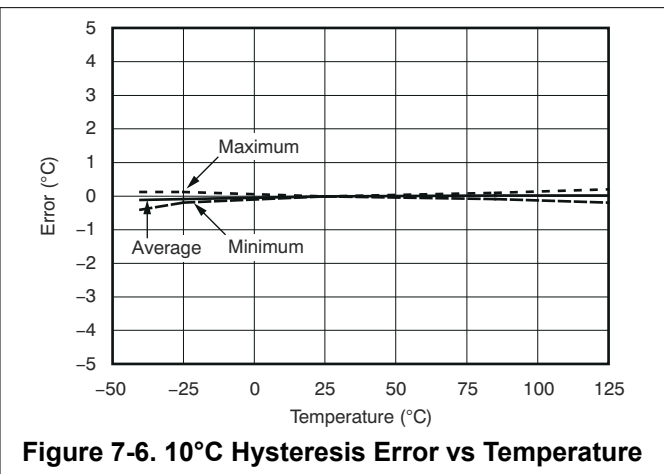


Figure 7-6. 10°C Hysteresis Error vs Temperature

Use bypass capacitors on the supplies as well as on the R_{SET} and analog out (V_{TEMP}) pins when in noisy environments, as shown in [Figure 7-7](#). These capacitors reduce premature triggering of the comparator.

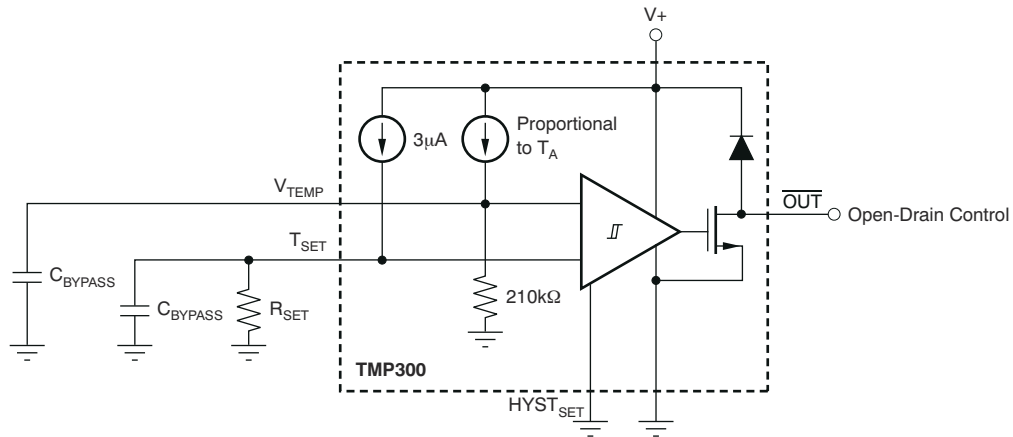


Figure 7-7. Bypass Capacitors Prevent Early Comparator Toggling Due to Circuit Board Noise

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP300AIDBVR	NRND	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T300	
TMP300AIDBVT	NRND	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T300	
TMP300AIDCKR	NRND	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BPN	
TMP300AIDCKT	NRND	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BPN	
TMP300BIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DUDC	Samples
TMP300BIDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DUDC	Samples
TMP300BIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QWL	Samples
TMP300BIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QWL	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TMP300 :

- Automotive : [TMP300-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP300AIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMP300AIDBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMP300AIDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TMP300AIDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TMP300BIDBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMP300BIDBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMP300BIDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TMP300BIDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP300AIDBVR	SOT-23	DBV	6	3000	200.0	183.0	25.0
TMP300AIDBVT	SOT-23	DBV	6	250	200.0	183.0	25.0
TMP300AIDCKR	SC70	DCK	6	3000	200.0	183.0	25.0
TMP300AIDCKT	SC70	DCK	6	250	200.0	183.0	25.0
TMP300BIDBVR	SOT-23	DBV	6	3000	200.0	183.0	25.0
TMP300BIDBVT	SOT-23	DBV	6	250	200.0	183.0	25.0
TMP300BIDCKR	SC70	DCK	6	3000	200.0	183.0	25.0
TMP300BIDCKT	SC70	DCK	6	250	200.0	183.0	25.0

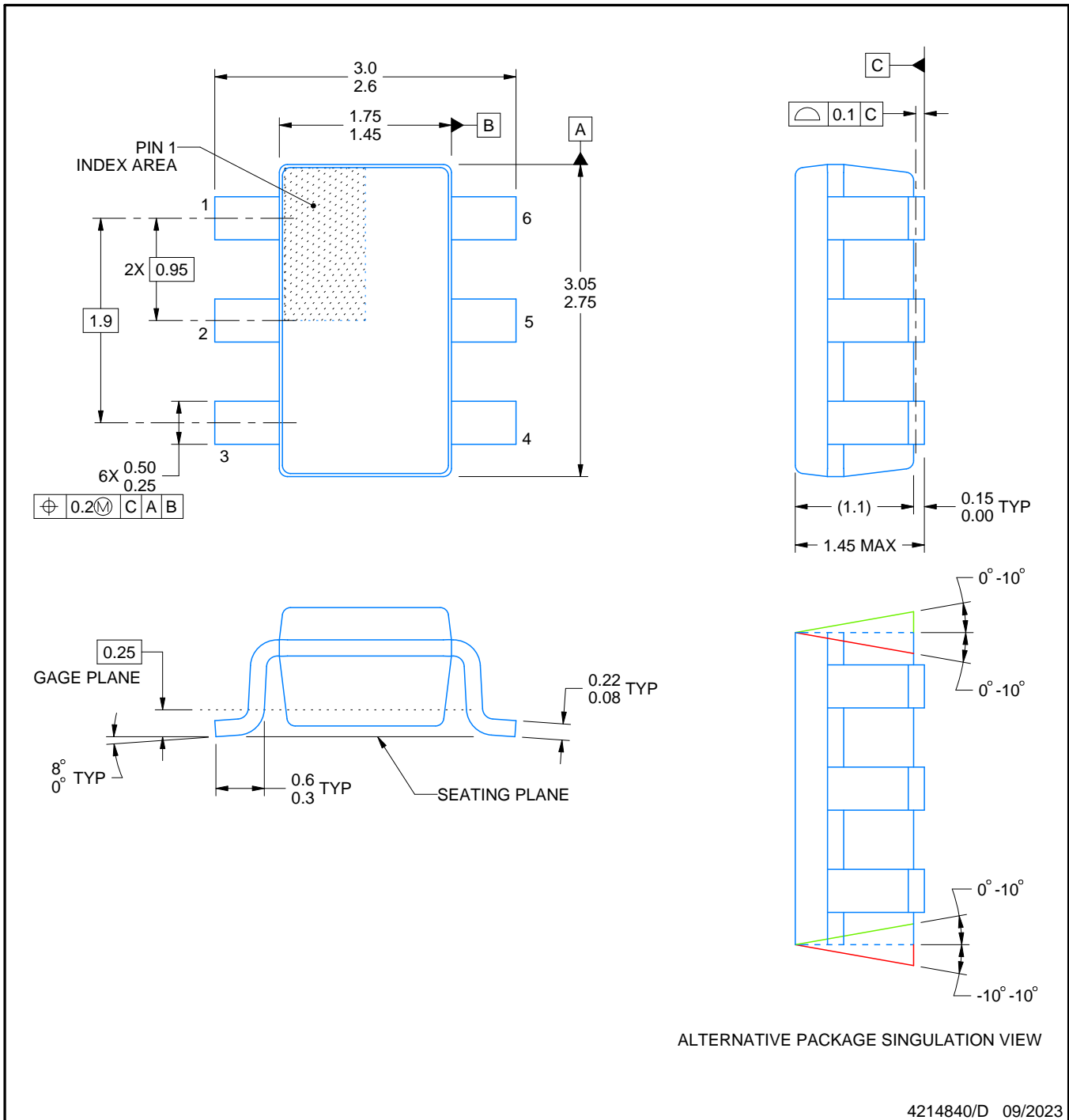


DBV0006A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

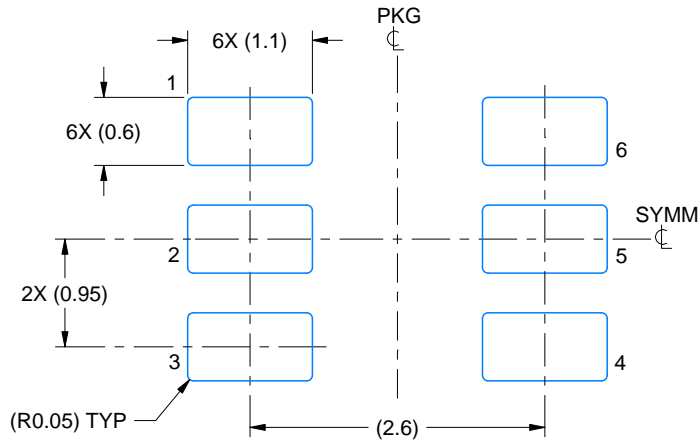
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

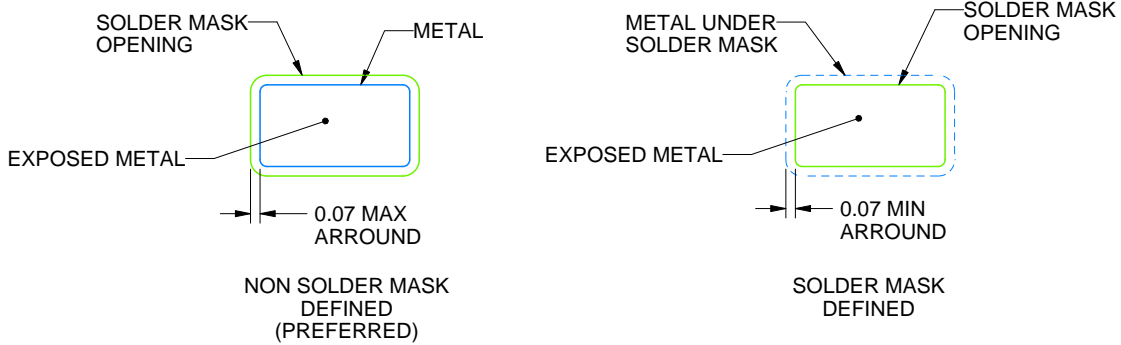
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

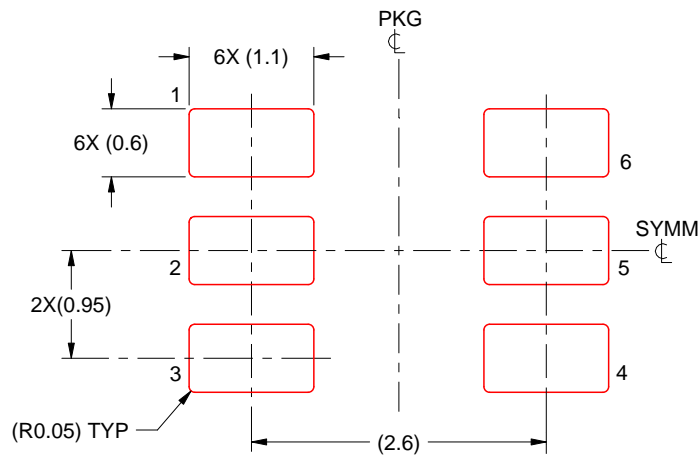
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/D 09/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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