TMUX720x 44 V, Low-RON, 1:1 (SPST), 1-Channel Precision Switch With Latch-Up Immunity and 1.8-V Logic

1 Features

- Latch-up immune
- Dual supply range: ±4.5 V to ±22 V
- Single supply range: 4.5 V to 44 V
- Low On-Resistance: 1.2 Ω
- Low charge injection: −10 pC
- –40°C to +125°C operating temperature
- Integrated Pull-Down resistor on logic pins
- 1.8 V logic compatible
- Fail-safe logic
- Rail to rail operation
- Bidirectional signal path
- Break-before-make switching

2 Applications

- Optical networking
- Optical test equipment
- Wired networking
- Factory automation and industrial controls
- Programmable logic controllers (PLC)
- Semiconductor test
- Ultrasound scanners
- Patient monitoring and diagnostics
- Remote radio units
- Data acquisition systems

3 Description

The TMUX720x is a complementary metal-oxide semiconductor (CMOS) switch with Latch-Up immunity in a single channel, 1:1 (SPST) configuration. The device works with a single supply (4.5 V to 44 V), dual supplies (±4.5 V to ±22 V), or asymmetric supplies (such as V_{DD} = 12 V, V_{SS} = –5 V). The TMUX720x supports bidirectional analog and digital signals on the source (S) and drain (D) pin ranging from V_{SS} to V_{DD}.

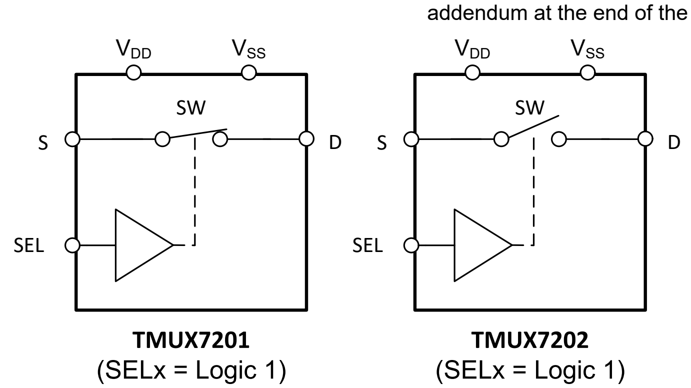
The TMUX720x can be enabled or disabled by controlling the SEL pin. When disabled, both signal path switches are off. All logic control inputs support logic levels from 1.8 V to V_{DD}, which is compatible for both TTL and CMOS logic when operating in the valid supply voltage range. Fail-Safe Logic circuitry allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage.

The TMUX72xx family provides Latch-Up immunity, preventing undesirable high current events between parasitic structures within the device typically caused by overvoltage events. A Latch-Up condition typically continues until the power supply rails are turned off and can lead to device failure. The Latch-Up immunity feature allows the TMUX72xx family of switches and multiplexers to be used in harsh environments.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMUX7202 TMUX7201	DGK (VSSOP, 8)	3.00 mm × 3.00 mm
	RQX (WQFN, 8)	3.00 mm × 2.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



Block Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2022) to Revision A (March 2023)	Page
• Changed the status of the data sheet from: *Advanced Information* to: *Production Data*	1

5 Pin Configuration and Functions

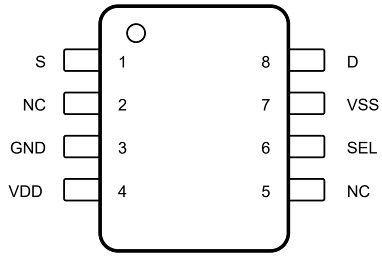

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Figure 5-1. DGK Package, 8-Pin VSSOP (Top View)

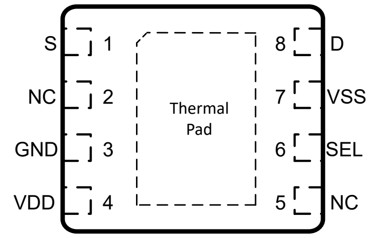

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Figure 5-2. RQX Package, 8-Pin WSON (Top View)

Table 5-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION(2)
NAME	DGK	RQX		
S	1	1	I/O	Source pin. Can be an input or output.
NC	2	2	NC	No connection. Not internally connected.
GND	3	3	P	Ground (0 V) reference
V_{DD}	4	4	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
NC	5	5	NC	No connection. Not internally connected.
SEL	6	6	I	Logic control input, has internal Pull-Down resistor. For information about the switch connection controls, see Section 8.5.
V_{SS}	7	7	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
D	8	8	I/O	Drain pin. Can be an input or output.
Thermal Pad			—	The thermal pad is not connected internally. No requirement to solder this pad, if connected it is recommended that the pad be left floating or tied to GND

(1) I = input, O = output, I/O = input or output, P = power, NC = no connection.
(2) For what to do with unused pins, refer to Section 8.4.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
$V_{DD} – V_{SS}$	Supply voltage		48	V
V_{DD}		–0.5	48	V
V_{SS}		–48	0.5	V
V_{SEL} or V_{EN}	Logic control input pin voltage (SELx)	–0.5	48	V
I_{SEL} or I_{EN}	Logic control input pin current (SELx)	–30	30	mA
V_S or V_D	Source or drain voltage (Sx, Dx)	V_{SS}–0.5	V_{DD}+0.5	V
I_{IK}	Diode clamp current(3)	–30	30	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, Dx)		I_{DC} + 10 %(4)	mA
T_A	Ambient temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Absolute Maximum Ratings*. If used outside the *Absolute Maximum Ratings* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(4) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

6.2 ESD Ratings

			VALUE	UNIT
TMUX720x				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC[1]		TMUX720x		UNIT
		DGK (VSSOP)	RQX (WQFN)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	152.1	62.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.4	54.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	73.2	31.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.1	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	71.8	30.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	23.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} – V_{SS}$ [1]	Power supply voltage differential	4.5		44	V
V_{DD}	Positive power supply voltage	4.5		44	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	V_{SS}		V_{DD}	V
V_{SEL} or V_{EN}	Address or enable pin voltage	0		44	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)			I_{DC} [2]	mA
T_A	Ambient temperature	–40		125	°C

(1) V_{DD} and V_{SS} can be any value as long as 4.5 V ≤ (V_{DD} – V_{SS}) ≤ 44 V, and the minimum V_{DD} is met.
(2) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

6.5 Source or Drain Continuous Current

at supply voltage of V_{DD} ± 10%, V_{SS} ± 10 % (unless otherwise noted)

CONTINUOUS CURRENT PER CHANNEL (I_{DC}) [2]		T_A = 25°C	T_A = 85°C	T_A = 125°C	UNIT
PACKAGE	TEST CONDITIONS				
DSK (VSSOP)	+44 V Dual Supply[1]	440	280	140	mA
	±15 V Dual Supply	420	260	130	mA
	+12 V Single Supply	330	210	125	mA
	±5 V Dual Supply	300	200	120	mA
RQX (WQFN)	+44 V Single Supply[1]	650	350	165	mA
	±15 V Dual Supply	600	340	150	mA
	+12 V Single Supply	500	300	145	mA
	±5 V Dual Supply	450	265	135	mA

(1) Specified for nominal supply voltage only.
(2) Refer to Total power dissipation (P_{tot}) limits in A*bsolute Maximum Ratings* table that must be followed with max continuous current specification.

6.6 ±15 V Dual Supply: Electrical Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10 V to +10 V I_D = –10 mA	25°C		1.2	1.7	Ω
			–40°C to +85°C			2	Ω
			–40°C to +125°C			2.5	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –10 V to +10 V I_D = –10 mA	25°C		0.3	0.5	Ω
			–40°C to +85°C			0.7	Ω
			–40°C to +125°C			0.8	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA	–40°C to +125°C		0.01		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V	25°C	–0.3	0.05	0.3	nA
			–40°C to +85°C	–3.4		3.4	nA
			–40°C to +125°C	–33		33	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V	25°C	–0.3	0.05	0.3	nA
			–40°C to +85°C	–3.4		3.4	nA
			–40°C to +125°C	–33		33	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is on V_S = V_D = ±10 V	25°C	–0.65	0.05	0.65	nA
			–40°C to +85°C	–2		2	nA
			–40°C to +125°C	–16		16	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.4	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		30	45	µA
			–40°C to +85°C			50	µA
			–40°C to +125°C			55	µA
I_{SS}	V_{SS} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		7	12	µA
			–40°C to +85°C			15	µA
			–40°C to +125°C			17	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.7 ±15 V Dual Supply: Switching Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		120	140	ns
			–40°C to +85°C			155	ns
			–40°C to +125°C			170	ns
t_{OFF}	Turn-off time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		130	150	ns
			–40°C to +85°C			160	ns
			–40°C to +125°C			190	ns
$t_{ON (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35 pF	–40°C to +125°C		0.2		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF	25°C		450		ps
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 100 pF	25°C		-15		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz	25°C		–70		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		–46		dB
BW	–3 dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 0 V	25°C		22		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		–0.11		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		–40		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 15 V, V_{BIAS} = 0 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.0007		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V, f = 1 MHz	25°C		45		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 0 V, f = 1 MHz	25°C		65		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 0 V, f = 1 MHz	25°C		240		pF

6.8 ±20 V Dual Supply: Electrical Characteristics

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –15 V to +15 V I_D = –10 mA	25°C		1	1.5	Ω
			–40°C to +85°C			1.8	Ω
			–40°C to +125°C			2.3	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –15 V to +15 V I_S = –10 mA	25°C		0.3	0.5	Ω
			–40°C to +85°C			0.7	Ω
			–40°C to +125°C			0.8	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA	–40°C to +125°C		0.009		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V	25°C	–0.4	0.05	0.4	nA
			–40°C to +85°C	–5		5	nA
			–40°C to +125°C	–35		35	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V	25°C	–0.4	0.05	0.4	nA
			–40°C to +85°C	–5		5	nA
			–40°C to +125°C	–35		35	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is on V_S = V_D = ±15 V	25°C	–0.7	0.05	0.7	nA
			–40°C to +85°C	–2		2	nA
			–40°C to +125°C	–18		18	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.4	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 22 V, V_{SS} = –22 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		38	50	µA
			–40°C to +85°C			60	µA
			–40°C to +125°C			70	µA
I_{SS}	V_{SS} supply current	V_{DD} = 22 V, V_{SS} = –22 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		8	15	µA
			–40°C to +85°C			19	µA
			–40°C to +125°C			23	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.9 ±20 V Dual Supply: Switching Characteristics

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		120	140	ns
			–40°C to +85°C			155	ns
			–40°C to +125°C			190	ns
t_{OFF}	Turn-off time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		120	150	ns
			–40°C to +85°C			160	ns
			–40°C to +125°C			190	ns
$t_{ON (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35 pF	–40°C to +125°C		0.2		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF	25°C		400		ps
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 100 pF	25°C		-20		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz	25°C		–65		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		–45		dB
BW	–3 dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 0 V	25°C		22		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		–0.10		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		–40		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 20 V, V_{BIAS} = 0 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.0008		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V, f = 1 MHz	25°C		42		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 0 V, f = 1 MHz	25°C		62		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 0 V, f = 1 MHz	25°C		240		pF

6.10 44 V Single Supply: Electrical Characteristics

V_{DD} = +44 V, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +44 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 40 V I_D = –10 mA	25°C		1.2	1.6	Ω
			–40°C to +85°C			2	Ω
			–40°C to +125°C			2.4	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to 40 V I_D = –10 mA	25°C		0.25	0.9	Ω
			–40°C to +85°C			1.1	Ω
			–40°C to +125°C			1.3	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 22 V, I_S = –10 mA	–40°C to +125°C		0.008		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 44 V, V_{SS} = 0 V Switch state is off V_S = 40 V / 1 V V_D = 1 V / 40 V	25°C	–1	0.05	1	nA
			–40°C to +85°C	–10		10	nA
			–40°C to +125°C	–60		60	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 44 V, V_{SS} = 0 V Switch state is off V_S = 40 V / 1 V V_D = 1 V / 40 V	25°C	–1	0.05	1	nA
			–40°C to +85°C	–10		10	nA
			–40°C to +125°C	–60		60	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 44 V, V_{SS} = 0 V Switch state is on V_S = V_D = 40 V or 1 V	25°C	–2	0.05	2	nA
			–40°C to +85°C	–5		5	nA
			–40°C to +125°C	–30		30	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.6	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 44 V, V_{SS} = 0 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		30	56	µA
			–40°C to +85°C			64	µA
			–40°C to +125°C			68	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.11 44 V Single Supply: Switching Characteristics

V_{DD} = +44 V, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +44 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 18 V R_L = 300 Ω, C_L = 35 pF	25°C		100	140	ns
			–40°C to +85°C			150	ns
			–40°C to +125°C			180	ns
t_{OFF}	Turn-off time from control input	V_S = 18 V R_L = 300 Ω, C_L = 35 pF	25°C		125	150	ns
			–40°C to +85°C			160	ns
			–40°C to +125°C			180	ns
$t_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35 pF	–40°C to +125°C		0.17		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF	25°C		1000		ps
Q_{INJ}	Charge injection	V_S = 22 V, C_L = 100 pF	25°C		-20		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz	25°C		–66		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		–46		dB
BW	–3 dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 6 V	25°C		22		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		–0.11		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		–36		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 22 V, V_{BIAS} = 22 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.0008		%
$C_{S(OFF)}$	Source off capacitance	V_S = 22 V, f = 1 MHz	25°C		45		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 22 V, f = 1 MHz	25°C		66		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 22 V, f = 1 MHz	25°C		240		pF

6.12 12 V Single Supply: Electrical Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 10 V I_D = –10 mA	25°C		2.1	3.2	Ω
			–40°C to +85°C			3.8	Ω
			–40°C to +125°C			4.2	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to 10 V I_S = –10 mA	25°C		0.5	1.2	Ω
			–40°C to +85°C			1.4	Ω
			–40°C to +125°C			1.6	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 6 V, I_S = –10 mA	–40°C to +125°C		0.017		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V	25°C	–0.4	0.05	0.4	nA
			–40°C to +85°C	–3		3	nA
			–40°C to +125°C	–25		25	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V	25°C	–0.4	0.05	0.4	nA
			–40°C to +85°C	–3		3	nA
			–40°C to +125°C	–25		25	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is on V_S = V_D = 10 V or 1 V	25°C	–0.65	0.05	0.65	nA
			–40°C to +85°C	–2		2	nA
			–40°C to +125°C	–12		12	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.4	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 13.2 V, V_{SS} = 0 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		27	35	µA
			–40°C to +85°C			40	µA
			–40°C to +125°C			45	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.13 12 V Single Supply: Switching Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 8 V R_L = 300 Ω, C_L = 35 pF	25°C		125	145	ns
			–40°C to +85°C			160	ns
			–40°C to +125°C			180	ns
t_{OFF}	Turn-off time from control input	V_S = 8 V R_L = 300 Ω, C_L = 35 pF	25°C		150	180	ns
			–40°C to +85°C			205	ns
			–40°C to +125°C			220	ns
$t_{ON (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35 pF	–40°C to +125°C		0.2		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF	25°C		1000		ps
Q_{INJ}	Charge injection	V_S = 6 V, C_L = 100 pF	25°C		-4		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz	25°C		–65		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		–45		dB
BW	–3 dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 6 V	25°C		23		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		–0.18		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		–40		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 6 V, V_{BIAS} = 6 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.0009		%
$C_{S(OFF)}$	Source off capacitance	V_S = 6 V, f = 1 MHz	25°C		53		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 6 V, f = 1 MHz	25°C		75		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 6 V, f = 1 MHz	25°C		240		pF

6.14 Typical Characteristics

at T_A = 25°C

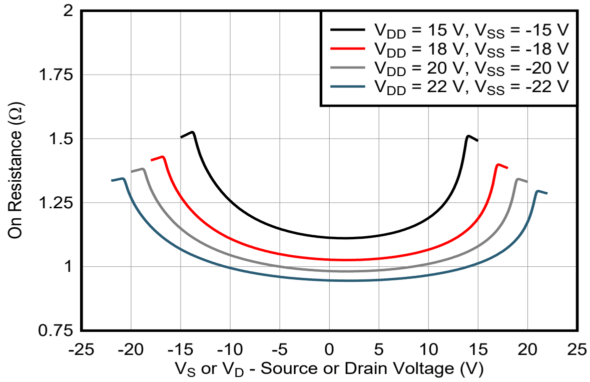


Figure 6-1. On-Resistance vs Source or Drain Voltage – Dual Supply

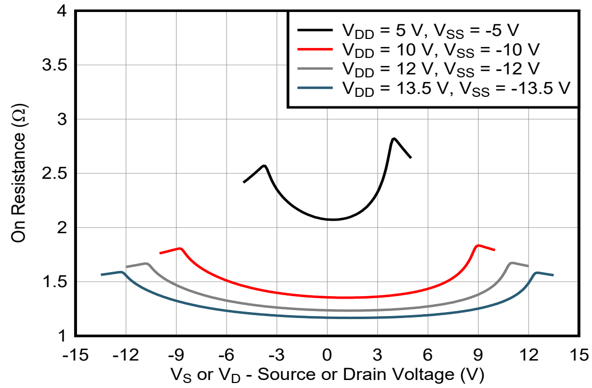


Figure 6-2. On-Resistance vs Source or Drain Voltage – Dual Supply

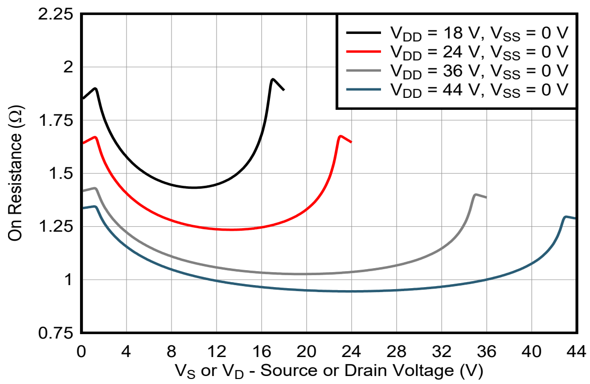


Figure 6-3. On-Resistance vs Source or Drain Voltage – Single Supply

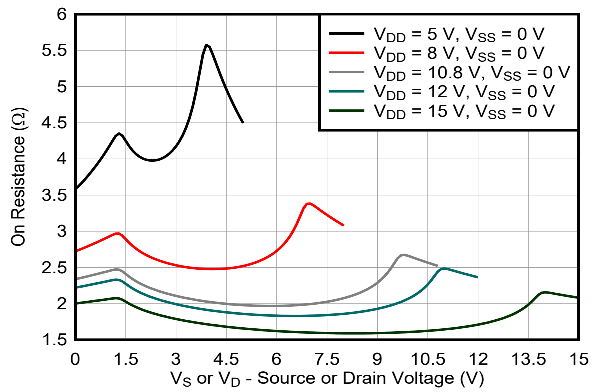
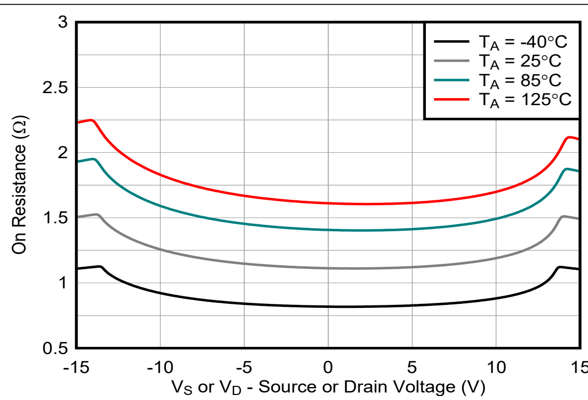
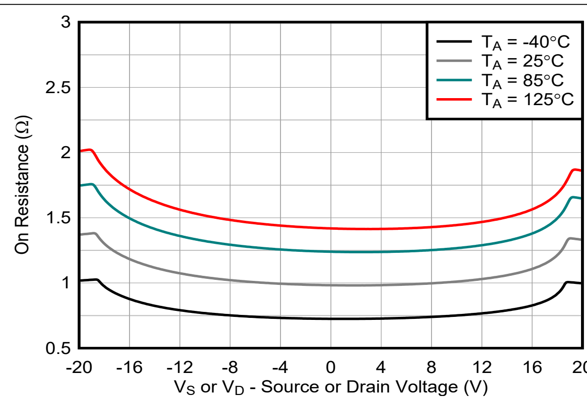


Figure 6-4. On-Resistance vs Source or Drain Voltage – Single Supply



V_{DD} = 15 V, V_{SS} = -15 V

Figure 6-5. On-Resistance vs Temperature

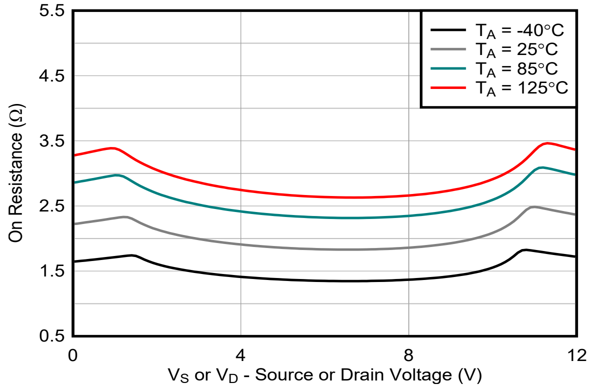


V_{DD} = 20 V, V_{SS} = -20 V

Figure 6-6. On-Resistance vs Temperature

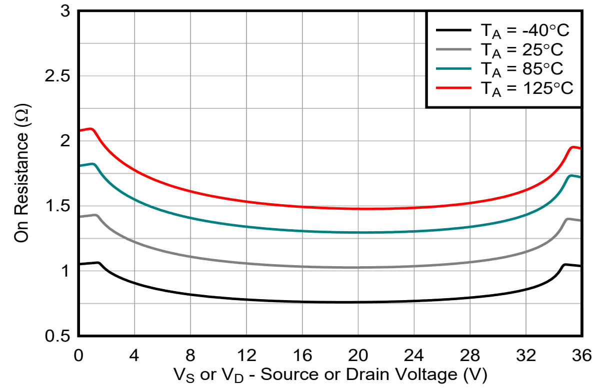
6.14 Typical Characteristics (continued)

at T_A = 25°C



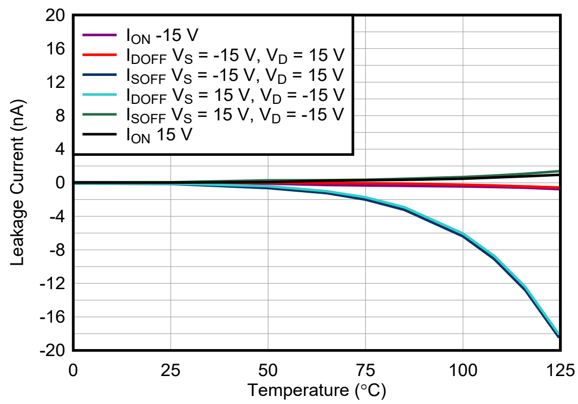
V_{DD} = 12 V, V_{SS} = 0 V

Figure 6-7. On-Resistance vs Temperature



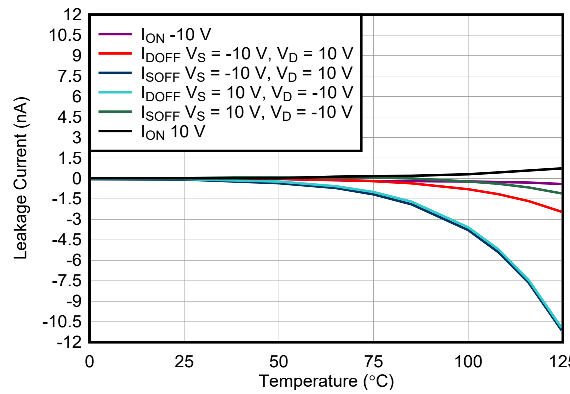
V_{DD} = 36 V, V_{SS} = 0 V

Figure 6-8. On-Resistance vs Temperature



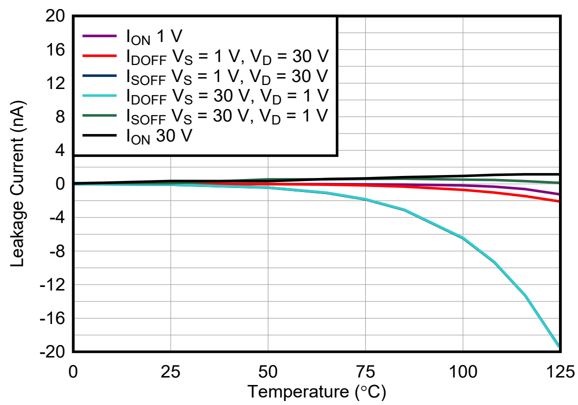
V_{DD} = 20 V, V_{SS} = -20 V

Figure 6-9. Leakage Current vs Temperature



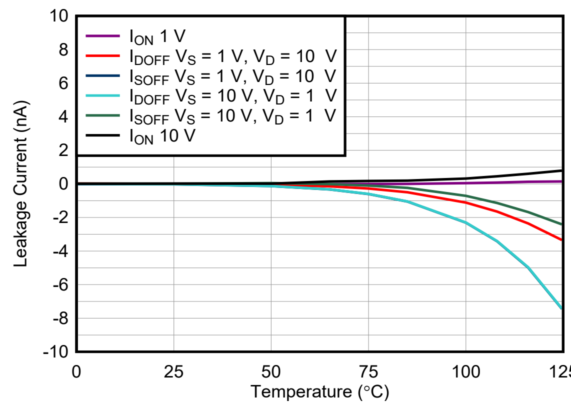
V_{DD} = 15 V, V_{SS} = -15 V

Figure 6-10. Leakage Current vs Temperature



V_{DD} = 36 V, V_{SS} = 0 V

Figure 6-11. Leakage Current vs Temperature



V_{DD} = 12 V, V_{SS} = 0 V

Figure 6-12. Leakage Current vs Temperature

6.14 Typical Characteristics (continued)

at T_A = 25°C

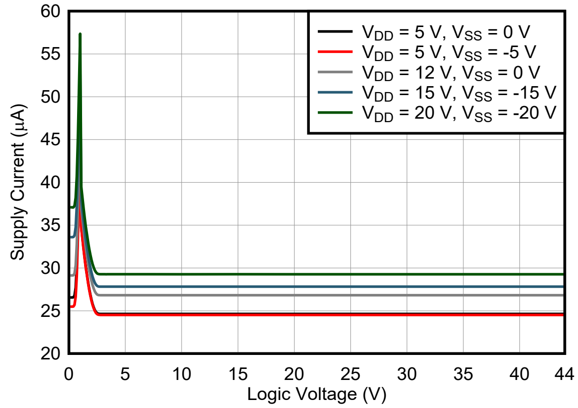


Figure 6-13. Supply Current vs Logic Voltage

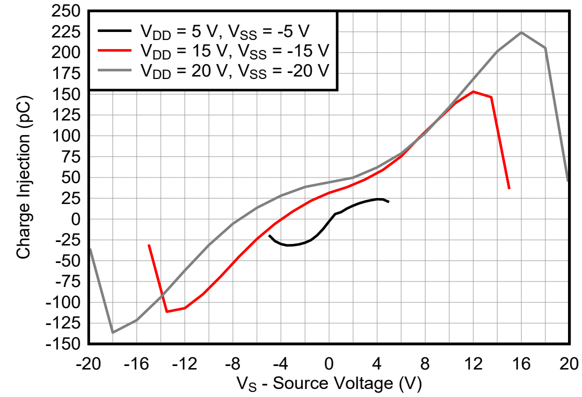


Figure 6-14. Charge Injection vs Source Voltage – Dual Supplies

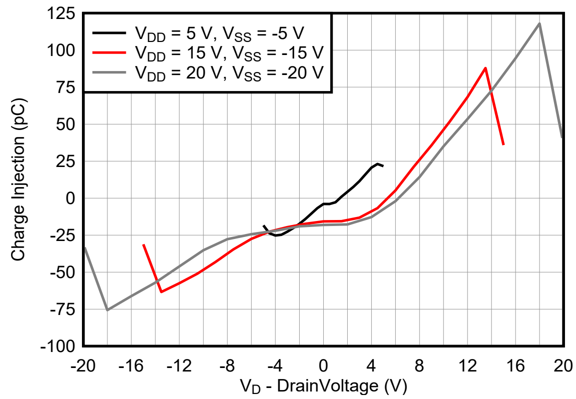


Figure 6-15. Charge Injection vs Drain Voltage – Dual Supplies

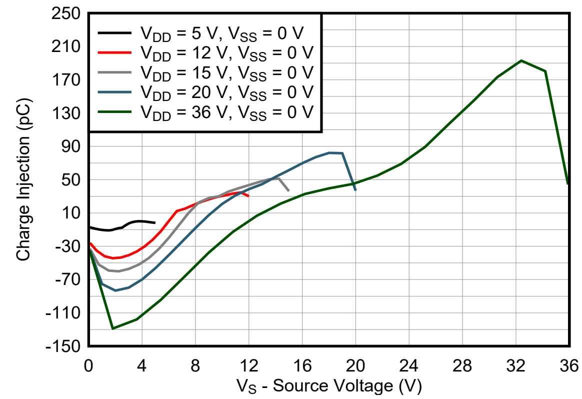


Figure 6-16. Charge Injection vs Source Voltage – Single Supplies

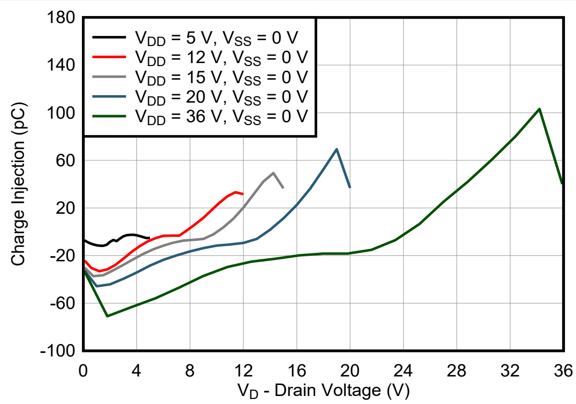
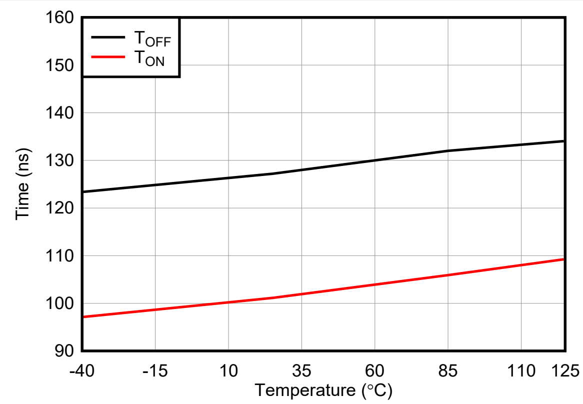


Figure 6-17. Charge Injection vs Drain Voltage – Single Supplies

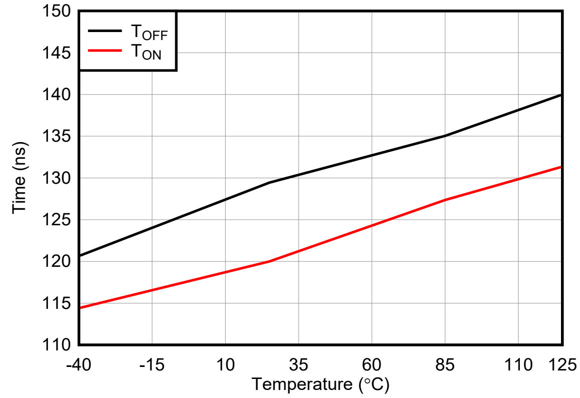


V_{DD} = 15 V, V_{SS} = -15 V

Figure 6-18. T_{ON} and T_{OFF} vs Temperature

6.14 Typical Characteristics (continued)

at T_A = 25°C



V_{DD} = 44 V, V_{SS} = 0 V

Figure 6-19. T_{ON} and T_{OFF} vs Temperature

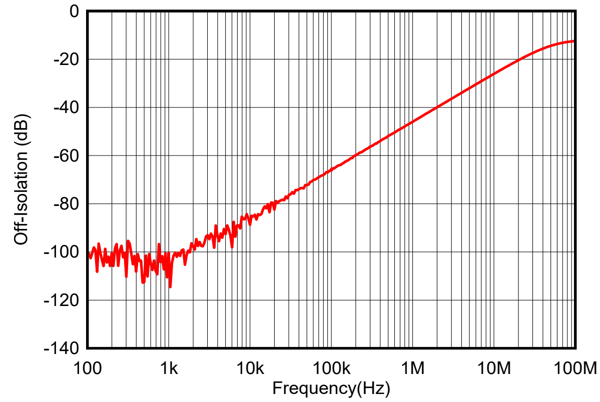


Figure 6-20. Off-Isolation vs Frequency

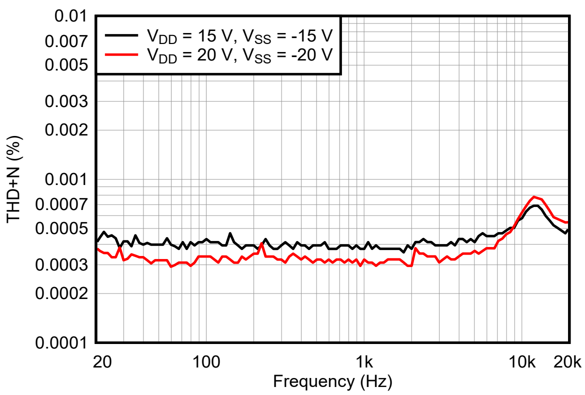


Figure 6-21. THD+N vs Frequency (Dual Supplies)

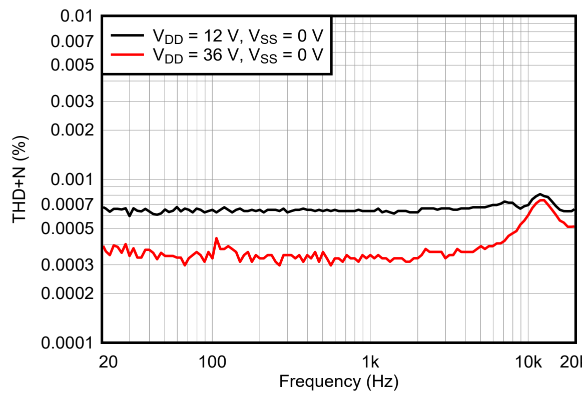
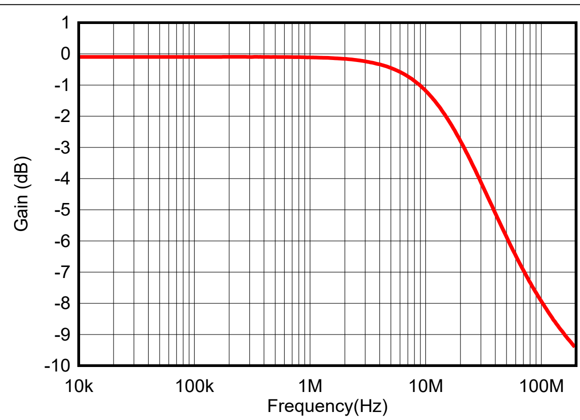
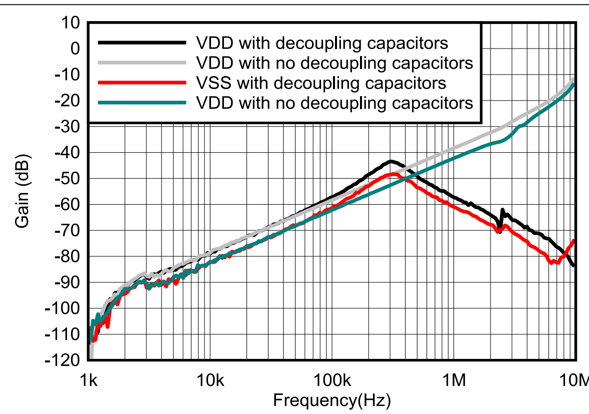


Figure 6-22. THD+N vs Frequency (Single Supplies)



V_{DD} = 15 V, V_{SS} = -15 V

Figure 6-23. On Response vs Frequency

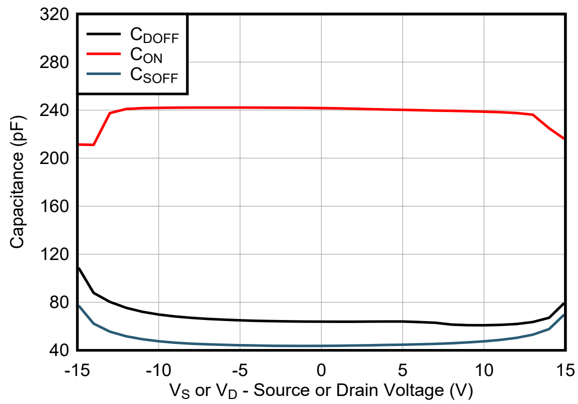


V_{DD} = +15 V, V_{SS} = -15 V

Figure 6-24. ACPSRR vs Frequency

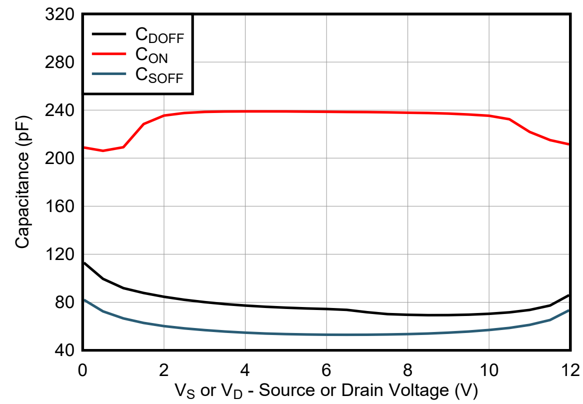
6.14 Typical Characteristics (continued)

at T_A = 25°C



V_{DD} = +15 V, V_{SS} = -15 V

Figure 6-25. Capacitance vs Source Voltage or Drain Voltage



V_{DD} = 12 V, V_{SS} = 0 V

Figure 6-26. Capacitance vs Source Voltage or Drain Voltage

7 Parameter Measurement Information

7.1 On-Resistance

The On-Resistance of a device is the ohmic resistance between the source (Sx) and drain (Dx) pins of the device. The On-Resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote On-Resistance. Figure 7-1 shows the measurement setup used to measure R_{ON}. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$.

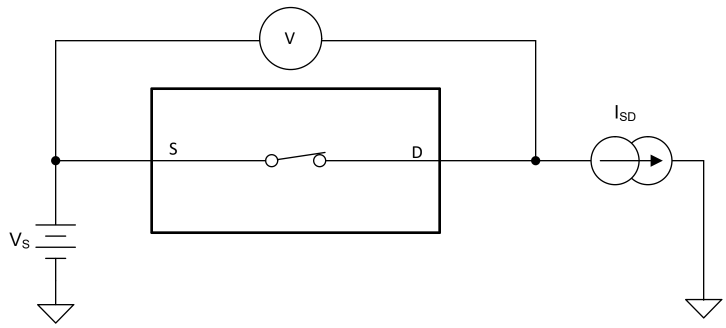


Figure 7-1. On-Resistance Measurement Setup

7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source Off-Leakage current.
2. Drain Off-Leakage current.

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

Figure 7-2 shows the setup used to measure both Off-Leakage currents.

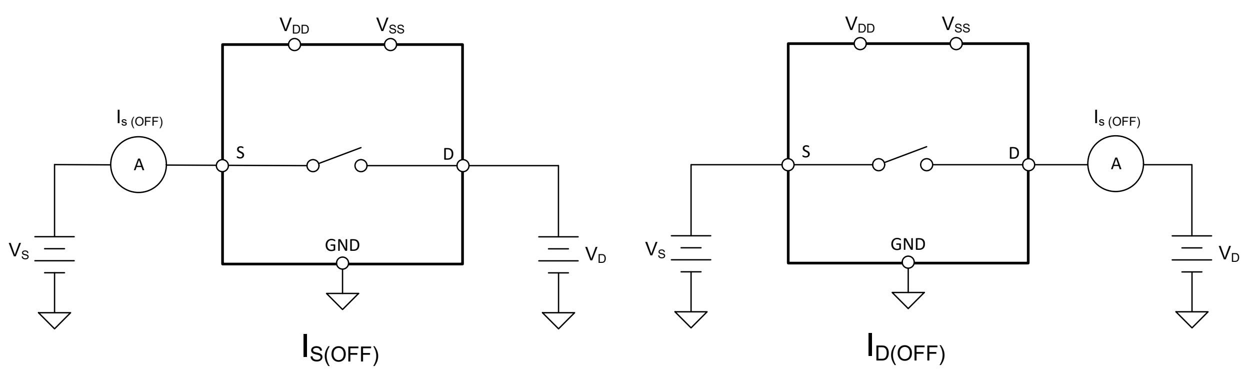


Figure 7-2. Off-Leakage Measurement Setup

7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 7-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

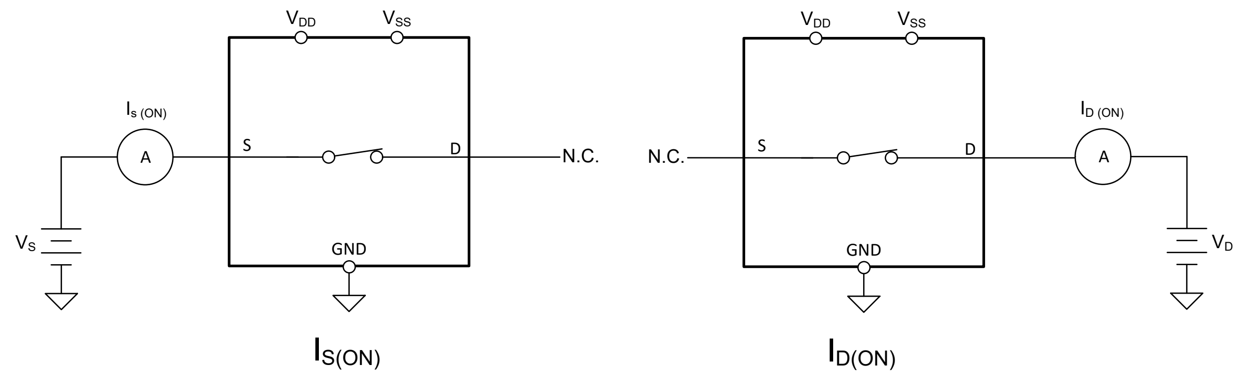


Figure 7-3. On-Leakage Measurement Setup

7.4 t_{ON} and t_{OFF} Time

Turn-on time is defined as the time taken by the output of the device to rise to 90% after the enable has risen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 7-4 shows the setup used to measure turn-on time, denoted by the symbol t_{ON}.

Turn-off time is defined as the time taken by the output of the device to fall to 10% after the enable has fallen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 7-4 shows the setup used to measure turn-off time, denoted by the symbol t_{OFF}.

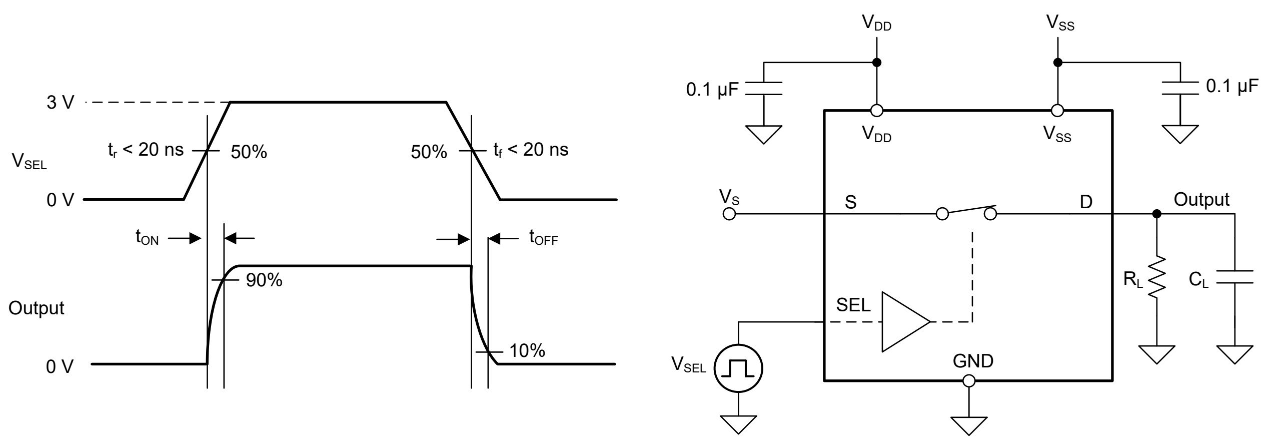


Figure 7-4. Turn-On and Turn-Off Time Measurement Setup

7.5 $t_{ON\ (VDD)}$ Time

The $t_{ON\ (VDD)}$ time is defined as the time taken by the output of the device to rise to 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. Figure 7-5 shows the setup used to measure turn on time, denoted by the symbol $t_{ON\ (VDD)}$.

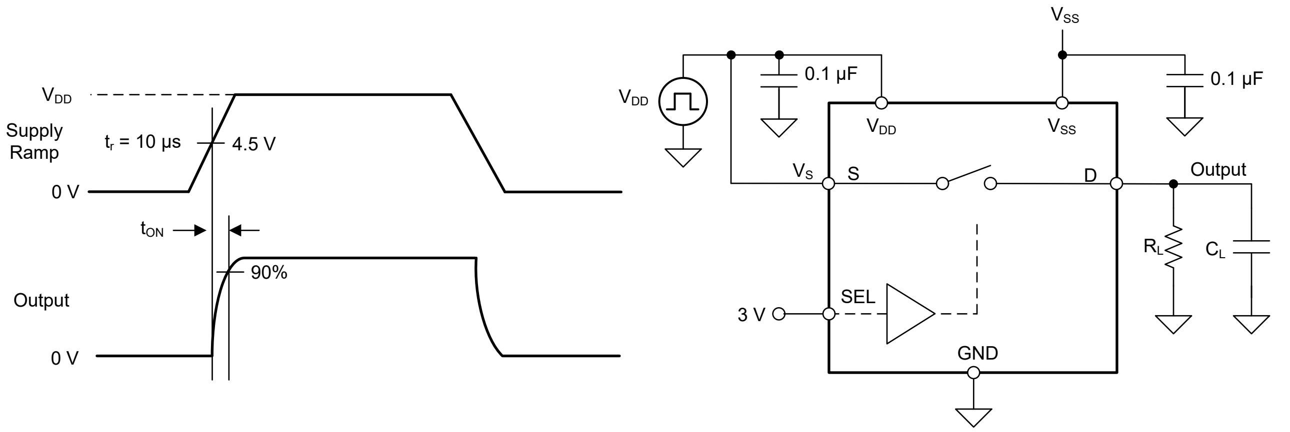


Figure 7-5. $t_{ON\ (VDD)}$ Time Measurement Setup

7.6 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. Figure 7-6 and Equation 1 shows the setup used to measure propagation delay, denoted by the symbol t_{PD}.

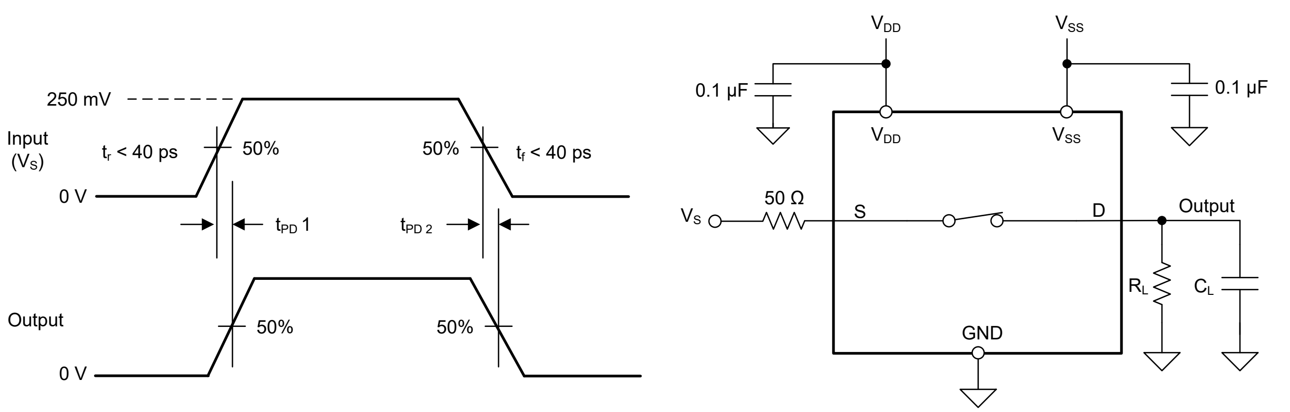


Figure 7-6. Propagation Delay Measurement Setup

$$t_{Prop\ Delay} = max\,(t_{PD}\,1,\ t_{PD}\,2) \tag{1}$$

7.7 Charge Injection

The TMUX720x devices have a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. Figure 7-7 shows the setup used to measure charge injection from source (Sx) to drain (Dx).

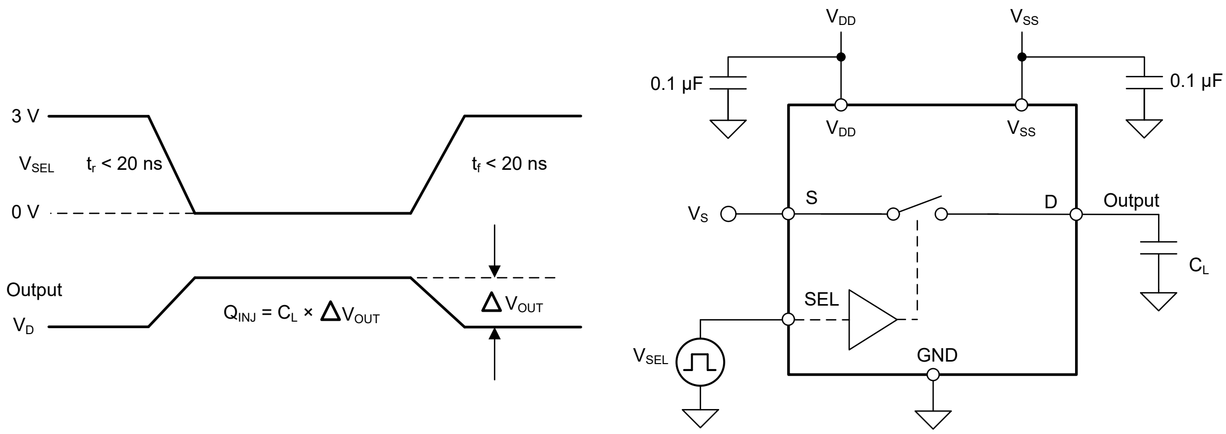


Figure 7-7. Charge-Injection Measurement Setup

7.8 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. The characteristic impedance, Z_0, for the measurement is 50 Ω. Figure 7-8 and Equation 2 shows the setup used to measure off isolation. Use off isolation equation to compute off isolation.

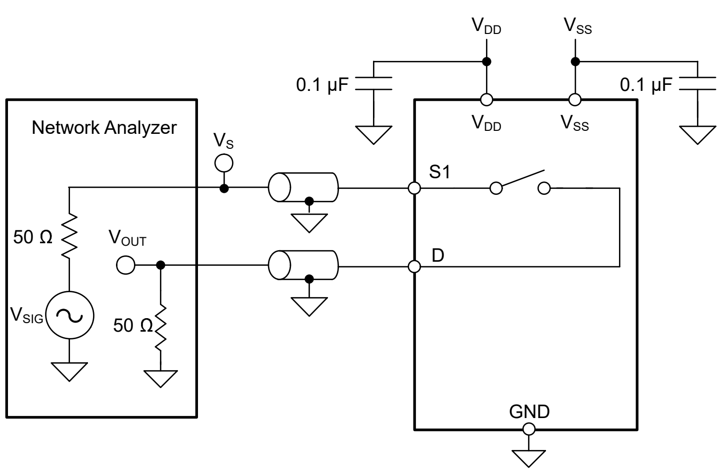


Figure 7-8. Off Isolation Measurement Setup

$$Off - Isolation = 20 \times Log\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

7.9 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx) of the device. The characteristic impedance, Z_0, for the measurement is 50 Ω. Figure 7-9 and Equation 3 shows the setup used to measure bandwidth.

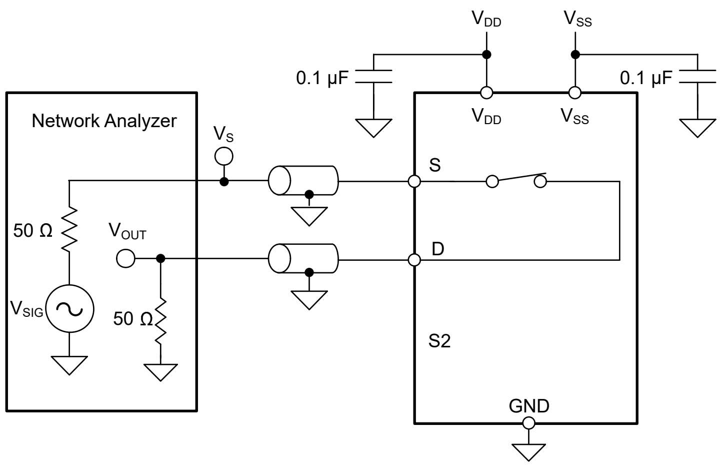


Figure 7-9. Bandwidth Measurement Setup

$$Bandwidth = 20 \times Log\left(\frac{V_{OUT}}{V_S}\right) \quad (3)$$

7.10 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The On-Resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD + N.

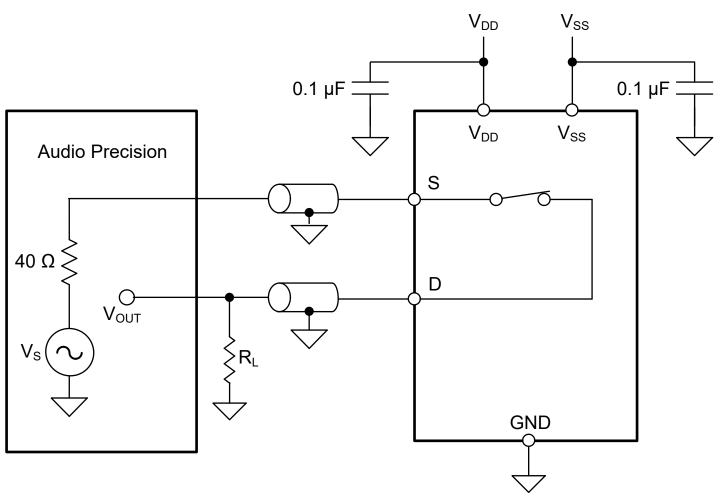


Figure 7-10. THD + N Measurement Setup

7.11 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 100 mV_{PP}. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the AC PSRR.

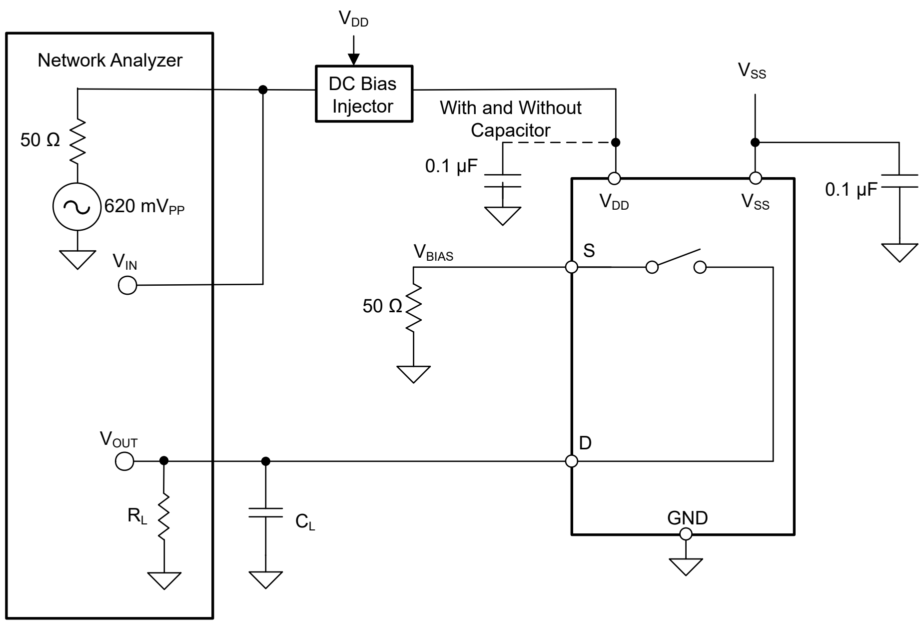


Figure 7-11. AC PSRR Measurement Setup

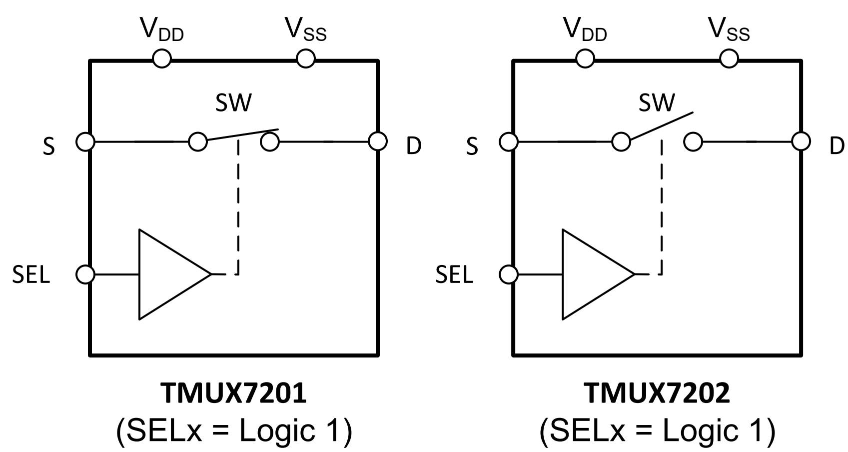
$$PSRR = 20 \times Log\left(\frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

8 Detailed Description

8.1 Overview

The TMUX720x are 1:1, 1-channel switches. The switch is turned on or turned off based on the state of the select pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bidirectional Operation

The TMUX720x conducts equally well from source (S) to drain (D) or from drain (D) to source (S). The switch has very similar characteristics in both directions and supports both analog and digital signals.

8.3.2 Rail-to-Rail Operation

The valid signal path input and output voltage for TMUX720x ranges from V_{SS} to V_{DD}.

8.3.3 1.8 V Logic Compatible Inputs

The TMUX720x has 1.8 V logic compatible control for all logic control inputs. 1.8 V logic level inputs allows the device to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations, refer to *Simplifying Design with 1.8 V logic Muxes and Switches*.

8.3.4 Integrated Pull-Down Resistor on Logic Pins

The TMUX7201 and TMUX7202 have internal weak Pull-Down resistors to GND to ensure the logic pins are not left floating. The value of this Pull-Down resistor is approximately 4 MΩ, but is clamped to about 1 µA at higher voltages. This feature integrates an external component and reduces system size and cost.

8.3.5 Fail-Safe Logic

The TMUX720x supports Fail-Safe Logic on the control input pins (SEL) allowing for operation up to 44 V above ground, regardless of the state of the supply pins. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the logic input pins of the TMUX720x to be ramped to +44 V while V_{DD} and V_{SS} = 0 V. The logic control inputs are protected against positive faults of up to +44 V in powered-off condition, but do not offer protection against negative overvoltage conditions.

8.3.6 Latch-Up Immune

Latch-up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The Latch-Up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX720x family of devices are constructed on silicon-on-insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The Latch-Up immunity feature allows the TMUX720x family of switches and multiplexers to be used in harsh environments.

8.3.7 Ultra-Low Charge Injection

Figure 8-1 shows how the TMUX720x devices have a transmission gate topology. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

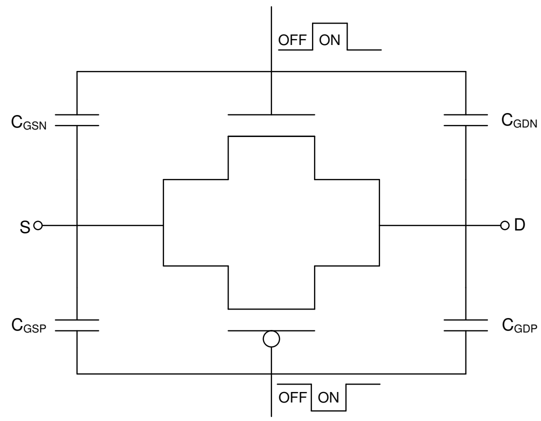


Figure 8-1. Transmission Gate Topology

The TMUX720x contains specialized architecture to reduce charge injection on the Drain (Dx). To further reduce charge injection in a sensitive application, a compensation capacitor (Cp) can be added on the Source (S). By design, the excess charge from the switch transition will be pushed into the compensation capacitor on the Source (S) instead of the Drain (D). As a general rule, Cp should be 20x larger than the equivalent load capacitance on the Drain (D). Figure 8-2 shows charge injection variation with different compensation capacitors on the Source side. This plot was captured on the TMUX7219 as part of the TMUX72xx family with a 100 pF load capacitance.

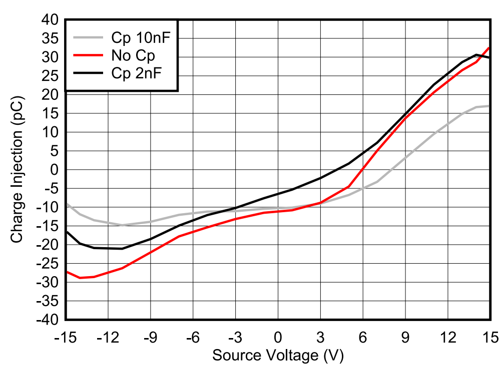


Figure 8-2. Charge Injection Compensation

8.4 Device Functional Modes

When the SEL pin of the TMUX720x is pulled high, the switches will close. When the SEL pin is pulled low, the switches will open. The control pins can be as high as 44 V.

The TMUX720x can operate without any external components except for the supply decoupling capacitors. The SEL pin has an internal Pull-Down resistor of 4 MΩ. If unused, then the SEL pin must be tied to GND so the device does not consume additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*.

8.5 Truth Tables

Table 8-1 provides the truth tables for the TMUX720x.

Table 8-1. TMUX720x Truth Table

SEL	Selected Source Connected To Drain (D) – TMUX7201	Selected Source Connected To Drain (D) – TMUX7202
0	All sources are off (HI-Z)	S
1	S	All sources are off (HI-Z)

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

TMUX720x is part of the precision switches and multiplexers family of devices. TMUX720x offers low RON, low on and off leakage currents and Ultra-Low charge injection performance. These properties make TMUX720x ideal for implementing high precision industrial systems requiring selection of one of two inputs or outputs.

9.2 Typical Applications

9.2.1 TIA Feedback Gain Switch

One application of the TMUX720x is to configure the feedback on a discrete transimpedance amplifier (TIA) implementation. Often, TIAs are used in applications such as photodiode inputs, which then feeds into an ADC or MCU/processor. Depending on the expected strength of the photodiode input, and the needed accuracy, multiple gain levels are needed. A switch like the TMUX720x allows for different gain values to be selected, changing the level of amplifications. This solution can be scaled, but as much as needed for multiple gain options.

Figure 9-1 shows the TMUX720x configured with a precision op amp to enable multiple gains.

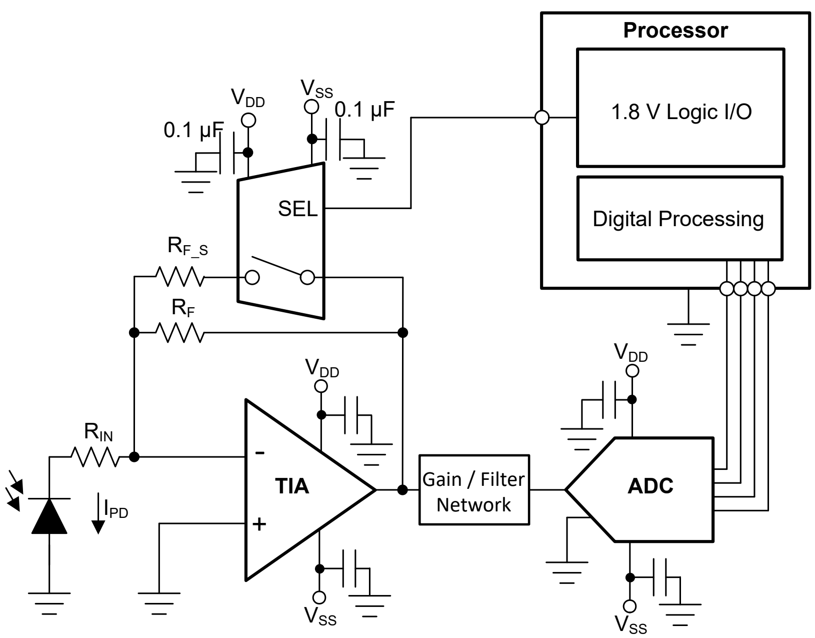


Figure 9-1. TIA Feedback Control

9.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 9-1.

Table 9-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	15 V
Supply (V_{SS})	−15 V
MUX I/O signal range	−15 V to 15 V (Rail-to-Rail)
Control logic thresholds	1.8 V compatible (up to V_{DD})

9.2.1.2 Detailed Design Procedure

Figure 9-1 shows an application that demonstrates how the TMUX720x can be used to select the gain of a TIA amplifier. Here R_F is used to prevent any open loop configuration. For the lowest error, the R_{ON} of the switch should be much smaller than R_{F_S}, as this will scale linearly with the potential error.

The TMUX720x can support 1.8 V logic signals on the control input, allowing the device to interface with low logic controls of an FPGA or MCU. The TMUX720x can operate without any external components except for the supply decoupling capacitors. The select pin has an internal Pull-Down resistor to prevent floating input logic. All inputs to the switch must fall within the recommend operating conditions of the TMUX720x including signal range and continuous current. For this design with a positive supply of 15 V on V_{DD} and negative supply of -15 V on V_{SS}, the signal range can be 15 V to -15 V. The maximum continuous current (I_{DC}) can be up to 330 mA (for wide-range current measurement, see the *Recommended Operating Conditions* section).

9.2.1.3 Application Curves

The low on and off leakage currents of TMUX720x and Ultra-Low charge injection performance make this device ideal for implementing high precision industrial systems. The TMUX720x contains specialized architecture to reduce charge injection on the source (Sx) (for more details, see Section 8.3.7). Figure 9-2 shows the plot for the charge injection versus source voltage for the TMUX720x.

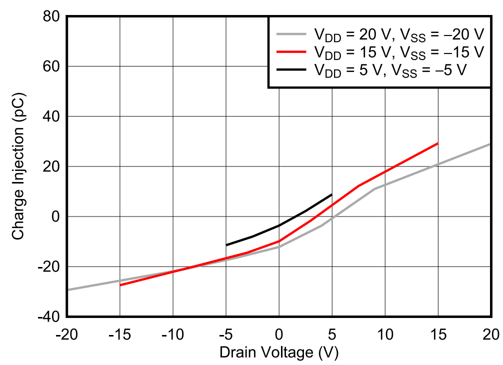


Figure 9-2. Charge Injection vs Source Voltage

9.3 Power Supply Recommendations

The TMUX720x operates across a wide supply range of ±4.5 V to ±22 V (4.5 V to 44 V in single-supply mode). The device also performs well with asymmetrical supplies such as V_{DD} = 12 V and V_{SS} = –5 V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 µF to 10 µF at both the V_{DD} and V_{SS} pins to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground and power planes. Always ensure the ground (GND) connection is established before supplies are ramped.

9.4 Layout

9.4.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 9-3 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

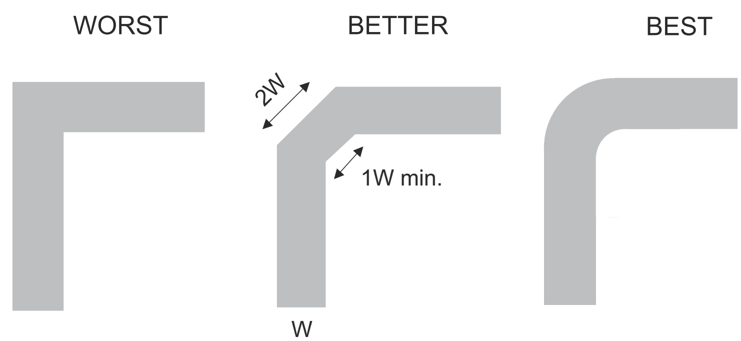


Figure 9-3. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Figure 9-4 shows an example of a PCB layout with the TMUX720x. Some key considerations are as follows:

- For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD/VSS and GND. We recommend a 0.1 µF and 1 µF capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

9.4.2 Layout Example

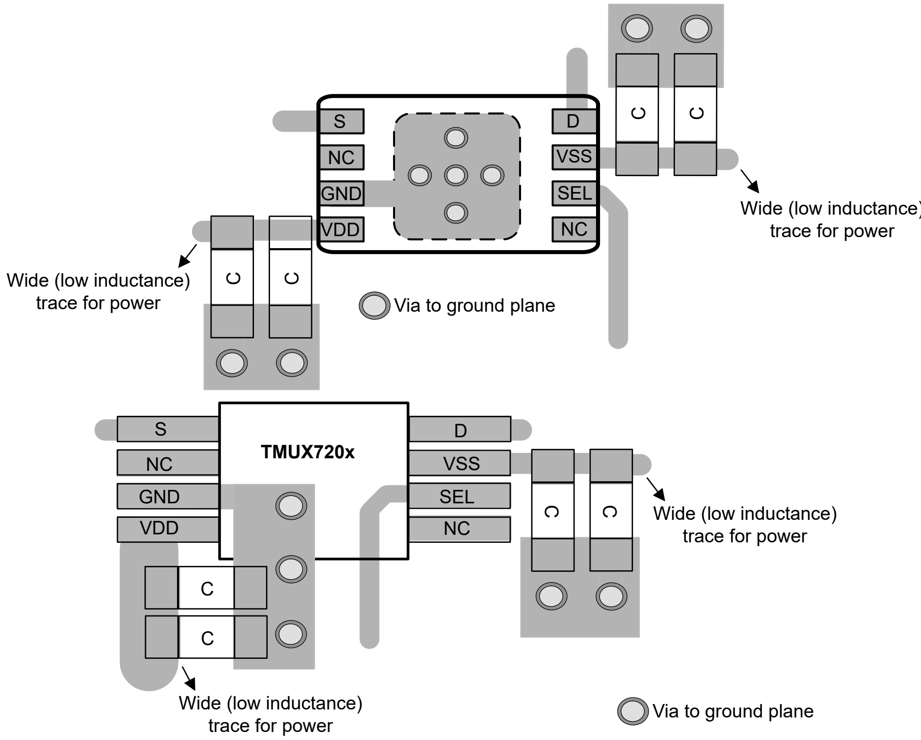


Figure 9-4. TMUX720x Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Improve Stability Issues with Low CON Multiplexers* application brief
- Texas Instruments, *Improving Signal Measurement Accuracy in Automated Test Equipment* application brief
- Texas Instruments, *Multiplexers and Signal Switches Glossary* application note
- Texas Instruments, *QFN/SON PCB Attachment* application note
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages* application note
- Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches* application brief
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers* application notes
- Texas Instruments, *True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit* circuit design

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX7201RQXR	ACTIVE	WSON	RQX	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H201	Samples
TMUX7202RQXR	ACTIVE	WSON	RQX	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H202	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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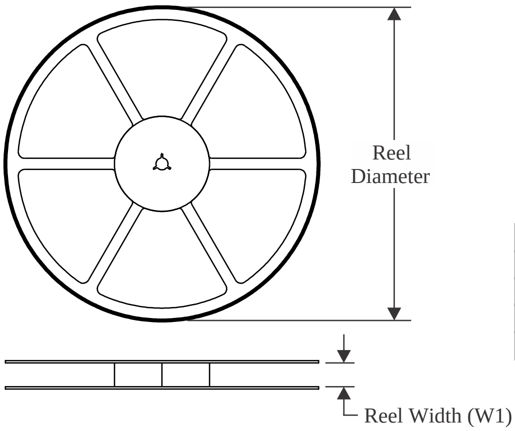
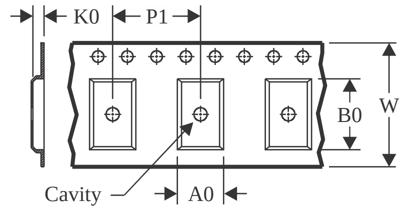
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

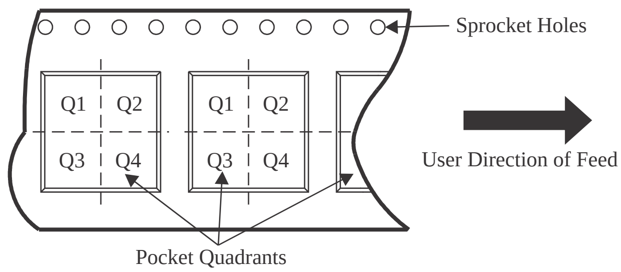


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

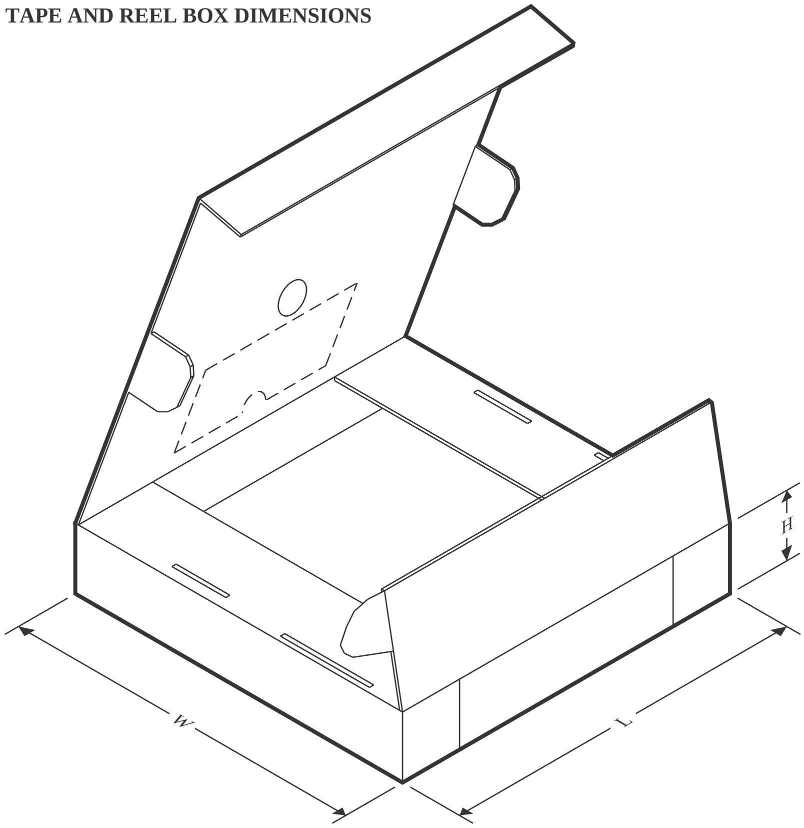
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

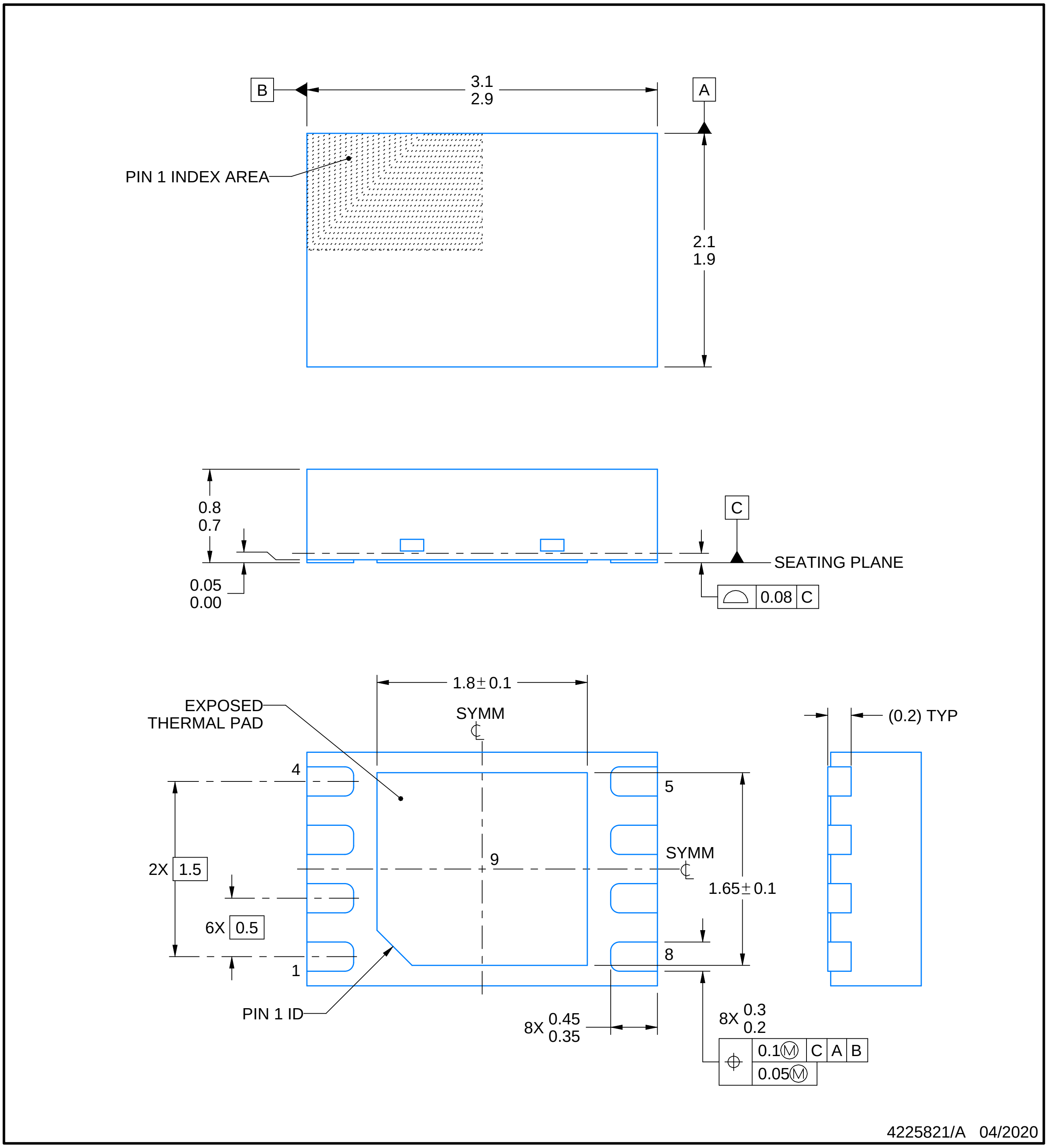
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX7201RQXR	WSON	RQX	8	2500	178.0	13.5	2.2	3.2	1.1	4.0	12.0	Q2
TMUX7202RQXR	WSON	RQX	8	2500	178.0	13.5	2.2	3.2	1.1	4.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



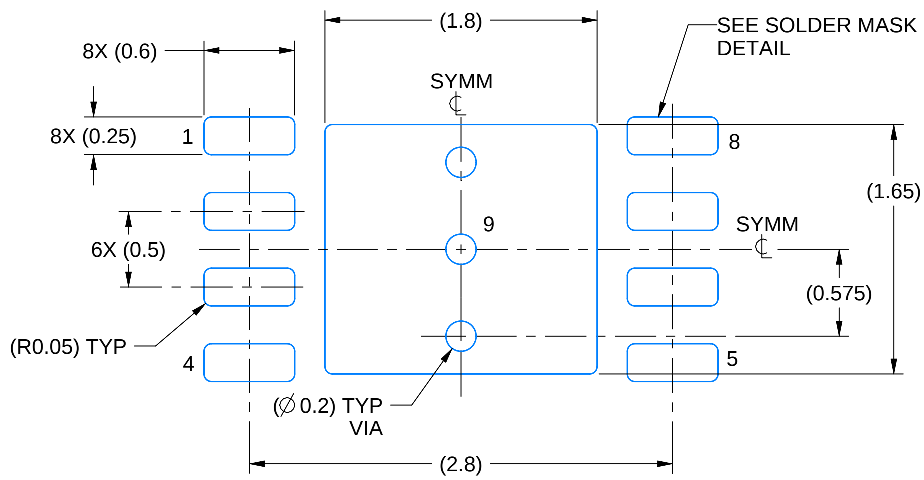
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX7201RQXR	WSON	RQX	8	2500	189.0	185.0	36.0
TMUX7202RQXR	WSON	RQX	8	2500	189.0	185.0	36.0

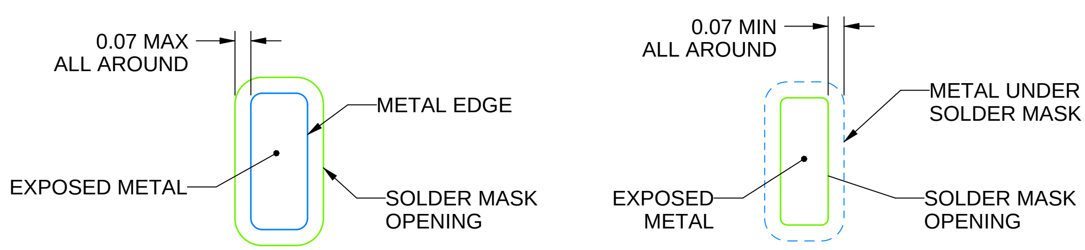


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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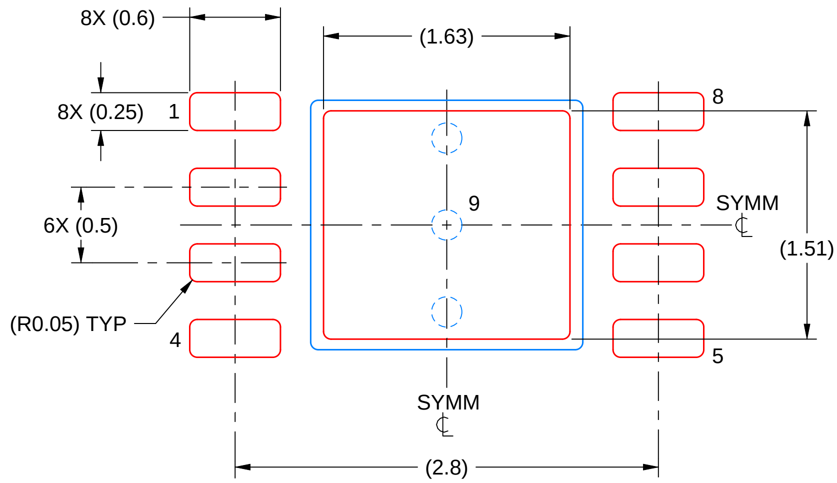
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 9
83% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225821/A 04/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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