TPD1E04U04 1-Channel ESD Protection Diode with Low $R_{\text{DYN}}$ for HDMI 2.0 and USB 3.0

1 Features

- IEC 61000-4-2 Level 4 ESD Protection
  - ±16-kV Contact Discharge
  - ±16-kV Air Gap Discharge
- IEC 61000-4-4 EFT Protection
  - 80 A (5/50 μs)
- IEC 61000-4-5 Surge Protection
  - 2.5 A (8/20 μs)
- IO Capacitance: 0.5-pF (Typ), 0.65-pF (Max)
- Ultra-low ESD Clamping Voltage
  - 8.9 V at 16-A TLP
  - –4.6 V at –16-A TLP
- Low $R_{\text{DYN}}$
  - 0.25 Ω IO to GND
  - 0.18 Ω GND to IO
- DC Breakdown Voltage: 5 V (Minimum)
- Ultra-low Leakage Current: 10 nA (Maximum)
- Supports High Speed Interfaces up to 6 Gbps
- Industrial Temperature Range: –40°C to +125°C
- Industry Standard 0402 and 0201 Packages

2 Applications

- End Equipment
  - Set-Top Boxes
  - Laptops and Desktops
  - TV and Monitors
  - Mobile and Tablets
  - DVR and NVR
- Interfaces
  - HDMI 2.0
  - HDMI 1.4b
  - USB 3.0
  - DisplayPort 1.2
  - PCI Express 3.0

3 Description

The TPD1E04U04 is a unidirectional TVS ESD protection diode for HDMI 2.0 and USB 3.0 circuit protection. The TPD1E04U04 is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard (Level 4).

This device features a 0.5-pF IO capacitance making it ideal for protecting high-speed interfaces up to 6 Gbps such as HDMI 2.0 and USB 3.0. The low dynamic resistance and ultra-low clamping voltage ensure system level protection against transient events for sensitive SoCs.

The TPD1E04U04 is offered in the industry standard 0402 (DPY) and 0201 (DPL) packages.

Device Information (1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPD1E04U04</td>
<td>X1SON (2)</td>
<td>0.60 mm × 1.00 mm</td>
</tr>
<tr>
<td>TPD1E04U04</td>
<td>X2SON (2)</td>
<td>0.60 mm × 0.30 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical HDMI 2.0 Application
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4 Revision History

Changes from Revision A (April 2016) to Revision B ........................................ Page
• Added new DPL package ........................................... 1
• Added DPL Package information in the Absolute Maximum Ratings table ........................................ 4
• Added Thermal information for DPL package in the Thermal Information table ........................................ 4
• Changed Vbr min spec from 5 V to 4.5 V in the Electrical Characteristics table ........................................ 5

Changes from Original (March 2016) to Revision A ........................................ Page
• Changed device status from Product Preview to Production Data ........................................ 1
5 Pin Configuration and Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IO</td>
<td>I/O ESD Protected Channel</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Ground. Connect to ground</td>
</tr>
</tbody>
</table>

DPL Package
2-Pin X2SON
Top View

DPY Package
2-Pin X1SON
Top View
6 Specifications

6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrical fast transient IEC 61000-4-4 (5/50 ns)</td>
<td>80</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Peak pulse IEC 61000-4-5 power ((t_p \cdot 8/20 \mu s)) - DPY Package</td>
<td>19</td>
<td>W</td>
<td></td>
</tr>
<tr>
<td>Peak pulse IEC 61000-4-5 power ((t_p \cdot 8/20 \mu s)) - DPL Package</td>
<td>16</td>
<td>W</td>
<td></td>
</tr>
<tr>
<td>Peak pulse IEC 61000-4-5 current ((t_p \cdot 8/20 \mu s))</td>
<td>2.5</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>(T_A) Operating free-air temperature</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>(T_{stg}) Storage temperature</td>
<td>–65</td>
<td>155</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>(V_{(ESD)}) Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
<td>±2500</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(2)</td>
<td>±1000</td>
<td>V</td>
</tr>
</tbody>
</table>

\(^{(1)}\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
\(^{(2)}\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

<table>
<thead>
<tr>
<th>(V_{(ESD)}) Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IEC 61000-4-2 contact discharge</td>
<td>±16000</td>
<td>V</td>
</tr>
<tr>
<td>IEC 61000-4-2 air-gap discharge</td>
<td>±16000</td>
<td>V</td>
</tr>
</tbody>
</table>

6.4 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{IO}) Input pin voltage</td>
<td>0</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>(T_A) Operating free-air temperature</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

6.5 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>TPD1E04U04</th>
<th>TPD1E04U04</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DPY (X1SON)</td>
<td>DPL (X2SON)</td>
</tr>
<tr>
<td>(R_{UA}) Junction-to-ambient thermal resistance</td>
<td>683.6</td>
<td>574</td>
</tr>
<tr>
<td>(R_{UJC(top)}) Junction-to-case (top) thermal resistance</td>
<td>494.2</td>
<td>332.2</td>
</tr>
<tr>
<td>(R_{UB}) Junction-to-board thermal resistance</td>
<td>568.7</td>
<td>237.6</td>
</tr>
<tr>
<td>(\psi_{JT}) Junction-to-top characterization parameter</td>
<td>217.4</td>
<td>150.2</td>
</tr>
<tr>
<td>(\psi_{JB}) Junction-to-board characterization parameter</td>
<td>568.7</td>
<td>238.2</td>
</tr>
<tr>
<td>(R_{UJC(bot)}) Junction-to-case (bottom) thermal resistance</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
## 6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{RWM}$</td>
<td>Reverse stand-off voltage</td>
<td>$I_O &lt; 10 \text{nA}$</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{BR}$</td>
<td>Breakdown voltage, IO pin to GND</td>
<td>$T_A = 25^\circ \text{C}^{(1)}$</td>
<td>4.5</td>
<td>6.2</td>
<td>7.5</td>
</tr>
<tr>
<td>$V_F$</td>
<td>Forward diode voltage, GND to IO pin</td>
<td>$I_O = 1 \text{mA}, ; T_A = 25^\circ \text{C}$</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{HOLD}$</td>
<td>Holding voltage</td>
<td>$I_O = 1 \text{mA}$</td>
<td>5.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{CLAMP}$</td>
<td>Clamping voltage</td>
<td>$I_{PP} = 1 \text{A}, ; \text{TLP, from IO to GND}$</td>
<td>5.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{PP} = 16 \text{A}, ; \text{TLP, from IO to GND}$</td>
<td>8.9</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{PP} = 1 \text{A}, ; \text{TLP, from GND to IO}$</td>
<td>1.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{PP} = 16 \text{A}, ; \text{TLP, from GND to IO}$</td>
<td>4.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{LEAK}$</td>
<td>Leakage current, any IO to GND</td>
<td>$V_{IO} = 2.5 \text{V}$</td>
<td>0.1</td>
<td>10</td>
<td>nA</td>
</tr>
<tr>
<td>$R_{DYN}$</td>
<td>Dynamic resistance</td>
<td>IO to GND</td>
<td>0.25</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>GND to IO</td>
<td>0.18</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_L$</td>
<td>Line capacitance</td>
<td>$V_{IO} = 0 \text{V}, ; f = 1 \text{MHz}, ; \text{IO to GND, } T_A = 25^\circ \text{C}$</td>
<td>0.5</td>
<td>0.65</td>
<td>pF</td>
</tr>
</tbody>
</table>

(1) Measured as the maximum voltage before device snaps back into $V_{HOLD}$ voltage.
6.7 Typical Characteristics

Figure 1. Positive TLP Curve

Figure 2. Negative TLP Curve

Figure 3. 8-kV IEC Waveform

Figure 4. –8-kV IEC Waveform

Figure 5. Surge Curve (t<sub>p</sub> = 8/20µs), IO Pin to GND

Figure 6. Capacitance vs Bias Voltage
Typical Characteristics (continued)

**Figure 7. Leakage Current vs Temperature**

**Figure 8. DC Voltage Sweep I-V Curve**

**Figure 9. Capacitance vs Frequency**

**Figure 10. Insertion Loss**

**Figure 11. HDMI2.0 6-Gbps TP2 Eye Diagram (Bare Board)**
Figure 12. HDMI2.0 6-Gbps TP2 Eye Diagram (With TPD1E04U04)
7 Detailed Description

7.1 Overview
The TPD1E04U04 is a unidirectional ESD Protection Diode with ultra-low capacitance designed for HDMI 2.0 and USB 3.0. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The extremely low clamping voltage and low $R_{DYN}$ make this device ideal for supporting the next-generation small feature size SoCs. The low capacitance also makes this device ideal for protecting any high-speed signal pins on these sensitive interface pins.

7.2 Functional Block Diagram

![Functional Block Diagram](image)

7.3 Feature Description

7.3.1 IEC 61000-4-2 ESD Protection
The IO pins can withstand ESD events up to ±16-kV contact and ±16-kV air gap. An ESD-surge clamp diverts the current to ground.

7.3.2 IEC 61000-4-4 EFT Protection
The IO pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground.

7.3.3 IEC 61000-4-5 Surge Protection
The IO pins can withstand surge events up to 2.5 A and 19 W (8/20 μs waveform). An ESD-surge clamp diverts this current to ground.

7.3.4 IO Capacitance
The capacitance between each IO pin to ground is 0.5-pF (typical) and 0.65-pF (maximum). This device supports data rates up to 6 Gbps.

7.3.5 Ultra-Low ESD Clamping Voltage
The IO pins feature an ESD clamp that is capable of clamping the voltage to 8.9 V ($I_{TLP} = 16$ A) and −4.6 V ($I_{TLP} = −16$ A).

7.3.6 Low $R_{DYN}$
The IO pins feature an ESD clamp that has an extremely low $R_{DYN}$ of 0.25 Ω (IO to GND) and 0.18 Ω (GND to IO) which prevents system damage during ESD events.

7.3.7 DC Breakdown Voltage
The DC breakdown voltage of each IO pin is a minimum of 5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of 3.6 V.
Feature Description (continued)

7.3.8 Ultra Low Leakage Current
The IO pins feature an ultra-low leakage current of 10 nA (maximum) with a bias of 2.5 V.

7.3.9 Supports High Speed Interfaces
This device is capable of supporting high speed interfaces up to 6 Gbps, because of the very low IO capacitance.

7.3.10 Industrial Temperature Range
This device features an industrial operating range of –40°C to +125°C.

7.3.11 Easy Flow-Through Routing Package
The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes
The TPD1E04U04 is a passive integrated circuit that triggers when voltages are above $V_{BR}$ or below $V_F$. During ESD events, voltages as high as ±16-kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of TPD1E04U04 (usually within 10s of nano-seconds) the device reverts to passive.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD1E04U04 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low $R_{\text{DYN}}$ of the triggered TVS holds this voltage, $V_{\text{CLAMP}}$, to a safe level for the protected IC.

8.2 Typical Application

8.2.1 Design Requirements

For this design example eight TPD1E04U04 devices and five TPD1E05U06 devices are being used in a HDMI 2.0 application. This provides a complete ESD protection scheme.

Given the HDMI 2.0 application, the parameters listed in Table 1 are known.

Table 1. Design Parameters

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal range on TMDS lines</td>
<td>0 V to 3.6 V</td>
</tr>
<tr>
<td>Operating frequency on TMDS lines</td>
<td>up to 3 GHz</td>
</tr>
<tr>
<td>Signal range on control lines</td>
<td>0 V to 5.5 V</td>
</tr>
</tbody>
</table>
8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The TPD1E04U04 supports signal ranges between 0 V and 3.6 V, which supports the TMDS pairs on the HDMI 2.0 application. The TPD1E05U06 supports signal ranges between 0 V and 5.5 V, which supports the control lines.

8.2.2.2 Operating Frequency

The TPD1E04U04 has a 0.5-pF (typical) capacitance, which supports the HDMI 2.0 data rates of 6-Gbps. The TPD1E05U06 has a 0.5-pF (typical) capacitance as well, which easily supports the control line data rates.

8.2.3 Application Curves

Figure 14. HDMI2.0 6-Gbps TP2 Eye Diagram (Bare Board)

Figure 15. HDMI2.0 6-Gbps TP2 Eye Diagram (With TPD1E04U04)
9 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended IO specification (0 V to 3.6 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
10.2 Layout Example

**Legend**

- □ Top Layer
- ○ VIA to GND Plane

![Layout Diagram]

Figure 16. HDMI2.0 Type-A Transmitter Port ESD Layout
11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation
For related documentation see the following:

- **TPD1E04U04 Evaluation Module User's Guide**
- **Picking ESD Diodes for Ultra High-Speed Data Lines**

11.2 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI’s views; see TI’s Terms of Use.

**TI E2E™ Online Community**  *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support**  *TI's Design Support*  Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks
E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary
SLYZ022 — *TI Glossary,*
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPD1E04U04DPLR</td>
<td>ACTIVE</td>
<td>X2SON</td>
<td>DPL</td>
<td>2</td>
<td>15000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>K</td>
<td></td>
</tr>
<tr>
<td>TPD1E04U04DPLT</td>
<td>ACTIVE</td>
<td>X2SON</td>
<td>DPL</td>
<td>2</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>K</td>
<td></td>
</tr>
<tr>
<td>TPD1E04U04DPYR</td>
<td>ACTIVE</td>
<td>X1SON</td>
<td>DPY</td>
<td>2</td>
<td>10000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>3K</td>
<td></td>
</tr>
<tr>
<td>TPD1E04U04DPYT</td>
<td>ACTIVE</td>
<td>X1SON</td>
<td>DPY</td>
<td>2</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>3K</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
## TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

![Diagram of reel dimensions](image)

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

![Diagram of quadrant assignments](image)

### PACKAGE MATERIALS INFORMATION

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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<tbody>
<tr>
<td>TPD1E04U04DPLR</td>
<td>X2SON</td>
<td>DPL</td>
<td>2</td>
<td>15000</td>
<td>178.0</td>
<td>12.3</td>
<td>0.39</td>
<td>0.68</td>
<td>0.38</td>
<td>2.0</td>
<td>8.0</td>
<td>Q1</td>
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<td>2.0</td>
<td>8.0</td>
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<td>8.0</td>
<td>Q1</td>
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<td>DPY</td>
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**Tape and Reel Box Dimensions**

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<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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<td>19.0</td>
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<td>19.0</td>
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</tbody>
</table>

*All dimensions are nominal*
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. SOIC (Small Outline No-Lead) package configuration.
DPY (R-PX1SON-N2)  PLASTIC SMALL OUTLINE NO-LEAD

Example Board Layout  Example Stencil Design
(Note E)

Non Solder Mask Defined Pad

Contact your PCB vendor for allowable solder mask clearance

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0.127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.
NOTES:  
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
B. This drawing is subject to change without notice.  
C. Small Outline No-Lead (SON) package configuration.  
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
**NOTES:**

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Publication IPC-7351 is recommended for alternate designs.

D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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