1 Features

- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 3B
  - HBM Level 15 kV
  - Device CDM ESD Classification Level C5
- IEC 61000-4-2 Level 4 ESD Protection
  - ±8-kV Contact Discharge
  - ±15-kV Air-Gap Discharge
- IEC 61000-4-5 Surge Protection
  - 5.5 A (8/20 µs)
- Low 1.5-pF Input Capacitance
- Low 10-nA Maximum Leakage Current
- 0.9-V to 5.5-V Supply Voltage Range

2 Applications

- End Equipment
  - Automotive Head Unit
  - Automotive Rear Seat Entertainment
  - Automotive Rear Camera Systems
- Interfaces
  - USB 2.0
  - Ethernet
  - Precision Analog Interfaces

3 Description

The TPD4E001-Q1 device is a low-capacitance TVS diode array designed for ESD protection in sensitive electronics connected to communication lines. Each channel consists of a pair of transient-voltage-suppression diodes that steer ESD pulses to $V_{CC}$ or GND. The TPD4E001-Q1 protects against ESD events up to ±8-kV contact discharge and ±15-kV air-gap discharge, as specified in IEC 61000-4-2 international standard. This device has a low capacitance of 1.5-pF per channel making it ideal for use in high-speed data interfaces. The low leakage current (10 nA maximum) ensures minimum power consumption for the system and high accuracy for analog interfaces.

Additionally, this device is ideal for protecting automotive head units, automotive rear seat entertainment, and automotive rear camera systems that use USB 2.0, Ethernet, or precision analog interfaces.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPD4E001-Q1</td>
<td>SOT-23 (6)</td>
<td>2.90 mm × 1.60 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Schematic
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (June 2017) to Revision F ................................. Page
• Added ISO Specification ........................................................................ 4

Changes from Revision D (March 2015) to Revision E ................................. Page
• Updated Typical Application Schematic ............................................. 9

Changes from Revision C (June 2013) to Revision D ................................. Page
• Added Pin Configuration and Functions section, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ...................................................... 1
  • Changed Device CDM ESD Classification Level from C4B to C5 ................................................................. 1

Changes from Revision B (February 2012) to Revision C ................................. Page
• Changed maximum Icc supply current in Electrical Characteristics ........................................................................ 5

Changes from Revision A (April 2013) to Revision B ................................. Page
• Revised text in DESCRIPTION section ............................................ 1
• Revised Figure 2 graph ................................................................. 5
• Revised APPLICATION INFORMATION schematic ................................. 9
5 Pin Configuration and Functions

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>NO.</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>2</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>IO1</td>
<td>1</td>
<td>I/O</td>
<td>ESD-protected channel</td>
</tr>
<tr>
<td>IO2</td>
<td>3</td>
<td>I/O</td>
<td>ESD-protected channel</td>
</tr>
<tr>
<td>IO3</td>
<td>4</td>
<td>I/O</td>
<td>ESD-protected channel</td>
</tr>
<tr>
<td>IO4</td>
<td>6</td>
<td>I/O</td>
<td>ESD-protected channel</td>
</tr>
<tr>
<td>VCC</td>
<td>5</td>
<td>I</td>
<td>Power-supply input. Bypass VCC to GND with a 0.1-μF ceramic capacitor</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) \(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CC})</td>
<td>-0.3</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IO})</td>
<td>-0.3</td>
<td>(V_{CC} + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>(I_{PP})</td>
<td>5.5</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>(P_{PP})</td>
<td>100</td>
<td>W</td>
<td></td>
</tr>
<tr>
<td>(T_A)</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>(T_J)</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>(T_{stg})</td>
<td>-65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC 61000-4-5.

6.2 ESD Ratings—AEC Specification

| \(V_{ESD}\) | Human-body model (HBM), per AEC Q100-002 \(^{(1)}\) | \(\pm 15000\) | V |
| Charged-device model (CDM), per AEC Q100-011 | \(\pm 750\) |

\(^{(1)}\) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings—IEC Specification

| \(V_{ESD}\) | IEC 61000-4-2 contact discharge | \(\pm 8000\) | V |
| IEC 61000-4-2 air-gap discharge | \(\pm 15000\) |

6.4 ESD Ratings—ISO Specification

| \(V_{ESD}\) | ISO 10605 (330 pF, 330 Ω) contact discharge | \(\pm 8000\) | V |
| ISO 10605 (330 pF, 330 Ω) air-gap discharge | \(\pm 15000\) |
6.5 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_A$ Free air operating temperature</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>$V_{CC}$ pin Operating voltage</td>
<td>0.9</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>$I_{O1, O2, O3, O4}$ pins Operating voltage</td>
<td>0</td>
<td>$V_{CC}$</td>
<td>V</td>
</tr>
</tbody>
</table>

6.6 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC$^{(1)}$</th>
<th>TPD4E001-Q1 DBV (SOT-23)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JUA}$ Junction-to-ambient thermal resistance</td>
<td>202.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JC(top)}$ Junction-to-case (top) thermal resistance</td>
<td>146.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JUB}$ Junction-to-board thermal resistance</td>
<td>47.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JT}$ Junction-to-top characterization parameter</td>
<td>37.6</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JB}$ Junction-to-board characterization parameter</td>
<td>46.7</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

$^{(1)}$ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.7 Electrical Characteristics

$V_{CC} = 5 \, V \pm 10\%$, over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP$^{(1)}$</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{CC}$ Supply current</td>
<td></td>
<td>1</td>
<td>200</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>$V_{F}$ Diode forward voltage</td>
<td>$I_F = 10 , mA$</td>
<td>0.65</td>
<td>0.95</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{BR}$ Breakdown voltage</td>
<td>$I_{BR} = 10 , mA$</td>
<td>11</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{CLAMP}$ Clamping voltage</td>
<td>Surge strike$^{(2)}$ on IO pin, GND pin grounded, $V_{CC} = 5.5 , V$, $I_{PP} = 5.5 , A$</td>
<td>16</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{RWM}$ Reverse standoff voltage</td>
<td>IO pin to GND pin</td>
<td>5.5</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{IO}$ Channel leakage current</td>
<td>$V_{IO} = \text{GND to } V_{CC}$</td>
<td>±10</td>
<td></td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>$C_{IO}$ Channel input capacitance</td>
<td>$V_{CC} = 5 , V$, bias of $V_{CC}/2$, f = 10 MHz</td>
<td>1.5</td>
<td></td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>

$^{(1)}$ Typical values are at $V_{CC} = 5 \, V$ and $T_A = 25^\circ C$.

$^{(2)}$ Non-repetitive current pulse 8/20 μs exponentially decaying waveform according to IEC 61000-4-5.
6.8 Typical Characteristics

Figure 1. IO Capacitance vs IO Voltage ($V_{CC} = 5 \text{ V}$)

Figure 2. IO Leakage Current vs Temperature

Figure 3. Peak Pulse Waveform, $V_{CC} = 5.5 \text{ V}$
7 Detailed Description

7.1 Overview
The TPD4E001-Q1 device is a low-capacitance, TVS diode array designed for ESD protection in sensitive electronics connected to communication lines. Each channel consists of a pair of transient voltage suppression diodes that steer ESD pulses to \( V_{CC} \) or GND. The TPD4E001-Q1 device protects against ESD events up to ±8-kV contact discharge and ±15-kV air-gap discharge, as specified in IEC 61000-4-2 international standard. This device has a low capacitance of 1.5-pF per channel making it ideal for use in high-speed data interfaces. The low-leakage current (10 nA maximum) ensures minimum power consumption for the system and high accuracy for analog interfaces.

7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 AEC-Q100 Qualified
This device is qualified according to the AEC-Q100 standard. The device temperature rating is Grade 1 (−40°C to +125°C). The HBM Classification Level passed is 3B (> 8 kV). The CDM Classification Level passed is C5 (all pins 750 V to <1000 V).

7.3.2 IEC 61000-4-2 Level 4 ESD Protection
The device is specified at ±8-kV contact discharge and ±15-kV air gap discharge.

7.3.3 IEC 61000-4-5 Surge Protection
This device is rated to pass at least 5.5-A of peak pulse current according to the IEC 61000-4-5 (8/20-μs pulse) standard.

7.3.4 Low 1.5-pF Input Capacitance
This device has a typical capacitance of 1.5-pF on each of the four IO pins. This allows for high speed signals on the IO pins in excess of 1 Gbps.

7.3.5 Low 10-nA (Maximum) Leakage Current
This device is rated to have a maximum leakage current of 10-nA on each of the four IO pins.

7.3.6 0.9-V to 5.5-V Supply Voltage Range
This device is specified to operate with a supply voltage (on \( V_{CC} \)) between 0.9-V and 5.5-V to ensure sufficient signal integrity.
7.4 Device Functional Modes

The TPD4E001-Q1 device is a passive integrated circuit that triggers when voltages are above $V_{BR}$ or below the lower diodes $V_F$ (−0.6 V). During ESD events, voltages as high as ±8 kV (contact) can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels of TPD4E001-Q1 (usually within 10s of nano-seconds) the device reverts back to its high-impedance state.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The TPD4E001-Q1 device is a TVS diode array which is typically used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The triggered TVS holds this voltage, $V_{\text{CLAMP}}$, to a safe level for the protected IC.

8.2 Typical Application
For this design example, one TPD4E001-Q1 device is being used in a dual USB 2.0 application. This provides a complete port protection scheme.

![Typical Application Schematic](image-url)
Typical Application (continued)

8.2.1 Design Requirements

For this design example, a single TPD4E001-Q1 device is used to protect all the pins on two USB2.0 connectors. Given the USB application, known parameters are listed in the Table 1.

Table 1. Design Parameters

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal range on IO1, IO2, IO3, or IO4</td>
<td>0 V to 3.6 V</td>
</tr>
<tr>
<td>Voltage range on V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>0 V to 5.25 V</td>
</tr>
<tr>
<td>Operating Frequency on IO1, IO2, IO3, or IO4</td>
<td>240 MHz</td>
</tr>
</tbody>
</table>

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer needs to know the following:
• Signal range on all protected lines
• Operating frequency on all protected lines

8.2.2.1 Signal Range on IO1 Through IO4

The TPD4E001-Q1 device has 4 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the 4 IO channels protects which signal lines. Any IO supports a signal range of 0 to (V<sub>CC</sub> + 0.3) V. Therefore, this device supports the USB 2.0 signal swing assuming V<sub>CC</sub> is set appropriately.

8.2.2.2 Voltage Range on V<sub>CC</sub>

The V<sub>CC</sub> pin can be connected in one of two ways:
• If the V<sub>CC</sub> pin connects to the system power supply, the TPD4E001-Q1 device works as a transient suppressor for any signal swing above V<sub>CC</sub> + V<sub>F</sub>. TI recommends a 0.1-μF capacitor on the device V<sub>CC</sub> pin for ESD bypass.
• If the V<sub>CC</sub> pin does not connect to the system power supply, the TPD4E001-Q1 device can tolerate higher signal swing in the range up to 10 V. Note that TI still recommends a 0.1-μF capacitor at the V<sub>CC</sub> pin for ESD bypass.

If this pin is connected to the USB 2.0 V<sub>BUS</sub> supply or left floating, the allowable signal swing is enough for a USB 2.0 application.

8.2.2.3 Bandwidth on IO1 Through IO4

Each IO pin on the TPD4E001-Q1 device has a typical capacitance of 1.5 pF. This capacitance is low enough to easily support USB 2.0 data rates.
8.2.3 Application Curve

Figure 5. IEC 61000-4-2 Voltage Clamp Waveform 8-kV Contact

9 Power Supply Recommendations

This device is a passive ESD protection device so there is no need to power it. Do not violate the maximum voltage specifications for each pin.
10 Layout

10.1 Layout Guidelines

When placed near the connector, the TPD4E001-Q1 device’s ESD solution offers little or no signal distortion during normal operation due to low IO capacitance and ultra-low leakage-current specifications. The TPD4E001-Q1 device ensures that the core circuitry is protected and the system is functioning properly in the event of an ESD strike. For proper operation, observe the following layout and design guidelines:

- Place the TPD4E001-Q1 device solution close to the connector. This allows the device to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
- Place a 0.1-μF capacitor very close to the VCC pin. This limits any momentary voltage surge at the IO pin during the ESD strike event.
- Ensure that there is enough metallization for the VCC and GND loop. During normal operation, the TPD4E001-Q1 device consumes nA leakage current. But during the ESD event, VCC and GND may see 15 A to 30 A of current, depending on the ESD level. Sufficient current path enables safe discharge of all the energy associated with the ESD strike.
- Leave the unused IO pins floating.
- One can connect the VCC pin in two different ways:
  a. If the VCC pin connects to the system power supply, the TPD4E001-Q1 works as a transient suppressor for any signal swing above VCC + VF. TI recommends a 0.1-μF capacitor on the device VCC pin for ESD bypass.
  b. If the VCC pin does not connect to the system power supply, the TPD4E001-Q1 can tolerate higher signal swing in the range up to 10 V. Note that TI still recommends a 0.1-μF capacitor at the VCC pin for ESD bypass.
- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example
11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation
For related documentation see the following:

- Reading and Understanding an ESD Protection Datasheet
- ESD Layout Guide

11.2 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks
E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary
SLYZ022 — TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/Ball material (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPD4E001QDBVRQ1</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>AAXQ</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPD4E001-Q1:**
Catalog: TPD4E001

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
**TAPE AND REEL INFORMATION**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width (W1) (mm)</th>
<th>A0  (mm)</th>
<th>B0  (mm)</th>
<th>K0  (mm)</th>
<th>P1  (mm)</th>
<th>W  (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPD4E001QDBVRQ1</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>3000</td>
<td>178.0</td>
<td>9.0</td>
<td>3.23</td>
<td>3.17</td>
<td>1.37</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*
### TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPD4E001QDBVRQ1</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>3000</td>
<td>180.0</td>
<td>180.0</td>
<td>18.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
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