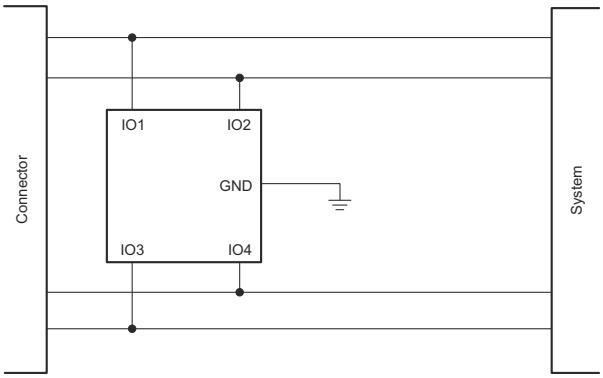
TPD4E1B06 4-Channel Ultra Low Leakage ESD Protection Device

1 Features

- Ultra low leakage current 0.5nA (maximum)
- Transient protection for 4 I/O lines:
  - IEC 61000-4-2 Contact Discharge ±12kV
  - IEC 61000-4-2 Air-Gap Discharge ±15kV
  - IEC 61000-4-5 Surge 3.0A (8/20µs)
- I/O capacitance 0.7pF (typical)
- Bi-directional ESD protection diode array
- Low ESD clamping voltage
- Industrial temperature range: –40°C to 125°C
- Small, easy-to-route DRL and DCK packages

2 Applications

- Glucose meter
- Tablets
- GPS
- Portable media players
- TV
- Set-top box



Simplified Schematic

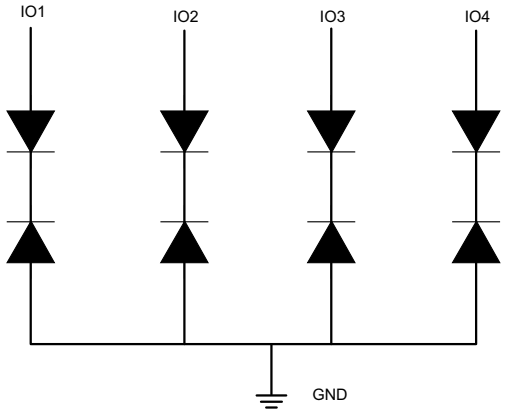
3 Description

The TPD4E1B06 is a 4-channel bi-directional Electrostatic Discharge (ESD) protection diode array. This device features ultra low leakage current (0.5nA) for precision analog measurements. The ±12kV contact and ±15kV air gap ESD protection exceeds IEC 61000-4-2 level 4 requirements. The TPD4E1B06 device's 0.7pF line capacitance makes it suitable for precision analog, USB2.0, Ethernet, SATA, LVDS, and 1394 interfaces.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPD4E1B06	DCK (SC70, 6)	2mm × 2.1mm
	DRL (SOT, 6)	1.6mm × 1.6mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

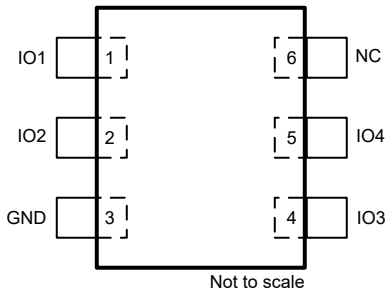

Figure 4-1. DCK Package, 6-Pin SC70 (Top View)

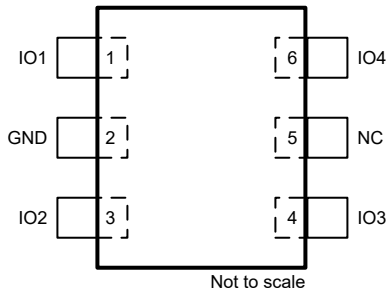

Figure 4-2. DRL Package, 6-Pin SOT (Top View)

Table 4-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	DCK	DRL		
IO1	1	1	I/O	ESD protected channel. Connect to data line as close to the connector as possible.
IO2	2	3	I/O	ESD protected channel. Connect to data line as close to the connector as possible.
IO3	4	4	I/O	ESD protected channel. Connect to data line as close to the connector as possible.
IO4	5	6	I/O	ESD protected channel. Connect to data line as close to the connector as possible.
GND	3	2	GND	Ground
NC	6	5	NC	Not internally connected

(1) I = input, O = output, GND = ground, NC = no connection

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
Operating temperature range	–40	125	°C
I_{PP}, peak pulse current (tp = 8/20 µs), IO pin to GND		3.0	A
P_{PP}, peak pulse power (tp = 8/20 µs)		45	W

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	155	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	–4.0	4.0	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	–1.5	1.5	
		IEC 61000-4-2 contact ESD	–12	12	
		IEC 61000-4-2 air-gap ESD	–15	15	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as 4 kV may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 1.5 kV may actually have higher performance.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	The voltage between any two device pins should not exceed 5.5 V	–5.5	5.5	V
T_A	Operating free-air temperature	–40	125	°C

5.4 Thermal Information

THERMAL METRIC[1]		TPD4E1B06		UNIT
		DCK	DRL	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	227.3	233.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.5	95.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	72.1	68.1	
ψ_{JT}	Junction-to-top characterization parameter	3.6	7.6	
ψ_{JB}	Junction-to-board characterization parameter	70.4	67.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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5.5 Electrical Characteristics

T_A = 25°C

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage		–5.5		5.5	V
V_{CLAMP}	Clamp voltage with ESD strike, IO to GND	I_{PP} = 1 A, tp = 8/20 µSec, from I/O to GND or GND to I/O		10.9		V
		I_{PP} = 3 A, tp = 8/20 µSec, from I/O to GND or GND to I/O		14.5		V
R_{DYN}	Dynamic resistance	I_{TLP} = 10 A to 20 A, I/O to GND		1		Ω
		I_{TLP} = 10 A to 20 A, GND to I/O		0.8		
C_L	Line capacitance	f = 1 MHz, V_{BIAS} = 2.5 V		0.7	0.95	pF
V_{BR}	Break-down voltage	I_{IO} = 1 mA, from I/O to GND or GND to I/O	7		9.5	V
I_{LEAK}	Leakage current	V_{IO} = 2.5 V			0.5	nA

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5.6 Typical Characteristics

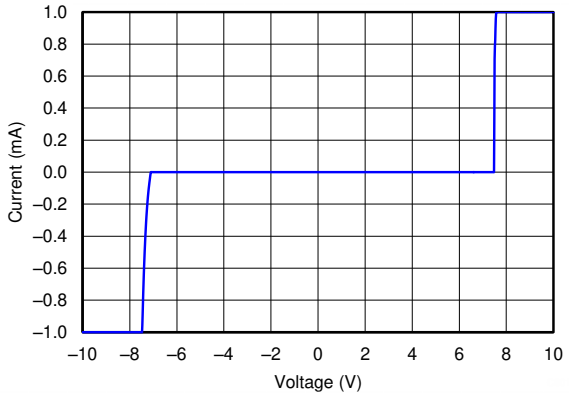

Figure 5-1. DC Voltage Sweep I-V Curve

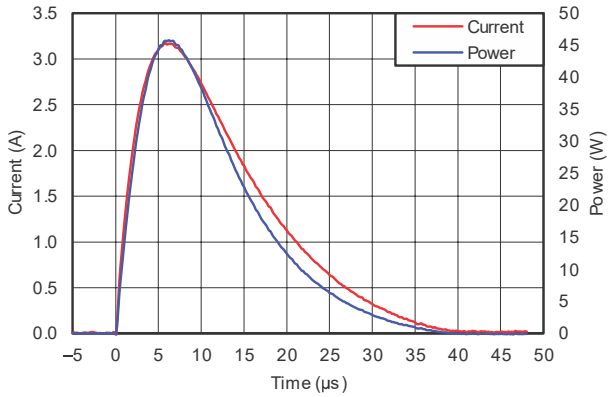

Figure 5-2. Surge Curve (tp = 8/20 µs), Pin IO to GND

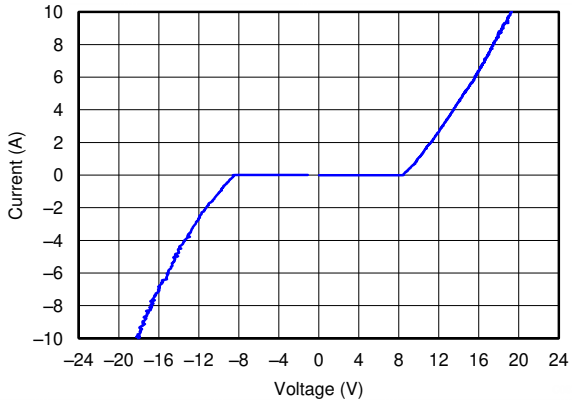

Figure 5-3. TLP Plot IO to GND

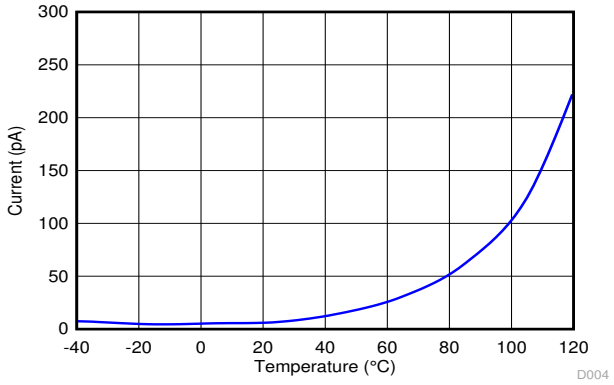

Figure 5-4. Leakage vs Temperature

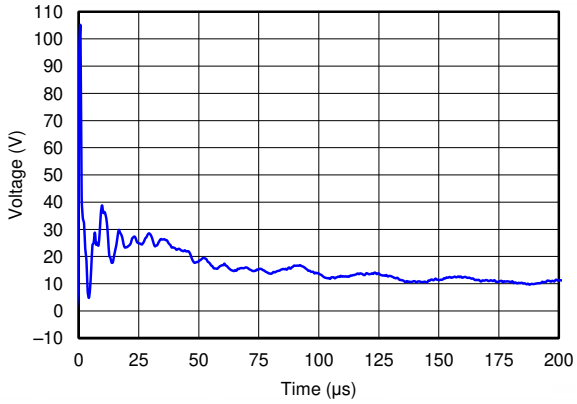

Figure 5-5. +8 kV IEC Waveform

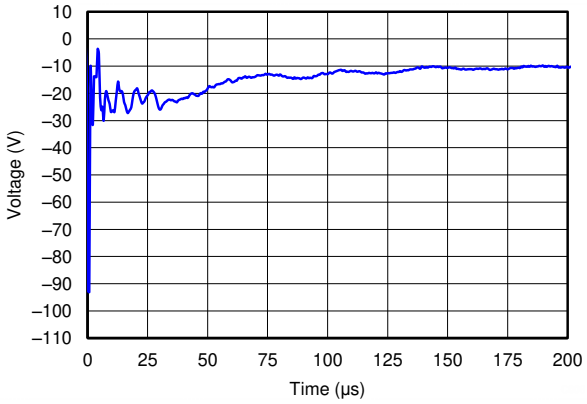

Figure 5-6. –8 kV IEC Waveform

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5.6 Typical Characteristics (continued)

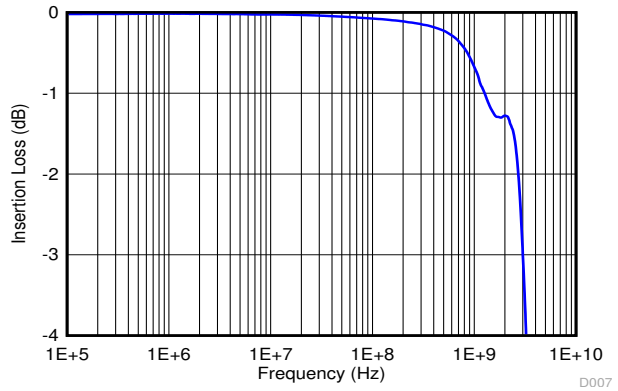


Figure 5-7. Insertion Loss

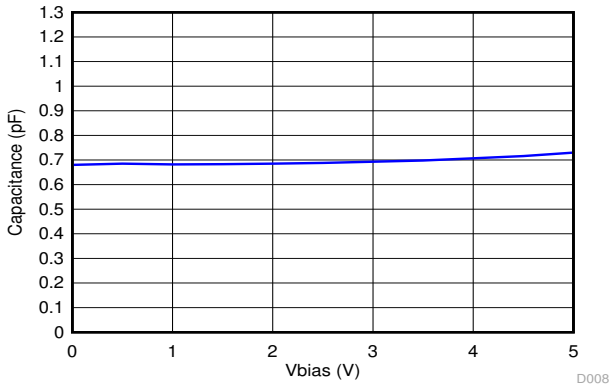


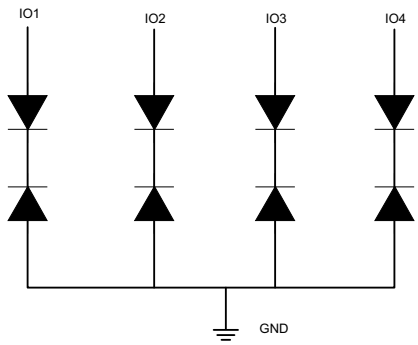
Figure 5-8. Capacitance vs V_{BIAS}

6 Detailed Description

6.1 Overview

The TPD4E1B06 is a 4-channel bi-directional Electrostatic Discharge (ESD) protection diode array. This device features ultra low leakage current (0.5 nA) for precision analog measurements. The ±12 kV contact and ±15 kV air gap ESD protection exceeds IEC 61000-4-2 level 4 requirements. The TPD4E1B06 0.7 pF line capacitance makes it suitable for precision analog, USB2.0, Ethernet, SATA, LVDS, and 1394 interfaces.

6.2 Functional Block Diagram



6.3 Feature Description

TPD4E1B06 diode array structure uses back-to-back diode topology to accommodate bi-directional signaling between –5.5 V and 5.5 V. Each pin has an additional 2 steering diodes, including the ground pin. The Zener diodes are not meant to be forward biased, creating the need for having the steering diodes. If there is +8 V on IO1 and 0V on IO2, the IO1 Zener diode will breakdown and forward bias one of the steering diodes on IO2. The current will then flow out of IO2.

6.3.1 Ultra Low Leakage Current 0.5 nA (Maximum)

TPD4E1B06 ultra-low leakage current supports long battery life and allows for precision analog measurements.

6.3.2 Transient Protection for 4 I/O Lines

The four I/O pins of TPD4E1B06 can withstand ESD events up to ±12 kV contact and ±15 kV air gap per IEC61000-4-2.

6.3.3 I/O Capacitance 0.7 pF (Typical)

TPD4E1B06 I/O pins present an ultra-low 0.7 pF capacitance to the protected signal lines, making it suitable for a wide range of applications.

6.3.4 Bi-Directional (ESD) Protection Diode Array

TPD4E1B06 diode array structure uses back to back diode topology to accommodate bi-directional signaling between –5.5 V and 5.5 V.

6.3.5 Low ESD Clamping Voltage

TPD4E1B06 clamps ESD events to a safe level to protect system components.

6.4 Device Functional Modes

TPD4E1B06 is a passive integrated circuit that activates whenever fast transient voltages above V_{BR} or below $–V_{BR}$ are present on the circuit being protected. During ESD events, voltages as high as ±12 kV can be directed to ground through the internal diode network. Once the voltages on the protected line fall below the trigger levels of TPD4E1B06 (usually within 10's of nano-seconds) the device reverts to passive.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

TPD4E1B06 is an ESD protection diode array which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the diode, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered diode holds this voltage, V_{CLAMP}, to a safe level to the protected IC.

7.2 Typical Application

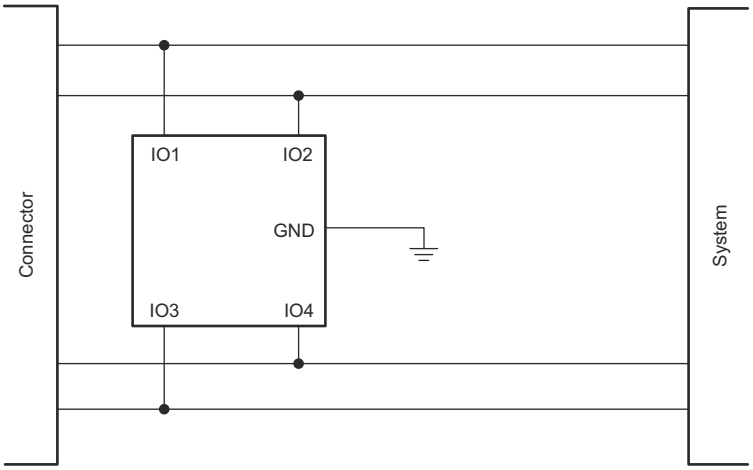

Figure 7-1. Protecting a Pair of Bi-Directional Differential Data Lines

The typical application of the TBD4E1B06 is to be placed in between the connector and the system. The low capacitance of the TBD4E1B06 gives flexibility in the end application, as it can be used on many different high speed interfaces.

7.2.1 Design Requirements

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Signal range on IO1, IO2, IO3, IO4 Pins	–5.5 V to 5.5 V
Operating frequency	1.7 GHz

7.2.2 Detailed Design Procedure

The designer needs to know the following:

- Signal range on all the protected lines
- Operating frequency

7.2.2.1 Signal Range on IO1, IO2, IO3, and IO4 Pins

TPD4E1B06 has 4 protection channels for signal lines. Any I/O will support a signal range of –5.5 V to 5.5 V.

7.2.2.2 Operating Frequency

The 0.7 pF capacitance of each I/O channel supports data rates up to 3.4 Gbps.

7.2.3 Application Curves

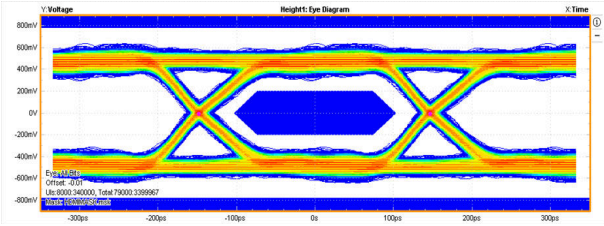

Figure 7-2. 3.4 Gbps HDMI 1.4 Eye Diagram in DCK Package

7.3 Layout

7.3.1 Layout Guidelines

- Place the device as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer should minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the diode and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the diode and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

7.3.2 Layout Examples

Figure 7-3 shows a layout example for theTPD4E1B06DCK. Pins 1 and 2 and 4 and 5 are routed differentially. Pin 3 is routed to the ground plane. Pin 6 does not have an internal connection in the device and does not need to be routed anywhere on the board. It is also acceptable to connect pin 6 to the ground plane.

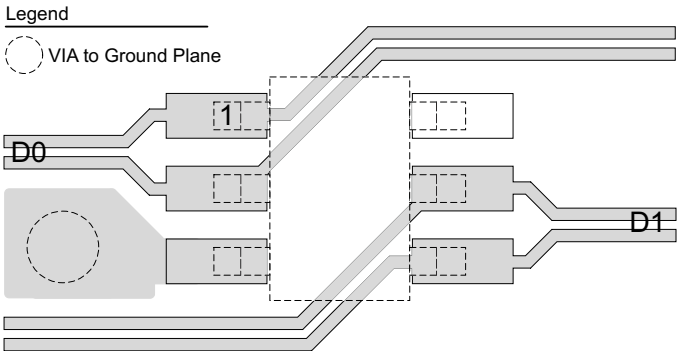

Figure 7-3. DCK Layout Example Showing Two Data Pairs, D0 and D1

Figure 7-4 shows a layout example for theTPD4E1B06DRL. Pins 1 and 6 and 3 and 4 are routed differentially. Pin 2 is routed to the ground plane. Pin 5 does not have an internal connection in the device and does not need to be routed anywhere on the board. It is also acceptable to connect pin 5 to the ground plane.

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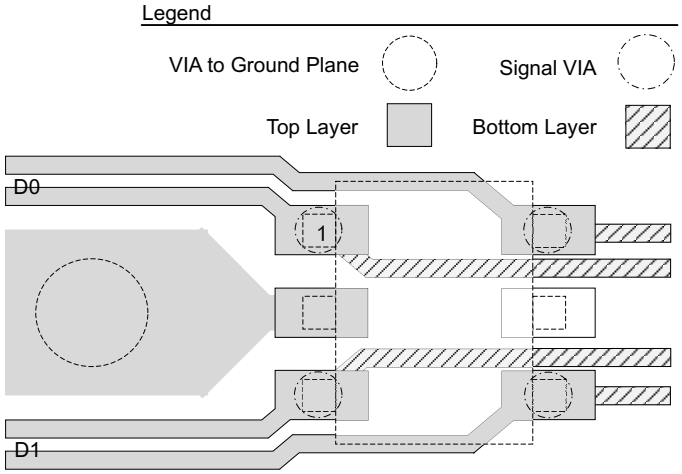

Figure 7-4. DRL Layout Example Showing Two Data Pairs, D0 and D1

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (October 2023) to Revision E (October 2024)	Page
• Updated Figure 4-1	3

Changes from Revision C (July 2014) to Revision D (October 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the *Package Information* table to include package lead size	1
• Updated the *Feature Description* section	8
• Updated the *Bi-directional (ESD) Protection Diode Array* section	8

Changes from Revision B (May 2014) to Revision C (July 2014)	Page
• Changed 2 device names from TPD4E6B06 to TPD4E1B06	9

Changes from Revision A (January 2013) to Revision B (May 2014)	Page
• Added DRL package to data sheet	1
• Changed I_{PP}, peak pulse current from 3.5 A to 3.0 A	4
• Added the ESD Ratings table	4
• Added Recommended Operating Conditions table	4
• Changed Electrical Characteristics table to reflect operating conditions at 25 °C	5
• Added MIN V_{RWM} value of –5.5 V	5
• Changed V_{CLAMP} at I_{PP} = 1 A from 10.5 V to 10.9 V.	5
• Changed Line Capacitance TYP value from 1 pF to 0.7 pF	5
• Added Line Capacitance MAX value of 0.95 pF.	5
• Changed I_{LEAK} from MAX of 10 nA to 0.5 nA	5

Changes from Revision * (December 2012) to Revision A (January 2013)	Page
• Fixed "f" units typo from GHz to MHz for C_L parameter in ELECTRICAL CHARACTERISTICS table	5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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