The TPIC6273 is a monolithic high-voltage high-current power logic octal D-type latch with DMOS transistor outputs designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

The TPIC6273 contains eight positive-edge-triggered D-type flip-flops with a direct clear input. Each flip-flop features an open-drain power DMOS transistor output.

When clear (CLR) is high, information at the D inputs meeting the setup time requirements is transferred to the DRAIN outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input (CLK) is at either the high or low level, the D input signal has no effect at the output. An asynchronous CLR is provided to turn all eight DMOS-transistor outputs off.

The TPIC6273 is characterized for operation over the operating case temperature range of \(-40^\circ\text{C}\) to \(125^\circ\text{C}\).
logic diagram (positive logic)
schematic of inputs and outputs

absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, \( V_{CC} \) (see Note 1) .................................................. 7 V
Logic input voltage range, \( V_I \) .......................................................... \(-0.3\) V to 7 V
Power DMOS drain-to-source voltage, \( V_{DS} \) (see Note 2) .................................. 45 V
Continuous source-drain diode anode current .................................................. 1 A
Pulsed source-drain diode anode current ......................................................... 2 A
Pulsed drain current, each output, all outputs on, \( I_{DN}, T_A = 25\degree C \) (see Note 3) . 750 mA
Continuous drain current, each output, all outputs on, \( I_{DN}, T_A = 25\degree C \) .................. 250 mA
Peak drain current single output, \( I_{DM}, T_A = 25\degree C \) (see Note 3) ......................... 2 A
Single-pulse avalanche energy, \( E_{AS} \) (see Figure 4) ........................................ 75 mJ
Avalanche current, \( I_{AS} \) (see Note 4) ......................................................... 1 A
Continuous total power dissipation .................................................................... See Dissipation Rating Table
Operating junction temperature range, \( T_J \) ................................................... \(-40\degree C\) to 150\degree C
Storage temperature range, \( T_{stg} \) ................................................................. \(-65\degree C\) to 150\degree C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds ...................... 260\degree C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Each power DMOS source is internally connected to GND.
3. Pulse duration \( \leq 100 \mu s \), duty cycle \( \leq 2\% \)
4. DRAIN supply voltage = 15 V, starting junction temperature \( T_{JS} = 25\degree C \), \( L = 100 \text{ mH}, I_{AS} = 1 \text{ A} \) (see Figure 4).

DISSIPATION RATING TABLE

<table>
<thead>
<tr>
<th>PACKAGE</th>
<th>( T_A \leq 25\degree C ) POWER RATING</th>
<th>DERATING FACTOR ABOVE ( T_A = 25\degree C )</th>
<th>( T_A = 125\degree C ) POWER RATING</th>
</tr>
</thead>
<tbody>
<tr>
<td>DW</td>
<td>1125 mW</td>
<td>9.0 mW/\degree C</td>
<td>225 mW</td>
</tr>
<tr>
<td>N</td>
<td>1150 mW</td>
<td>9.2 mW/\degree C</td>
<td>230 mW</td>
</tr>
</tbody>
</table>
recommended operating conditions over recommended operating temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic supply voltage, ( V_{CC} )</td>
<td>4.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>High-level input voltage, ( V_{IH} )</td>
<td>0.85 ( V_{CC} )</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Low-level input voltage, ( V_{IL} )</td>
<td>0.15 ( V_{CC} )</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Pulsed drain output current, ( T_{C} = 25^\circ C, V_{CC} = 5 ) V (see Notes 3 and 5)</td>
<td>-1.8</td>
<td>1.5</td>
<td>A</td>
</tr>
<tr>
<td>Setup time, D high before CLK( \uparrow ), ( t_{SU} ) (see Figure 2)</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Hold time, D high after CLK( \uparrow ), ( t_{H} ) (see Figure 2)</td>
<td>15</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Pulse duration, ( t_{W} ) (see Figure 2)</td>
<td>25</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Operating case temperature, ( T_{C} )</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

electrical characteristics, \( V_{CC} = 5 \) V, \( T_{C} = 25^\circ C \) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{(BR)DSX} ) Drain-source breakdown voltage</td>
<td>( I_{D} = 1 ) mA</td>
<td>45</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{SD} ) Source-drain diode forward voltage</td>
<td>( I_{F} = 250 ) mA, See Note 3</td>
<td>0.85</td>
<td>1</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{IH} ) High-level input current</td>
<td>( V_{CC} = 5.5 ) V, ( V_{I} = V_{CC} )</td>
<td>1</td>
<td></td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( I_{IL} ) Low-level input current</td>
<td>( V_{CC} = 5.5 ) V, ( V_{I} = 0 )</td>
<td>1</td>
<td></td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( I_{CC} ) Logic supply current</td>
<td>( I_{O} = 0 ), All inputs low</td>
<td>15</td>
<td>100</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( I_{N} ) Nominal current</td>
<td>( V_{DS(on)} = 0.5 ) V, ( I_{N} = I_{D} ), ( T_{C} = 85^\circ C )</td>
<td>250</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( I_{DSX} ) Off-state drain current</td>
<td>( V_{DS} = 40 ) V</td>
<td>0.05</td>
<td>1</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( I_{DSX} ) Off-state drain current</td>
<td>( V_{DS} = 40 ) V, ( T_{C} = 125^\circ C )</td>
<td>0.15</td>
<td>5</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( r_{DS(on)} ) Static drain-source on-state resistance</td>
<td>( I_{D} = 250 ) mA, ( V_{CC} = 4.5 ) V</td>
<td>1.3</td>
<td>2</td>
<td>( \Omega )</td>
<td></td>
</tr>
<tr>
<td>( r_{DS(on)} ) Static drain-source on-state resistance</td>
<td>( I_{D} = 250 ) mA, ( T_{C} = 125^\circ C ), ( V_{CC} = 4.5 ) V</td>
<td>2</td>
<td>3.2</td>
<td>( \Omega )</td>
<td></td>
</tr>
<tr>
<td>( r_{DS(on)} ) Static drain-source on-state resistance</td>
<td>( I_{D} = 500 ) mA, ( V_{CC} = 4.5 ) V</td>
<td>1.3</td>
<td>2</td>
<td>( \Omega )</td>
<td></td>
</tr>
</tbody>
</table>

switching characteristics, \( V_{CC} = 5 \) V, \( T_{C} = 25^\circ C \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{PLH} ) Propagation delay time, low-to-high-level output from CLK</td>
<td>( Q_{L} = 30 ) pF, ( I_{D} = 250 ) mA, See Figures 1, 2, and 10</td>
<td>625</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{PHL} ) Propagation delay time, high-to-low-level output from CLK</td>
<td>( I_{F} = 250 ) mA, di/dt = 20 A/( \mu )s, See Notes 5 and 6</td>
<td>150</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{r} ) Rise time, drain output</td>
<td>( I_{F} = 250 ) mA, ( t_{r} ) = 20 A/( \mu )s, See Notes 5 and 6 and Figures 8 and 9</td>
<td>675</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{a} ) Fall time, drain output</td>
<td>( I_{F} = 250 ) mA, ( t_{a} ) = 20 A/( \mu )s, See Notes 5 and 6 and Figure 3</td>
<td>400</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{d} ) Reverse-recovery-current rise time</td>
<td>( I_{F} = 250 ) mA, di/dt = 20 A/( \mu )s, See Notes 5 and 6 and Figure 3</td>
<td>100</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{r} ) Reverse-recovery time</td>
<td>( I_{F} = 250 ) mA, di/dt = 20 A/( \mu )s, See Notes 5 and 6 and Figure 3</td>
<td>300</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

NOTES:
3. Pulse duration \( \leq 100 \) \( \mu \)s, duty cycle \( \leq 2\% \)
5. Technique should limit \( T_{J} – T_{C} \) to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at \( T_{C} = 85^\circ C \).

thermal resistance

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{0JA} ) Thermal resistance, junction-to-ambient</td>
<td>DW package, All 8 outputs with equal power</td>
<td>111</td>
<td>108</td>
<td>°C/W</td>
</tr>
</tbody>
</table>
PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

VCC

DUT

CLK

D

DRAIN

GND

Word Generator
(see Note A)

11

1

5 V

20

24 V

Ip

R_L = 95 Ω

CLR

4–7, 14–17

Output

C_L = 30 pF
(see Note B)

VOLTAGE WAVEFORMS

CLK

D

Output

Figure 1. Resistive Load Normal Operation

TEST CIRCUIT

VCC

DUT

CLK

D

DRAIN

GND

Word Generator
(see Note A)

11

1

5 V

20

24 V

Ip

R_L = 95 Ω

CLR

4–7, 14–17

Output

C_L = 30 pF
(see Note B)

SWITCHING TIMES

CLK

D

D

5 V

0 V

24 V

10%

90%

90%

10%

20

10

1

11

24 V

4–7, 14–17

Output

C_L = 30 pF
(see Note B)

INPUT SETUP AND HOLD WAVEFORMS

CLK

D

5 V

0 V

5 V

0 V

5 V

0 V

Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

NOTES:  
A. The word generator has the following characteristics: t_r ≤ 10 ns, t_f ≤ 10 ns, t_w = 300 ns, pulsed repetition rate (PRR) = 5 KHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
PARAMETER MEASUREMENT INFORMATION

NOTES:  
A. The VGG amplitude and RG are adjusted for di/dt = 20 A/µs. A VGG double-pulse train is used to set IF = 0.25 A, where t1 = 10 µs, t2 = 7 µs, and t3 = 3 µs.  
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode

NOTES:  
A. The word generator A has the following characteristics: trif ≤ 10 ns, tff ≤ 10 ns, ZO = 50 Ω.  
B. Input pulse duration, tw, is increased until peak current IAS = 1 A. 
Energy test is defined as EAS = IAS x V(BR)DSX x tav/2 = 75 mJ, where tav = avalanche time.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms
TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

MAXIMUM CONTINUOUS DRAIN CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

Figure 5

Figure 6

Figure 7
TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE VS DRAIN CURRENT

- $V_{CC} = 5 \text{ V}$
- $I_D = 250 \text{ mA}$

See Note A

$T_C = 125 \degree C$
$T_C = 25 \degree C$
$T_C = -40 \degree C$

Figure 8

STATIC DRAIN-SOURCE ON-STATE RESISTANCE VS LOGIC SUPPLY VOLTAGE

- $V_{CC}$ – Logic Supply Voltage – $V$
- $I_D = 250 \text{ mA}$

See Note A

$T_C = 125 \degree C$
$T_C = 25 \degree C$
$T_C = -40 \degree C$

Figure 9

SWITCHING TIME VS FREE-AIR TEMPERATURE

- $t_{PLH}$
- $t_{PHL}$
- $t_f$
- $t_r$
- $I_D = 250 \text{ mA}$

See Note A

Figure 10

NOTE A: Technique should limit $T_J - T_C$ to 10\degree C maximum.
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPIC6273DW</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>25</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>TPIC6273</td>
<td></td>
</tr>
<tr>
<td>TPIC6273DWG4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>25</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>TPIC6273</td>
<td></td>
</tr>
<tr>
<td>TPIC6273DWR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>2000</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>TPIC6273</td>
<td></td>
</tr>
<tr>
<td>TPIC6273DWRG4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>2000</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>TPIC6273</td>
<td></td>
</tr>
<tr>
<td>TPIC6273N</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>N</td>
<td>20</td>
<td>20</td>
<td>Pb-Free (RoHS)</td>
<td>NIPDAU</td>
<td>N / A for Pkg Type</td>
<td>-40 to 125</td>
<td>TPIC6273N</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substances do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
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## TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

### PACKAGE MATERIALS INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0  (mm)</th>
<th>B0  (mm)</th>
<th>K0  (mm)</th>
<th>P1  (mm)</th>
<th>W  (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPIC6273DWR</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>2000</td>
<td>330.0</td>
<td>24.4</td>
<td>10.8</td>
<td>13.3</td>
<td>2.7</td>
<td>12.0</td>
<td>24.0</td>
<td>Q1</td>
</tr>
<tr>
<td>TPIC6273DWRG4</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>2000</td>
<td>330.0</td>
<td>24.4</td>
<td>10.8</td>
<td>13.3</td>
<td>2.7</td>
<td>12.0</td>
<td>24.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*
<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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</thead>
<tbody>
<tr>
<td>TPIC6273DWR</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>2000</td>
<td>350.0</td>
<td>350.0</td>
<td>43.0</td>
</tr>
<tr>
<td>TPIC6273DWRG4</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>2000</td>
<td>350.0</td>
<td>350.0</td>
<td>43.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
\[\Delta\] Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
\[\Delta\] The 20 pin end lead shoulder width is a vendor option, either half or full width.
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
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