TEXAS INSTRUMENTS
TPL1401
SNAS806 – SEPTEMBER 2020

TPL1401 256-Tap, High-Accuracy, Digital Potentiometer With Buffered Wiper

1 Features

- 256-position digital potentiometer for voltage-divider applications
- 1 LSB INL and DNL
- Wide operating range
  - Power supply: 1.8 V to 5.5 V
  - Temperature range: –40°C to +125°C
- Buffered wiper for improved load regulation
- FB pin for precision current sink applications
- Wiper lock function to protect from accidental writes to the digital potentiometer
- I^2C interface
  - Standard, fast, and fast plus modes
  - 1.62-V V_{IH} with V_{DD} = 5.5 V
- User-programmable nonvolatile memory (NVM/EEPROM)
  - Save and recall all register settings
- Internal reference
- Very low power: 0.2 mA at 1.8 V
- Flexible startup: High impedance or 10K-GND
- Tiny package: 8-pin WSON (2 mm × 2 mm)

2 Applications

- Exit and emergency lighting
- Barcode scanner
- Barcode reader
- Smart speaker
- Video doorbell
- Cordless vacuum cleaner
- Robotic lawn mower
- Laser distance meter

3 Description

The TPL1401 is a digital potentiometer (digipot) with a buffered wiper. Unlike standard digipots, this device offers higher load regulation in voltage-divider applications as a result of the integrated buffered wiper.

The TPL1401 makes in-factory calibration and trimming easier with integrated nonvolatile memory (NVM), and a simple I^2C digital interface to communicate with the device. This device supports I^2C standard mode (100 kbps), fast mode (400 kbps), and fast mode plus (1 Mbps).

The TPL1401 operates with either the internal reference or with the power supply as the reference, and provides a full-scale output of 1.8 V to 5.5 V. This device also includes a wiper lock feature, a feedback (FB) pin for current-sink applications, and two bytes of user-programmable NVM space. The TPL1401 has a power-on-reset (POR) circuit that makes sure all the registers start with default or user-programmed settings using NVM. The digipot output powers on in high-impedance mode (default); this setting can be programmed to 10kΩ-GND using NVM.

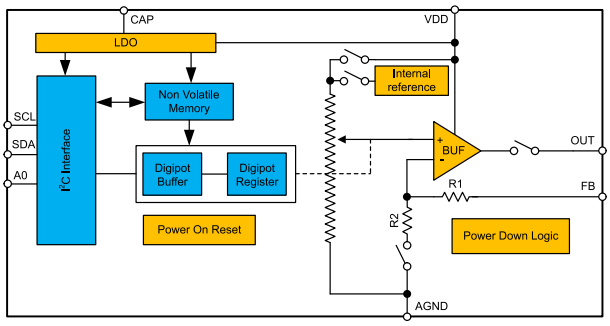
The TPL1401 is tiny, feature rich, and an easy-to-use building block device that can be integrated into many applications.

The TPL1401 operates within the temperature range of –40°C to +125°C.

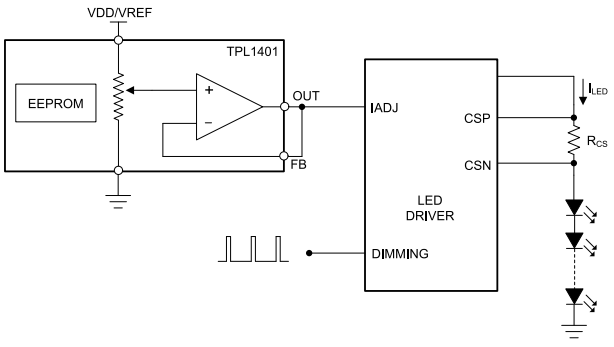
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPL1401	WSON (8)	2.00 mm × 2.00 mm

(1) For all available packages, refer to the package option addendum at the end of the data sheet.



Functional Block Diagram



Programmable Current Limit With TPL1401

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4 Revision History

DATE	REVISION	NOTES
September 2020	*	Initial release.

5 Pin Configuration and Functions

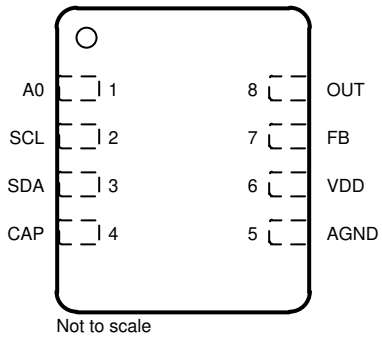


Figure 5-1. DSG Package, 8-Pin WSON, Top View

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A0	1	Input	Four-state address input
AGND	5	Ground	Ground reference point for all circuitry on the device
CAP	4	Input	External capacitor for the internal LDO. Connect a capacitor (around 1.5 µF) between CAP and AGND.
FB	7	Input	Voltage feedback pin
OUT	8	Output	Analog output voltage from digipot buffer
SCL	2	Input	Serial interface clock. This pin must be connected to the supply voltage with an external pullup resistor.
SDA	3	Input/output	Data are clocked into or out of the input register. This pin is a bidirectional, and must be connected to the supply voltage with an external pullup resistor.
VDD	6	Power or reference input	Analog supply voltage: 1.8 V to 5.5 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage / reference, V_{DD} to A_{GND}	–0.3	6	V
	Digital input(s) to A_{GND}	–0.3	V_{DD} + 0.3	V
	CAP to A_{GND}	–0.3	1.65	V
	V_{FB} to A_{GND}	–0.3	V_{DD} + 0.3	V
	V_{OUT} to A_{GND}	–0.3	V_{DD} + 0.3	V
	Current into any pin	–10	10	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, pins 1, 4, 5, 8(2)	±750	
		Charged device model (CDM), per JEDEC specification JESD22-C101, pins 2, 3, 6, 7(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Positive supply voltage to ground (A_{GND})	1.71		5.5	V
V_{IH}	Digital input high voltage, 1.7 V < V_{DD} ≤ 5.5 V	1.62			V
V_{IL}	Digital input low voltage			0.4	V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPL1401 DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

all minimum/maximum specifications at T_A = –40°C to +125°C and typical specifications at T_A = 25°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, reference tied to V_{DD}, gain = 1x, digipot output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), and digital inputs at V_{DD} or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution		8			Bits
INL	Relative accuracy(1)		–1		1	LSB
DNL	Differential nonlinearity(1)		–1		1	LSB
	Zero code error	Code 0d into digipot		6	12	mV
		Internal V_{REF}, gain = 4x, V_{DD} = 5.5 V		6	15	
	Zero code error temperature coefficient			±10		µV/°C
	Offset error	V_{REF} tied to V_{DD}, measured between end-point codes 2d and 254d, output unloaded	–0.5	0.25	0.5	%FSR
	Offset error temperature coefficient	V_{REF} tied to V_{DD}, measured between end-point codes 2d and 254d, output unloaded		±0.0003		%FSR/°C
	Gain error	V_{REF} tied to V_{DD}, measured between end-point codes 2d and 254d, output unloaded	–0.5	0.25	0.5	%FSR
	Gain error temperature coefficient	V_{REF} tied to V_{DD}, measured between end-point codes 2d and 254d, output unloaded		±0.0008		%FSR/°C
	Full scale error	1.8 V ≤ V_{DD} < 2.7 V, code 511d into digipot, no headroom	–1	0.5	1	%FSR
		2.7 V ≤ V_{DD} ≤ 5.5 V, code 511d into digipot, no headroom	–0.5	0.25	0.5	
	Full scale error temperature coefficient			±0.0008		%FSR/°C
OUTPUT CHARACTERISTICS						
	Output voltage	Reference tied to V_{DD}	0		5.5	V
C_L	Capacitive load(2)	R_L = Infinite, phase margin = 30°			1	nF
		R_L = 5 kΩ, phase margin = 30°			2	
	Load regulation	Digipot at midscale, –10 mA ≤ I_{OUT} ≤ 10 mA, V_{DD} = 5.5 V		0.4		mV/mA
	Short circuit current	V_{DD} = 1.8 V, full-scale output shorted to A_{GND} or zero-scale output shorted to V_{DD}		10		mA
		V_{DD} = 2.7 V, full-scale output shorted to A_{GND} or zero-scale output shorted to V_{DD}		25		
		V_{DD} = 5.5 V, full-scale output shorted to A_{GND} or zero-scale output shorted to V_{DD}		50		
	Output voltage headroom(1)	To V_{DD} (digipot output unloaded, internal reference = 1.21 V), V_{DD} ≥ 1.21 × gain + 0.2 V		0.2		V
		To V_{DD} (digipot output unloaded)		0.8		%FSR
		To V_{DD} (I_{LOAD} = 10 mA at V_{DD} = 5.5 V, I_{LOAD} = 3 mA at V_{DD} = 2.7 V, I_{LOAD} = 1 mA at V_{DD} = 1.8 V), digipot code = full scale	10			
	V_{OUT} dc output impedance	Digipot output enabled and digipot code = midscale		0.25		Ω
		Digipot output enabled and digipot code = 2d		0.25		
		Digipot output enabled and digipot code = 254d		0.26		
Z_O	V_{FB} dc output impedance(3)	Digipot output enabled	160	200	240	kΩ
	V_{OUT} + V_{FB} dc output leakage(2)	At start up, measured when digipot output is disabled and held at V_{DD} / 2 for V_{DD} = 5.5 V			5	nA
	Power supply rejection ratio (dc)	Internal V_{REF}, gain = 2x, digipot at midscale; V_{DD} = 5 V ±10%		0.25		mV/V

6.5 Electrical Characteristics (continued)

all minimum/maximum specifications at T_A = –40°C to +125°C and typical specifications at T_A = 25°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, reference tied to V_{DD}, gain = 1x, digipot output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), and digital inputs at V_{DD} or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE						
t_{sett}	Output voltage settling time	1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, V_{DD} = 5.5 V		8		µs
		1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, V_{DD} = 5.5 V, internal V_{REF}, gain = 4x		12		
	Slew rate	V_{DD} = 5.5 V		1		V/µs
	Power on glitch magnitude	At start up (buffer output disabled), R_L = 5 kΩ, C_L = 200 pF		75		mV
		At start up (buffer output disabled), R_L = 100 kΩ		200		
	Output enable glitch magnitude	Buffer output disabled to enabled (digipot registers at zero scale, R_L = 100 kΩ		250		mV
V_n	Output noise voltage (peak to peak)	0.1 Hz to 10 Hz, digipot at midscale, V_{DD} = 5.5 V		34		μV_{PP}
		Internal V_{REF}, gain = 4x, 0.1 Hz to 10 Hz, digipot at midscale, V_{DD} = 5.5 V		70		
	Output noise density	Measured at 1 kHz, digipot at midscale, V_{DD} = 5.5 V		0.2		µV/√Hz
		Internal VREF, gain = 4x, measured at 1 kHz, digipot at midscale, VDD = 5.5 V		0.7		
	Power supply rejection ratio (ac)(3)	Internal V_{REF}, gain = 4x, 200-mV 50 or 60 Hz sine wave superimposed on power supply voltage, digipot at midscale		–71		dB
	Code change glitch impulse	±1 LSB change around mid code (including feedthrough)		10		nV-s
	Code change glitch impulse magnitude	±1 LSB change around mid code (including feedthrough)		15		mV
VOLTAGE REFERENCE						
	Initial accuracy	T_A = 25°C		1.212		V
	Reference output temperature coefficient(2)				50	ppm/°C
EEPROM						
	Endurance	–40°C ≤ T_A ≤ 85°C		20000		Cycles
		T_A > 85°C		1000		
	Data retention(2)	T_A = 25°C		50		Years
	EEPROM programming write cycle time(2)		10		20	ms
DIGITAL INPUTS						
	Digital feedthrough	Digipot output static at midscale, fast mode plus, SCL toggling		20		nV-s
	Pin capacitance	Per pin		10		pF
POWER						
	Load capacitor - CAP pin(2)		0.5		15	µF
I_{DD}	Current flowing into VDD	Normal mode, digipot at full scale, digital pins static		0.5	0.8	mA
		Digipot power-down, internal reference power down		80		µA

(1) Measured with digipot output unloaded. For external reference between end-point codes 2d and 254d. For internal reference VDD ≥ 1.21 x gain + 0.2 V, between end-point codes 2d and 254d.
(2) Specified by design and characterization, not production tested.
(3) Specified with 200-mV headroom with respect to reference value when internal reference is used.

6.6 Timing Requirements: I²C Standard Mode

all input signals are timed from VIL to 70% of V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.8 V ≤ $V_{pull-up}$ ≤ V_{DD} (unless otherwise specified)

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			0.1	MHz
t_{BUF}	Bus free time between stop and start conditions	4.7			µs
t_{HDSTA}	Hold time after repeated start	4			µs
t_{SUSTA}	Repeated start setup time	4.7			µs
t_{SUSTO}	Stop condition setup time	4			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	250			ns
t_{LOW}	SCL clock low period	4700			ns
t_{HIGH}	SCL clock high period	4000			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			1000	ns

6.7 Timing Requirements: I²C Fast Mode

all input signals are timed from VIL to 70% of V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.8 V ≤ $V_{pull-up}$ ≤ V_{DD} (unless otherwise specified)

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			0.4	MHz
t_{BUF}	Bus free time between stop and start conditions	1.3			µs
t_{HDSTA}	Hold time after repeated start	0.6			µs
t_{SUSTA}	Repeated start setup time	0.6			µs
t_{SUSTO}	Stop condition setup time	0.6			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	100			ns
t_{LOW}	SCL clock low period	1300			ns
t_{HIGH}	SCL clock high period	600			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			300	ns

6.8 Timing Requirements: I²C Fast Mode Plus

all input signals are timed from VIL to 70% of V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.8 V ≤ $V_{pull-up}$ ≤ V_{DD} (unless otherwise specified)

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			1	MHz
t_{BUF}	Bus free time between stop and start conditions	0.5			µs
t_{HDSTA}	Hold time after repeated start	0.26			µs
t_{SUSTA}	Repeated start setup time	0.26			µs
t_{SUSTO}	Stop condition setup time	0.26			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	50			ns
t_{LOW}	SCL clock low period	0.5			µs
t_{HIGH}	SCL clock high period	0.26			µs
t_F	Clock and data fall time			120	ns
t_R	Clock and data rise time			120	ns

6.9 Typical Characteristics: V_{DD} = 1.8 V (Reference = V_{DD}) or V_{DD} = 2 V (Internal Reference)

at T_A = 25°C and digipot outputs unloaded (unless otherwise noted)

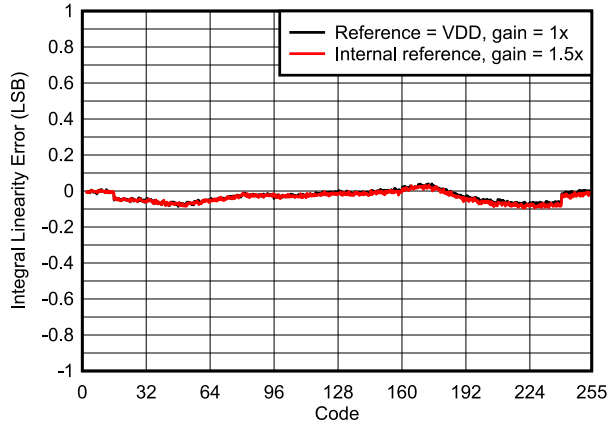


Figure 6-1. Integral Linearity Error vs Digital Input Code

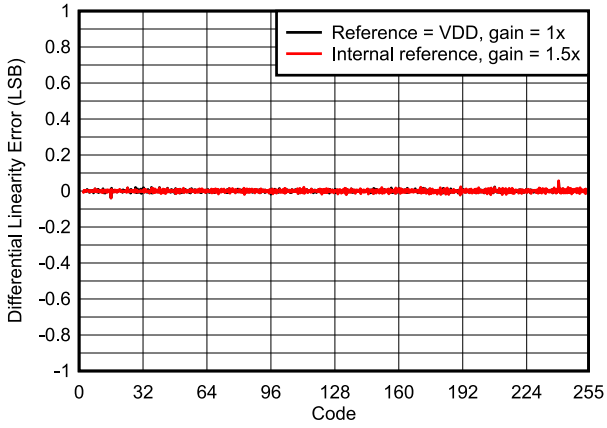


Figure 6-2. Differential Linearity Error vs Digital Input Code

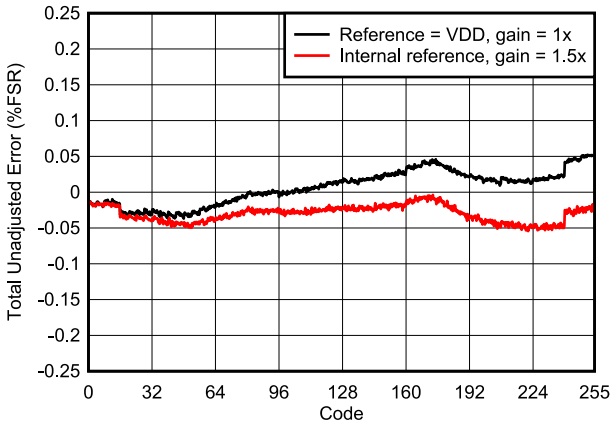


Figure 6-3. Total Unadjusted Error vs Digital Input Code

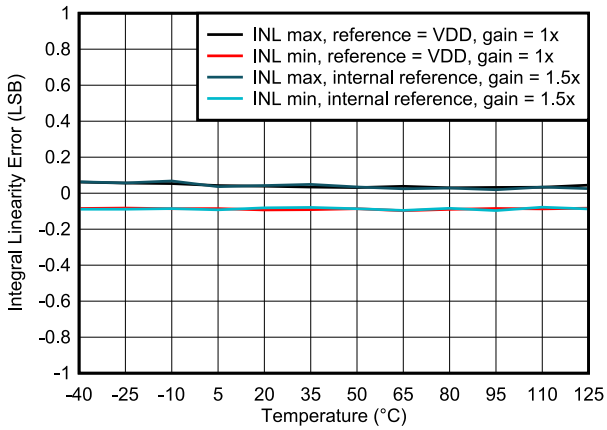


Figure 6-4. Integral Linearity Error vs Temperature

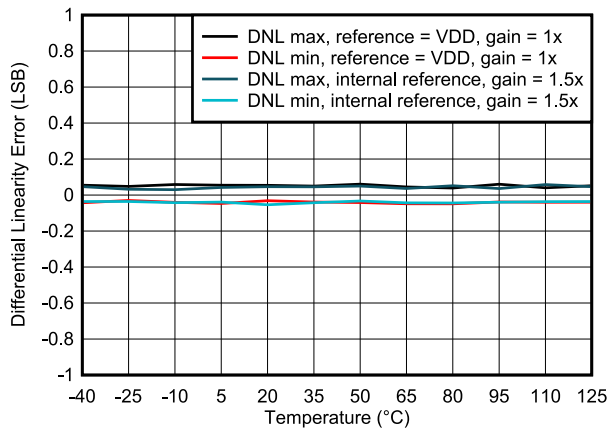


Figure 6-5. Differential Linearity Error vs Temperature

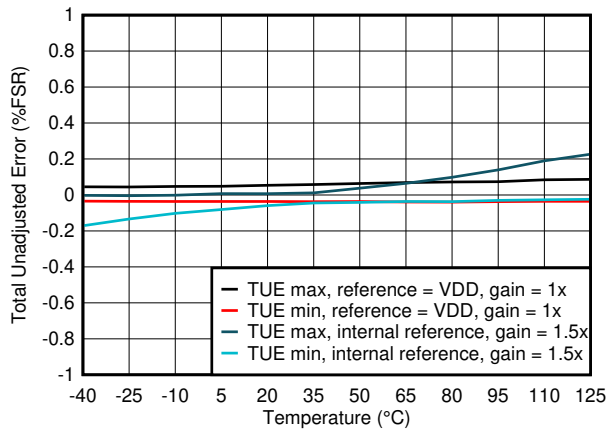
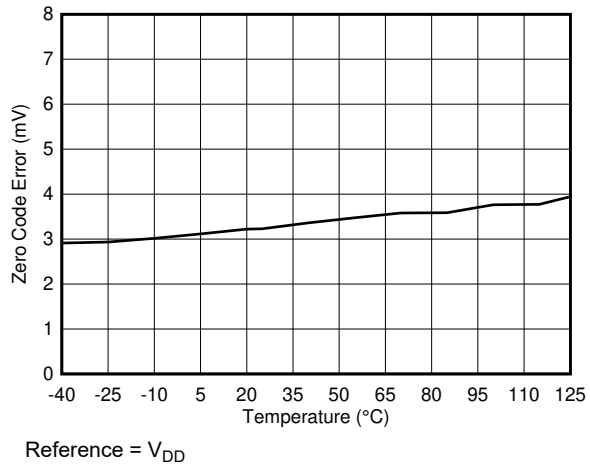


Figure 6-6. Total Unadjusted Error vs Temperature

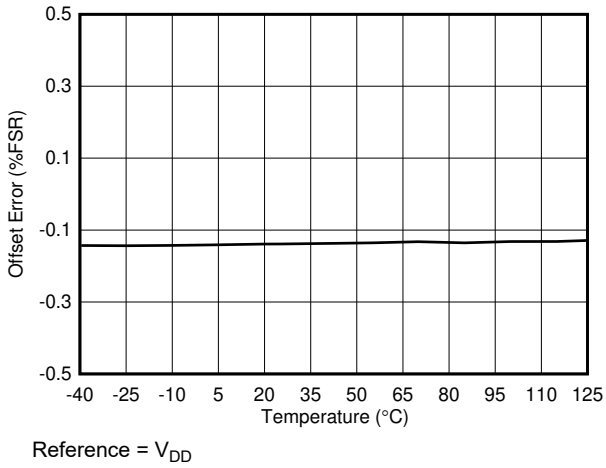
6.9 Typical Characteristics: V_{DD} = 1.8 V (Reference = V_{DD}) or V_{DD} = 2 V (Internal Reference) (continued)

at T_A = 25°C and digipot outputs unloaded (unless otherwise noted)



Reference = V_{DD}

Figure 6-7. Zero Code Error vs Temperature



Reference = V_{DD}

Figure 6-8. Offset Error vs Temperature

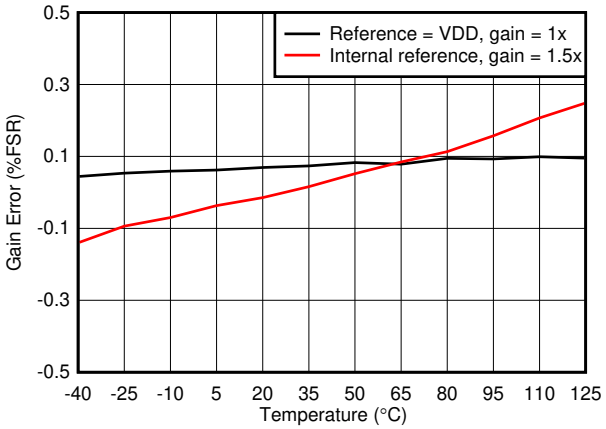


Figure 6-9. Gain Error vs Temperature

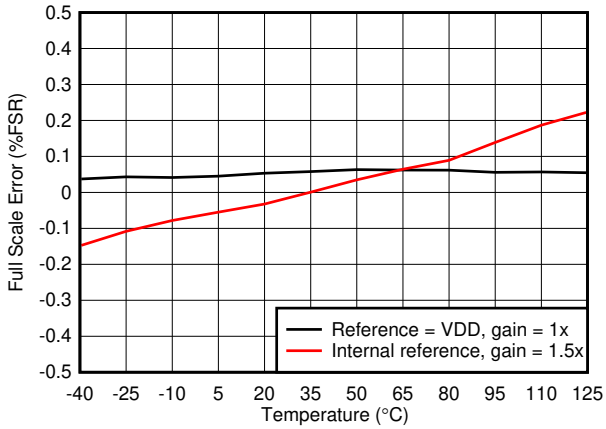


Figure 6-10. Full-Scale Error vs Temperature

6.10 Typical Characteristics: V_{DD} = 5.5 V (Reference = V_{DD}) or V_{DD} = 5 V (Internal Reference)

at T_A = 25°C and digipot outputs unloaded (unless otherwise noted)

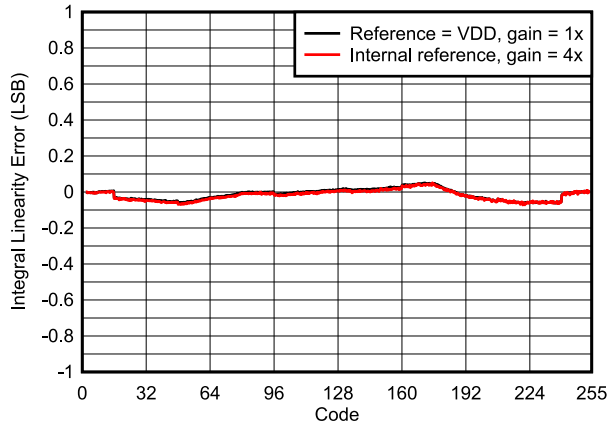


Figure 6-11. Integral Linearity Error vs Digital Input Code

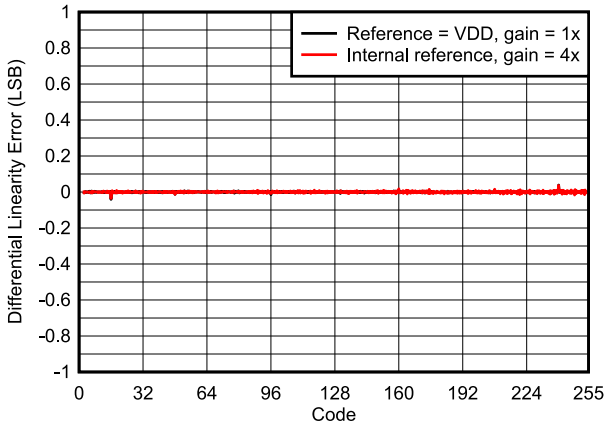


Figure 6-12. Differential Linearity Error vs Digital Input Code

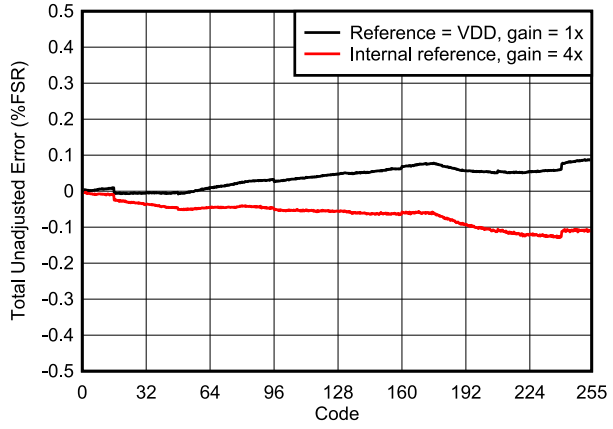


Figure 6-13. Total Unadjusted Error vs Digital Input Code

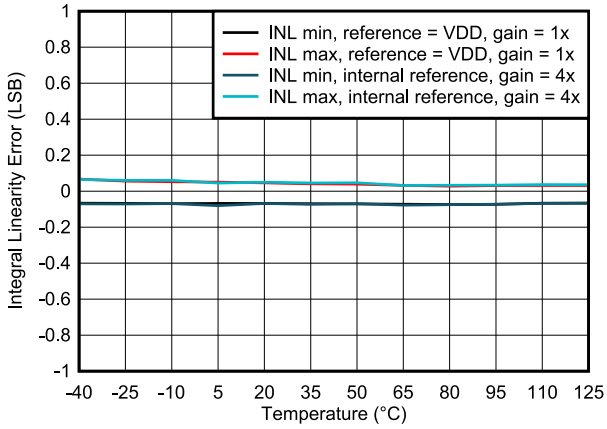


Figure 6-14. Integral Linearity Error vs Temperature

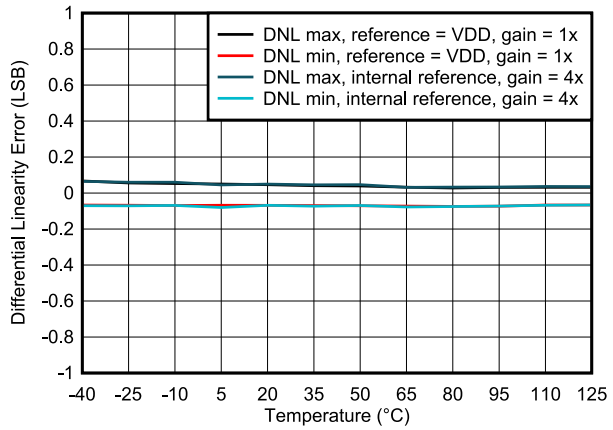


Figure 6-15. Differential Linearity Error vs Temperature

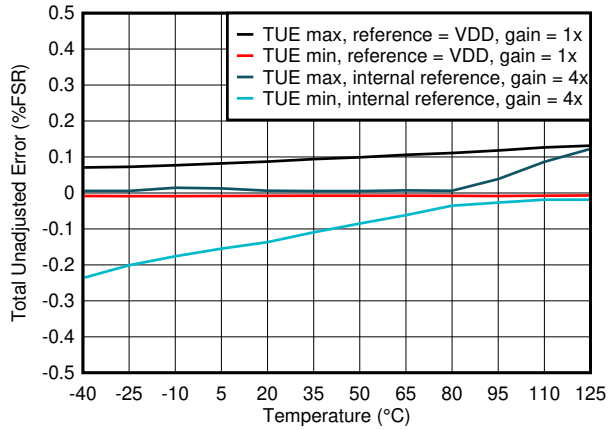
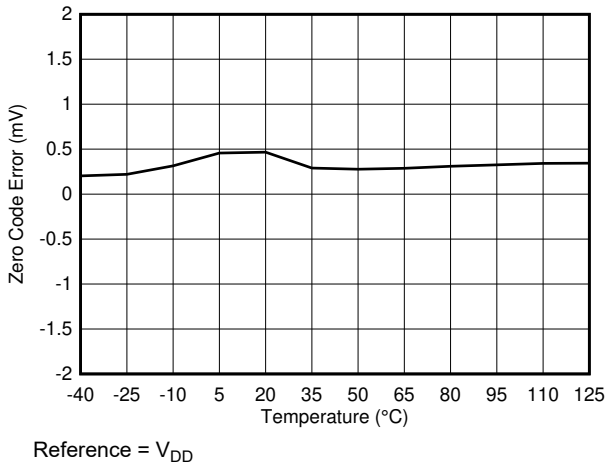


Figure 6-16. Total Unadjusted Error vs Temperature

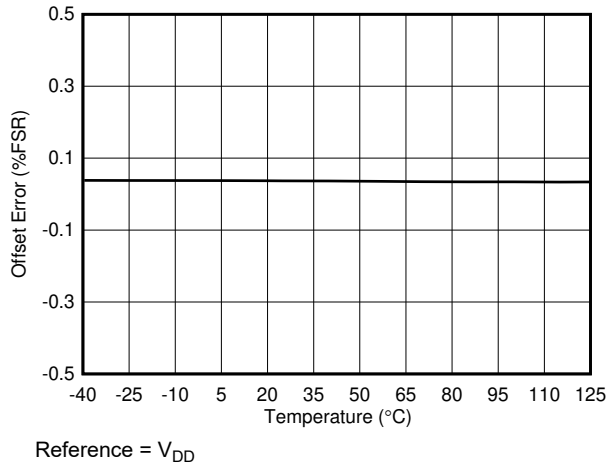
6.10 Typical Characteristics: V_{DD} = 5.5 V (Reference = V_{DD}) or V_{DD} = 5 V (Internal Reference) (continued)

at T_A = 25°C and digipot outputs unloaded (unless otherwise noted)



Reference = V_{DD}

Figure 6-17. Zero Code Error vs Temperature



Reference = V_{DD}

Figure 6-18. Offset Error vs Temperature

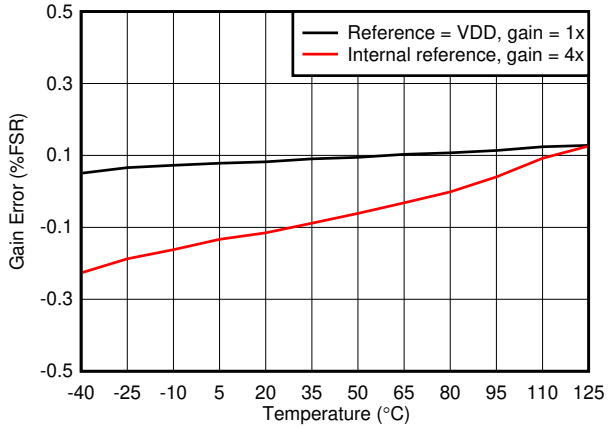


Figure 6-19. Gain Error vs Temperature

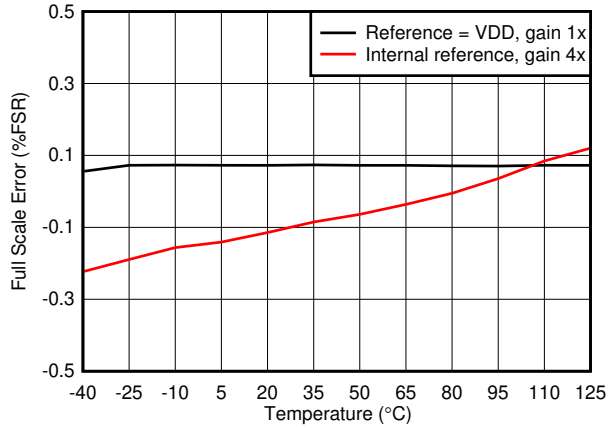
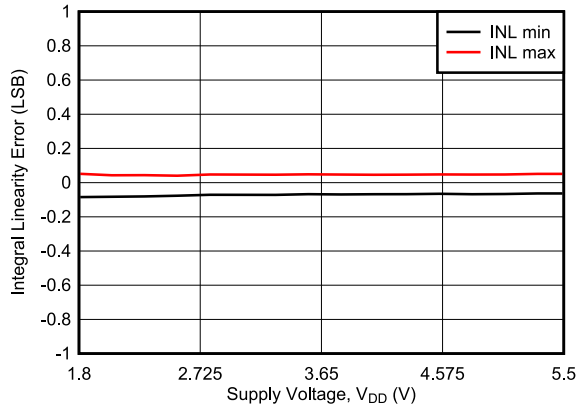


Figure 6-20. Full-Scale Error vs Temperature

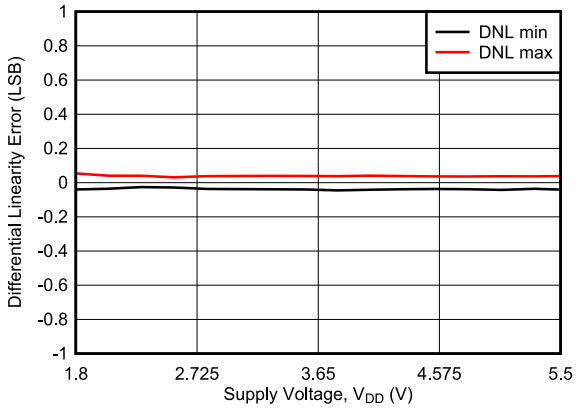
6.11 Typical Characteristics

at T_A = 25°C and digipot outputs unloaded (unless otherwise noted)



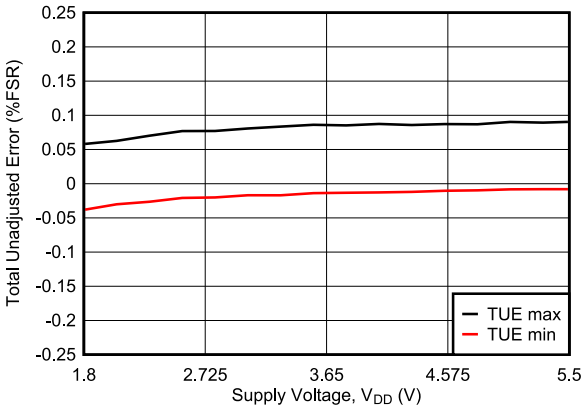
Reference = V_{DD}

Figure 6-21. Integral Linearity Error vs Supply Voltage



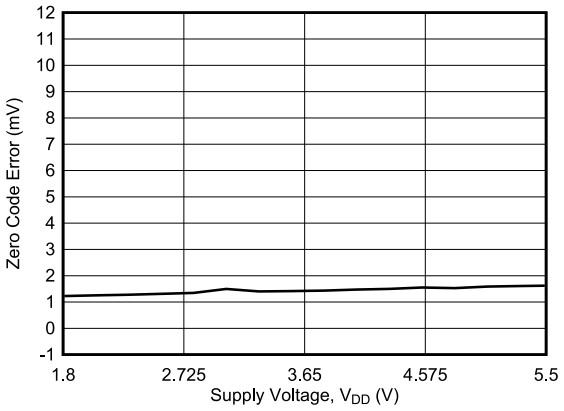
Reference = V_{DD}

Figure 6-22. Differential Linearity Error vs Supply Voltage



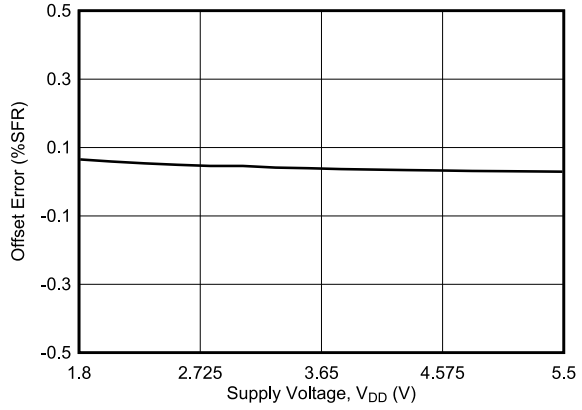
Reference = V_{DD}

Figure 6-23. Total Unadjusted Error vs Supply Voltage



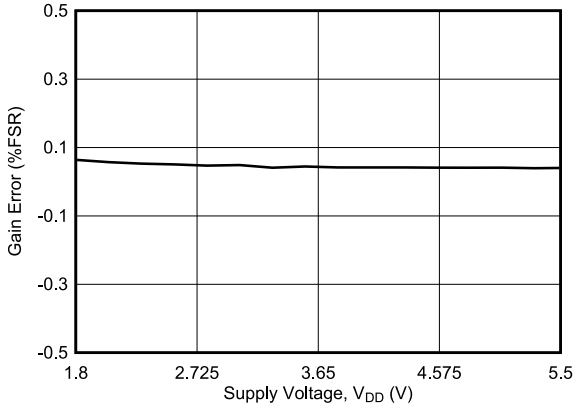
Reference = V_{DD}

Figure 6-24. Zero-Code Error vs Supply Voltage



Reference = V_{DD}

Figure 6-25. Offset Error vs Supply Voltage

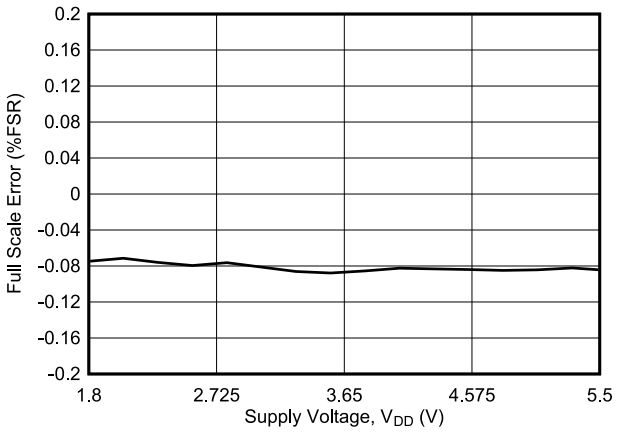


Reference = V_{DD}

Figure 6-26. Gain Error vs Supply Voltage

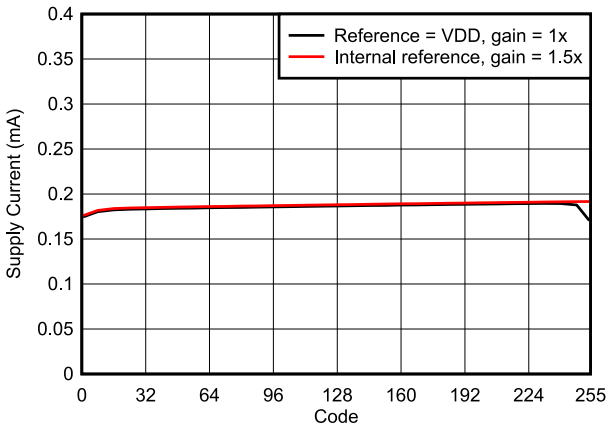
6.11 Typical Characteristics (continued)

at T_A = 25°C and digipot outputs unloaded (unless otherwise noted)



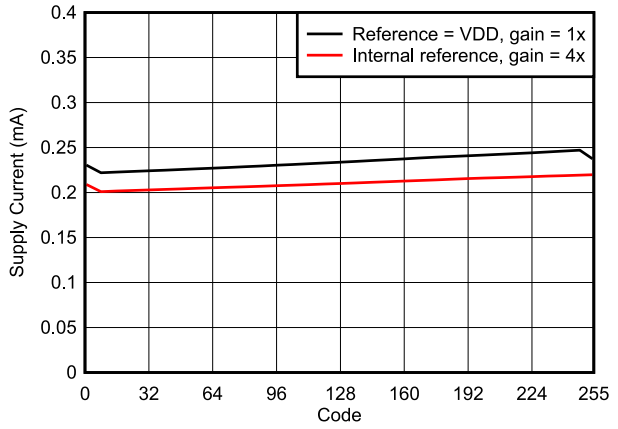
Reference = V_{DD}

Figure 6-27. Full-Scale Error vs Supply Voltage



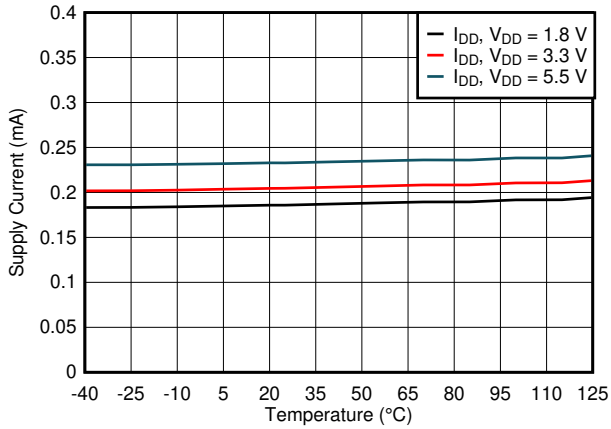
V_{DD} = 1.8 V

Figure 6-28. Supply Current vs Digital Input Code



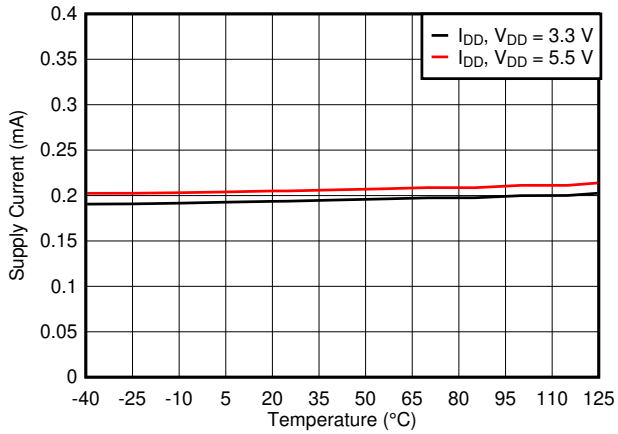
V_{DD} = 5.5 V

Figure 6-29. Supply Current vs Digital Input Code



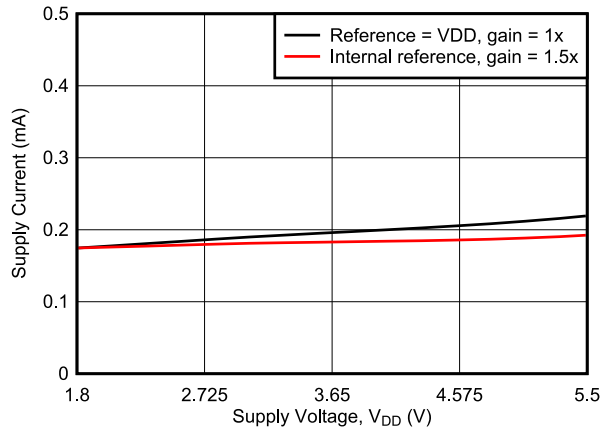
Reference = V_{DD}, digipot at midscale

Figure 6-30. Supply Current vs Temperature



Internal reference (gain = 4x), digipot at midscale

Figure 6-31. Supply Current vs Temperature

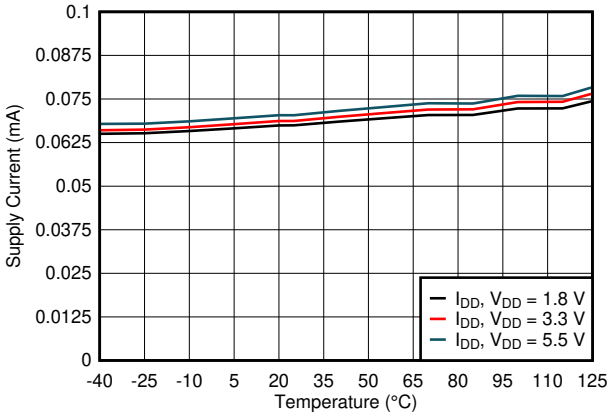


Digipot at midscale

Figure 6-32. Supply Current vs Supply Voltage

6.11 Typical Characteristics (continued)

at T_A = 25°C and digipot outputs unloaded (unless otherwise noted)



Reference = V_{DD}, digipot powered down

Figure 6-33. Power-Down Current vs Temperature

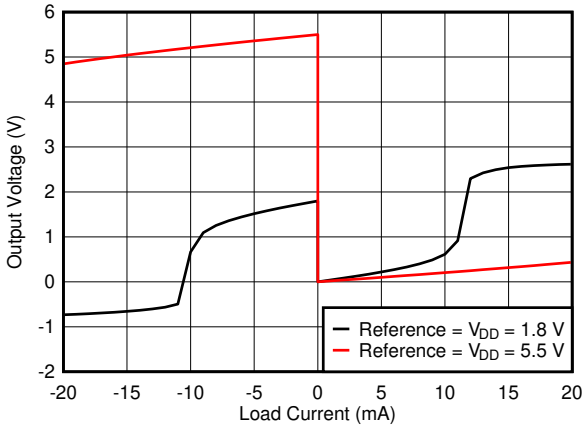
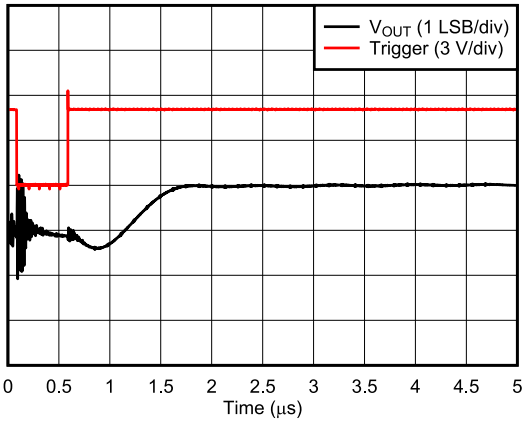
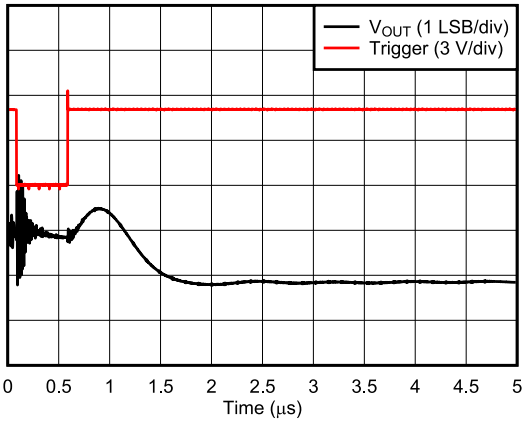


Figure 6-34. Source and Sink Capability



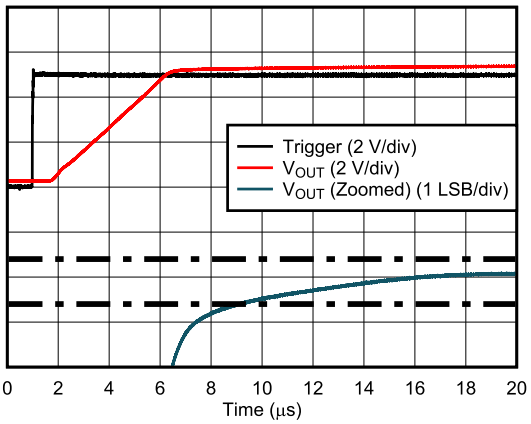
Reference = V_{DD} = 5.5 V, digipot code transition from midscale to midscale + 1 LSB, digipot load = 5 kΩ || 200 pF

Figure 6-35. Glitch Impulse, Rising Edge, 1-LSB Step



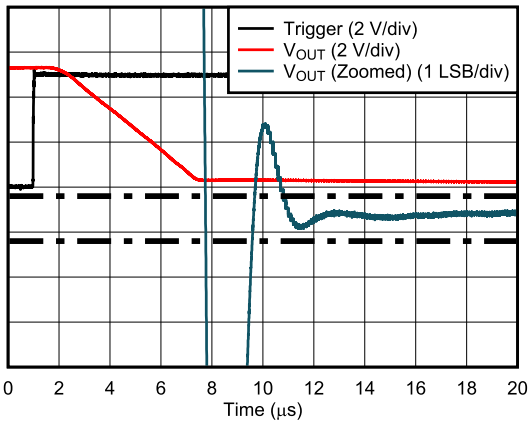
Reference = V_{DD} = 5.5 V, digipot code transition from midscale to midscale – 1 LSB, digipot load = 5 kΩ || 200 pF

Figure 6-36. Glitch Impulse, Falling Edge, 1-LSB Step



Reference = V_{DD} = 5.5 V, digipot load = 5 kΩ || 200 pF

Figure 6-37. Full-Scale Settling Time, Rising Edge

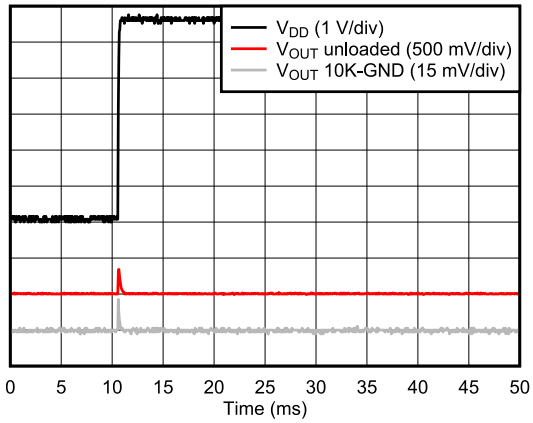


Reference = V_{DD} = 5.5 V, digipot load = 5 kΩ || 200 pF

Figure 6-38. Full-Scale Settling Time, Falling Edge

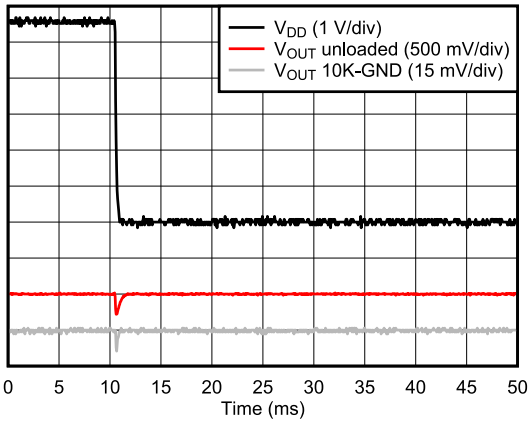
6.11 Typical Characteristics (continued)

at T_A = 25°C and digipot outputs unloaded (unless otherwise noted)



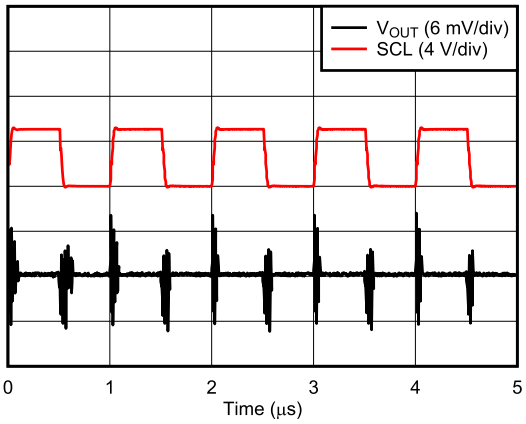
Reference = V_{DD} = 5.5 V

Figure 6-39. Power-on Glitch



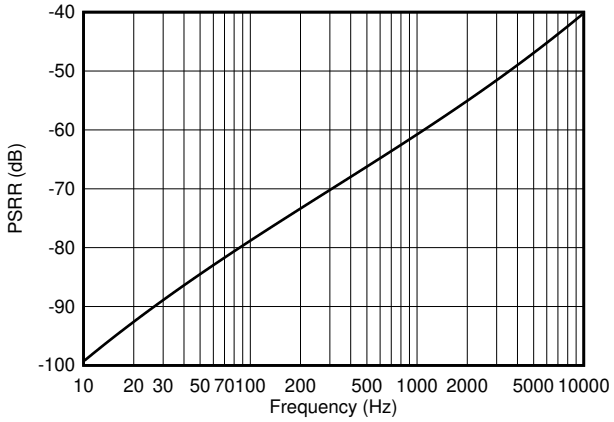
Reference = V_{DD} = 5.5 V

Figure 6-40. Power-off Glitch



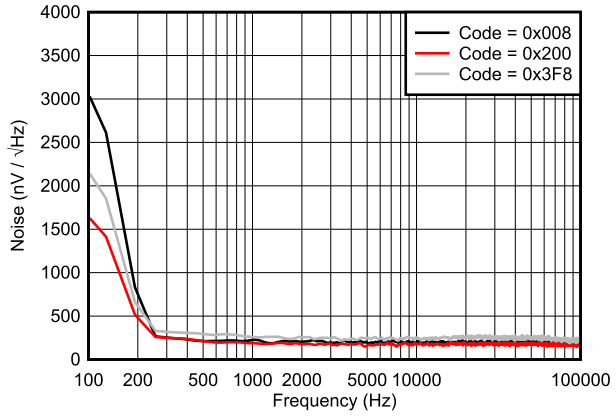
Reference = V_{DD} = 5.5 V, fast mode plus, digipot at midscale, digipot load = 5 kΩ || 200 pF

Figure 6-41. Clock Feedthrough



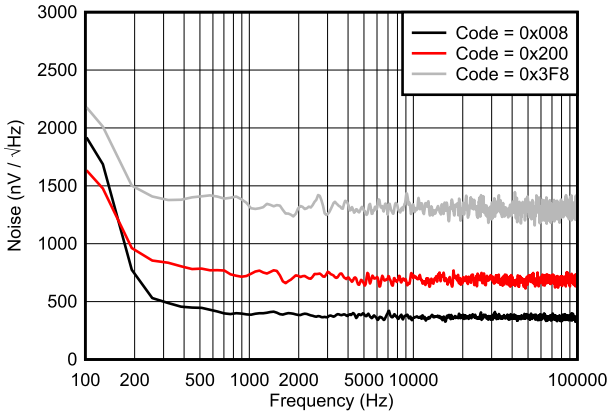
Internal reference (gain = 4x), V_{DD} = 5.25 V + 0.25 V_{PP}, digipot at midscale, digipot load = 5 kΩ || 200 pF

Figure 6-42. Output AC PSRR vs Frequency



Reference = V_{DD} = 5.5 V

Figure 6-43. Output Noise Spectral Density

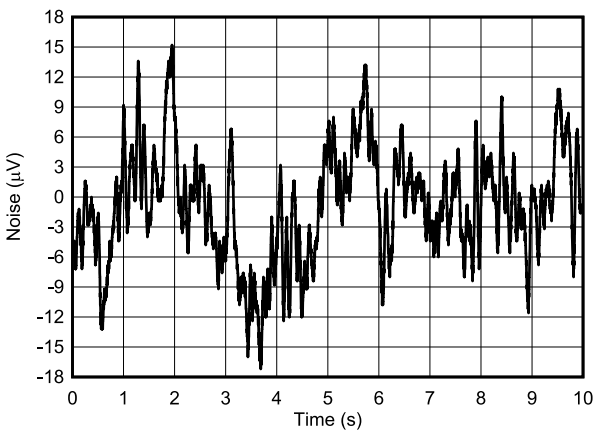


Internal reference (gain = 4x), V_{DD} = 5.5 V

Figure 6-44. Output Noise Spectral Density

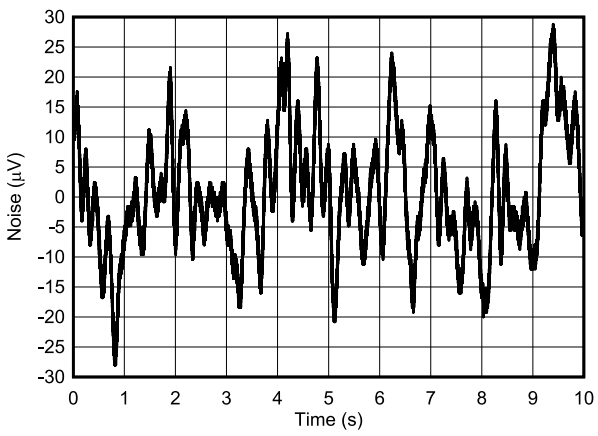
6.11 Typical Characteristics (continued)

at T_A = 25°C and digipot outputs unloaded (unless otherwise noted)



Reference = V_{DD} = 5.5 V, digipot at midscale

Figure 6-45. Digipot Output Noise: 0.1 Hz to 10 Hz



Internal reference (gain = 4x), V_{DD} = 5.5 V, digipot at midscale

Figure 6-46. Digipot Output Noise: 0.1 Hz to 10 Hz

7 Detailed Description

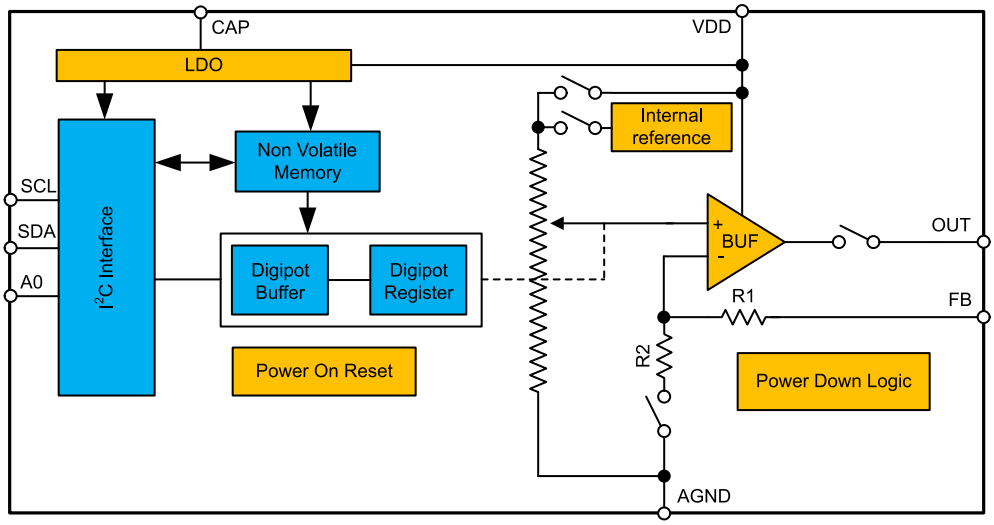
7.1 Overview

The TPL1401 is a digital potentiometer with buffered wiper. The buffered wiper helps achieve a higher load regulation as compared to standard digital potentiometers used in voltage-divider applications. This digipot contains nonvolatile memory (NVM) and an I^2C interface. This makes the TPL1401 easy to use for factory trimming and calibration device in analog set-point applications. The TPL1401 operates with either the internal reference or the power supply as the reference, and provides a full-scale output of 1.8 V to 5.5 V.

The TPL1401 communicates through an I^2C interface. This device supports I^2C standard mode (100 kbps), fast mode (400 kbps), and fast mode plus (1 Mbps). This device also includes a wiper lock feature, an FB pin for current sink application, and 2 bytes of user-programmable NVM space.

The TPL1401 has a power-on-reset (POR) circuit that makes sure all the registers start with default or user-programmed settings using NVM. The digipot output powers on in high-impedance mode (default); this setting can be programmed to 10kΩ-GND using NVM.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Digital Potentiometer (Digipot) Architecture

The TPL1401 consists of string architecture with an output buffer amplifier. *Section 7.2* shows the digipot architecture within the block diagram. This digipot architecture operates from a 1.8-V to 5.5-V power supply. This device consume only 0.2 mA of current when using a 1.8-V power supply. The digipot output gets loaded from the NVM at power up. Write the required code so that the load circuit starts with a predictable operating point at power up.

7.3.1.1 Reference Selection and Digipot Transfer Function

The device writes the input data to the DPOT_POSITION register in straight-binary format. After a power-on or a reset event, the device sets all digipot registers to the values set in the NVM.

7.3.1.1.1 Power Supply as Reference

By default, the TPL1401 operates with the power-supply pin (VDD) as a reference. Equation 1 shows the digipot transfer function when the power-supply pin is used as a reference.

$$V_{OUT} = \frac{DPOT\_POS}{256} \times V_{DD} \quad (1)$$

where:

- DPOT_POS is the decimal equivalent of the binary code that is loaded to the digipot register.
- DPOT_POS ranges from 0 to 255.
- V_{DD} is used as the digipot reference voltage.

7.3.1.1.2 Internal Reference

The TPL1401 also contains an internal reference that is disabled by default. Enable the internal reference by writing 1 to REF_EN (address D1h). The internal reference generates a fixed 1.21-V voltage (typical). Using the OUT_SPAN (address D1h) bits, a gain of 1.5x, 2x, 3x, 4x can be achieved for the digipot output voltage (V_{OUT}) Equation 2 shows digipot transfer function when the internal reference is used.

$$V_{OUT} = \frac{DPOT\_POS}{256} \times V_{REF} \times GAIN \quad (2)$$

where:

- DPOT_POS is the decimal equivalent of the binary code that is loaded to the digipot register
- DPOT_POS ranges from 0 to 255.
- V_{REF} is the internal reference voltage = 1.21 V.
- GAIN = 1.5x, 2x, 3x, 4x based on OUT_SPAN (address D1h) bits.

7.3.2 Digipot Update

The digipot output pin (OUT) is updated at the end of I^2C digipot write frame.

7.3.3 Nonvolatile Memory (EEPROM or NVM)

The TPL1401 contains nonvolatile memory (NVM) bits. These NVM bits are user programmable and erasable, and retain the set values in the absence of a power supply. All the register bits, as shown in Table 7-1, can be stored in the device NVM by setting NVM_PROG = 1 (address D3h). The NVM_BUSY bit (address D0h) is set to 1 by the device when an NVM write or reload operation is ongoing. During this time, the device blocks all write operations to the device. The NVM_BUSY bit is set to 0 after the write or reload operation is complete; at this point, all write operations to the device are allowed. The default value for all the registers in the TPL1401 is loaded from NVM as soon as a POR event is issued. Do not perform a read operation from the digipot register while NVM_BUSY = 1.

The TPL1401 also implements NVM_RELOAD bit (address D3h). Set this bit to 1 for the device to start an NVM reload operation. After the operation is complete, the device autoresets this bit to 0. During the NVM_RELOAD operation, the NVM_BUSY bit is set to 1.

Table 7-1. NVM Programmable Registers

REGISTER ADDRESS	REGISTER NAME	BIT ADDRESS	BIT NAME
D1h	GENERAL_CONFIG	13	DEVICE_LOCK
		4:3	DPOT_PDN
		2	REF_EN
		1:0	OUT_SPAN
10h	DPOT_POSITION	11:2	DPOT_POS
25h	USER_BYTE1	11:4	USER_BYTE1 (8 most significant bits)
26h	USER_BYTE2	11:4	USER_BYTE2 (8 most significant bits)

7.3.3.1 NVM Cyclic Redundancy Check

The TPL1401 implements a cyclic redundancy check (CRC) feature to make sure that the data stored in the device NVM are uncorrupted. There are two types of CRC alarm bits implemented in TPL1401:

- NVM_CRC_ALARM_USER (address D0h) — This bit indicates the status of the user-programmable NVM bits.
- NVM_CRC_ALARM_INTERNAL (address D0h) — This bit indicates the status of the internal NVM bits.

The CRC feature is implemented by storing a 10-bit CRC (CRC-10-ATM) along with the NVM data each time NVM program operation (write or reload) is performed and during the device start up. The device reads the NVM data and validates the data with the stored CRC. The CRC alarm bits report any errors after the data are read from the device NVM.

7.3.3.1.1 NVM_CRC_ALARM_USER Bit

A logic 1 on NVM_CRC_ALARM_USER bit indicates that the user-programmable NVM data is corrupt. During this condition, all registers in the digipot are initialized with factory reset values, and any digipot registers can be written to or read from. To reset the alarm bits to 0, issue a *Software Reset* command, or cycle power to the digipot. A power cycle reloads the user-programmable NVM bits. After the reset, write the desired data to the registers and assert the NVM_PROG bit in the PROTECT register to program the NVM.

7.3.3.1.2 NVM_CRC_ALARM_INTERNAL Bit

A logic 1 on NVM_CRC_ALARM_INTERNAL bit indicates that the internal NVM data is corrupt. During this condition, all registers in the digipot are initialized with factory reset values, and any digipot registers can be written to or read from. To reset the alarm bits to 0, issue a *Software Reset* command, or cycle power to the digipot. The NVM_PROG bit in the PROTECT register (address D3h) is blocked when the NVM_CRC_ALARM_INTERNAL bit is set. The device reset or power cycle does not reset the CRC error if there is a permanent NVM failure.

7.3.4 Power-On Reset (POR)

The TPL1401 includes a power-on reset (POR) function that controls the output voltage at power up. After the V_{DD} supply has been established, a POR event is issued. The POR causes all registers to initialize to default values, and communication with the device is valid only after a 30-ms POR delay. The default value for all the registers in the TPL1401 is loaded from NVM as soon as the POR event is issued.

When the device powers up, a POR circuit sets the device to the default mode. The POR circuit requires specific V_{DD} levels, as indicated in Figure 7-1, in order to make sure that the internal capacitors discharge and reset the device on power up. To make sure that a POR occurs, V_{DD} must be less than 0.7 V for at least 1 ms. When V_{DD} drops to less than 1.65 V, but remains greater than 0.7 V (shown as the undefined region), the device may or may not reset under all specified temperature and power-supply conditions. In this case, initiate a POR. When V_{DD} remains greater than 1.65 V, a POR does not occur.

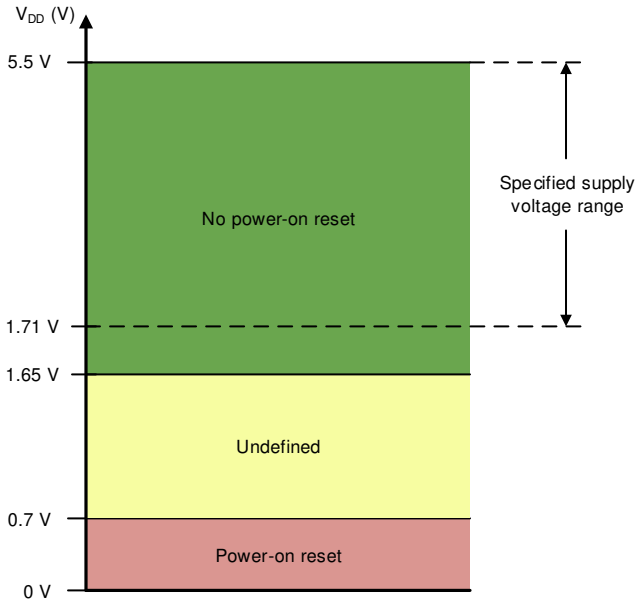


Figure 7-1. Threshold Levels for V_{DD} POR Circuit

7.3.5 Software Reset

To initiate a device software reset event, write reserved code 1010 to the SW_RESET bits (address D3h). A software reset initiates a POR event.

7.3.6 Device Lock Feature

The TPL1401 implements a device lock feature that prevents an accidental or unintended write to the digipot registers. The device locks all the registers when the DEVICE_LOCK bit (address D1h) is set to 1. To bypass the DEVICE_LOCK setting, write 0101 to the DEVICE_UNLOCK_CODE bits (address D3h).

7.4 Device Functional Modes

7.4.1 Power Down Mode

The TPL1401 output amplifier and internal reference can be independently powered down through the DPOT_PDN bits (address D1h).

At power up, the digipot output and the internal reference are disabled by default.

In power-down mode, the digipot output (OUT pin) is in a high-impedance state.

To change this state to 10kΩ-A_{GND} (at power up), use the DPOT_PDN bits (address D1h).

The digipot power-up state can be programmed to any state (power-down or normal mode) using the NVM. Table 7-2 shows the digipot power-down bits.

Table 7-2. Digipot Power-Down Bits

REGISTER ADDRESS AND NAME	DPOT_PDN[1]	DPOT_PDN[0]	DESCRIPTION
D1h, GENERAL_CONFIG	0	0	Power up
	0	1	Power down to 10 kΩ
	1	0	Power down to high impedance (HiZ) (default)
	1	1	Power down to 10 kΩ

7.5 Programming

The TPL1401 devices have a 2-wire serial interface (SCL and SDA), and one address pin (A0), as shown in *Section 5*. The I^{2}C bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^{2}C-compatible devices connect to the I^{2}C bus through the open drain I/O pins, SDA and SCL.

The I^{2}C specification states that the device that controls communication is called a *master*, and the devices that are controlled by the master are called *slaves*. The master device generates the SCL signal. The master device also generates special timing conditions (start condition, repeated start condition, and stop condition) on the bus to indicate the start or stop of a data transfer. Device addressing is completed by the master. The master device on an I^{2}C bus is typically a microcontroller or digital signal processor (DSP). The TPL1401 operates as a slave device on the I^{2}C bus. A slave device acknowledges master commands, and upon master control, receives or transmits data.

Typically, the TPL1401 operates as a slave receiver. A master device writes to the TPL1401, a slave receiver. However, if a master device requires the TPL1401 internal register data, the TPL1401 operate as a slave transmitter. In this case, the master device reads from the TPL1401. According to I^{2}C terminology, read and write refer to the master device.

The TPL1401 is a slave and supports the following data transfer modes:

- Standard mode (100 kbps)
- Fast mode (400 kbps)
- Fast mode plus (1.0 Mbps)

The data transfer protocol for standard and fast modes is exactly the same; therefore, both modes are referred to as F/S-mode in this document. The fast mode plus protocol is supported in terms of data transfer speed, but not output current. The low-level output current would be 3 mA; similar to the case of standard and fast modes. The TPL1401 supports 7-bit addressing. The 10-bit addressing mode is not supported. The device supports the general call reset function. Sending the following sequence initiates a software reset within the device: start or repeated start, 0x00, 0x06, stop. The reset is asserted within the device on the rising edge of the ACK bit, following the second byte.

Other than specific timing signals, the I^{2}C interface works with serial bytes. At the end of each byte, a ninth clock cycle generates and detects an acknowledge signal. Acknowledge is when the SDA line is pulled low during the high period of the ninth clock cycle. A not-acknowledge is when the SDA line is left high during the high period of the ninth clock cycle as shown in Figure 7-2.

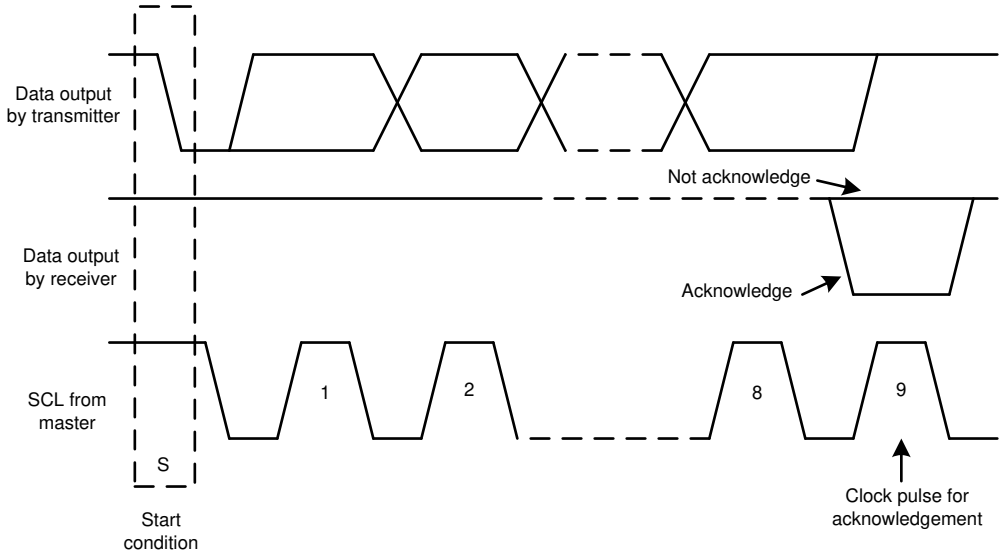


Figure 7-2. Acknowledge and Not Acknowledge on the I^{2}C Bus

7.5.1 F/S Mode Protocol

The following steps explain a complete transaction in F/S mode.

1. The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 7-3. All I^2C-compatible devices recognize a start condition.
2. The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit (R/$\overline{W}$) on the SDA line. During all transmissions, the master makes sure that data are valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse, as shown in Figure 7-4. All devices recognize the address sent by the master and compare the address to the respective internal fixed address. Only the slave device with a matching address generates an acknowledge by pulling the SDA line low during the entire high period of the ninth SCL cycle, as shown in Figure 7-2. When the master detects this acknowledge, the communication link with a slave has been established.
3. The master generates further SCL cycles to transmit (R/$\overline{W}$ bit 0) or receive (R/$\overline{W}$ bit 1) data to the slave. In either case, the receiver must acknowledge the data sent by the transmitter. The acknowledge signal can be generated by the master or by the slave, depending on which is the receiver. The 9-bit valid data sequences consists of 8-data bits and 1 acknowledge-bit, and can continue as long as necessary.
4. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low-to-high while the SCL line is high (see Figure 7-4). This action releases the bus and stops the communication link with the addressed slave. All I^2C-compatible devices recognize the stop condition. Upon receipt of a stop condition, the bus is released, and all slave devices then wait for a start condition followed by a matching address.

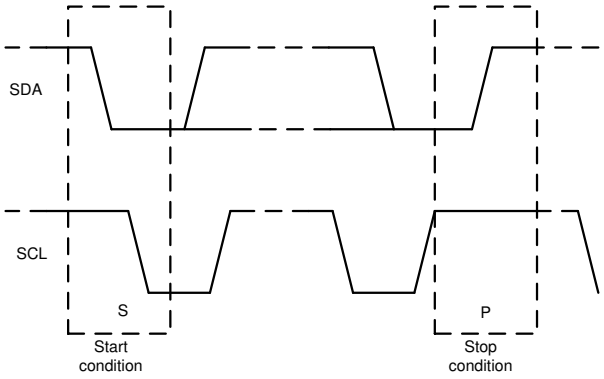


Figure 7-3. Start and Stop Conditions

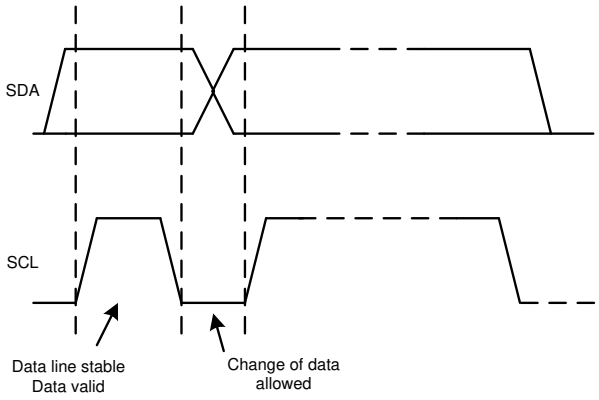


Figure 7-4. Bit Transfer on the I^2C Bus

7.5.2 I^2C Update Sequence

For a single update, the TPL1401 requires a start condition, a valid I^2C address byte, a command byte, and two data bytes, as listed in Table 7-3.

Table 7-3. Update Sequence

MSB	....	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
Address (A) byte Section 7.5.3				Command byte Section 7.5.4				Data byte - MSDB Section 8.2.3				Data byte - LSDB Section 8.2.3			
DB [31:24]				DB [23:16]				DB [15:8]				DB [7:0]			

After each byte is received, the TPL1401 acknowledges the byte by pulling the SDA line low during the high period of a single clock pulse, as shown in Figure 7-5. These four bytes and acknowledge cycles make up the 36 clock cycles required for a single update to occur. A valid I^2C address byte selects the TPL1401 device.

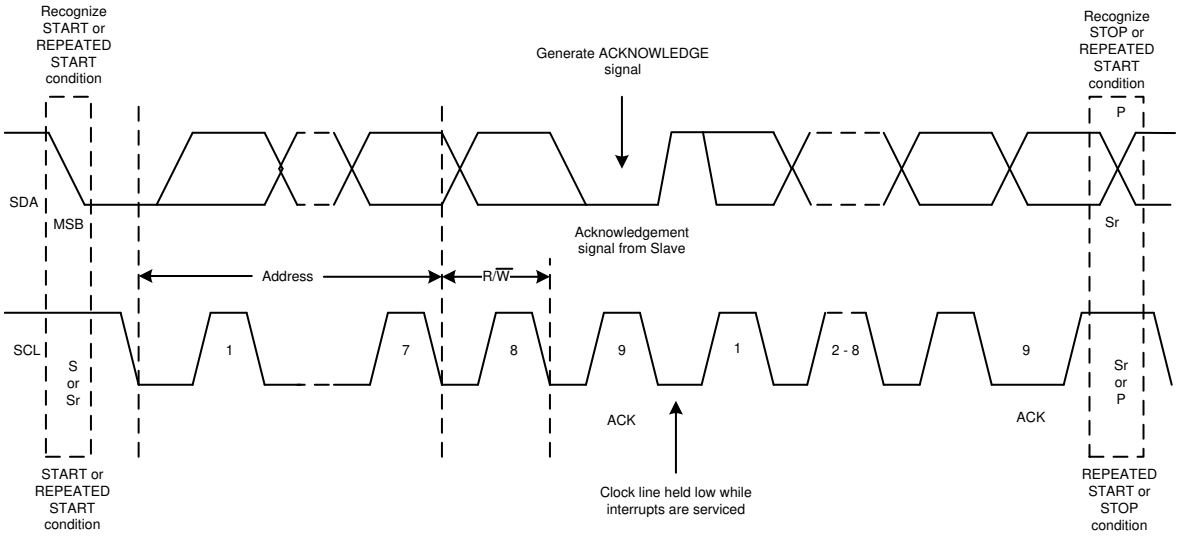


Figure 7-5. I²C Bus Protocol

The command byte sets the operating mode of the selected TPL1401. For a data update to occur when the operating mode is selected by this byte, the TPL1401 must receive two data bytes: the most significant data byte (MSDB) and least significant data byte (LSDB). The TPL1401 performs an update on the falling edge of the acknowledge signal that follows the LSDB.

When using fast mode (clock = 400 kHz), the maximum digipot update rate is limited to 10 kSPS. Using the fast mode plus (clock = 1 MHz), the maximum digipot update rate is limited to 25 kSPS. When a stop condition is received, the TPL1401 releases the I²C bus and awaits a new start condition.

7.5.3 Address Byte

The address byte, as shown in Table 7-4, is the first byte received from the master device following the start condition. The first four bits (MSBs) of the address are factory preset to 1001. The next three bits of the address are controlled by the A0 pin. The A0 pin input can be connected to VDD, AGND, SCL, or SDA. The A0 pin is sampled during the first byte of each data frame to determine the address. The device latches the value of the address pin, and consequently responds to that particular address according to Table 7-5.

The TPL1401 supports broadcast addressing, which is used for synchronously updating or powering down multiple TPL1401 devices. When the broadcast address is used, the TPL1401 responds regardless of the address pin state. Broadcast is supported only in write mode.

Table 7-4. Address Byte

COMMENT	MSB							LSB
—	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/ $\overline{W}$
General address	1	0	0	1	See Table 7-5 (slave address column)			0 or 1
Broadcast address	1	0	0	0	1	1	1	0

Table 7-5. Address Format

SLAVE ADDRESS	A0 PIN
000	AGND
001	VDD
010	SDA
011	SCL

7.5.4 Command Byte

Table 7-6 lists the command byte.

Table 7-6. Command Byte (Register Names)

ADDRESS	REGISTER NAME
D0h	STATUS
D1h	GENERAL_CONFIG
D3h	PROTECT
21h	DPOT_POSITION
25h	USER_BYTE1
26h	USER_BYTE2

7.5.5 I²C Read Sequence

To read any register, the following command sequence must be used, as shown in Table 7-7:

1. Send a start or repeated start command with a slave address and the R/$\overline{W}$ bit set to 0 for writing. The device acknowledges this event.
2. Send a command byte for the register to be read. The device acknowledges this event again.
3. Send a repeated start with the slave address and the R/$\overline{W}$ bit set to 1 for reading. The device acknowledges this event.
4. The device writes the MSDB byte of the addressed register. The master must acknowledge this byte.
5. Finally, the device writes out the LSDB of the register.

An alternative reading method allows for reading back the value of the last register written. The sequence is a start or repeated start with the slave address and the R/ $\overline{W}$ bit set to 1, and the two bytes of the last register are read out.

The broadcast address cannot be used for reading.

Table 7-7. Read Sequence

S	MSB	…	R/ $\overline{W}$ (0)	ACK	MSB	…	LSB	ACK	Sr	MSB	…	R/ $\overline{W}$ (1)	ACK	MSB	…	LSB	ACK	MSB	…	LSB	ACK
	ADDRESS BYTE Section 7.5.3				COMMAND BYTE Section 7.5.4				Sr	ADDRESS BYTE Section 7.5.3				MSDB				LSDB			
From Master				Slave	From Master			Slave	From Master				Slave	From Slave			Master	From Slave			Master

7.6 Register Map

Table 7-8. Register Map

ADDRESS	MOST SIGNIFICANT DATA BYTE (MSDB)								LEAST SIGNIFICANT DATA BYTE (LSDB)							
	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
D0h	NVM_CRC_ALARM_USER	NVM_CRC_ALARM_INTERNAL	NVM_BUSY	X[1]	X						DEVICE_ID				VERSION_ID	
D1h	RESERVED		DEVICE_LOCK	RESERVED								DPOT_PDN		REF_EN	OUT_SPAN	
D3h	DEVICE_UNLOCK_CODE				X		DEVICE_CONFIG_RESET	RESERVED			NVM_RELOAD	NVM_PROG	SW_RESET			
21h	X				DPOT_POS[7:0]										X	
25h	X				USER_BYTE1[7:0]										X	
26h	X				USER_BYTE2[7:0]										X	

(1) X = Don't care.

Table 7-9. Register Names

ADDRESS	REGISTER NAME	SECTION
D0h	STATUS	Section 7.6.1
D1h	GENERAL_CONFIG	Section 7.6.2
D3h	PROTECT	Section 7.6.3
21h	DPOT_POSITION	Section 7.6.4
25h	USER_BYTE1	Section 7.6.5
26h	USER_BYTE2	Section 7.6.6

Table 7-10. Access Type Codes

Access Type	Code	Description
X	X	Don't care
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.1 STATUS Register (address = D0h) (reset = 000Ch or 0014h)

Table 7-11. STATUS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NVM_CRC_ALARM_USER	NVM_CRC_ALARM_INTERNAL	NVM_BUSY	X	X						DEVICE_ID				VERSION_ID	
R-0h	R-0h	R-0h	R-0h	X-00h						R-14h				R-0h	

Table 7-12. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NVM_CRC_ALARM_USER	R	0	0 : No CRC error in user NVM bits 1: CRC error in user NVM bits
14	NVM_CRC_ALARM_INTERNAL	R	0	0 : No CRC error in internal NVM 1: CRC error in internal NVM bits
13	NVM_BUSY	R	0	0 : NVM write or load completed, Write to digipot registers allowed 1 : NVM write or load in progress, Write to digipot registers not allowed
12	X	R	0	Don't care
11 - 6	X	X	00h	Don't care
5 - 2	DEVICE_ID	R	14h	14h
1 - 0	VERSION_ID	R		Version ID as per the silicon version

7.6.2 GENERAL_CONFIG Register (address = D1h) (reset = 01F0h)

Figure 7-5. GENERAL_CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		DEVICE_LOCK	RESERVED								DPOT_PDN		REF_EN	OUT_SPAN	
R-0h		$\overline{W}$-0h	R-0Fh								R/ $\overline{W}$-2h		R/ $\overline{W}$-0h	R/ $\overline{W}$-0h	

Table 7-13. GENERAL_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	RESERVED	R	00	Always write 00b
13	DEVICE_LOCK	$\overline{W}$	0	0 : Device not locked 1: Device locked, the device locks all the registers. This bit can be reset (unlock device) by writing 0101 to the DEVICE_UNLOCK_CODE bits (address D3h)
12 - 5	RESERVED	R	0Fh	Always write 0Fh
4 - 3	DPOT_PDN	R/ $\overline{W}$	10	00: Power up 01: Power down to 10K 10: Power down to high impedance (default) 11: Power down to 10K
2	REF_EN	R/ $\overline{W}$	0	0: Internal reference disabled, V_{DD} is digipot reference voltage, digipot output range from 0 V to V_{DD}. 1: Internal reference enabled, digipot reference = 1.21 V
1 - 0	OUT_SPAN	R/ $\overline{W}$	00	Only applicable when internal reference is enabled. 00: Reference to V_{OUT} gain 1.5x 01: Reference to V_{OUT} gain 2x 10: Reference to V_{OUT} gain 3x 11: Reference to V_{OUT} gain 4x

7.6.3 PROTECT Register (address = D3h) (reset = 0008h)

Figure 7-6. PROTECT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEVICE_UNLOCK_CODE				X		DEVICE_CONFIG_RESET	RESERVED			NVM_RELOAD	NVM_PROG	SW_RESET			
W-0h				X		W-0h	R-0h			W-0h	W-0h	W-8h			

Table 7-14. PROTECT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	DEVICE_UNLOCK_CODE	W	0000	Write 0101 to unlock the device to bypass DEVICE_LOCK bit.
11 - 10	X	X	0h	Don't care
9	DEVICE_CONFIG_RESET	W	0	0: Device configuration reset not initiated 1: Device configuration reset initiated. All registers loaded with factory reset values.
8 - 6	RESERVED	R	000	Always write 000b
5	NVM_RELOAD	W	0	0: NVM reload not initiated 1: NVM reload initiated, applicable digipot registers loaded with corresponding NVM. NVM_BUSY bit set to 1 while this operation is in progress. This bit is self-resetting.
4	NVM_PROG	W	0	0: NVM write not initiated 1: NVM write initiated, NVM corresponding to applicable digipot registers loaded with existing register settings. NVM_BUSY bit set to 1 while this operation is in progress. This bit is self-resetting.
3 - 0	SW_RESET	W	1000	1000: Software reset not initiated 1010: Software reset initiated, digipot registers loaded with corresponding NVMs, all other registers loaded with default settings.

7.6.4 DPOT_POSITION Register (address = 21h) (reset = 0000h)

Table 7-15. DPOT_POSITION Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X				DPOT_POS[7:0] – MSB Left aligned										X	
X-0h				R/W-000h										X-0h	

Table 7-16. DPOT_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	X	X	0h	Don't care
11-2	DPOT_POS[7:0]	R/W	000h	Writing to the DPOT_POSITION register forces the digipot to update the active register data to the DPOT_POS. Data are in straight binary format and use the following format: { DPOT_POS[7:0], X, X } X = Don't care bits
1-0	X	X	0h	Don't care

7.6.5 USER_BYTE1 Register (address = 25h) (reset = 0000h)

Table 7-17. USER_BYTE1 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X				USER_BYTE1[7:0] – MSB Left aligned										X	
X-0h				R/$\overline{W}$-000h										X-0h	

Table 7-18. USER_BYTE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	X	X	0h	Don't care
11-2	USE_BYTE1[7:0] – MSB Left aligned	R/$\overline{W}$	000h	8-bit user-programmable data. Data are in straight binary format and use the following format: { USER_BYTE1[7:0], X, X } X = Don't care bits
1-0	X	X	0h	Don't care

7.6.6 USER_BYTE2 Register (address = 26h) (reset = 0000h)

Table 7-19. USER_BYTE2 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X				USER_BYTE2[7:0] – MSB Left aligned										X	
X-0h				R/$\overline{W}$-000h										X-0h	

Table 7-20. USER_BYTE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	X	X	0h	Don't care
11-2	USER_BYTE2[7:0] – MSB Left aligned	R/$\overline{W}$	000h	8-bit user-programmable data. Data are in straight binary format and follows the format below: { USER_BYTE2[7:0], X, X } X = Don't care bits
1-0	X	X	0h	Don't care

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPL1401 is a buffered, force-sense-output, single-channel, digipot that includes an internal reference and NVM, and is available in a tiny 2 mm × 2 mm package. This device interfaces to a processor using I^2C. There are 4 I^2C addresses possible by configuring the A0 pin as shown in Table 7-5. The NVM allows processor-less operation of this device after programming at factory. The force-sense output can work with a transitor to create a programmable current sink that can bias LEDs. These digipots are designed for general-purpose applications in a wide range of end equipment. Some of the most common applications for these devices are programmable current limits, adjustable power supplies, and offset and gain trimming in precision circuits.

8.2 Typical Application

Many analog and power devices, such as LED drivers, power amplifiers, high-side switches, e-fuses, and DC-DC converters, provide an analog input for an adjustable output current limit. Some of these devices recommend a resistor from this pin to ground for static settings. The TPL1401 is a very compact way to address the adjustable current limit requirements of such devices enabling scalability and configurability of these power devices. The integrated EEPROM makes sure the setting is retained even after power cycling, allowing the current limit to work without a processor. This section explains the design details of a programmable current limit application with an example LED driver, the TPS92692. Figure 8-1 shows the simplified circuit diagram of this application.

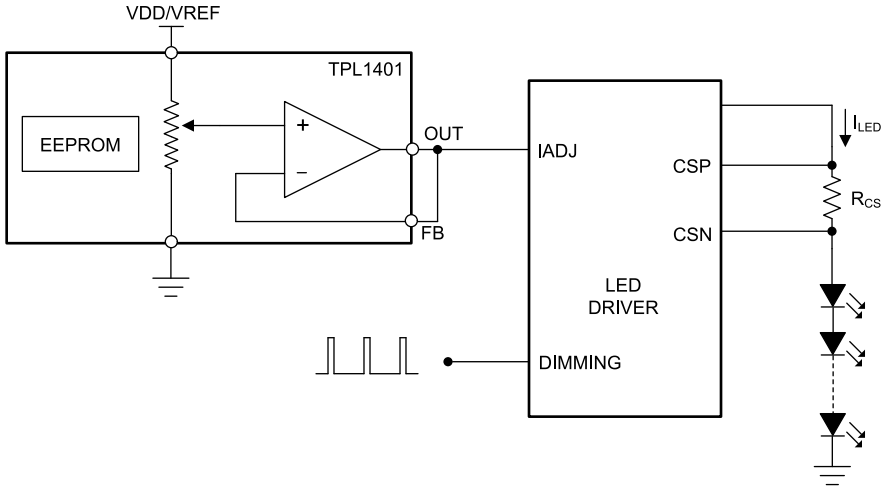


Figure 8-1. Programmable Current Limit

8.2.1 Design Requirements

- LED driver: TPS92692
- LED driver current limit: 100 mA

8.2.2 Detailed Design Procedure

The TPS92692 data sheet provides the equation for the voltage required to set a given LED current limit. Use a sense resistor of 1-Ω for the TPS92692.The voltage at the IADJ pin, V_{IADJ}, must be 1.4 V for an LED current of 100 mA. The range for V_{IADJ} is 2.5 V. Enable the internal reference with 2x gain to set the digipot output range to 2.42 V that will fairly be in the range of current adjustment for the LED driver. Calculate the code needed to set the digipot output to 1.4 V using the following equation:

$$DPOT\_POS = \frac{V_{IADJ}}{V_{REF} \times GAIN} \times 256 \quad (3)$$

The hex value for 148 is 0x94. Shift this value by 4 bits before writing to the DPOT_POSITION register, resulting in 0x940.

The pseudocode for the programmable current limit application is as follows:

```
//SYNTAX: WRITE <REGISTER NAME (Hex code)>, <MSB DATA>, <LSB DATA>
//Power-up the device, enable internal reference with 2x output span
WRITE GENERAL_CONFIG(0xD1), 0x11, 0xE5
//Write digipot code (12-bit aligned)
WRITE DPOT_POSITION(0x21), 0x09, 0x40
//Write settings to the NVM
WRITE PROTECT(0xD3), 0x00, 0x10
```

8.2.3 Application Curves

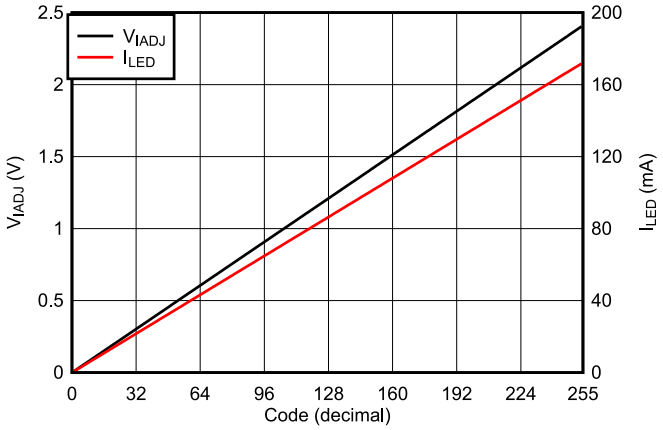


Figure 8-2. Digipot Code vs LED Current

9 Power Supply Recommendations

The TPL1401 does not require specific supply sequencing. The device requires a single power supply, V_{DD}. Use a 0.1-µF decoupling capacitor for the V_{DD} pin. Use a bypass capacitor with a value greater than 1.5-µF for the CAP pin.

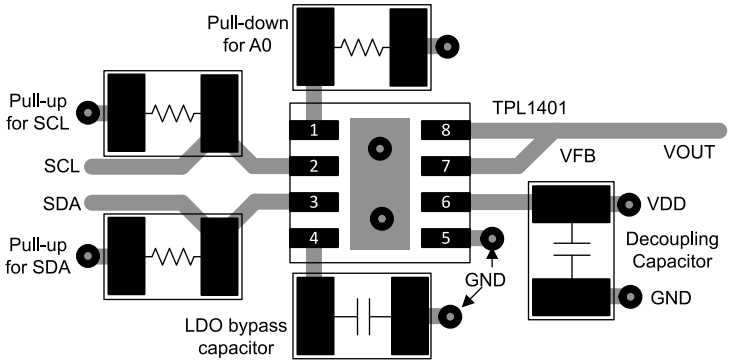
10 Layout

10.1 Layout Guidelines

The TPL1401 pin configuration separates the analog, digital, and power pins for an optimized layout. For signal integrity, separate the digital and analog traces, and place decoupling capacitors close to the device pins.

10.2 Layout Example

Figure 10-1 shows an example layout drawing with decoupling capacitors and pullup resistors.



(Note: Ground and Power planes omitted for clarity)

Figure 10-1. Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

Texas, Instruments *TPL1401EVM* user's guide

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPL1401DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	14_1
TPL1401DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	14_1
TPL1401DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	14_1
TPL1401DSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	14_1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

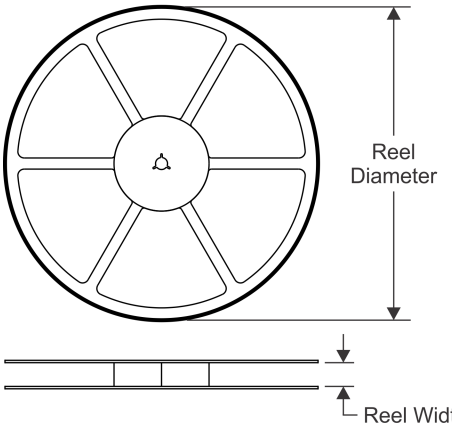
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

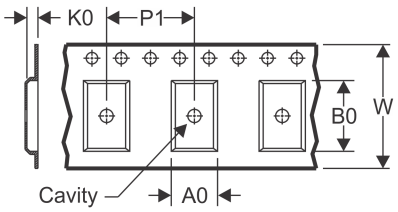
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

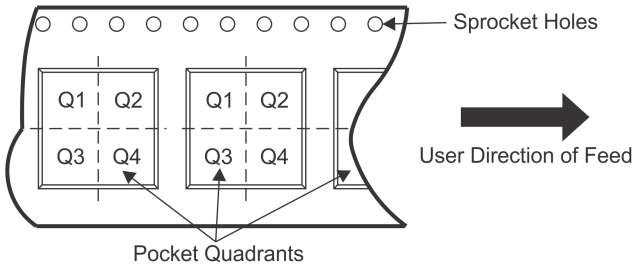


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

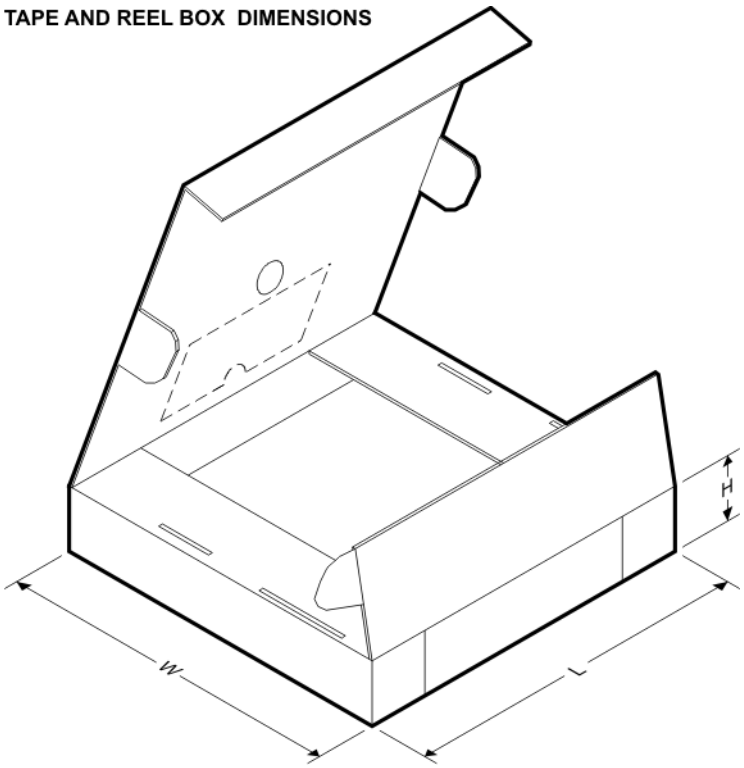
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPL1401DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPL1401DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPL1401DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPL1401DSGT	WSON	DSG	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

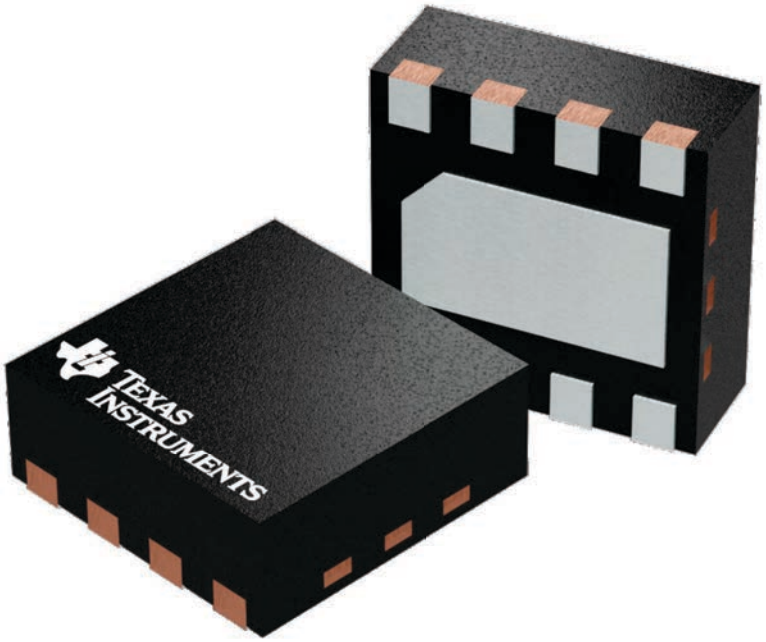
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



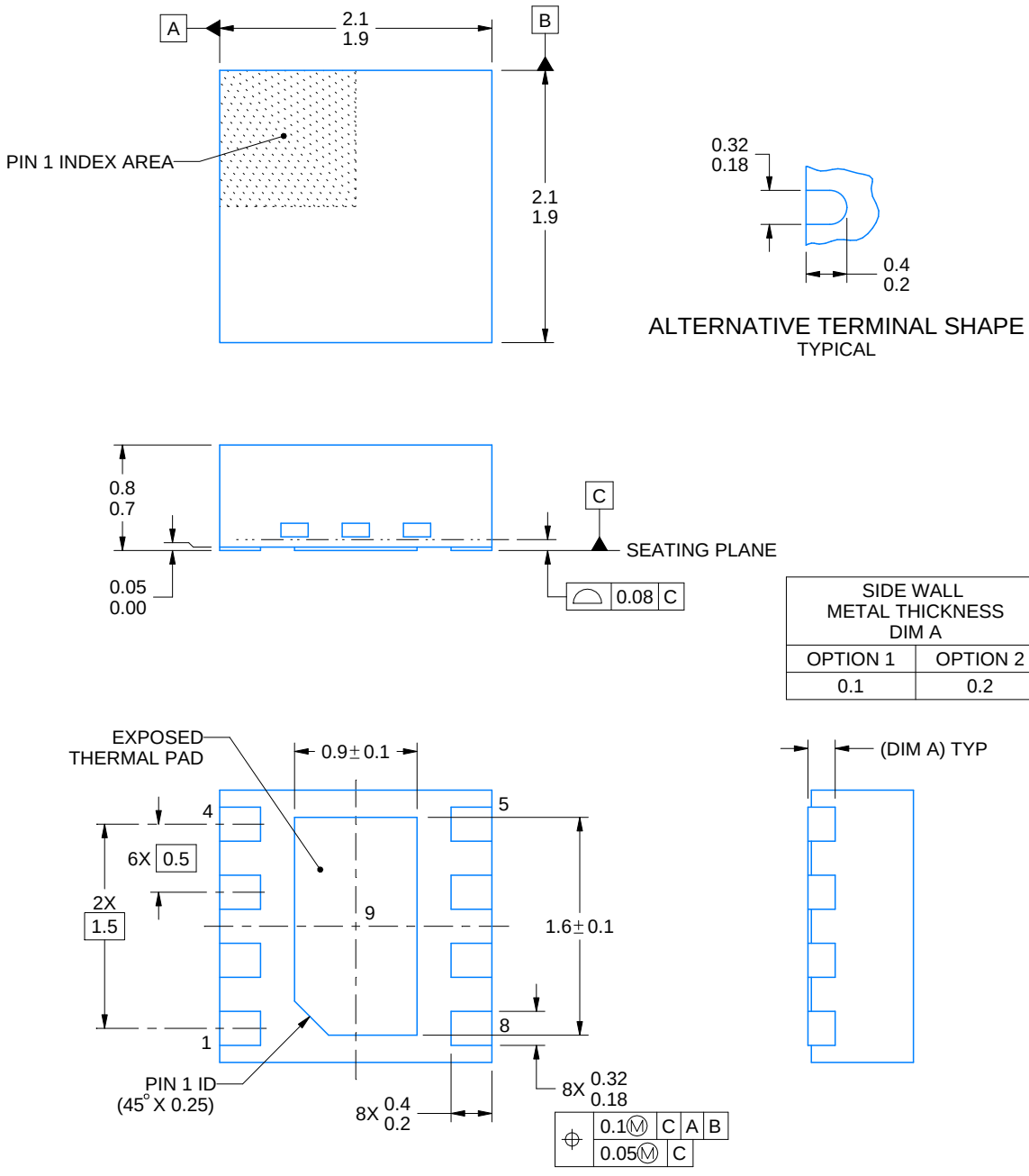
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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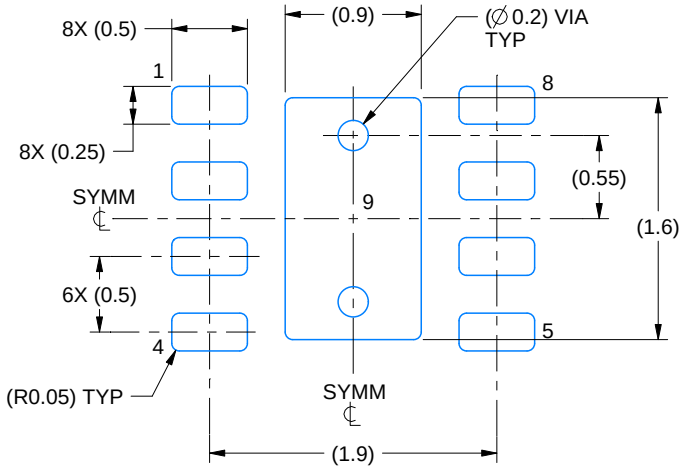
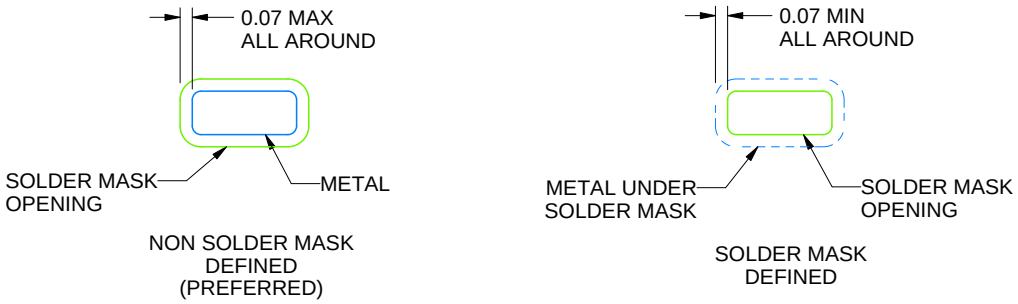
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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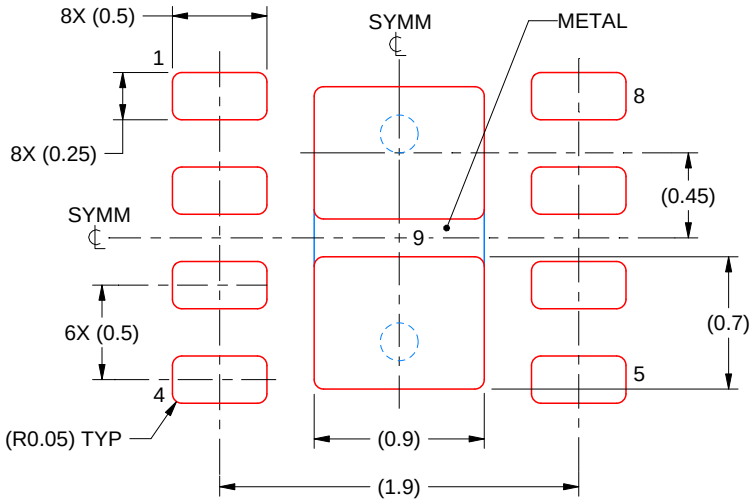
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025