1 Features

- Selectable Time Intervals: 100 ms to 7200 s
- Timer Accuracy: 1% (Typical)
- Current Consumption at 2.5 V and 35 nA (Typical)
- Resistor Selectable Time Interval
- Manual Power-On Input
- One-Shot Feature
- Supply Voltage Range: 1.8 V to 5.5 V

2 Applications

- Duty Cycle Control of Battery-Powered Systems
- Internet of Things (IoT)
- Intruder Detection
- Tamper Detection
- Home Automation Sensors
- Thermostats
- Consumer Electronics
- Remote Sensor
- White Goods

3 Description

The TPL5111 Nano Timer is a low-power system timer designed for power gating in duty cycled or battery-powered applications. Consuming only 35 nA, the TPL5111 can be used to enable and disable the power supply for a micro-controller or other system device, drastically reducing the overall system standby current during the sleep time. This power saving enables the use of significantly smaller batteries for energy harvesting or wireless sensor applications. The TPL5111 provides selectable timing intervals from 100 ms to 7200 s. In addition, the TPL5111 has a unique one-shot feature where the timer will only assert its enable pulse for one cycle. The TPL5111 is available in a 6-pin SOT23 package.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPL5111</td>
<td>SOT (6) DDC</td>
<td>3.00 mm × 3.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History

Changes from Revision A (July 2015) to Revision B

Page

• Changed T_{ADC} and R_{f} equations in the Quantization Error section ........................................ 14
• Added Receiving Notification of Documentation Updates section ........................................... 18

Changes from Original (June 2015) to Revision A

Page

• Added full data sheet. ............................................... 1
### 5 Pin Configuration and Functions

#### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE(1)</th>
<th>DESCRIPTION</th>
<th>APPLICATION INFORMATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NO.</td>
<td>NAME</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>VDD</td>
<td>P</td>
<td>Supply voltage</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>G</td>
<td>Ground</td>
</tr>
<tr>
<td>3</td>
<td>DELAY/</td>
<td>I</td>
<td>Time interval configuration (during power on) and logic input for manual Power ON</td>
</tr>
<tr>
<td></td>
<td>M_DRV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>DONE</td>
<td>I</td>
<td>Logic Input for watchdog functionality</td>
</tr>
<tr>
<td>5</td>
<td>DRVn</td>
<td>O</td>
<td>Power Gating output signal generated every ( t_P )</td>
</tr>
<tr>
<td>6</td>
<td>EN/</td>
<td>I</td>
<td>Select mode of operation</td>
</tr>
<tr>
<td></td>
<td>ONE_SHOT</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) G= Ground, P= Power, O= Output, I= Input.
6 Specifications

6.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (VDD-GND)</td>
<td>−0.3</td>
<td>6.0</td>
</tr>
<tr>
<td>Input Voltage at any pin</td>
<td>−0.3</td>
<td>VDD + 0.3</td>
</tr>
<tr>
<td>Input Current on any pin</td>
<td>−5</td>
<td>5</td>
</tr>
<tr>
<td>Junction Temperature, $T_J$</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature, $T_{stg}$</td>
<td>−65</td>
<td>150</td>
</tr>
</tbody>
</table>

1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2) The voltage between any two pins should not exceed 6 V.

3) The maximum power dissipation is a function of $T_J(\text{MAX})$, $R_{\theta JA}$, and the ambient temperature, $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_{\text{DMAX}} = (T_J(\text{MAX}) - T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly onto a printed-circuit board (PCB).

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>±1000</td>
<td>V</td>
</tr>
<tr>
<td>±250</td>
<td>V</td>
</tr>
</tbody>
</table>

1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Ratings

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.8</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>−40</td>
<td>105</td>
<td>°C</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC</th>
<th>TPL5111 DDC (SOT-23)</th>
<th>TPL5111 DDC 6 PINS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\theta JA}$</td>
<td>163 °C/W</td>
<td>163 °C/W</td>
</tr>
<tr>
<td>$R_{\theta JC(top)}$</td>
<td>26 °C/W</td>
<td>26 °C/W</td>
</tr>
<tr>
<td>$R_{\theta JB}$</td>
<td>57 °C/W</td>
<td>57 °C/W</td>
</tr>
<tr>
<td>$\psi_{JT}$</td>
<td>7.5 °C/W</td>
<td>7.5 °C/W</td>
</tr>
<tr>
<td>$\psi_{JB}$</td>
<td>57 °C/W</td>
<td>57 °C/W</td>
</tr>
<tr>
<td>$R_{\theta JC(bot)}$</td>
<td>N/A °C/W</td>
<td>N/A °C/W</td>
</tr>
</tbody>
</table>

1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report (SPRA953).
6.5 Electrical Characteristics

Specifications are for $T_A = 25^\circ C$, $VDD$-$GND = 2.5$ V, unless otherwise stated.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN(2)</th>
<th>TYP(3)</th>
<th>MAX(2)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDD</td>
<td>Supply current(4)</td>
<td>Operation mode</td>
<td>35</td>
<td>50</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Digital conversion of external resistance (Rext)</td>
<td>200</td>
<td>400</td>
<td>µA</td>
</tr>
</tbody>
</table>

**POWER SUPPLY**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN(2)</th>
<th>TYP(3)</th>
<th>MAX(2)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>TIp</td>
<td>Time interval Period</td>
<td>1650 selectable Time intervals</td>
<td>Minimum time interval</td>
<td>100</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Maximum time interval</td>
<td>7200</td>
<td>s</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time interval Setting Accuracy(5)</td>
<td>Excluding the precision of Rext</td>
<td>±0.6%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time interval Setting Accuracy over supply voltage</td>
<td>$1.8 , V \leq VDD \leq 5.5 , V$</td>
<td>±25</td>
<td>ppm/V</td>
<td></td>
</tr>
<tr>
<td>TOSC</td>
<td>Oscillator Accuracy</td>
<td>–0.5%</td>
<td>0.5%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Oscillator Accuracy over temperature(6)</td>
<td>$-40^\circ C \leq T_A \leq 105^\circ C$</td>
<td>±100</td>
<td>±400</td>
<td>ppm/°C</td>
</tr>
<tr>
<td></td>
<td>Oscillator Accuracy over supply voltage</td>
<td>$1.8 , V \leq VDD \leq 5.5 , V$</td>
<td>±0.4</td>
<td>%/V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Oscillator Accuracy over life time(7)</td>
<td>–0.24%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TDONE</td>
<td>DONE Pulse width (6)</td>
<td>100</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DRVn</td>
<td>DRVn Pulse width</td>
<td>DONE signal not received</td>
<td>TIp-50</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>T_Rext</td>
<td>Time to convert Rext</td>
<td>100</td>
<td>120</td>
<td>ms</td>
<td></td>
</tr>
</tbody>
</table>

**DIGITAL LOGIC LEVELS**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN(2)</th>
<th>TYP(3)</th>
<th>MAX(2)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logic High Threshold DONE pin</td>
<td>$0.7 \times VDD$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Logic Low Threshold DONE pin</td>
<td>$0.3 \times VDD$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>Logic output High Level DRVn pin</td>
<td>$I_{out} = 100 , \mu A$</td>
<td>VDD – 0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{out} = 1 , mA$</td>
<td>VDD – 0.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>Logic output Low Level DRVn pin</td>
<td>$I_{out} = -100 , \mu A$</td>
<td>VDD – 0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{out} = -1 , mA$</td>
<td>VDD – 0.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VIHM_DRV</td>
<td>Logic High Threshold DELAY/MDRV pin</td>
<td>1.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Electrical Characteristics values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

(2) Limits are specified by testing, design, or statistical analysis at $25^\circ C$. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.

(4) The supply current excludes load and pullup resistor current. Input pins are at GND or VDD.

(5) The accuracy for time interval settings below 1 second is ±10 0ms.

(6) This parameter is specified by design and/or characterization and is not tested in production.

(7) Operational life time test procedure equivalent to 10 years.
6.6 Timing Requirements

<table>
<thead>
<tr>
<th></th>
<th>MIN(^{(1)})</th>
<th>NOM(^{(2)})</th>
<th>MAX(^{(1)})</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{\text{DRVn}})</td>
<td>Rise Time DRVn(^{(3)}) Capacitive load 50 pF</td>
<td>50</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>(t_{\text{DRVn}})</td>
<td>Fall Time DRVn(^{(3)}) Capacitive load 50 pF</td>
<td>50</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>(t_{\text{DONE}})</td>
<td>DONE to DRVn delay Minimum delay (^{(4)})</td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>(t_{\text{DRV}})</td>
<td>Maximum delay (^{(4)})</td>
<td>(t_{\text{DRVn}})</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{\text{M_DRV}})</td>
<td>Valid manual MOSFET Power ON Observation time 30 ms</td>
<td>20</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>(t_{\text{DB}})</td>
<td>De-bounce manual MOSFET Power ON</td>
<td>20</td>
<td>ms</td>
<td></td>
</tr>
</tbody>
</table>

(1) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.

(3) This parameter is specified by design and/or characterization and is not tested in production.

(4) From DRVn rising edge.

Figure 1. TPL5111 Timing
6.7 Typical Characteristics

Figure 2. $I_{DD}$ vs. $V_{DD}$

Figure 3. $I_{DD}$ vs. Temperature

Figure 4. Oscillator Accuracy vs. $V_{DD}$

Figure 5. Oscillator Accuracy vs. Temperature

Figure 6. $I_{DD}$ vs. Time

Figure 7. Time Interval Setting Accuracy
### 7 Detailed Description

#### 7.1 Overview

The TPL5111 is a timer with power gating feature. The TPL5111 can be used in power-cycled applications and provides selectable timing from 100 ms to 7200 s.

When configured in timer mode (EN/ONE_SHOT = HIGH), the TPL5111 periodically asserts a DRVn signal to an LDO or DC-DC converter that is used to turn on a microcontroller. If the microcontroller replies with a DONE signal within the programmed time interval (< t\text{DRVn}), the TPL5111 de-asserts DRVn. Otherwise, the TPL5111 asserts DRVn for a time equal to t\text{DRVn}.

The TPL5111 can also work in a one-shot mode (EN/ONE_SHOT = LOW). In this mode, the DRVn signal is asserted just one time at the power on of the TPL5111. If the μC replies with a DONE signal within the programmed time interval (< t\text{DRVn}), the TPL5111 de-asserts DRVn. Otherwise, the TPL5111 asserts DRVn for a time equal to t\text{DRVn}.

#### 7.2 Functional Block Diagram

![Functional Block Diagram](image)

#### 7.3 Feature Description

The TPL5111 implements a periodic power gating feature or one-shot power gating according to the EN/ONE_SHOT voltage. A manual Power ON function is realized by momentarily pulling the DELAY/M_DRV pin to VDD.

##### 7.3.1 DRVn

The DRVn pin may be connected to the enable input of an LDO or DC-DC converter. The pulse generated at DRVn is equal to the programmed time interval period (t\text{Ip}), minus 50 ms. It is shorter if a DONE signal is received from the μC before t\text{Ip} – 50 ms. If the DONE signal is not received within t\text{Ip} – 50 ms, the DRVn signal will be LOW for the last 50 ms of t\text{Ip} before the next cycle starts.

The default value (after resistance reading) is HIGH. The signal is sent out from the TPL5111 when the programmed time interval starts. When the DRVn is HIGH, the manual power ON signal is ignored.

##### 7.3.2 DONE

The DONE pin is driven by a μC to signal that the μC is working properly. The TPL5111 recognizes a valid DONE signal as a low to high transition. If two or more DONE signals are received within the time interval, only the first DONE signal is processed. The minimum DONE signal pulse length is 100 ns. When the TPL5111 receives the DONE signal it asserts DRVn logic LOW.
7.4 Device Functional Modes

7.4.1 Start-Up

During start-up after POR, the TPL5111 executes a one-time measurement of the resistance attached to the \text{DELAY/M_DRV} pin in order to determine the desired time interval for \text{DRVn}. This measurement interval is \text{t}_{R_{EXT}}. During this measurement a constant current is temporarily flowing into \text{R_{EXT}}.

Once the reading of the external resistance is complete, the TPL5111 enters automatically in one of the two modes according to the \text{EN/ONE_SHOT} value. The \text{EN/ONE_SHOT} pin must be hard wired to GND or VDD according to the required mode of operation.

![Figure 8. Startup - Timer Mode](image)

7.4.2 Timer Mode

During timer mode (\text{EN/ONE_SHOT} = \text{HIGH}), the TPL5111 asserts periodic \text{DRVn} pulses according to the programmed time interval. The length of the \text{DRVn} pulses is set by the receiving of a \text{DONE} pulse from the \text{µC}. See Figure 8.

7.4.3 One-Shot Mode

During one-shot mode (\text{EN/ONE_SHOT} = \text{LOW}), the TPL5111 generates just one pulse at the \text{DRVn} pin which lasts according to the programmed time interval. In one-shot mode, other \text{DRVn} pulses can be triggered using the \text{DELAY/M_DRV} pin. If a valid manual power ON occurs when \text{EN/ONE_SHOT} is \text{LOW}, the TPL5111 generates just one pulse at the \text{DRVn} pin. The duration of the pulse is set by the programmed time interval. Also in this case, if a \text{DONE} signal is received within the programmed time interval (minus 50 ms), the \text{DRVn} output is asserted \text{LOW}. See Figure 9 and Figure 10.

![Figure 9. Start-Up One-Shot Mode (DONE Received Within \text{t}_{\text{IP}})](image)
Device Functional Modes (continued)

7.5 Programming

7.5.1 Configuring the Time Interval With the DELAY/M_DRV Pin

The time interval between two adjacent DRVn pulses (rising edges, in timer mode) is selectable through an external resistance ($R_{\text{EXT}}$) between the DELAY/M_DRV pin and ground. The resistance ($R_{\text{EXT}}$) must be in the range between 500 Ω and 170 kΩ. At least a 1% precision resistance is recommended. See Selection of the External Resistance on how to set the time interval using $R_{\text{EXT}}$. During start-up, the external resistance is read immediately after POR.

7.5.2 Manual Power ON Applied to the DELAY/M_DRV Pin

If VDD is applied to the DELAY/M_DRV pin after start-up is completed, the TPL5111 recognizes this as a manual Power ON condition. In this case $R_{\text{EXT}}$ is not re-read. If the manual Power ON is asserted during the POR or during the $R_{\text{EXT}}$ reading procedure, the reading procedure is aborted and is restarted as soon as the manual Power ON switch is released. A pulse on the DELAY/M_DRV pin is recognized as a valid manual Power ON only if it lasts at least 20 ms (observation time is 30 ms). If DRVn is already HIGH the manual Power ON is ignored. The manual Power ON may be implemented using a switch (momentary mechanical action).

---

Figure 10. Start-Up One-Shot Mode (No DONE Received Within $t_{\text{IP}}$)

Figure 11. Manual Power ON in Timer Mode
Programming (continued)

![Diagram of Manual Power ON in One-Shot Mode]

**Figure 12. Manual Power ON in One-Shot Mode**

### 7.5.2.1 DELAY/M_DRV

A resistance in the range between 500 Ω and 170 kΩ must be connected to the DELAY/M_DRV pin to select a valid time interval. At POR and during the reading of $R_{\text{EXT}}$, the DELAY/M_DRV pin is internally connected to an analog signal chain through a multiplexer. After the reading of $R_{\text{EXT}}$, the analog circuit is switched off and the DELAY/M_DRV pin is internally connected to a digital circuit.

In this state, a logic HIGH applied to the DELAY/M_DRV pin is interpreted by the TPL5111 as a manual power ON. The manual power ON detection is provided with a de-bounce feature (on both edges) which makes the TPL5111 insensitive to the glitches on the DELAY/M_DRV.

The DELAY/M_DRV pin must stay HIGH for at least 20 ms to be valid. Once a valid signal at DELAY/M_DRV is understood as a manual power on, the DRVn signal will be asserted within the next 10 ms. Its duration will be according to the programmed time interval (minus 50 ms), or less if the DONE is received.

A manual power ON signal resets all the counters. The counters will restart as soon as a valid manual power ON signal is recognized and the signal at DELAY/M_DRV pin is asserted LOW. Due to the asynchronous nature of the manual power ON signal and its arbitrary duration, the HIGH status of the DRVn signal may have an uncertainty of about ±5 ms.

An extended assertion of a logic HIGH at the DELAY/M_DRV pin will turn on DRVn for a time longer than the programmed time interval. DONE signals received while the DELAY/M_DRV is HIGH are ignored. If the DRVn is already HIGH the manual power ON is ignored.

### 7.5.2.2 Circuitry

The manual Power ON may be implemented using a switch (momentary mechanical action). Using a single-pole single-throw (SPST) switch offers a low cost solution. The DELAY/M_DRV pin may be directly connected to $V_{\text{DD}}$ with $R_{\text{EXT}}$ in the circuit. The current drawn from the supply voltage during the manual power ON is given by $V_{\text{DD}}/R_{\text{EXT}}$. 
Programming (continued)

7.5.3 Selection of the External Resistance

To set the time interval, the external resistance \( R_{\text{EXT}} \) is selected according to Equation 1:

\[
R_{\text{EXT}} = 100 \left( \frac{-b + \sqrt{b^2 - 4a(c - 100T)}}{2a} \right)
\]

where
- \( T \) is the desired time interval (\( t_{\text{IP}} \)) in seconds.
- \( R_{\text{EXT}} \) is the resistance value in \( \Omega \).
- \( a, b, c \) are coefficients depending on the value of the desired time interval. The coefficients are selected from Table 1 based on the range in which the desired \( t_{\text{IP}} \) falls. (1)

Table 1. Coefficients for Equation 1

<table>
<thead>
<tr>
<th>SET</th>
<th>TIME INTERVAL RANGE (S)</th>
<th>( a )</th>
<th>( b )</th>
<th>( c )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1 &lt; ( T ) ≤ 5</td>
<td>0.2253</td>
<td>-20.7654</td>
<td>570.5679</td>
</tr>
<tr>
<td>2</td>
<td>5 &lt; ( T ) ≤ 10</td>
<td>-0.1284</td>
<td>46.9861</td>
<td>-2651.8889</td>
</tr>
<tr>
<td>3</td>
<td>10 &lt; ( T ) ≤ 100</td>
<td>0.1972</td>
<td>-19.3450</td>
<td>692.1201</td>
</tr>
<tr>
<td>4</td>
<td>100 &lt; ( T ) ≤ 1000</td>
<td>0.2617</td>
<td>-56.2407</td>
<td>5957.7934</td>
</tr>
<tr>
<td>5</td>
<td>( T &gt; 1000 )</td>
<td>0.3177</td>
<td>-136.2571</td>
<td>34522.4680</td>
</tr>
</tbody>
</table>

EXAMPLE

Required time interval: 8 s

Coefficient set number 2 is used in this case. The formula becomes Equation 2.

\[
R_{\text{EXT}} = 100 \left( \frac{46.9861 - \sqrt{46.9861^2 + 4 \times 0.1284(-2561.8889 - 100T)}}{2 \times 0.1284} \right)
\]

The resistance value is 10.18 k\( \Omega \).

Table 2 and Table 3 contain example values of \( t_{\text{IP}} \) and their corresponding value of \( R_{\text{EXT}} \).
Table 2. First 9 Time Intervals

<table>
<thead>
<tr>
<th>(t_\text{IP}) (ms)</th>
<th>RESISTANCE (Ω)</th>
<th>CLOSEST REAL VALUE (Ω)</th>
<th>PARALLEL of TWO 1% TOLERANCE RESISTORS, (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>500</td>
<td>500</td>
<td>1.0 // 1.0</td>
</tr>
<tr>
<td>200</td>
<td>1000</td>
<td>1000</td>
<td>-</td>
</tr>
<tr>
<td>300</td>
<td>1500</td>
<td>1500</td>
<td>2.43 // 3.92</td>
</tr>
<tr>
<td>400</td>
<td>2000</td>
<td>2000</td>
<td>-</td>
</tr>
<tr>
<td>500</td>
<td>2500</td>
<td>2500</td>
<td>4.42 // 5.76</td>
</tr>
<tr>
<td>600</td>
<td>3000</td>
<td>3000</td>
<td>5.36 // 6.81</td>
</tr>
<tr>
<td>700</td>
<td>3500</td>
<td>3500</td>
<td>4.75 // 13.5</td>
</tr>
<tr>
<td>800</td>
<td>4000</td>
<td>4000</td>
<td>6.19 // 11.3</td>
</tr>
<tr>
<td>900</td>
<td>4500</td>
<td>4501</td>
<td>6.19 // 16.5</td>
</tr>
</tbody>
</table>

Table 3. Most Common Time Intervals Between 1s to 2h

<table>
<thead>
<tr>
<th>(t_\text{IP})</th>
<th>CALCULATED RESISTANCE (kΩ)</th>
<th>CLOSEST REAL VALUE (kΩ)</th>
<th>PARALLEL of TWO 1% TOLERANCE RESISTORS, (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1s</td>
<td>5.20</td>
<td>5.202</td>
<td>7.15 // 19.1</td>
</tr>
<tr>
<td>2s</td>
<td>6.79</td>
<td>6.788</td>
<td>12.4 // 15.0</td>
</tr>
<tr>
<td>3s</td>
<td>7.64</td>
<td>7.628</td>
<td>12.7 // 19.1</td>
</tr>
<tr>
<td>4s</td>
<td>8.30</td>
<td>8.306</td>
<td>14.7 // 19.1</td>
</tr>
<tr>
<td>5s</td>
<td>8.85</td>
<td>8.852</td>
<td>16.5 // 19.1</td>
</tr>
<tr>
<td>6s</td>
<td>9.27</td>
<td>9.223</td>
<td>18.2 // 18.7</td>
</tr>
<tr>
<td>7s</td>
<td>9.71</td>
<td>9.673</td>
<td>19.1 // 19.6</td>
</tr>
<tr>
<td>8s</td>
<td>10.18</td>
<td>10.180</td>
<td>11.5 // 8.87</td>
</tr>
<tr>
<td>9s</td>
<td>10.68</td>
<td>10.68</td>
<td>17.8 // 26.7</td>
</tr>
<tr>
<td>10s</td>
<td>11.20</td>
<td>11.199</td>
<td>15.0 // 44.2</td>
</tr>
<tr>
<td>20s</td>
<td>14.41</td>
<td>14.405</td>
<td>16.9 // 97.6</td>
</tr>
<tr>
<td>30s</td>
<td>16.78</td>
<td>16.778</td>
<td>32.4 // 34.8</td>
</tr>
<tr>
<td>40s</td>
<td>18.75</td>
<td>18.748</td>
<td>22.6 // 110.0</td>
</tr>
<tr>
<td>50s</td>
<td>20.047</td>
<td>20.047</td>
<td>28.7 // 66.5</td>
</tr>
<tr>
<td>1min</td>
<td>22.02</td>
<td>22.021</td>
<td>40.2 // 48.7</td>
</tr>
<tr>
<td>2min</td>
<td>29.35</td>
<td>29.349</td>
<td>35.7 // 165.0</td>
</tr>
<tr>
<td>3min</td>
<td>34.73</td>
<td>34.729</td>
<td>63.4 // 76.8</td>
</tr>
<tr>
<td>4min</td>
<td>39.11</td>
<td>39.097</td>
<td>63.4 // 102.0</td>
</tr>
<tr>
<td>5min</td>
<td>42.90</td>
<td>42.887</td>
<td>54.9 // 196.0</td>
</tr>
<tr>
<td>6min</td>
<td>46.29</td>
<td>46.301</td>
<td>75.0 // 121.0</td>
</tr>
<tr>
<td>7min</td>
<td>49.38</td>
<td>49.392</td>
<td>97.6 // 100.0</td>
</tr>
<tr>
<td>8min</td>
<td>52.24</td>
<td>52.224</td>
<td>88.7 // 127.0</td>
</tr>
<tr>
<td>9min</td>
<td>54.92</td>
<td>54.902</td>
<td>86.6 // 150.0</td>
</tr>
<tr>
<td>10min</td>
<td>57.44</td>
<td>57.437</td>
<td>107.0 // 124.0</td>
</tr>
<tr>
<td>20min</td>
<td>77.57</td>
<td>77.579</td>
<td>140.0 // 174.0</td>
</tr>
<tr>
<td>30min</td>
<td>92.43</td>
<td>92.233</td>
<td>182.0 // 187.0</td>
</tr>
<tr>
<td>40min</td>
<td>104.67</td>
<td>104.625</td>
<td>130.0 // 536.00</td>
</tr>
<tr>
<td>50min</td>
<td>115.33</td>
<td>115.331</td>
<td>150.0 // 499.00</td>
</tr>
<tr>
<td>1h</td>
<td>124.91</td>
<td>124.856</td>
<td>221.0 // 287.00</td>
</tr>
<tr>
<td>1h 30min</td>
<td>149.39</td>
<td>149.398</td>
<td>165.0 // 1580.0</td>
</tr>
<tr>
<td>2h</td>
<td>170.00</td>
<td>170.00</td>
<td>340.0 // 340.0</td>
</tr>
</tbody>
</table>
7.5.4 Quantization Error

The TPL5111 can generate 1650 discrete timer intervals in the range of 100 ms to 7200 s. The first 9 intervals are multiples of 100 ms. The remaining 1641 intervals cover the range between 1 s to 7200 s. Because they are discrete intervals, there is a quantization error associated with each value.

The quantization error can be evaluated according to Equation 3:

$$ Err = 100 \left( \frac{T_{desired} - T_{ADC}}{T_{desired}} \right) $$

where

$$ T_{ADC} = \text{INT} \left[ \frac{1}{100} (a R_0^2 + b R_D + c) \right] $$

$$ R_D = \frac{R_{EXT}}{100} $$

Equation 3

$R_{EXT}$ is the resistance calculated with Equation 1 and $a$, $b$, $c$ are the coefficients of the equation listed in Table 1.

7.5.5 Error Due to Real External Resistance

$R_{EXT}$ is a theoretical value and may not be available in standard commercial resistor values. It is possible to closely approach the theoretical $R_{EXT}$ using two or more standard values in parallel. However, standard values are characterized by a certain tolerance. This tolerance will affect the accuracy of the time interval.

The accuracy can be evaluated using the following procedure:

1. Evaluate the min and max values of $R_{EXT}$ ($R_{EXT_{MIN}}$, $R_{EXT_{MAX}}$) with Equation 1 using the selected commercial resistance values and their tolerances.
2. Evaluate the time intervals ($T_{ADC_{MIN}}[R_{EXT_{MIN}}]$, $T_{ADC_{MAX}}[R_{EXT_{MAX}}]$) with the $T_{ADC}$ equation mentioned in Equation 3.
3. Find the errors using Equation 3 with $T_{ADC_{MIN}}$, $T_{ADC_{MAX}}$.

The results of the formula indicate the accuracy of the time interval.

The example below illustrates the procedure.

- Desired time interval, $T_{desired} = 600$ s,
- Required $R_{EXT}$ from Equation 1, $R_{EXT} = 57.44$ kΩ.

From Table 3 $R_{EXT}$ can be built with a parallel combination of two commercial values with 1% tolerance: $R1 = 107$ kΩ, $R2 = 124$ kΩ. The uncertainty of the equivalent parallel resistance can be found using Equation 4:

$$ uR_n = R_n \left( \frac{uR_1}{R1} \right)^2 + \left( \frac{uR_2}{R2} \right)^2 $$

where

- $uR_n$ (n=1,2) represent the uncertainty of a resistance (see Equation 5)

$$ u_{R_n} = R_n \frac{Tolerance}{\sqrt{3}} $$

Equation 4

The uncertainty of the parallel resistance is 0.82%, which means the value of $R_{EXT}$ may range between $R_{EXT_{MIN}} = 56.96$ kΩ and $R_{EXT_{MAX}} = 57.90$ kΩ.

Using these value of $R_{EXT}$, the digitized timer intervals calculated by $T_{ADC}$ equation mentioned in Equation 3 are respectively $T_{ADC_{MIN}} = 586.85$ s and $T_{ADC_{MAX}} = 611.3$ s, giving an error range of $-1.88% / +2.19%$. The asymmetry of the error range is due to the quadratic transfer function of the resistance digitizer.
8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

In battery-powered applications one design constraint is the need for low current consumption. The TPL5111 is suitable in applications where there is a need to monitor environmental conditions at a fixed time interval, but at a very low rate. In these applications a watchdog or other internal timer in a µC is often used to implement a wake-up function. Typically, the power consumption of these timers is not optimized. Using the TPL5111 to implement a periodic power gating of the µC or of the entire system can reduce current consumption to only tens of nA.

8.2 Typical Application

The TPL5111 can be used in environment sensor nodes such as humidity and temperature sensor node. The measured the humidity and temperature data may be transmitted to a host controller through a low power RF micro such as the CC2531. The temperature and the humidity in a home application do not change quickly, so the measurement and the transmission of the data can be done at very low rate, such as every 30 seconds. Using the TPL5111 as a system timer it is possible to completely turn off the RF micro when not transmitting and extend the battery life, as shown in Figure 14. The TPL5111 will turn on the LDO when the programmed time interval elapses. The manual Power ON switch can also be used to override the periodic turn-on behavior and enable on-demand power on.

![Figure 14. Sensor Node](image)

8.2.1 Design Requirements

Assume that the system design requirements include a low current consumption constraint to maximize battery life. The data may be acquired at a rate which is in the range between 30 s and 60 s, so the programmability of the TPL5111 allows optimization of system power consumption.
Typical Application (continued)

8.2.2 Detailed Design Procedure

When the primary constraint is battery life, the selection of a low power voltage regulator or DC-DC converter to power the µC is mandatory. The first step in the design is to calculate the power consumption of each device in the different modes of operation. An example is the HDC1000 digital humidity and temperature sensor combined with an RF micro. In measurement mode, the RF micro is in normal operating and transmission mode. The LDO or DC-DC converter should be selected to provide the necessary current source. For example, the HDC1000 consumes a maximum of 220 µA during a humidity measurement, and 300 µA during start-up. The CC2531 consumes 29 mA in TX mode. The LDO should be capable of sourcing > 30 mA, which is an easy requirement to meet.

Assuming the desired wake-up interval is 30 seconds, then referring to Table 3, the values for parallel R\text{\_EXT} resistors are 32.4 kΩ and 34.8 kΩ.

8.2.3 Application Curve

![Figure 15. Effect of TPL5111 on Current Consumption](image)

9 Power Supply Recommendations

The TPL5111 requires a voltage supply within 1.8 V and 5.5 V. A multilayer ceramic bypass X7R capacitor of 0.1 μF between VDD and GND pin is recommended.

10 Layout

10.1 Layout Guidelines

The DELAY/M\_DRV pin is sensitive to parasitic capacitance. TI recommends that the traces connecting the resistance on this pin to GROUND be kept as short as possible to minimize parasitic capacitance. This capacitance can affect the initial set up of the time interval. Signal integrity on the DRVn pin is also improved by keeping the trace length between the TPL5111 and the enable input of the LDO/DC-DC converter short to reduce the parasitic capacitance. The EN/ONE\_SHOT should to be tied to GND or VDD with short traces, and should never be left floating. The DONE input should never be left floating. If not tied to a µC GPIO, the DONE pin should be tied to ground.
10.2 Layout Example

Figure 16. Layout
11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources
The following links connect to TI community resources. Linked contents are provided “AS IS” by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks
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11.4 Electrostatic Discharge Caution
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary
SLYZ022 — Ti Glossary. This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
# PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead finish/Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPL5111DDCR</td>
<td>ACTIVE</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>6</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 105</td>
<td>ZFVX</td>
<td>Samples</td>
</tr>
<tr>
<td>TPL5111DDCT</td>
<td>ACTIVE</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>6</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 105</td>
<td>ZFVX</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

---

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
**TAPE AND REEL INFORMATION**

### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

### REEL DIMENSIONS

- **Reel Diameter**
- **Reel Width (W1)**

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Screw Holes**
- **User Direction of Feed**
- **Pocket Quadrants**

### PACKAGING MATERIALS INFORMATION

- **Device**: TPL5111DDCR
- **Package Type**: SOT-23-THIN
- **Drawing**: DDC
- **Pins**: 6
- **SPQ**: 3000
- **Reel Diameter (mm)**: 178.0
- **Reel Width W1 (mm)**: 8.4
- **A0 (mm)**: 3.2
- **B0 (mm)**: 3.2
- **K0 (mm)**: 1.4
- **P1 (mm)**: 4.0
- **W (mm)**: 8.0
- **Pin1 Quadrant**: Q3

- **Device**: TPL5111DDC
- **Package Type**: SOT-23-THIN
- **Drawing**: DDC
- **Pins**: 6
- **SPQ**: 250
- **Reel Diameter (mm)**: 178.0
- **Reel Width W1 (mm)**: 8.4
- **A0 (mm)**: 3.2
- **B0 (mm)**: 3.2
- **K0 (mm)**: 1.4
- **P1 (mm)**: 4.0
- **W (mm)**: 8.0
- **Pin1 Quadrant**: Q3

*All dimensions are nominal*
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPL5111DDCR</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>6</td>
<td>3000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPL5111DDCT</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>6</td>
<td>250</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

---

Pack Materials-Page 2
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

7. Board assembly site may have different recommendations for stencil design.
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