TPS1211-Q1 45-V, Automotive, Smart High-Side Driver with Protection and Diagnostics

1 Features

- AEC-Q100 qualified with the following results
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- 3.5-V to 40-V input range (45-V absolute maximum)
- Integrated 12-V charge pump with 100-µA capacity
- Low 1.7-µA shutdown current (EN/UVLO=Low)
- Strong pullup and pulldown gate driver: 4 A
- Drives external back-to-back N-Channel MOSFETs
- Variant with integrated precharge switch driver (TPS12111-Q1) to drive capacitive loads
- Two-level adjustable overcurrent protection (IWRN, ISCP) with adjustable response time (TMR) and fault flag output (FLT_I)
- Fast short-circuit protection: 1.2 µs (TPS12111-Q1), 5 µs (TPS12110-Q1)
- Accurate analog current monitor output (IMON) – ±2% at 30 mV (Vsense)
- Adjustable undervoltage lockout (UVLO) and overvoltage protection (OV)
- Remote overtemperature sensing (DIODE) and protection with fault flag output (FLT_T)
- Pin-to-pin compatible with TPS4811-Q1

2 Applications

- Power distribution box
- Body control module
- DC/DC converter

3 Description

The TPS1211-Q1 family is a 45-V, smart high-side driver with protection and diagnostics. With wide operating voltage range of 3.5 V – 40 V, the device is suitable for 12-V system designs.

The device has a strong 4-A sink (PD) and source (PU) gate driver that enables power switching using parallel FETs in high-current system designs. Use INP as the gate driver control input.

The device has accurate current sensing (±2% at 30 mV) output (IMON) enabling systems for energy management. The device has integrated two-level overcurrent protection with FLT_I output with complete adjustability of thresholds and response time. Auto-retry and latch-off fault behavior can be configured. The device features remote overtemperature protection with FLT_T output.

The TPS12111-Q1 integrates a precharge driver (G) with control input (INP_G). This features enables designs that must drive large capacitive loads. In shutdown mode (EN/UVLO < 0.3 V), the controller draws IQ of 1.7 µA.

The TPS1211-Q1 is available in a 19-pin VSSOP package.

Package Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE(1)</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS12110-Q1,</td>
<td>DGX (VSSOP, 19)</td>
<td>5.10 mm × 3.00 mm</td>
</tr>
<tr>
<td>TPS12111-Q1(2)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) PRODUCT PREVIEW.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for preproduction products; subject to change without notice.
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>July 2022</td>
<td>*</td>
<td>Initial Release</td>
</tr>
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</table>
5 Device Comparison Table

<table>
<thead>
<tr>
<th>Feature</th>
<th>TPS12110-Q1</th>
<th>TPS12111-Q1(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overvoltage protection</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Precharge driver</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Short-circuit protection</td>
<td></td>
<td></td>
</tr>
<tr>
<td>response time</td>
<td>5 µs</td>
<td>1.2 µs</td>
</tr>
<tr>
<td>Overtemperature fault response</td>
<td>Auto-retry with fixed 512-ms timer</td>
<td>Latch-off</td>
</tr>
</tbody>
</table>

(1) PRODUCT PREVIEW

6 Pin Configuration and Functions

Table 6-1. Pin Functions

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>TPS12110-Q1 TYPE</th>
<th>TPS12111-Q1(1) TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN/UVLO</td>
<td>DGX-19 (VSSOP)</td>
<td>1</td>
<td>I</td>
</tr>
<tr>
<td>OV</td>
<td>2</td>
<td>—</td>
<td>I</td>
</tr>
<tr>
<td>INP_G</td>
<td>—</td>
<td>2</td>
<td>I</td>
</tr>
<tr>
<td>INP</td>
<td>3</td>
<td>3</td>
<td>I</td>
</tr>
<tr>
<td>PIN</td>
<td>NAME</td>
<td>TPS12110-Q1</td>
<td>TPS12111-Q1(1)</td>
</tr>
<tr>
<td>-----</td>
<td>------</td>
<td>------------</td>
<td>---------------</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DGX-19 (VSSOP)</td>
<td></td>
</tr>
<tr>
<td>FLT_T</td>
<td>4</td>
<td>4</td>
<td>O</td>
</tr>
<tr>
<td>FLT_I</td>
<td>5</td>
<td>5</td>
<td>O</td>
</tr>
<tr>
<td>GND</td>
<td>6</td>
<td>6</td>
<td>G</td>
</tr>
<tr>
<td>IMON</td>
<td>7</td>
<td>7</td>
<td>O</td>
</tr>
<tr>
<td>IWRN</td>
<td>8</td>
<td>8</td>
<td>I</td>
</tr>
<tr>
<td>TMR</td>
<td>9</td>
<td>9</td>
<td>I</td>
</tr>
<tr>
<td>DIODE</td>
<td>10</td>
<td>10</td>
<td>I</td>
</tr>
<tr>
<td>G</td>
<td>—</td>
<td>11</td>
<td>O</td>
</tr>
<tr>
<td>N.C</td>
<td>11</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>BST</td>
<td>12</td>
<td>12</td>
<td>O</td>
</tr>
<tr>
<td>SRC</td>
<td>13</td>
<td>13</td>
<td>O</td>
</tr>
<tr>
<td>PD</td>
<td>14</td>
<td>14</td>
<td>O</td>
</tr>
<tr>
<td>PU</td>
<td>15</td>
<td>15</td>
<td>O</td>
</tr>
<tr>
<td>CS-</td>
<td>17</td>
<td>17</td>
<td>I</td>
</tr>
<tr>
<td>CS+</td>
<td>18</td>
<td>18</td>
<td>I</td>
</tr>
<tr>
<td>ISCP</td>
<td>19</td>
<td>19</td>
<td>I</td>
</tr>
<tr>
<td>VS</td>
<td>20</td>
<td>20</td>
<td>Power</td>
</tr>
</tbody>
</table>

(1) PRODUCT PREVIEW
7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

<table>
<thead>
<tr>
<th>Input Pins</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VS, CS+, CS-, ISCP to GND</td>
<td>–1</td>
<td>45</td>
<td>V</td>
</tr>
<tr>
<td>VS, CS+, CS- to SRC</td>
<td>–60</td>
<td>45</td>
<td>V</td>
</tr>
<tr>
<td>SRC to GND</td>
<td>–30</td>
<td>45</td>
<td>V</td>
</tr>
<tr>
<td>PU, PD, G, BST to SRC</td>
<td>–0.3</td>
<td>16</td>
<td>mA</td>
</tr>
<tr>
<td>TMR, IWRN, DIODE to GND</td>
<td>–0.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>OV, EN/UVLO, INP, INP_ G, FLT_I, FLT_T to GND</td>
<td>–1</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>CS+ to CS-</td>
<td>–0.3</td>
<td>0.3</td>
<td>mA</td>
</tr>
<tr>
<td>I_{FLT_T}, I_{FLT_I}</td>
<td>10</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>I_{CS+} to I_{CS-}, 1ms</td>
<td>–100</td>
<td>100</td>
<td>mA</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Output Pins</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>PU, PD, G, BST to GND</td>
<td>–30</td>
<td>60</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IMON to GND</td>
<td>–1</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Operating junction temperature, Tj (2)</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>–40</td>
<td></td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Storage temperature, Tstg</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>–40</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.2 ESD Ratings

<table>
<thead>
<tr>
<th>ELECTROSTATIC DISCHARGE</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human body model (HBM), per AEC Q100-002(1)</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Charged device model (CDM), per AEC Q100-011</td>
<td>Corner pins (EN/UVLO, DIODE, G, VS)</td>
<td>±750</td>
</tr>
<tr>
<td>Other pins</td>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

<table>
<thead>
<tr>
<th>Input Pins</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VS, CS+, CS- to GND</td>
<td>0</td>
<td>40</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>EN/UVLO, OV to GND</td>
<td>0</td>
<td>15</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Output Pins</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>FLT_T, FLT_I to GND</td>
<td>0</td>
<td>15</td>
<td>nF</td>
<td></td>
</tr>
<tr>
<td>IMON to GND</td>
<td>0</td>
<td>5</td>
<td>µF</td>
<td></td>
</tr>
</tbody>
</table>

| External Capacitor | VS, SRC to GND | 22 | nF |
|                    | BST to SRC    | 0.1| µF |

<table>
<thead>
<tr>
<th>Tj</th>
<th>Operating Junction temperature(2)</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>–40</td>
<td></td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.

(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.
7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC</th>
<th>TPS1211x-Q1</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{\theta JA} )</td>
<td>Junction-to-ambient thermal resistance</td>
<td>87 °C/W</td>
</tr>
<tr>
<td>( R_{\theta JC(top)} )</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>26.5 °C/W</td>
</tr>
<tr>
<td>( R_{\theta JB} )</td>
<td>Junction-to-board thermal resistance</td>
<td>43.7 °C/W</td>
</tr>
<tr>
<td>( \Psi_{JT} )</td>
<td>Junction-to-top characterization parameter</td>
<td>0.5 °C/W</td>
</tr>
<tr>
<td>( \Psi_{JB} )</td>
<td>Junction-to-board characterization parameter</td>
<td>43.3 °C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

\[ T_J = -40 \degree C \text{ to } +125 \degree C, \ V(S) = V_{(CS+)} = V_{(CS-)} = 12 \text{ V}, \ V_{(BST-SRC)} = 12 \text{ V}, \ V_{(SRC)} = 0 \text{ V} \]

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
</table>

**SUPPLY VOLTAGE**
- \( V_S \) : Operating input voltage
- \( V_{(S\_PORR)} \) : Input supply POR threshold, rising
- \( V_{(S\_PORF)} \) : Input supply POR threshold, falling
- Total System Quiescent current, \( I_{(GND)} \) \( V_{(ENUVLO)} = 2 \text{ V} \)
- \( I_{(SHDN)} \) : SHDN current, \( I_{(GND)} \) \( V_{(ENUVLO)} = 0 \text{ V}, \ V_{(SRC)} = 0 \text{ V} \)

**ENABLE AND UNDERVOLTAGE LOCKOUT (EN/UVLO)**
- \( V_{(UVLO)} \) : UVLO threshold voltage, rising
- \( V_{(UVLOF)} \) : UVLO threshold voltage, falling
- \( V_{(ENF)} \) : Enable threshold voltage for low \( I_q \) shutdown, falling

**OVER VOLTAGE PROTECTION (OV) INPUT – TPS12110-Q1 Only**
- \( V_{(OVR)} \) : Overvoltage threshold input, rising
- \( V_{(OVF)} \) : Overvoltage threshold input, falling

**CHARGE PUMP (BST-SRC)**
- \( I_{(BST)} \) : Charge Pump Supply current \( V_{(BST-SRC)} = 10 \text{ V} \)
- \( V_{(BST-SRC)} \) : Charge Pump Turn ON voltage
- \( V_{(BST\_UVLO)} \) : UVLO voltage threshold, rising
- \( V_{(BST\_SRC)} \) : UVLO voltage threshold, falling
- \( V_{(BST-SRC)} \) : Charge Pump Voltage at \( V_S = 3.5 \text{ V} \)

**GATE DRIVER OUTPUTS (PU, PD, G)**
- \( I_{(PU)} \) : Peak Source Current
- \( I_{(PD)} \) : Peak Sink Current
- \( I_{(G)} \) : Gate charge (sourcing) current, on state
- \( I_{(G)} \) : Gate discharge (sinking) current, off state

**CURRENT SENSE AND OVER CURRENT PROTECTION (CS+, CS-, IMON, ISCP, IWRN)**
- \( V_{(OS\_SET)} \) : Input referred offset (\( V_{SNS} \) to \( V_{IMON} \) scaling)

\[ R_{SET} = 100 \text{Ω}, \ R_{IMON} = 5 \text{kΩ}, \ 10 \text{kΩ} \ (\text{corresponds to} \ V_{SNS} = 6 \text{mV to} \ 30 \text{mV}) \text{ Gain of 45 and 90 respectively.} \]

\( -350 \text{ µV} \)
### 7.5 Electrical Characteristics (continued)

\( T_J = -40 \, ^\circ\text{C} \) to \( +125 \, ^\circ\text{C} \), \( V_{(S)} = V_{(CS+)} = V_{(CS-)} = 12 \, \text{V}, V_{(BST-SRC)} = 12 \, \text{V}, V_{(SRC)} = 0 \, \text{V} \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{(SNS_WRN)} )</td>
<td>OCP threshold</td>
<td>28</td>
<td>30</td>
<td>32</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>OCP threshold</td>
<td>10</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>( I_{SCP} )</td>
<td>SCP Input Bias current</td>
<td>13</td>
<td>15</td>
<td>17</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( V_{(SNS_SCP)} )</td>
<td>SCP threshold</td>
<td>35</td>
<td>40</td>
<td>45</td>
<td>mV</td>
</tr>
</tbody>
</table>

#### DELAY TIMER (TMR)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{(TMR_SRC_CB)} )</td>
<td>TMR source current</td>
<td>77</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{(TMR_SRC_FLT)} )</td>
<td>TMR source current</td>
<td>2.5</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{(TMR_SNK)} )</td>
<td>TMR sink current</td>
<td>2.5</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
</tbody>
</table>

#### FAULT FLAG (FLT_1, FLT_7), INPUT CONTROLS (INP, INP_G)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{(FLT_T)} )</td>
<td>FLT Pull-down resistance</td>
<td>70</td>
<td></td>
<td></td>
<td>( \Omega )</td>
</tr>
<tr>
<td>( I_{(FLT_T)} )</td>
<td>FLT Input leakage current</td>
<td>0 V ≤ ( V_{(FLT_T)} ) ≤ 20 V</td>
<td>400</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>( V_{(INP_H)} )</td>
<td>2 V</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{(INP_L)} )</td>
<td>0.8 V</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{(INP_G_H)} )</td>
<td>TPS12111-Q1 Only</td>
<td>2 V</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{(INP_G_L)} )</td>
<td>0.8 V</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

#### TEMPERATURE SENSING AND PROTECTION (DIODE)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{(DIODE)} )</td>
<td>External diode current source</td>
<td>High level</td>
<td>160</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Low level</td>
<td>10</td>
<td>( \mu A )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_{(DIODE_TSD_rising)})</td>
<td>DIODE sense TSD rising threshold</td>
<td>16 A/A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>155</td>
<td>( ^\circ\text{C} )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) PRODUCT PREVIEW

### 7.6 Switching Characteristics

\( T_J = -40 \, ^\circ\text{C} \) to \( +125 \, ^\circ\text{C} \), \( V_{(CS+)} = V_{(CS-)} = 12 \, \text{V}, V_{(BST-SRC)} = 12 \, \text{V}, V_{(SRC)} = 0 \, \text{V} \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{(PU(INP_H))} )</td>
<td>INP Turn ON propagation Delay</td>
<td>( \text{INP} \uparrow \text{to PU} \uparrow ), ( C_L = 47 , \text{nF} )</td>
<td>2</td>
<td>( \mu s )</td>
<td></td>
</tr>
<tr>
<td>( t_{(PD(INP_L))} )</td>
<td>INP Turn OFF propagation Delay</td>
<td>( \text{INP} \downarrow \text{to PD} \downarrow ), ( C_L = 47 , \text{nF} )</td>
<td>1</td>
<td>( \mu s )</td>
<td></td>
</tr>
<tr>
<td>( t_{(G(INP_G_H))} )</td>
<td>INP_G Turn ON propagation Delay</td>
<td>( \text{INP}_G \uparrow \text{to G} \uparrow ), ( C_L = 1 , \text{nF}, \text{TPS12111-Q1 Only} )</td>
<td>25</td>
<td>( \mu s )</td>
<td></td>
</tr>
<tr>
<td>( t_{(G(INP_G_L))} )</td>
<td>INP_G Turn OFF propagation Delay</td>
<td>( \text{INP}_G \downarrow \text{to G} \downarrow ), ( C_L = 1 , \text{nF}, \text{TPS12111-Q1 Only} )</td>
<td>1</td>
<td>( \mu s )</td>
<td></td>
</tr>
<tr>
<td>( t_{(PD(UVLO_OFF))} )</td>
<td>UVLO Turn-OFF Propagation Delay</td>
<td>UVLO ( \downarrow \text{to PD} \downarrow ), ( C_L = 47 , \text{nF} )</td>
<td>4</td>
<td>( \mu s )</td>
<td></td>
</tr>
<tr>
<td>( t_{(PD(VS_OFF))} )</td>
<td>PD Turn-OFF delay during input supply (Vs) interruption</td>
<td>( \text{Vs} \downarrow \text{V}_{(SPOR_R)} \text{to PD} \downarrow ), ( C_L = 47 , \text{nF}, \text{INP = EN/UVLO = 2 V} )</td>
<td>40</td>
<td>( \mu s )</td>
<td></td>
</tr>
<tr>
<td>( t_{(PU(VS_ON))} )</td>
<td>PU Turn-ON delay during input supply (Vs) recovery</td>
<td>( \text{Vs} \uparrow \text{V}<em>{(SPOR_F)} \text{to PU} \uparrow ), ( C_L = 47 , \text{nF}, \text{INP = EN/UVLO = 2 V, V}</em>{(BST-SRC)} &gt; V_{(BST UVLOR)} )</td>
<td>350</td>
<td>( \mu s )</td>
<td></td>
</tr>
<tr>
<td>( t_{(PU(EN_ON))} )</td>
<td>PU Turn-ON delay during transition from shutdown mode to active mode with ( C_{BST} ) pre-biased</td>
<td>( \text{EN/UVLO} \uparrow \text{to PU} \uparrow ), ( C_L = 47 , \text{nF, INP = 2 V, V}<em>{(BST-SRC)} &gt; V</em>{(BST UVLOR)} )</td>
<td>350</td>
<td>( \mu s )</td>
<td></td>
</tr>
<tr>
<td>( t_{(PD(OV_OFF))} )</td>
<td>OV Turn-Off propogation Delay</td>
<td>( \text{OV} \uparrow \text{to PD} \downarrow ), ( C_L = 47 , \text{nF, TPS12110-Q1 Only} )</td>
<td>3</td>
<td>( \mu s )</td>
<td></td>
</tr>
<tr>
<td>( t_{(SC)} )</td>
<td>Short-Circuit Protection propagation Delay</td>
<td>( \text{INP}_S \uparrow \text{to PD} \uparrow ), ( C_L = 47 , \text{nF, TPS12111-Q1 Only} )</td>
<td>5</td>
<td>( \mu s )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( t_{(SC)} \uparrow \text{to PD} \downarrow ), ( C_L = 47 , \text{nF, TPS12111-Q1 Only} )</td>
<td>1.2</td>
<td>( \mu s )</td>
<td></td>
</tr>
</tbody>
</table>
### 7.6 Switching Characteristics (continued)

\( T_J = -40 \, ^\circ\text{C} \) to \(+125\, ^\circ\text{C} \). \( V_{(CS+)} = V_{(CS-)} = 12 \, \text{V} \), \( V_{(BST-SRC)} = 12 \, \text{V} \), \( V_{(SRC)} = 0 \, \text{V} \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{(OC)} )</td>
<td>Overcurrent protection delay</td>
<td>( (V_{(CS+)} - V_{(CS-)} \uparrow I_{(OC)} ) to PD ( \downarrow ), ( C_L = 47 , \text{nF}, C_{(TMR)} = 0 , \text{nF} )</td>
<td>24</td>
<td></td>
<td>( \mu\text{s} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( (V_{(CS+)} - V_{(CS-)} \uparrow I_{(OC)} ) to PD ( \downarrow ), ( C_L = 47 , \text{nF}, C_{(TMR)} = 18 , \text{nF} )</td>
<td>312</td>
<td></td>
<td>( \mu\text{s} )</td>
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<tr>
<td>( t_{\text{FLT}_I(\text{FLT}_\text{ASSERT})} )</td>
<td>FLT_ assertion delay</td>
<td></td>
<td>290</td>
<td></td>
<td>( \mu\text{s} )</td>
</tr>
<tr>
<td>( t_{\text{FLT}_I(\text{FLT}_\text{DE_ASSERT})} )</td>
<td>FLT_ de-assertion delay</td>
<td></td>
<td>260</td>
<td></td>
<td>( \mu\text{s} )</td>
</tr>
<tr>
<td>( t_{\text{FLT}_T(\text{AR})} )</td>
<td>TSD Auto-retry</td>
<td>TPS12110-Q1 Only</td>
<td>512</td>
<td></td>
<td>( \text{ms} )</td>
</tr>
</tbody>
</table>

(1) PRODUCT PREVIEW
8 Detailed Description

8.1 Overview

The TPS1211-Q1 family is a 45-V smart high-side drivers with protection and diagnostics. With wide operating voltage range of 3.5 V – 40 V, the device is suitable for 12-V system designs.

The device has a strong 4-A sink (PD) and source (PU) gate driver that enables power switching using parallel FETs in high current system designs. Use INP as the gate driver control input. MOSFET slew rate control (ON and OFF) is possible by placing external R-C components.

The device has accurate current sensing (±2% at 30 mV) output (IMON) enabling systems for energy management. The device has integrated two-level, overcurrent protection with FLT_I output with complete adjustability of thresholds and response time. Auto-retry and latch-off fault behavior can be configured.

The device features remote overtemperature protection with FLT_T output enabling robust system protection.

TPS12110-Q1 has an accurate overvoltage protection (±3%), providing robust load protection.

The TPS12111-Q1 integrates a precharge driver (G) with control input (INP_G). This feature enables system designs that must drive large capacitive loads by precharging first and then turning ON the main power FETs.

TPS1211-Q1 has an accurate undervoltage protection (±3%) using the EN/UVLO pin. Pull EN/UVLO low (< 0.3 V) to turn OFF the device and enter into shutdown mode. In shutdown mode, the controller draws a total IQ of 3 µA (maximum) at 12-V supply input.

8.2 Functional Block Diagram

Figure 8-1. TPS12110-Q1 Functional Block Diagram
8.3 Feature Description

8.3.1 Charge Pump and Gate Driver Output (VS, PU, PD, BST, SRC)

Figure 8-3 shows a simplified diagram of the charge pump and gate driver circuit implementation. The device houses a strong 3.7-A source and 4-A sink gate drivers. The strong gate drivers enable paralleling of FETs in high power system designs ensuring minimum transition time in saturation region. A 12-V, 100-µA charge pump is derived from VS terminal and charges the external boot-strap capacitor, C\textsubscript{BST} that is placed across the gate driver (BST and SRC).

In switching applications, if the charge pump supply demand is higher than 100 µA, then supply BST externally using a low leakage diode and 12-V supply as shown in the Figure 8-3.

VS is the supply pin to the controller. With VS applied and EN/UVLO pulled high, the charge pump turns ON and charges the C\textsubscript{BST} capacitor. After the voltage across C\textsubscript{BST} crosses V\textsubscript{(BST_UVLOR)}, the GATE driver section is activated. The device has a 1-V (typical) UVLO hysteresis to ensure chattering less performance during initial GATE turn ON. Choose C\textsubscript{BST} based on the external FET QG and allowed dip during FET turn-ON. The charge pump remains enabled until the BST to SRC voltage reaches 12.3 V, typically, at which point the charge pump is disabled decreasing the current draw on the VS pin. The charge pump remains disabled until the BST to SRC voltage discharges to 11.7 V typically at which point the charge pump is enabled. The voltage between BST and SRC continue to charge and discharge between 12.3 V and 11.7 V as shown in the Figure 8-4.
Use the following equation to calculate the initial gate driver enable delay.

\[ T_{\text{DRV\_EN}} = \frac{C_{\text{BST}} \times V_{\text{BST\_UVLOR}}}{100 \, \mu\text{A}} \]  

(1)

Where,

- \( C_{\text{BST}} \) is the charge pump capacitance connected across BST and SRC pins.
- \( V_{\text{BST\_UVLOR}} = 7.5 \, \text{V} \) (typical).
If $T_{\text{DRV\_EN}}$ must be reduced, then pre-bias the BST terminal externally using an external 12-V supply through a low leakage diode D1 as shown in Figure 8-3. With this connection, $T_{\text{DRV\_EN}}$ reduces to 350 $\mu$s.

### 8.3.2 Capacitive Load Driving

Certain end equipments like automotive power distribution unit power different loads including other ECUs. These ECUs can have large input capacitances. If power to the ECUs is switched on in uncontrolled way, large inrush currents can occur potentially damaging the power FETs.

To limit the inrush current during capacitive load switching, the following system design techniques can be used with TPS1211x-Q1 devices.

#### 8.3.2.1 FET Gate Slew Rate Control

For limiting inrush current during turn-ON of the FET with capacitive loads, use $R_1$, $R_2$, $C_1$ as shown in Figure 8-5. The $R_1$ and $C_1$ components slow down the voltage ramp rate at the gate of the FET. The FET source follows the gate voltage resulting in a controlled voltage ramp across the output capacitors.

![Figure 8-5. Inrush Current Limiting with FET Gate Slew Rate Control](image)

Use the Equation 2 to calculate the inrush current during turn-ON of the FET.

$$I_{\text{INRUSH}} = C_{\text{LOAD}} \times \frac{V_{\text{BATT}}}{T_{\text{charge}}}$$

(2)

$$I_{\text{INRUSH}} = \frac{0.63 \times V_{\text{(BST-SRC)}} \times C_{\text{LOAD}}}{R_1 \times C_1}$$

(3)

Where,

- $C_{\text{LOAD}}$ is the load capacitance,
- $V_{\text{BATT}}$ is the input voltage and $T_{\text{charge}}$ is the charge time,
- $V_{\text{(BST-SRC)}}$ is the charge pump voltage (12 V).

Use a damping resistor $R_2$ (approximately 10 $\Omega$) in series with $C_1$. Equation 3 can be used to compute required $C_1$ value for a target inrush current. A 100-k$\Omega$ resistor for $R_1$ can be a good starting point for calculations.

Connecting PD pin of TPS1211x-Q1 directly to the gate of the external FET ensures fast turn-OFF without any impact of $R_1$ and $C_1$ components.

$C_1$ results in an additional loading on $C_{\text{BST}}$ to charge during turn-ON. Use Equation 4 to calculate the required $C_{\text{BST}}$ value.

$$C_{\text{BST}} > Q_{g(\text{total})} + 10 \times C_1$$

(4)

Where, $Q_{g(\text{total})}$ is the total gate charge of the FET.
8.3.2.2 Using Precharge FET - (with TPS12111-Q1 Only)

In high-current applications where several FETs are connected in parallel, the gate slew rate control for the main FETs is not recommended due to unequal distribution of inrush currents among the FETs. This action makes FET selection complex and results in over sizing of the FETs.

The TPS12111-Q1 integrates precharge gate driver (G) with a dedicated control input (INP_G). This feature can be used to drive a separate FET that can be used to precharge the capacitive load. Figure 8-6 shows the precharge FET implementation for capacitive load charging using TPS12111-Q1. An external capacitor \( C_g \) reduces the gate turn-ON slew rate and controls the inrush current.

Figure 8-6. Capacitor Charging Using Gate Slew Rate Control of Precharge FET

During power up with EN/UVLO high and \( C_{BST} \) voltage above \( V_{BST_{UVLO}} \) threshold, INP and INP_G controls are active. For the precharge functionality, drive INP low to keep the main FETs OFF and drive INP_G high. G output gets pulled up to BST with \( I_G \). Use Equation 5 to calculate the required \( C_g \) value.

\[
I_G = C_g \times \frac{I_{INRUSH}}{C_{OUT}}
\]

Where,

\( I_G \) is 100 µA (typical),

Use Equation 2 to calculate the \( I_{INRUSH} \).

A series resistor \( R_g \) must be used in conjunction with \( C_g \) to limit the discharge current from \( C_g \) during turn-off. The recommended value for \( R_g \) is between 220 Ω to 470 Ω. After the output capacitor is charged, turn OFF the precharge FET by driving INP_G low. G gets pulled low to SRC with an internal 135-mA pulldown switch. The main FETs can be turned ON by driving INP high.

Figure 8-7 shows other system design approaches to charge large output capacitors in high current applications. The designs involve an additional power resistor in series in series with precharge FET. The back-to-back FET topology shown is typically used in bi-directional power control applications like battery management systems.
8.3.3 Overcurrent and Short-Circuit Protection

TPS1211x-Q1 has two-level current protection.
- Adjustable overcurrent protection ($I_{OC}$) threshold and response time ($T_{OC}$).
- Adjustable short-circuit threshold ($I_{SC}$) with internally fixed fast response ($T_{SC}$).

Figure 8-8 shows the I-T characteristics.

![Figure 8-8. Overcurrent and Short-Circuit Protection Characteristics](image)

The device senses the voltage across the external current sense resistor through CS+ and CS-. Set the overcurrent protection threshold using an external resistor $R_{IWRN}$ across IWRN and GND. Use Equation 6 to calculate the required $R_{IWRN}$ value.

$$R_{IWRN} (\Omega) = \frac{11.9 \times R_{SET} \times R_{SNS} \times I_{OC}}{R_{SNS} \times I_{OC}}$$

Where, $R_{SET}$ is the resistor connected across CS+ and VS, $R_{SNS}$ is the current sense resistor, and $I_{OC}$ is the overcurrent level.
8.3.3.1 Overcurrent Protection with Auto-Retry

The C_{TMR} programs the over current protection delay (T_{OC}) and auto-retry time (T_{RETRY}). Once the voltage across CS+ and CS– exceeds the set point, the C_{TMR} starts charging with 77-µA pullup current. After the C_{TMR} charges up to V_{TMR_FLT}, FLT_I asserts low providing warning on impending FET turn OFF. After C_{TMR} charges to V_{TMR_OC}, PD pulls low to SRC turning OFF the FET. Post this event, the auto-retry behavior starts. The C_{TMR} capacitor starts discharging with 2.5-uA pulldown current. After the voltage reaches V_{TMR_Low} level, the capacitor starts charging with 2.5-uA pullup. After 32 charging, discharging cycles of C_{TMR} the FET turns ON back and FLT_I de-asserts after de-assertion delay of 260 µs.

Use Equation 7 to calculate the T_{OC} duration.

\[ T_{OC} = \frac{1.2 \times C_{TMR}}{77.5 \mu} \]

Where, T_{OC} is the delay to turn OFF the FET, C_{TMR} is the capacitance across TMR to GND.

Use Equation 8 to calculate the T_{FLT} duration.

\[ T_{FLT} = \frac{1.1 \times C_{TMR}}{77.5 \mu} \]

Where, T_{FLT} is the FLT_I assertion delay.

The auto-retry time can be computed as, T_{RETRY} = 22.7 \times 10^6 \times C_{TMR}.

If the overcurrent pulse duration is below T_{OC}, then the FET remains ON and C_{TMR} gets discharged using internal pulldown switch.

![Figure 8-9. Overcurrent Protection with Auto-Retry](image)

8.3.3.2 Overcurrent Protection with Latch-Off

Connect an approximately 100-kΩ resistor across C_{TMR} as shown in the following figure. With this resistor, during the charging cycle, the voltage across C_{TMR} gets clamped to a level below V_{TMR_OC} resulting in a latch-off behavior.
Toggle INP or EN/UVLO (below ENF) or power cycle Vs below \( V_{SPORF} \) to reset the latch. At low edge, the timer counter is reset and \( C_{(TMR)} \) is discharged. PU pulls up to BST when INP is pulled high.

![Diagram](https://www.ti.com/lit/an/slua418b/slua418b.pdf)

**Figure 8-10. Overcurrent Protection with Latch-Off**

### 8.3.3.3 Short-Circuit Protection

Connect a resistor, \( R_{ISCP} \), as shown in Figure 8-11.

Use Equation 9 to calculate the required \( R_{ISCP} \) value.

\[
R_{ISCP} (\Omega) = \frac{I_{SC} \times R_{SNS}}{14.5 \mu A} - 600
\]

(9)

Where, \( R_{SNS} \) is the current sense resistor, and \( I_{SC} \) is the desired short-circuit protection level. After the current exceeds the \( I_{SC} \) threshold then, PD pulls low to SRC within 1.2 \( \mu s \) in TPS12111-Q1 and 5 \( \mu s \) in TPS12110-Q1, protecting the FET. FLT\( I_{L} \) asserts low at the same time. Subsequent to this event, the charge and discharge cycles of \( C_{(TMR)} \) starts similar to the behavior post FET OFF event in the over current protection scheme.

Latch-off can also achieved in the similar way as explained in the overcurrent protection scheme.

### 8.3.4 Analog Current Monitor Output (IMON)

TPS1211x-Q1 features an accurate analog load current monitor output (IMON) with adjustable gain. The current source at IMON terminal is configured to be proportional to the current flowing through the \( R_{SNS} \) current sense resistor. This current can be converted to a voltage using a resistor \( R_{IMON} \) from IMON terminal to GND terminal. This voltage, computed using Equation 10 can be used as a means of monitoring current flow through the system.

Use Equation 10 to calculate the \( V_{IMON} \).

\[
V_{IMON} = (V_{SNS} + V_{OS\_SET}) \times \text{Gain}
\]

(10)

Where \( V_{SNS} = I_{LOAD} \times R_{SNS} \) and \( V_{OS\_SET} \) is the input referred offset (± 350 \( \mu V \)) of the current sense amplifier (\( V_{SNS} \) to \( V_{IMON} \) scaling). Use the following equation to calculate gain.
Gain = \frac{0.9 \times R_{IMON}}{R_{SET}} \tag{11}

Where 0.9 is the current mirror factor between the current sense amplifier and the IMON pass FET.

The maximum voltage range for monitoring the current (V(IMONmax)) is limited to minimum([V(VS) – 0.5V], 5.5V) to ensure linear output. This puts limitation on maximum value of R_{IMON} resistor. The IMON pin has an internal clamp of 6.5 V (typical).

Accuracy of the current mirror factor is < ± 1%. Use the following equation to calculate the overall accuracy of V_{IMON}:

\% V_{IMON} = \frac{V_{OS\_SET}}{V_{SNS}} \times 100 \tag{12}

Figure 8-11 shows external connections and simplified block diagram of current sensing and overcurrent protection implementation.
8.3.5 Overvoltage (OV) and Undervoltage Protection (UVLO)

![Diagram of Overvoltage and Undervoltage Protection Threshold]

Figure 8-12. Programming Overvoltage and Undervoltage Protection Threshold

8.3.6 Remote Temperature Sensing and Protection (DIODE)

The device features an integrated remote temperature sensing, protection and dedicated fault output. With a companion BJT, MMBT3904 as a remote temperature sense element, the controller gets the temperature information of the sense point. Connect the DIODE pin of TPS1211-Q1 to the collector, base of a MMBT3904 BJT. After the sensed temperature reaches approximately 155°C, the device pulls PD low to SRC, turning off the external FET and also asserts FLT_T low. After the temperature reduces to 125°C (minimum), an internally fixed auto-retry cycle of 512 ms commences. FLT_T de-asserts and the external FET turns ON after the re-try duration of 512 ms is lapsed.

In TPS12111-Q1, after the sensed temperature crosses 155°C, PD and G get pulled low to SRC. After the TSD hysteresis, PU and G stays latched OFF. The latch gets reset by toggling EN/UVLO below V(ENF) or by power cycling Vs below VSPORF.

8.3.7 TPS1211x-Q1 as a Simple Gate Driver

Figure 8-13 shows application schematics of TPS1211x-Q1 as a simple gate driver in load disconnect switch as well as back-to-back FETs driving topologies. The protection features like two-level overcurrent protection, overvoltage protection, and overtemperature protection are disabled.

![Diagram of Simple Gate Driver Design]

Figure 8-13. Connection Diagram of TPS12110-Q1 for Simple Gate Driver Design
8.4 Device Functional Modes

The TPS1211-Q1 has two modes of operation. Active mode and low IQ shutdown mode. If the EN/UVLO pin voltage is greater than the rising threshold, then the device is in active mode. In active state the internal charge pump is enabled, gate drivers and all the protection and diagnostic features are enabled. If the EN/UVLO voltage is pulled < 0.3 V, the device enters into low IQ shutdown mode. In this mode, the charge pump, gate drivers and all the protection features are disabled. The external FETs turn OFF. The TPS1211-Q1 consumes low IQ of 1.7 µA (typical) in this mode.
9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS1211x-Q1 family is a 45-V smart high-side driver with protection and diagnostics. The TPS1211x-Q1 device controls external N-channel MOSFETs and its drive architecture is suitable to drive back-to-back N-Channel MOSFETs. The strong gate 4-A source and sink capabilities enable switching parallel MOSFETs in high current applications such as circuit breaker in powertrain (DC/DC converter), driving loads in power distribution unit, electric power steering, driving PTC heater loads, and so forth. The TPS1211x-Q1 device provides two-level, adjustable, overcurrent protection with adjustable circuit breaker timer, fast short-circuit protection, accurate analog current monitor output, and remote overtemperature protection.

The variant TPS12111-Q1 features a separate precharge driver (G) with independent control input (INP_G). This feature enables system designs that must precharge the large output capacitance before turning ON the main power path.

The following design procedure can be used to select the supporting component values based on the application requirement.

9.2 Typical Application: Driving Zonal Controller Loads on 12-V Line in Power Distribution Unit

Figure 9-1. Typical Application Schematic: Driving Zonal Controller Loads with Precharging the Output Capacitance
9.2.1 Design Requirements

Table 9-1 shows the design parameters for this application example.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical input voltage, $V_{IN}$</td>
<td>12 V</td>
</tr>
<tr>
<td>Undervoltage lockout set point, $V_{IN_{UVLO}}$</td>
<td>6.5 V</td>
</tr>
<tr>
<td>Maximum load current, $I_{OUT}$</td>
<td>25 A</td>
</tr>
<tr>
<td>Overcurrent protection threshold, $I_{OC}$</td>
<td>30 A</td>
</tr>
<tr>
<td>Short-circuit protection threshold, $I_{SC}$</td>
<td>35 A</td>
</tr>
<tr>
<td>Fault timer period ($T_{OC}$)</td>
<td>1 ms</td>
</tr>
<tr>
<td>Fault response</td>
<td>Auto-retry</td>
</tr>
<tr>
<td>Load capacitance, $C_{OUT}$</td>
<td>1 mF</td>
</tr>
<tr>
<td>Charging time, $T_{start}$</td>
<td>10 ms</td>
</tr>
</tbody>
</table>

9.2.2 Detailed Design Procedure

Selection of Current Sense Resistor, $R_{SNS}$

The recommended range of the overcurrent protection threshold voltage, $V_{(SNS\_WRN)}$, extends from 10 mV to 30 mV. Values near the low threshold of 10 mV can be affected by the system noise. Values near the upper threshold of 30 mV can cause high power dissipation in the current sense resistor. To minimize both the concerns, 25 mV is selected as the overcurrent protection threshold voltage. Use the following equation to calculate the current sense resistor, $R_{SNS}$.

$$
R_{SNS} = \frac{V_{(SNS-WRN)}}{I_{WRN}} = \frac{25 \text{ mV}}{30 \text{ A}} = 833 \mu\Omega
$$

(13)

The next smaller available sense resistor 800 µΩ, 1% is chosen.

To improve signal to noise ratio or for better overcurrent protection accuracy, higher overcurrent protection threshold voltage, $V_{(SNS\_WRN)}$ can be selected. The maximum allowed $V_{(SNS\_WRN)}$ voltage is 250 mV.

Selection of Scaling Resistor, $R_{SET}$

$R_{SET}$ is the resistor connected between $V_S$ and $CS+$ pins. This resistor scales the overcurrent protection threshold voltage and coordinates with $R_{IWRN}$ and $R_{IMON}$ to determine the overcurrent protection threshold and current monitoring output. The recommended range of $R_{SET}$ is 50 Ω – 100 Ω.

$R_{SET}$ is selected as 100 Ω, 1% for this design example.

Programming the Overcurrent Protection Threshold – $R_{IWRN}$ Selection

The $R_{IWRN}$ sets the overcurrent protection threshold, whose value can be calculated using Equation 14.

$$
R_{IWRN} (\Omega) = \frac{11.9 \times R_{SET}}{R_{SNS} \times I_{OC}}
$$

(14)

To set 30 A as overcurrent protection threshold, $R_{IWRN}$ value is calculated to be 49.5 kΩ.

Choose the closest available standard value: 49.9 kΩ, 1%
**Programming the Short-Circuit Protection Threshold – $R_{\text{ISC}}$ Selection**

The $R_{\text{ISC}}$ sets the short-circuit protection threshold. Use the following equation to calculate the value.

$$R_{\text{ISC}} \ (\Omega) = \frac{I_{\text{SC}} \times R_{\text{SNS}}}{14.5 \ \mu A} - 600$$

(15)

To set 35 A as overcurrent protection threshold, $R_{\text{ISC}}$ value is calculated to be 1.33 kΩ.

Choose the closest available standard value: 1.43 kΩ, 1%.

In case where large di/dt is involved, the system and layout parasitic inductances can generate large differential signal voltages between $I_{\text{SCP}}$ and CS– pins. This action can trigger false short-circuit protection and nuisance trips in the system. To overcome such scenario, TI recommends to add filter capacitor of 1 nF across $I_{\text{SCP}}$ and CS– pins close to the device. Because nuisance trips are dependent on the system and layout parasitics, TI recommends to test the design in a real system and tweaked as necessary.

**Programming the Fault timer Period – $C_{\text{TMR}}$ Selection**

For the design example under discussion, overcurrent transients are allowed for 1-ms duration. This blanking interval, $T_{\text{OC}}$ can be set by selecting appropriate capacitor $C_{\text{TMR}}$ from TMR pin to ground. Use the following equation to calculate the value of $C_{\text{TMR}}$ to set 1 ms for $T_{\text{OC}}$.

$$C_{\text{TMR}} = \frac{T_{\text{OC}} \times 77.5 \ \mu A}{1.2} = 64.58 \ \text{nF}$$

(16)

Choose closest available standard value: 68 nF, 10%.

**Selection of MOSFETs, $Q_1$ and $Q_2$**

For selecting the MOSFET $Q_1$, important electrical parameters are the maximum continuous drain current $I_D$, the maximum drain-to-source voltage $V_{\text{DS(MAX)}}$, the maximum drain-to-source voltage $V_{\text{GS(MAX)}}$, and the drain-to-source ON-resistance $R_{\text{DS(ON)}}$.

The maximum continuous drain current, $I_D$, rating must exceed the maximum continuous load current.

The maximum drain-to-source voltage, $V_{\text{DS(MAX)}}$, must be high enough to withstand the highest voltage seen in the application. Considering 35 V as the maximum application voltage, MOSFETs with $V_{\text{DS}}$ voltage rating of 40 V is suitable for this application.

The maximum $V_{\text{GS}}$ TPS1211-Q1 can drive is 13 V, so a MOSFET with 15-V minimum $V_{\text{GS}}$ rating must be selected.

To reduce the MOSFET conduction losses, lowest possible $R_{\text{DS(ON)}}$ is preferred.

Based on the design requirements, BUK7S0R5-40HJ is selected and its ratings are:

- 40-V $V_{\text{DS(MAX)}}$ and 20-V $V_{\text{GS(MAX)}}$
- $R_{\text{DS(ON)}}$ is 0.47-mΩ typical at 10-V $V_{\text{GS}}$
- MOSFET $Q_{g(total)}$ is 190 nC

**Selection of Bootstrap Capacitor, $C_{\text{BST}}$**

The internal charge pump charges the external bootstrap capacitor (connected between BST and SRC pins) with approximately 100 µA. Use the following equation to calculate the minimum required value of the bootstrap capacitor for driving two parallel BUK7S0R5-40HJ MOSFETs.

$$C_{\text{BST}} = \frac{Q_{g(total)}}{1 \ \text{V}} = 380 \ \text{nF}$$

(17)
Choose closest available standard value: 470 nF, 10%.

**Setting the Undervoltage Lockout**

The undervoltage lockout (UVLO) can be adjusted using an external voltage divider network of $R_1$ and $R_2$ connected between VS, EN/UVLO and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated by solving Equation 18.

$$V_{(UVLO)} = \frac{R_2}{(R_1 + R_2)} \times V_{IN_{UVLO}}$$

Equation 18

For minimizing the input current drawn from the power supply, TI recommends to use higher values of resistance for $R_1$ and $R_2$. However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, $I(R_{12})$ must be chosen to be 20 times greater than the leakage current of UVLO pin.

From the device electrical specifications, $V_{(UVLO)} = 1.18$ V. From the design requirements, $V_{IN_{UVLO}}$ is 6.5 V. To solve the equation, first choose the value of $R_1 = 470$ kΩ and use Equation 18 to solve for $R_2 = 104.24$ kΩ. Choose the closest standard 1% resistor values: $R_1 = 470$ kΩ, and $R_2 = 105$ kΩ.

**Selection of Precharge Path Components, $C_g$ and $R_g$**

For charging the large capacitors on output, the output slew rate can be controlled by using a capacitor on the gate (G) of the precharge FET Q3. The target inrush current to charge 1 mF of output capacitance to 12-V in 10 ms can be estimated by Equation 19. The required gate capacitance $C_g$ to limit the inrush current to 1.2 A can be calculated by using Equation 16, where $I_g = 100$ μA (typical) is the gate charging current of pin ‘G’. By solving Equation 20, we get $C_g$ as 83.33 nF.

Choose the closest available standard value: 82 nF, 10%.

$$I_{INRUSH} = C_{OUT} \times \frac{V_{IN}}{T_{start}} = 1.2$ A

Equation 19

$$I_g = C_g \times \frac{I_{INRUSH}}{C_{OUT}}$$

Equation 20

A series resistor $R_g$ must be used in conjunction with $C_g$ to limit the discharge current from $C_g$ during turn-off and to stabilize the gate ‘G’ during slew rate control. The recommended value for $R_g$ is between 220 Ω to 470 Ω.

**Choosing the Current Monitoring Resistor, $R_{IMON}$**

Voltage at IMON pin $V_{IMON}$ is proportional to the output load current. This can be connected to an ADC of the downstream system for monitoring the operating condition and health of the system. The $R_{IMON}$ must be selected based on the maximum load current and the input voltage range of the ADC used. $R_{IMON}$ is set using Equation 21.

$$V_{IMON} = (V_{SNS} + V_{OS\_SET}) \times \frac{0.9 \times R_{IMON}}{R_{SET}}$$

Equation 21

Where $V_{SNS} = I_{WRN} \times R_{SNS}$ and $V_{OS\_SET}$ is the input referred offset ($\pm 350$ μV) of the current sense amplifier.

The maximum voltage range for monitoring the current ($V(\text{IMONmax})$) is limited to minimum($V(VS) - 0.5V$, 5.5V) to ensure linear output. This puts a limitation on the maximum value of $R_{IMON}$ resistor. The IMON pin has an internal clamp of 6.5 V (typical).
For \( I_{WRN} = 30 \text{ A} \) and considering the operating range of ADC to be 0 V to 3.3 V (for example, \( V_{IMON} = 3.3 \text{ V} \)), \( R_{IMON} \) can be calculated as

\[
R_{IMON} = \frac{V_{IMON} \times R_{SET}}{(V_{SNS} + V_{OS\_SET}) \times 0.9} = 16.52 \text{ k}\Omega
\]  

(22)

Selecting \( R_{IMON} \) value less than shown in Equation 22 ensures that ADC limits are not exceeded for maximum value of load current. Choose the closest available standard value: 16.5 k\( \Omega \), 1\%. 

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TPS1211-Q1
SLUSEQ9 – JULY 2022

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Product Folder Links: TPS1211-Q1
9.2.3 Application Curves

Figure 9-2. Start-Up Profile of Bootstrap Voltage for INP = GND

Figure 9-3. Start-Up Profile of Bootstrap Voltage for INP = HIGH

Figure 9-4. Turn-ON Response of TPS12111-Q1 for INP -> LOW to HIGH

Figure 9-5. Turn-OFF Response of TPS12111-Q1 for INP -> HIGH to LOW

Figure 9-6. IMON Response During 12-A Load Step

Figure 9-7. Overcurrent Response of TPS12111-Q1 for a Load Step from 20 A to 32 A with 30-A Overcurrent Protection Setting
Figure 9-8. Auto-Retry Response of TPS12111-Q1 for an Overcurrent Fault

Figure 9-9. Latch-Off Response of TPS12111-Q1 for an Overcurrent Fault

Figure 9-10. Response During Coming out of Overload Fault with INP Reset

Figure 9-11. Precharge Profile of the Output Capacitance (VIN = 12 V, C_{OUT} = 1 mF, No Load)

Figure 9-12. Output Hot-Short Response of the TPS12111-Q1 Device
9.3 Typical Application: Reverse Polarity Protection with TPS12110-Q1

For applications such as powering electronic power steering (EPS) system, the input must be protected from any possible reverse polarity scenarios. The TPS12110-Q1 configured as shown in Figure 9-13 meets the system requirements. The back-to-back FET (Q₁ and Q₂) configuration blocks reverse current flow and provides protection for the load against static input reverse polarity event. The N-MOSFET (Q₄) in the ground path protects the TPS12110-Q1 controller, and Zener diode D₁ is added for VGS protection of Q₄.

### 9.3.1 Design Requirements

Table 9-2 shows the design parameters for this application example.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical input voltage, Vᵢᵣᵣ</td>
<td>12 V</td>
</tr>
<tr>
<td>Undervoltage lockout set point, VINUVLO</td>
<td>6.5 V</td>
</tr>
<tr>
<td>OV set point, VINOVP</td>
<td>36 V</td>
</tr>
<tr>
<td>Maximum load current, Iᵪᵦ</td>
<td>20 A</td>
</tr>
<tr>
<td>Overcurrent protection threshold, Iᵪᵦ</td>
<td>24 A</td>
</tr>
<tr>
<td>Short-circuit protection threshold, Iᵦᵦ</td>
<td>30 A</td>
</tr>
<tr>
<td>Fault timer period (Tᵦᵦ)</td>
<td>1 ms</td>
</tr>
<tr>
<td>Fault response</td>
<td>Auto-retry</td>
</tr>
<tr>
<td>Input reverse polarity protection</td>
<td>Yes</td>
</tr>
</tbody>
</table>
9.3.2 External Component Selection

By following similar design procedure as outlined in Detailed Design Procedure, the external component values are calculated as below:

- \( R_{SNS} = 1 \text{ m}\Omega \).
- \( R_{SET} = 100 \Omega \).
- \( R_{IWRN} = 49.9 \text{ k}\Omega \) to set 24 A as overcurrent protection threshold.
- \( R_{ISC} = 1.468 \text{ k}\Omega \) to set 30 A as short-circuit protection threshold.
- \( C_{TMR} = 68 \text{ nF} \) to set 1-ms over current protection time.
- \( R_1, R_2, R_3 \) are selected as 390 k\Ω, 71.5 k\Ω and 15.8 k\Ω respectively to set VIN undervoltage lockout threshold at 6.5 V and overvoltage cutoff threshold at 36 V.
- \( R_{IMON} = 15 \text{ k}\Omega \) to limit maximum \( V_{(IMON)} \) voltage to 3.3 V at full-load current of 24 A.
- To reduce conduction losses, BUK7S0R5-40HJ MOSFET is selected. Two FETs are used in back-to-back configuration for reverse current blocking.
  - 40-V \( V_{DS(\text{MAX})} \) and 20-V \( V_{GS(\text{MAX})} \).
  - \( R_{DS(\text{ON})} \) is 0.47-m\Ω typical at 10-V \( V_{GS} \).
  - \( Q_g \) of each MOSFET is 190 nC.
- \( C_{BST} = (2 \times Q_g) / 1 \text{ V} = 380 \text{ nF} \); Choose the closest available standard value: 470 nF, 10%.
- \( Q_4 \) selection: Any signal N-MOSFET with 40-V \( V_{DS} \) support is sufficient. DMN601WKQ-7 is selected for the current design and a 12-V Zener diode SZMM3Z12VST1G is used for \( V_{GS} \) protection.

9.3.3 Application Curves

![Figure 9-14. Overvoltage Cutoff Response of TPS12110-Q1 at 36-V Level](image)

![Figure 9-15. Input Reverse Polarity Protection with TPS12110-Q1](image)

9.4 Power Supply Recommendations

When the external MOSFETs turn OFF during the conditions such as INP control, overvoltage cutoff, overcurrent protection causing an interruption of the current flow, the input parasitic line inductance generates a positive voltage spike on the input and output parasitic inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the Absolute Maximum Ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Use of a TVS diode and input capacitor filter combination across input to and GND to absorb the energy and dampen the positive transients.
- Use of a diode or a TVS diode across the output and GND to absorb negative spikes.

The TPS1211-Q1 gets powered from the Vs pin. Voltage at this pin must be maintained above \( V_{(S\_\text{POR})} \) level to ensure proper operation. If the input power supply source is noisy with transients, then TI recommends to place
a R\textsubscript{VS}-C\textsubscript{VS} filter between the input supply line and Vs pin to filter out the supply noise. TI recommends R\textsubscript{VS} value around 100 Ω.

The following figure shows the circuit implementation with optional protection components.

![Circuit Implementation with Optional Protection Components for TPS1211-Q1](image)

**Figure 9-16. Circuit Implementation with Optional Protection Components for TPS1211-Q1**

9.5 Layout

9.5.1 Layout Guidelines

- The sense resistor (R\textsubscript{SNS}) must be placed close to the TPS1211x-Q1 and then connect R\textsubscript{SNS} using the Kelvin techniques. Refer to *Choosing the Right Sense Resistor Layout* for more information on the Kelvin techniques.
- For all the applications, TI recommends a 0.1 µF or higher value ceramic decoupling capacitor between VS terminal and GND. Consider adding RC network at the supply pin (VS) of the controller to improve decoupling against the power line disturbances.
- The high-current path from the board input to the load, and the return path, must be parallel and close to each other to minimize loop inductance.
- The external MOSFETs must be placed close to the controller such that the GATE of the MOSFETs are close to PU/PD pins to form short GATE loop. Consider adding a place holder for a resistor in series with the Gate of each external MOSFET to damp high frequency oscillations if need arises.
- Place a TVS diode at the input to clamp the voltage transients during hot-plug and fast turn-off events.
- The external boot-strap capacitor must be placed close to BST and SRC pins to form very short loop.
- The ground connections for the various components around the TPS1211x-Q1 must be connected directly to each other, and to the TPS1211x-Q1 GND, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.
- The DIODE pin sources current to measure the temperature. TI recommends BJT MMBT3904 to use as a remote temperature sense element. Take care in the PCB layout to keep the parasitic resistance between the DIODE pin and the MMBT3904 low so as not to degrade the measurement. In addition, TI recommends to make a Kelvin connection from the emitter of the MMBT3904 to the GND of the part to ensure an accurate measurement. Additionally, a small 1000=pF bypass capacitor must be placed in parallel with the MMBT3904 to reduce the effects of noise.
9.5.2 Layout Example

Figure 9-17. Typical PCB Layout Example for TPS12110-Q1 with B2B MOSFETs
10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on Subscribe to updates to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
11.1 Tape and Reel Information

**REEL DIMENSIONS**

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

**TAPE DIMENSIONS**

- Q1, Q2, Q3, Q4: Pocket Quadrants
- Sprocket Holes
- User Direction of Feed

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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<td>VSSOP</td>
<td>DGX</td>
<td>19</td>
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<td>330</td>
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<td>12</td>
<td>Q1</td>
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<tr>
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<td>Q1</td>
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</table>
## TAPE AND REEL BOX DIMENSIONS

<table>
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<th>Device</th>
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<th>Width (mm)</th>
<th>Height (mm)</th>
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<tbody>
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<tr>
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<td>19</td>
<td>5000</td>
<td>853.0</td>
<td>449.0</td>
<td>35</td>
</tr>
</tbody>
</table>
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
5. Features may differ or may not be present.
EXAMPLE BOARD LAYOUT

DGX0019A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).

9. Size of metal pad may vary due to creepage requirement.

10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.
12. Board assembly site may have different recommendations for stencil design.
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