TPS16890 9V–80V, 3.65mΩ, 20A Stackable Integrated Hotswap (eFuse) With PMBus® Digital Telemetry

1 Features

- Input operating voltage range: 9V to 80V
  - 92V absolute maximum rating
  - Withstands negative transient voltages up to –5V at output
- Integrated FET with low ON-resistance
  - R_{ON} = 3.65mΩ (typ)
- PMBus interface for telemetry, control, configuration, and debug
  - PIN/EIN/VIN/VOUT/IIN temperature and fault monitoring
  - VIN/VOUT monitoring accuracy: ±0.5%
  - Programmable overcurrent protection
    - Adjustable overcurrent threshold: 2A to 20A
    - Programmable transient overcurrent timer (OC_TIMER)
  - Programmable slew rate control (dvdt)
  - Programmable Power Good/fault/alert indication
  - Programmable overtemperature protection
  - Non-volatile configuration memory for configuration values
  - Blackbox fault recording with option to store in external EEPROM
- Fast trip response to severe overcurrent (short-circuit) events
- Precise analog load current monitoring (IMON)
  - <3% error over 50%–100% of max current
- Small footprint: QFN 6mm × 5mm
  - IPC9592B clearance for 60V

2 Applications

- Server and high performance computing
- Network interface cards
- Graphics and hardware accelerator cards
- Datacenter switches and routers
- Input hotswap and hotplug
- Fan trays

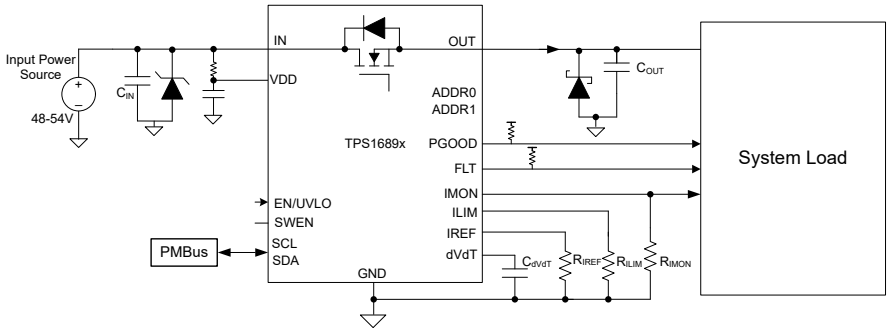
3 Description

The TPS1689x is an integrated high current circuit protection and power management solution in a small package. The device provides multiple protection modes using very few external components and is a robust defense against overloads, short circuits and excessive inrush current. The integrated PMBus™ interface allows a host controller to monitor, control and configure the system in real-time. Key system parameters can be read back for remote telemetry. Various protection/warning thresholds and coefficients can be configured through PMBus or stored in non-volatile configuration memory. An integrated fast and accurate sense analog load current monitor facilitates predictive maintenance and advanced dynamic platform power management such as Intel® PSYS and PROCHOT to optimize server and data-center performance. Blackbox fault recording feature helps in debug of field failure/returns. For higher current support, TPS1689x can be connected in parallel with TPS1685x. The devices are characterized for operation over a junction temperature range of –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS16890	VMA (LQFN, 23)	5mm × 6mm

(1) For all available packages, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Pin Configuration and Functions

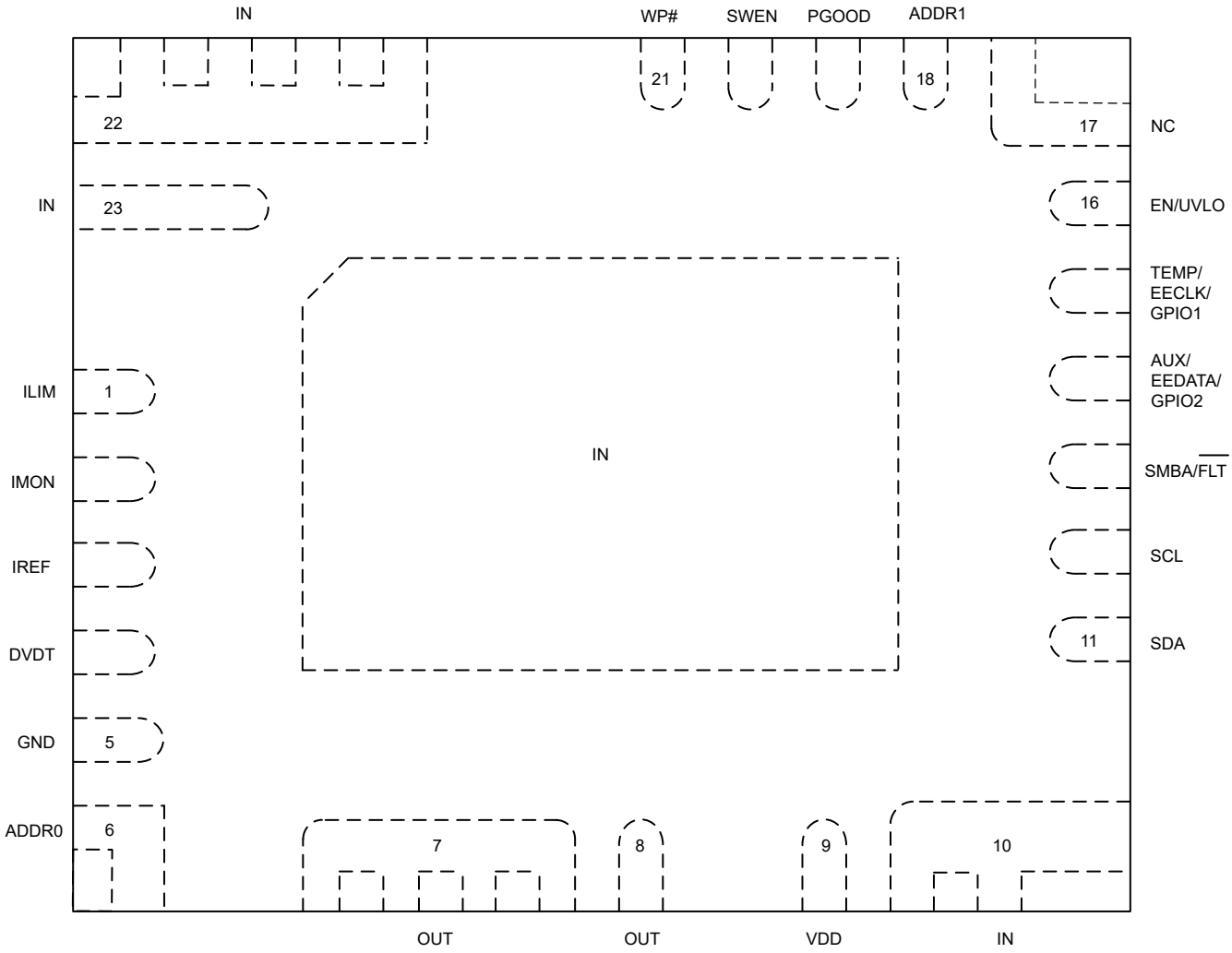

Figure 4-1. TPS16890 VMA Package 23-pin LQFN Top View

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
ILIM	1	O	An external resistor from this pin to GND sets the active current sharing threshold during steady-state. This pin also serves as individual eFuse current monitor output during steady state. **Do not leave floating.**
IMON	2	O	An external resistor from this pin to GND sets the overcurrent/circuit-breaker threshold and fast trip threshold during steady state. This pin also acts as a fast and accurate analog output load current monitor signal during state. **Do not leave floating.**
IREF	3	O	Programmable reference voltage for overcurrent protection block, generated using internal DAC. Can be used to drive reference votlage for other secondary devices in primary/secondary parallel configurations.
DVDT	4	O	Startup Output Slew Rate control pin. Leave it open to allow fastest startup. Connect capacitor to ground to slow down the slew rate to manage inrush current.
GND	5	G	Device Ground reference pin. Connect to System Ground.

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Table 4-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
ADDR0	6	I	I²C Address Configuration Pin. Pin strap to open/short to ground or resistor to ground to generate different address combinations.
OUT	7, 8	P	Power output. Must be soldered to the output power plane uniformly for proper heat dissipation
VDD	9	P	Controller power input pin. Can be used to power the internal control circuitry with a filtered and stable supply which is not affected by system transients. Connect this pin to VIN through a series resistor and add a decoupling capacitor to GND.
IN	10, 22, 23, Exposed Pad	P	Power Input. Must be soldered to input power plane uniformly to ensure proper heat dissipation and to maintain optimal current distribution through the device.
SDA	11	I/O	I²C Data Line for PMBus interface. Needs external Pull-up resistor.
SCL	12	I	I²C Clock Line for PMBus interface. Needs external Pull-up resistor.
SMBA/$\overline{\text{FLT}}$	13	O	FAULTB output. Or SMBus Alert Output. Needs external Pull-up resistor.
AUX/EEDATA/ GPIO2	14	I/O	Auxiliary input for ADC or External EEPROM Data IO or General-Purpose Digital IO
TEMP/EECLK/ GPIO1	15	I/O	Analog temperature output. Can be tied together with TEMP outputs of multiple devices in a parallel configuration to get the peak temperature of the chain. Or External EEPROM Clock output or General-Purpose Digital IO.
EN/UVLO	16	I	Active High Enable input. Connect resistor divider from input supply to set the Undervoltage threshold. **Do not leave floating.**
NC	17	-	No internal Connection.
ADDR1	18	I	I²C Address Configuration Pin. Pin strap to open/short to ground or resistor to ground to generate different address combinations.
PGOOD	19	O	Open-drain active high power good output. This pin has weak internal pull-up to internal supply voltage.
SWEN	20	I/O	Open drain signal to indicate and control power switch ON/OFF status. This facilitates synchronization of multiple devices in a parallel chain. This pin has internal Pull-up.
WP#	21	I	Write Protect: Connect this pin to GND to disable PMBus write access to the device completely. When this pin is floating, PMBuswrite access is controlled by the MFR_WRITE_PROTECT command.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		Pin	MIN	MAX	UNIT
V_{INMAX}, V_{DDMAX}	Maximum Input and Supply Voltage (-40℃ ≤ T_J ≤ 125℃)	IN, VDD	–0.3	90	V
$V_{INMAX,25}$, $V_{DDMAX,25}$	Maximum Input and Supply Voltage (25℃ ≤ T_J ≤ 125℃)	IN, VDD	–0.3	92	V
V_{OUTMAX}	Maximum Output Voltage	OUT	–5(2)	Min(92 V, VIN + 0.3)	
V_{IN} - V_{OUT}	Maximum difference between IN and OUT	IN, OUT	-0.3	90	V
$V_{ILIMMAX}$	Maximum ILIM Pin Voltage	ILIM	–0.3	Internally Limited	V
$V_{IMONMAX}$	Maximum IMON Pin Voltage	IMON	–0.3	Internally Limited	V
$V_{ADDRMAX}$	Maximum ADDR1, ADDR0 Pin Voltage	ADDR1, ADDR0	–0.3	Internally Limited	V
V_{I2CMAX}	Maximum SCL, SDA Pin Voltage	SCL, SDA	–0.3	6	V
$V_{IREFMAX}$	Maximum IREF Pin Voltage	IREF	–0.3	6	V
$V_{DVDTMAX}$	Maximum DVDT Pin Voltage	DVDT	–0.3	6	V
V_{AUXMAX}	Maximum AUX/EEDATA/GPIO2 Pin Voltage	AUX/EEDATA/ GPIO2	–0.3	6	V
$V_{SWENMAX}$	Maximum SWEN Pin Voltage	SWEN	–0.3	6	V
$I_{SWENMAX}$	Maximum SWEN Pin Sink	SWEN		10	mA
V_{ENMAX}	Maximum EN/UVLO Pin Voltage	EN/UVLO	–0.3	6	V
$V_{FLTBMAX}$	Maximum SMBA/$\overline{FLT}$ Pin Voltage	SMBA/$\overline{FLT}$	–0.3	6	V
$I_{FLTBMAX}$	Maximum SMBA/$\overline{FLT}$ Pin Sink Current	SMBA/$\overline{FLT}$		10	mA
$V_{PGOODMAX}$	Maximum PGOOD Pin Voltage	PGOOD	–0.3	6	V
$I_{PGOODMAX}$	Maximum PGOOD Pin Sink Current	PGOOD		10	mA
$V_{TEMPMAX}$	Maximum TEMP/EECLK/GPIO1 Pin Voltage	TEMP/EECLK/ GPIO1	–0.3	6	V
I_{MAX}	Maximum Continuous Switch Current	IN to OUT	Internally Limited		A
T_{JMAX}	Junction temperature		Internally Limited		℃

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) During FET OFF condition for negative transients up-to 5µs.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1500	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Input Voltage Range	IN	9	80	V
V_{DD}	Supply Voltage Range	VDD	9	80	V
V_{OUT}	Output Voltage Range	OUT		V_{IN}	V

ADVANCE INFORMATION

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
$V_{EN/UVLO}$	Enable Pin Voltage Range	EN/UVLO		5	V
V_{dVdT}	dVdT Pin Cap Voltage Rating	dVdT	4		V
V_{PGOOD}	PGOOD Pin Pull-up Voltage Range	PG		5	V
V_{I2C}	I^2C Pull-up Voltage Range	SCL, SDA	1.8	5	V
C_{I2C}	I^2C bus capacitance	SCL, SDA		200	pF
$V_{TEMP/EECLK/GPIO1}$	TEMP/EECLK/GPIO1 Pin Voltage Range	TEMP/EECLK/ GPIO1		5	V
$V_{SMBA/FLTb}$	SMBA/$\overline{FLT}$ Pin Pull-up Voltage Range	SMBA/$\overline{FLT}$		5	V
V_{SWEN}	SWEN Pin Pull-up Voltage Range	SWEN		5	V
V_{AUX}	AUX Pin Voltage Rating	AUX		1.2	V
V_{IREF}	IREF Pin Voltage Range	IREF	0.3	1.2	V
V_{ILIM}	ILIM Pin Voltage Range	ILIM		0.4	V
V_{IMON}	IMON Pin Voltage Range	IMON		1.2	V
C_{IN}	Capacitance on IN pin	IN	10		nF
C_{OUT}	Capacitance on OUT pin	OUT	10		µF
$dV_{IN/dt}$	Slew rate on IN pin	IN		500	V/µs
I_{MAX}	Continuous Switch Current	IN to OUT		20	A
$I_{MAX, Pulse}$	Peak Output Current for ≤10 ms duration, T_A ≤ 70 °C	IN to OUT		27	A
T_J	Junction temperature		–40	125	°C

5.4 Thermal Information

THERMAL METRIC		TPS1689x LQFN PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.7	°C/W

5.5 Electrical Characteristics

–40°C ≤ T_J ≤ +125°C, VIN = V_{DD} = 45 V to 60 V, OUT = Open, R_{ILIM} = 931 Ω R_{IMON} = 2.55 kΩ, V_{IREF} = 1 V , $\overline{FLT}$ = 33 kΩ pull-up to 3.3 V, PGOOD = 33 kΩ pull-up to 3.3 V, C_{OUT} = 10 µF, C_{IN} = 10 nF, dVdT = Open , $V_{EN/UVLO}$ = 2 V, TEMP/EECLK/GPIO1 = Open, AUX/EEDATA/GPIO2 = Open, ADDR0 = Open, ADDR1 = Open, SCL = 330Ω pull-up to 3.3 V, SDA = 330Ω pull-up to 3.3 V. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (VDD)						
V_{IN}	Input voltage range		9		80	V
V_{DD}	Input voltage range		V_{IN}		80	V
$I_{QON(VDD)}$	V_{DD} ON state quiescent current	V_{DD} > V_{UVPR}, V_{EN} ≥ V_{UVLOR}, V_{OVP} < V_{OVPF}		4.5		mA
V_{UVPR}	V_{DD} Undervoltage Protection Threshold Rising	V_{DD} Rising		8.5		V
V_{UVPF}	V_{DD} Undervoltage Protection Threshold falling	V_{DD} Falling		7.05		V
V_{UVPHYS}	UVP Hysteresis VDD			1.45		V
INPUT SUPPLY (IN)						
$V_{UVLOR(VIN)}$	VIN undervoltage threshold rising	V_{IN} Rising, VIN_UV_FLT = 0x71		40.3		V
$V_{UVLOF(VIN)}$	VIN undervoltage threshold falling	V_{IN} Falling, VIN_UV_FLT = 0x71		38.7		V
$I_{QON(VIN)}$	V_{IN} ON state quiescent current	V_{EN} ≥ V_{UVLOR}		1.38		mA

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{QOFF(VIN)}$	V_{IN} OFF state current	V_{SDR} < V_{EN} < V_{UVLO}		1.83		mA
$I_{SD(VIN)}$	V_{IN} shutdown current	V_{EN} < V_{SDF}		1.81		mA
ENABLE / UNDERVOLTAGE LOCKOUT (EN/UVLO)						
V_{UVLOR}	EN/UVLO pin voltage threshold for turning on, rising	EN/UVLO Rising		1.2		V
V_{UVLOF}	EN/UVLO pin voltage threshold for turning off and engaging QOD, falling (primary device)	EN/UVLO Falling		1.12		V
$V_{UVLOHYS}$	UVLO Hysteresis			94		mV
V_{SDF}	Shutdown threshold	EN/UVLO Falling		0.46		V
V_{SDR}	Shutdown threshold	EN/UVLO Rising		0.51		V
OVERVOLTAGE PROTECTION (IN)						
$V_{IN-OVPR}$	IN overvoltage protection threshold (rising)	VIN_OV_FLT = 0xb1		60.1		V
$V_{IN-OVPF}$	IN overvoltage protection threshold (falling)	VIN_OV_FLT = 0xb1		57		V
$V_{IN-OVPHYS}$	IN overvoltage protection threshold (Hysterisis)	VIN_OV_FLT = 0xb1		3		V
ON-RESISTANCE (IN - OUT)						
R_{ON}	ON state resistance	I_{OUT} = 12 A		3.65		mΩ
CURRENT LIMIT REFERENCE (IREF)						
V_{IREF}	Current Limit Reference DAC output voltage	VIREF = 0x32 (Default)		1		V
V_{IREF}	Current Limit Reference DAC output voltage	VIREF = 0x00		0.3		V
V_{IREF}	Current Limit Reference DAC output voltage	VIREF = 0x3F		1.182		V
CURRENT LIMIT (ILIM)						
$G_{ILIM(LIN)}$	Current Monitor Gain (ILIM:IOUT) vs. IOUT.	Device in steady state (PG asserted), I_{OUT} = 12 A		18.26		uA/A
$I_{start-up}$	IOUT Start-up Current limit regulation threshold	V_{IN} - V_{OUT} = 350 mV		0.47		A
V_{FB}	Foldback voltage			2.11		V
OUTPUT CURRENT MONITOR AND OVERCURRENT PROTECTION (IMON)						
G_{IMON}	Current Monitor Gain (IMON:IOUT)	Device in steady state (PG asserted), I_{OUT} = 12 A		18.25		uA/A
G_{IMON}	Current Monitor Gain (IMON:IOUT)	Device in steady state (PG asserted), I_{OUT} = 4 A		18.28		uA/A
I_{TRIP}	IOUT Current limit trip (Circuit-Breaker) threshold	R_{IMON} = 2.32 Ω, V_{IREF} = 1 V		21.52		A
CURRENT FAULT TIMER (ITIMER)						
SHORT-CIRCUIT PROTECTION						
I_{FFT}	Fixed fast trip threshold in steady state (primary)	PG asserted High (MODE = Open)		87.27		A
I_{SFT}	Scalable fast trip current:I_{TRIP} ratio	DEVICE_CONFIG [12:11] = 00		40		A
I_{SFT}	Scalable fast trip current:I_{TRIP} ratio	DEVICE_CONFIG [12:11] = 01		2.5		A/A
I_{SFT}	Scalable fast trip current:I_{TRIP} ratio	DEVICE_CONFIG [12:11] = 10		2		A/A
I_{SFT}	Scalable fast trip current:I_{TRIP} ratio	DEVICE_CONFIG [12:11] = 11		1.5		A/A
ACTIVE CURRENT SHARING						
$R_{ON(ACS)}$	R_{ON} during Active current sharing	V_{ILIM} > 1.1 x (1/3)xV_{IREF}		4.67		mΩ

ADVANCE INFORMATION

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$G_{IMON(ACS)}$	IMON:IOUT ratio during active current limiting	PG asserted High, V_{ILIM} > 1.1 x V_{IREF}		18.7		uA/A
$CL_{REF(ACS)}$	Ratio of Active current sharing trigger threshold to steady state circuit-breaker threshold	PG asserted High		36.80		%
INRUSH CURRENT PROTECTION (DVDT)						
I_{DVDT}	dVdt Pin Charging Current (Primary/ Standalone mode)	DEVICE_CONFIG[10:9] = 11		3.15		uA
I_{DVDT}	dVdt Pin Charging Current (Primary/ Standalone mode)	DEVICE_CONFIG[10:9] = 10		2.1		uA
I_{DVDT}	dVdt Pin Charging Current (Primary/ Standalone mode)	DEVICE_CONFIG[10:9] = 01		1.05		uA
I_{DVDT}	dVdt Pin Charging Current (Primary/ Standalone mode)	DEVICE_CONFIG[10:9] = 00		0.53		uA
G_{DVDT}	dVdt Gain	0.4 V < V_{dVdt} < 2.4 V		24.9		V/V
R_{DVDT}	dVdt Pin to GND Discharge Resistance			490		Ω
GHI						
$V_{GS(GHI)}$ Rising	G-S Threshold when GHI/PG is asserted			7		V
$V_{GS(GHI)}$ Falling	G-S Threhold when GHI/PG is de-asserted			3.4		V
$R_{ON(GHI)}$	Ron When GHI/PG is asserted			3.9		mΩ
QUICK OUTPUT DISCHARGE (QOD)						
I_{QOD}	Quick Output Discharge pull-down current	$V_{SD(R)}$ < V_{EN} < V_{UVLO}, 0 < Tj < 125 ℃, VIN = 51 V		21		mA
OVERTEMPERATURE PROTECTION (OTP)						
TSD	Absolute Thermal Shutdown Rising Threshold	T_J Rising, , VIN = 51 V		150		°C
TSD_{HYS}	Absolute Thermal shutdown hysteresis	T_J Falling, VIN = 51 V		13		°C
FET HEALTH MONITOR						
V_{DSFLT}	FET D-S Fault Threshold	SWEN = L, VIN = 51 V		0.5		V
ADDRESS SELECT (ADDR0/ADDR1)						
I_{ADDRx}	ADDR0 pin pull-up current			5.05		µA
	ADDR1 pin pull-up current			5.05		µA
I_{OC_BKP}	Back-up overcurrent protection threshold	IMON short to GND		39		A

5.6 PMBus and GPIO DC Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIOx						
V_{OL}	GPIOx output logic low	Pin configured as output, de-asserted Low. Sink current = 20mA.		0.138	0.5	V
V_{OH}	GPIOx output logic high	Pin configured as output, asserted high	4.8	4.9		V
R_{GPIO}	GPIOx pin pull-down resistance	Pin configured as output, de-asserted Low		6.8		Ω
I_{GPIO}	GPIOx pin leakage current	Pin configured as output, asserted high			1	uA
V_{IH}	GPIOx input logic high	Pin configured as input	1.56			V
V_{IL}	GPIOx input logic low	Pin configured as input			0.82	V

ADVANCE INFORMATION

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PMBus (SCL/SDA)						
V_{IL_PMBus}	SDA Input logic low				0.85	V
V_{IL_PMBus}	SCL Input logic low				0.85	V
V_{IH_PMBus}	SCL Input logic high		1.35			V
V_{IH_PMBus}	SDA Input logic high		1.35			V
V_{OL_PMBus}	Low-level output voltage - SCL	I_{OL} = -20 mA			0.4	V
V_{OL_PMBus}	Low-level output voltage - SDA	I_{OL} = -20 mA			0.4	V

5.7 Telemetry

T_A = 25℃ to 85℃

Parameter	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Telemetry					
ADC Resolution			10		bits
Sampling Rate	ADC High Performance mode		150		KHz
VAUX Absolute error	ADC High Perf mode, VAUX = 1.95 V (Full-scale) , 1 sample		0.4		%FS
VIN Absolute error	ADC High Perf mode, VIN = 48V, 1 sample		0.4		%FS
VOUT Absolute error	ADC High Perf mode, VOUT = 48 V, 1 sample		0.4		%FS
VTEMP Absolute error	ADC High Perf mode		5		℃
VIMON Absolute error	ADC High Perf mode, VIMON = 0.8 V, 1 sample		0.4		%FS
PIN Absolute error	ADC High Perf mode, VIN = 48V, VIMON = 0.8 V, 1 sample		1		%FS
EIN Absolute error	Accumulated energy over 5 ms window. VIN = 48 V DC, VIMON = 0.8 V		1.5		%

5.8 Logic Interface

–40°C ≤ T_J ≤ +125°C, VIN = V_{DD} = 45 V to 60 V, OUT = Open, R_{ILIM} = 931 Ω R_{IMON} = 2.55 kΩ, V_{IREF} = 1 V , $\overline{FLT}$ = 33 kΩ pull-up to 3.3 V, PGOOD = 33 kΩ pull-up to 3.3 V, C_{OUT} = 10 µF, C_{IN} = 10 nF, dVdT = Open , $V_{EN/UVLO}$ = 2 V, TEMP/EECLK/GPIO1 = Open, AUX/EEDATA/GPIO2 = Open, ADDR0 = Open, ADDR1 = Open, SCL = 330Ω pull-up to 3.3 V, SDA = 330Ω pull-up to 3.3 V. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
WPB						
I_{WPBLKG}	WPB pin leakage current				1	uA
V_{IH_WPB}	WPB input logic high		2.5			V
V_{IL_WPB}	WPB input logic low				0.5	V
SWEN						
R_{SWEN}	SWEN pin pull-down resistance	SWEN de-asserted Low		7		Ω
$I_{SWENLKG}$	SWEN pin leakage current	SWEN asserted high, pulled up to 5 V through 10kohms			2	uA
FAULT INDICATION (FLTB)						
R_{FLTB}	FLTB pin pull-down resistance	FLTB asserted Low		7		Ω
$I_{FLTBLKG}$	FLTB pin leakage current	FLTB de-asserted High, pulled up to 5V through 10kohms			2	uA
POWER GOOD INDICATION (PG)						
R_{PG}	PG pin pull-down resistance	PG de-asserted Low		7		Ω

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PGKG}	PG pin leakage current	PG asserted High, pulled up to 5V through 10kohms			2	uA

5.9 Timing Requirements

–40°C ≤ T_J ≤ +125°C, VIN = V_{DD} = 45 V to 60 V, OUT = Open, R_{ILIM} = 931 Ω R_{IMON} = 2.55 kΩ, V_{IREF} = 1 V , $\overline{FLT}$ = 33 kΩ pull-up to 3.3 V, PGOOD = 33 kΩ pull-up to 3.3 V, C_{OUT} = 10 µF, C_{IN} = 10 nF, dVdT = Open , $V_{EN/UVLO}$ = 2 V, TEMP/EECLK/GPIO1 = Open, AUX/EEDATA/GPIO2 = Open, ADDR0 = Open, ADDR1 = Open, SCL = 330Ω pull-up to 3.3 V, SDA = 330Ω pull-up to 3.3 V. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVP}	Overvoltage protection response time	V_{OVP} > V_{OVPR} V to SWEN↓		1.5		µs
t_{Insdly}	Insertion delay	INS_DLY = 0x00, $V_{EN/UVLO}$ > $V_{UVLO(R)}$ to SWEN↑		10		ms
		INS_DLY = 0x07, $V_{EN/UVLO}$ > $V_{UVLO(R)}$ to SWEN↑		560		ms
t_{FFT}	Fixed Fast-Trip response time Hard Short	V_{DS} > 1.5 x V_{DSCOMP} to I_{OUT}↓		200		ns
t_{SFT}	Scalable Fast-Trip response time	I_{OUT} > 3 x I_{TRIP} to IOUT↓		400		ns
t_{ITIMER}	Overcurrent blanking interval	I_{OUT} = 1.5 x I_{TRIP}, OC_TIMER = 0x00		0		ms
t_{ITIMER}	Overcurrent blanking interval	I_{OUT} = 1.5 x I_{TRIP}, OC_TIMER = 0x14 (Default)		2.1		ms
t_{ITIMER}	Overcurrent blanking interval	I_{OUT} = 1.5 x I_{TRIP}, OC_TIMER = 0xFF		27.3		ms
t_{RST}	Auto-Retry Interval	RETRY_CONFIG[2:0] = 100		800		ms
$t_{EN(DG)}$	EN/UVLO de-glitch time			10		µs
t_{SU_TMR}	Start-up timeout interval	SWEN↑ to FLT↓		8		s
$t_{Discharge}$	QOD discharge time (90% to 10% of V_{OUT})	V_{SD} < $V_{EN/UVLO}$ < V_{UVLO}, C_{OUT} = 0.5 mF, V_{IN} = 51 V.		1300		ms
t_{QOD}	QOD enable timer	V_{SD} < $V_{EN/UVLO}$ < V_{UVLO}		5.9		ms
t_{PGA}	PG assertion delay	DEVICE_CONFIG[15] = 0, Device in steady state, VOUT > VOUT_PGTH to PG↑		100		µs
t_{PGD}	PG De-assertion delay	Device in steady state, VOUT < VOUT_PGTH to PG↓		3		µs

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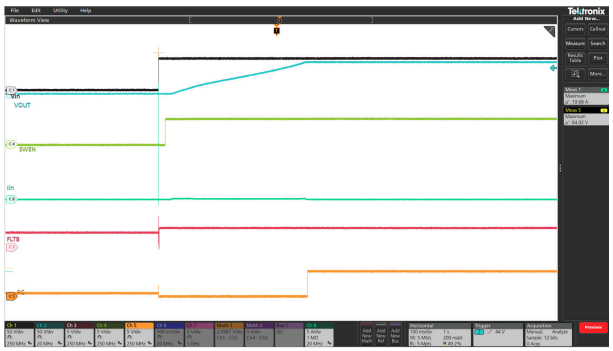
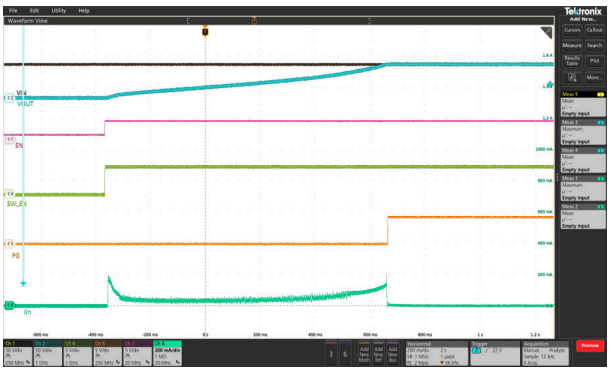
5.10 Typical Characteristics



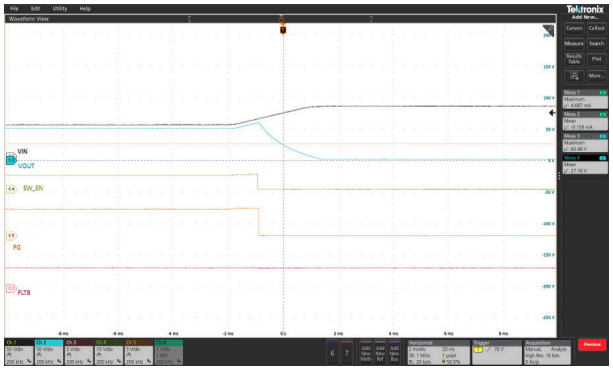
EN held high, IN supply ramped up to 51V. C_{OUT} = 1mF, C_{dVdt} = 68nF

Figure 5-1. Power Up Using Supply



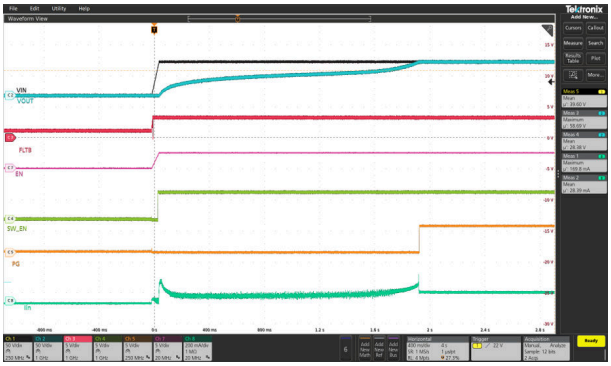
IN supply held steady at 54V, EN pin toggled from low to high. C_{OUT} = 1mF, C_{dVdt} = 68nF

Figure 5-2. Power Up Using EN



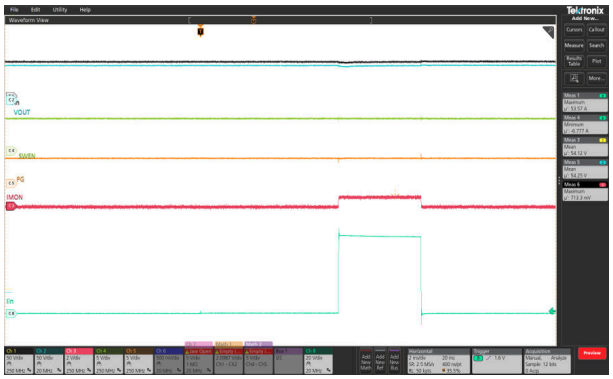
VIN Overvoltage rising threshold programmed to 60.47V, EN held high, IN supply ramped up from 54V to 80V with ramp rate of 10V/ms. C_{OUT} = 1mF, C_{dVdt} = 68nF

Figure 5-3. Input Overvoltage Protection



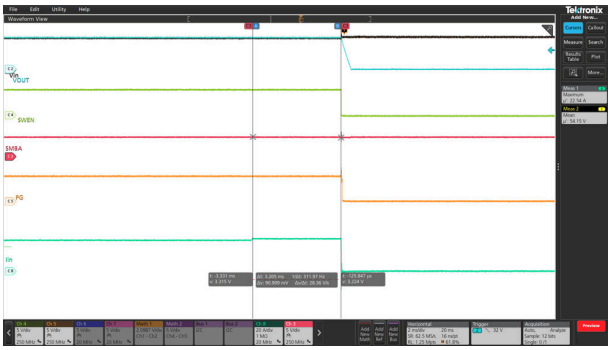
IN supply ramped to 54V along with EN, C_{OUT} = 500µF, C_{dVdt} = 68nF, R_{out}=820Ω DVDT scaling at 100 %

Figure 5-4. Inrush with R and C



Device in steady-state, Load current of 48A applied for 3ms and then removed. Overcurrent blanking delay set to 3.2ms. Vin = 54V

Figure 5-5. Transient Overcurrent Blanking



Device in steady-state, Load current ramped up to 48A for >3.2ms. Overcurrent blanking delay set to 3.2ms

Figure 5-6. Overcurrent Protection

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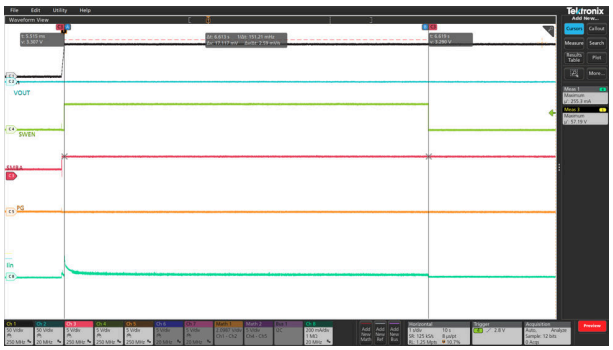
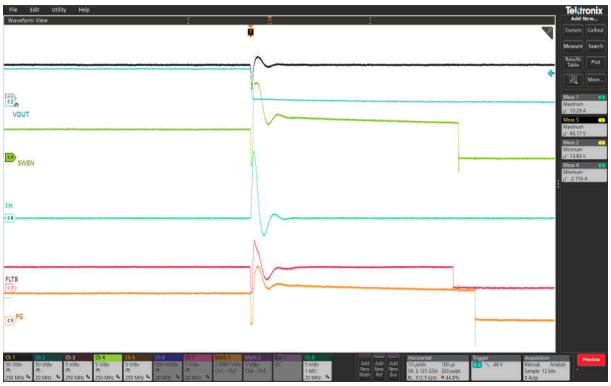
5.10 Typical Characteristics (continued)



OUT shorted to GND. IN supply held steady at 54V, EN pin toggled from low to high.

Figure 5-7. Power Up into Short-Circuit Protection



Device in steady-state, OUT shorted to GND. Vin = 51V. C_{out}=3uF. Device turns off in 131ns

Figure 5-8. Short-Circuit Protection During Steady-state

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6 Detailed Description

6.1 Overview

The TPS1689x is an eFuse with integrated power switch that is used to manage load voltage and load current. TPS1689x is equipped with a PMBus compatible digital interface which allows a host to control, configure, monitor and debug the device. The device starts the operation by monitoring the VDD and IN bus. When V_{DD} & V_{IN} exceed the respective Undervoltage Protection (UVP) thresholds, the device waits for the insertion delay timer duration to allow the supply to stabilize before starting up. Next, the device samples the EN/UVLO pin. As long as EN/UVLO is held low, the internal MOSFET is turned off along with the internal control/digital circuits. A high level on this pin enables the internal control circuits and prepares the PMBus engine to receive commands from the host.

After a successful start-up sequence, TPS1689x device now actively monitors the load current and input voltage, and controls the internal FET to make sure that the programmed over-current threshold I_{TRIP} is not exceeded and overvoltage spikes are cut-off. This keeps the system safe from harmful levels of voltage and current. At the same time, a user programmable overcurrent blanking timer allows the system to pass transient peaks in the load current profile without tripping the eFuse. This maintains a robust protection against real faults which is also immune to transients, thereby maximizing system uptime.

The device has integrated protection circuits to maintain device safety and reliability under recommended operating conditions. The internal FET is protected at all time using the thermal shutdown mechanism, which turns off the FET whenever the junction temperature (Tj) becomes too hot for the device to work reliably.

The TPS1689x has integrated high accuracy and high bandwidth analog load current monitor, which allows the system to precisely monitor the load current in steady state as well as during transients. This facilitates the implementation of advanced dynamic platform power management techniques to maximize system power utilization and throughput without sacrificing safety and reliability..

The TPS1689x allows the host to monitor various system parameters and status over the PMBus interface. It's also possible to change the device configuration over PMBus to control the device behavior as per system needs. This includes various warning/fault thresholds, timers and pin functions. The configuration values can also be stored in the internal non-volatile memory so that the device can start up with some pre-defined configuration without host intervention.

The TPS1689x also provides advanced telemetry features such as high-speed ADC sample buffering and Blackbox fault recording which facilitate system design and debug.

For systems needing higher load current support, TPS1689x can be connected in parallel with TPS1685x. The TPS16890 acts as a primary controller and enables control, telemetry and configuration of the whole chain over PMBus. Each device synchronizes the operating state to enable a graceful startup, shutdown and response to faults.

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6.2 Functional Block Diagram

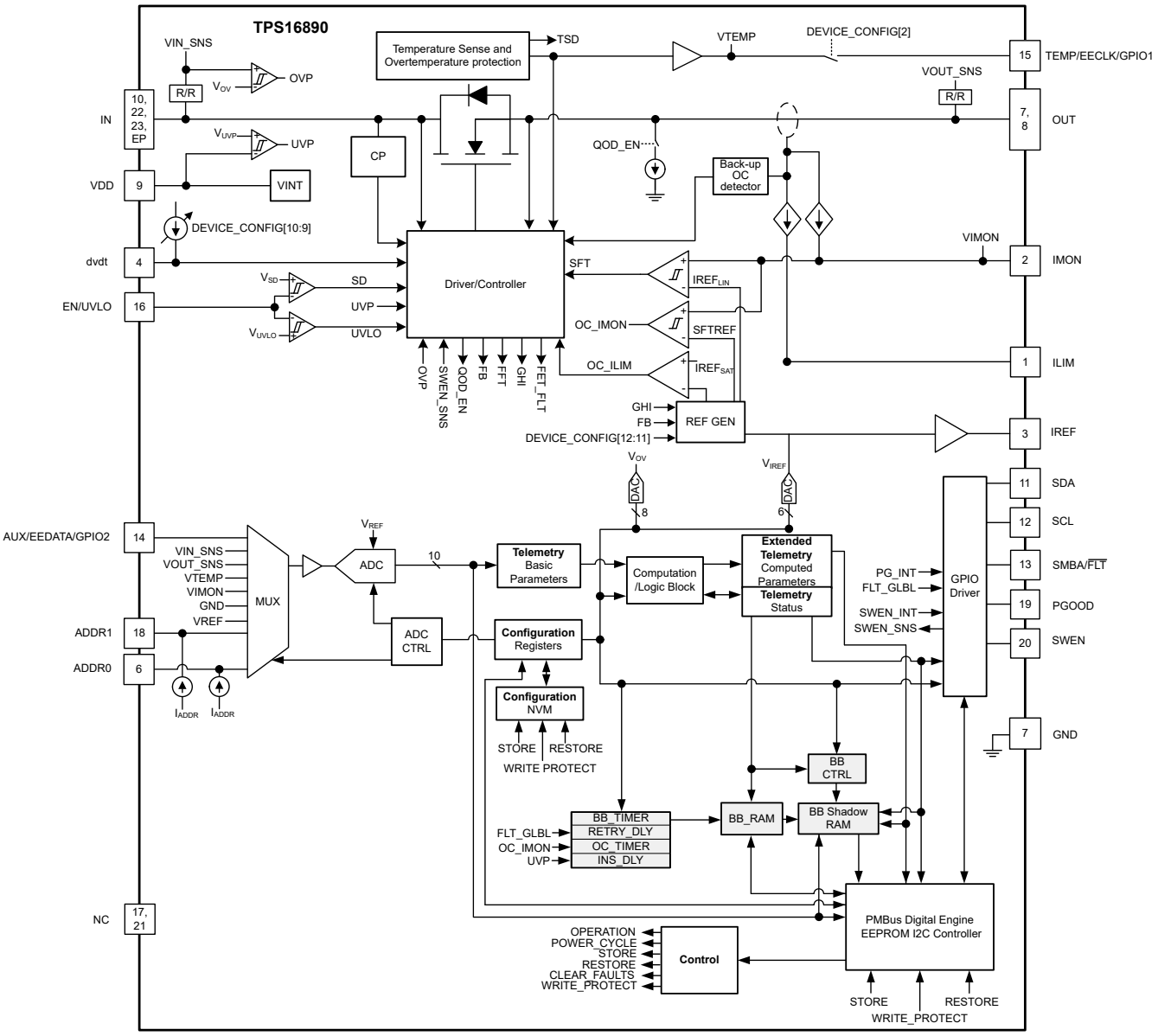

Figure 6-1. TPS16890 Functional Block Diagram

6.3 Feature Description

The TPS1689 eFuse is a highly integrated, advanced power management device that provides monitoring, detection, protection and reporting in the event of system faults.

6.3.1 Undervoltage Protection

The TPS1689 implements undervoltage lockout on VDD and VIN in case the applied voltage becomes too low for the system or device to properly operate. The undervoltage lockout has a default internal threshold (V_{UVP}) on VDD and programmable threshold (V_{UVLOIN}) on VIN. Alternatively, the UVLO comparator on the EN/UVLO pin allows the undervoltage protection threshold to be externally adjusted to a user defined value. Figure 6-2 and Equation 1 show how a resistor divider can be used to set the UVLO set point for a given voltage supply.

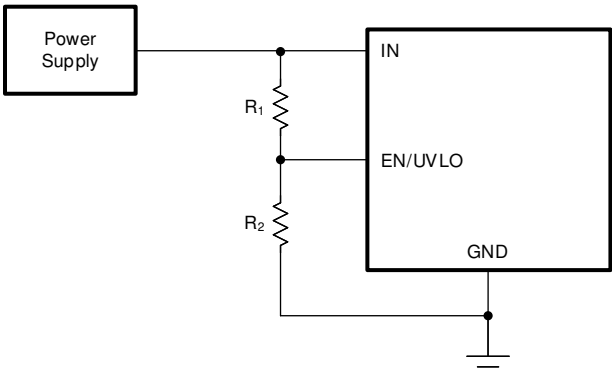

Figure 6-2. Adjustable Undervoltage Protection

$$V_{IN(UV)} = V_{UVLO(R)}\frac{R_1 + R_2}{R_2} \quad (1)$$

The VIN UVLO fault threshold can also be programmed using PMBus® writes to VIN_UV_FLT register.

The EN/UVLO pin implements a bi-level threshold and can be used to control the device from an external host.

1. $V_{EN} > V_{UVLO(R)}$: Device is fully ON.
2. $V_{SD(F)} < V_{EN} < V_{UVLO(F)}$: The FET along with most of the controller circuitry is turned OFF, except for some critical bias and digital circuitry. Holding the EN/UVLO pin in this state for a duration greater than t_{QOD} activates the Output Discharge function.
3. $V_{EN} < V_{SD(F)}$: All active circuitry inside the part is turned OFF and the device retains no digital state memory. The device also resets latched faults, status flags and configuration values written to the registers through PMBus® writes.

6.3.2 Insertion Delay

The TPS1689 implements insertion delay at start-up to make sure the supply has stabilized before the device tries to turn on the power to the load. This is helpful in hotswap applications where a card is hot-plugged into a live backplane and can have some contact bounce before the card is firmly plugged into the connector. The device initially waits for the VDD supply to rise above the V_{UVP} threshold and all the internal bias voltages to settle. After that, the device remains off for an additional delay of t_{INSDLY} irrespective of the EN/UVLO pin condition. This action helps to prevent any unexpected behavior in the system if the device tries to turn on before the card has made firm contact with the backplane or if there is any supply ringing or noise during start-up.

The insertion delay can be changed by programming the INS_DLY register value in the Non-volatile memory/ EEPROM using PMBus®.

6.3.3 Overvoltage Protection

The TPS1689x implements overvoltage lockout to protect the load from input overvoltage conditions. If the input voltage on IN exceeds the OVP rising threshold, the power FET is turned OFF within t_{OVP}. The OVP comparator on the IN pin uses a default internal overvoltage protection threshold of $V_{OVP(R)}$, which can be changed by programming the non-volatile configuration memory or dynamically through PMBus® register writes to the VIN_OV_FLT register. The OVP comparator has in-built hysteresis for improved noise immunity. After the voltage on IN falls below the OVP falling threshold ($V_{OVP(F)}$), the FET is turned ON in a dVdt controlled manner.

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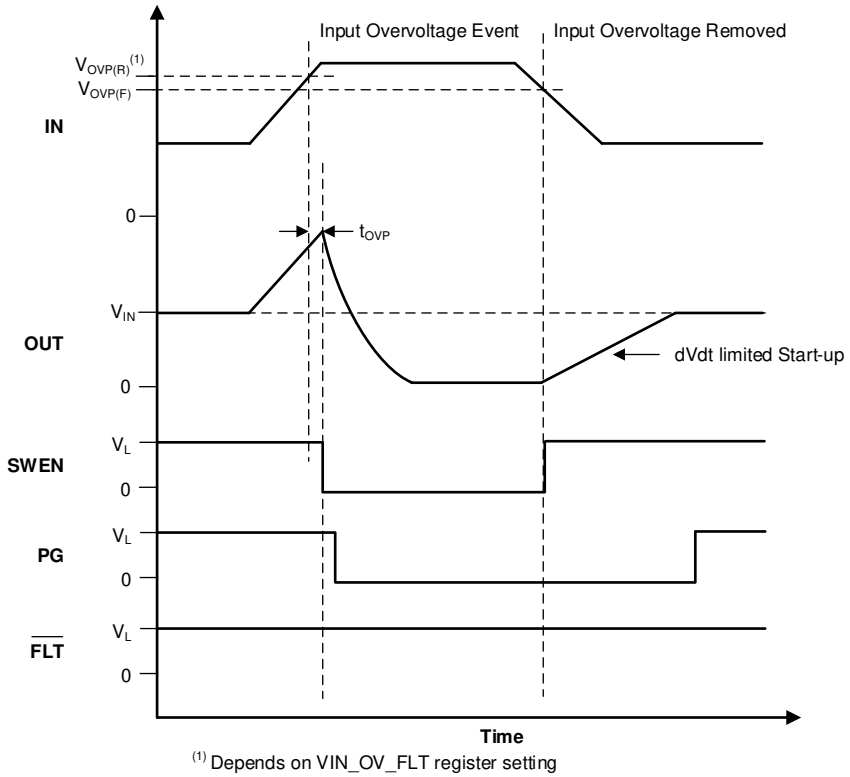

Figure 6-3. Input Overvoltage Protection Response

6.3.4 Inrush Current, Overcurrent, and Short-Circuit Protection

TPS1689 incorporates four levels of protection against overcurrent:

1. Adjustable slew rate (dVdt) for inrush current control
2. Active current limit with an adjustable threshold (I_{LIM}) for overcurrent protection during start-up
3. Circuit-breaker with an adjustable threshold (I_{OCP}) and blanking timer (t_{OC_TIMER}) for overcurrent protection during steady-state
4. Fast-trip response to severe overcurrent faults with a programmable threshold to quickly protect against severe short-circuits under all conditions, as well as a fixed threshold (I_{FFT}) during steady state

6.3.4.1 *Slew rate (dVdt) and Inrush Current Control*

During hot-plug events or while trying to charge a large output capacitance, there can be a large inrush current. If the inrush current is not managed properly, it can put excessive stress on the system power supply causing it to droop and even damage the input connectors. This action can lead to unexpected restarts elsewhere in the system. The inrush current during turn-on is directly proportional to the load capacitance and rising slew rate. Equation 2 can be used to find the slew rate (SR) required to limit the inrush current (I_{INRUSH}) for a given load capacitance (C_{LOAD}):

$$SR\left(\frac{V}{ms}\right) = \frac{I_{INRUSH}\,(mA)}{C_{OUT}\,(\mu F)} \tag{2}$$

A capacitor can be added to the DVDT pin to control the rising slew rate and lower the inrush current during turn-on. This is also a function of the dVdt rate scaling factor which can be digitally programmed through PMBus® writes to the DEVICE_CONFIGregister. The required C_{dVdt} capacitance to produce a given slew rate can be calculated using Equation 3.

$$C_{dVdt}\,(pF) = \frac{50000 \times k}{SR\left(\frac{V}{ms}\right)} \tag{3}$$

where k = 0.25, if DEVICE_CONFIG[10:9] = 00 (Default)

k = 0.5, if DEVICE_CONFIG[10:9] = 01

k = 1, if DEVICE_CONFIG[10:9] = 10

k = 1.5, if DEVICE_CONFIG[10:9] = 11

The fastest output slew rate is achieved by leaving the dVdt pin open and setting DEVICE_CONFIG[10:9] = 11.

The slew rate is also a function of the energy dissipated during start-up. The slew rate control via DVDT is only below the Start-up current limit $I_{Startup}$. The current will be clamped at $I_{startup}$ if the start-up current due to dvdt pin exceeds it and the slew rate will be slower

Note

High turn-on slew rates in combination with high input power path inductance can result in oscillations during start-up. This can be mitigated using one or more of the following steps:

1. Reduce the input inductance.
2. Increase the capacitance on VIN pin.
3. Increase the DVDT pin capacitor value or change the DVDT scaling factor using DEVICE_CONFIG[10:9] register bits to reduce the slew rate or increase the start-up time. TI recommends using a minimum start-up time of 30 ms.

6.3.4.1.1 Start-Up Timeout

If the start-up is not completed, that is, the FET is not fully turned on within a certain timeout interval (t_{SU_TMR}) after SWEN is asserted, the device registers it as a fault. The fault status is reported in the STATUS_MFR_SPECIFIC register Bit[6]. $\overline{FLT}$ is asserted low and the device goes into latch-off or auto-retry mode depending on the RETRY_CONFIG register setting.

6.3.4.2 Steady-State Overcurrent Protection (Circuit-Breaker)

The TPS1689 responds to output overcurrent conditions during steady-state by performing a circuit-breaker action after a user-adjustable transient fault blanking interval. This action allows the device to support a higher peak current for a short user-defined interval but also ensures robust protection in case of persistent output faults.

The device constantly senses the output load current and provides an analog current output (I_{IMON}) on the IMON pin which is proportional to the load current, which in turn produces a proportional voltage (V_{IMON}) across the IMON pin resistor (R_{IMON}) as per Equation 4.

$$V_{IMON} = I_{OUT} \times G_{IMON} \times R_{IMON} \quad (4)$$

Where G_{IMON} is the current monitor gain (I_{IMON} : I_{OUT})

The overcurrent condition is detected by comparing this voltage against the voltage on the IREF pin as a reference. The reference voltage (V_{IREF}) can be controlled in two ways, which sets the overcurrent protection threshold (I_{OCP}) accordingly.

- The reference voltage (V_{IREF}) can be generated using internal DAC and can be changed by programming the non-volatile configuration memory or dynamically through PMBus® writes to the VIREF register.
- It is also possible to drive the IREF pin from an external low impedance precision reference voltage source.

The overcurrent protection threshold during steady-state (I_{OCP}) can be calculated using Equation 5.

$$I_{OCP} = \frac{V_{IREF}}{G_{IMON} \times R_{IMON}} \quad (5)$$

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Note

TI recommends to add a 1 nF capacitor from IREF pin to GND for improved noise immunity.

After an overcurrent condition is detected, that is the load current exceeds the programmed current limit threshold (I_{OCP}), but stays lower than the short-circuit threshold (I_{SCP}), the device starts running the internal overcurrent blanking digital timer (OC_TIMER). If the load current drops below the current limit threshold before the OC_TIMER expires, the circuit-breaker action is not engaged. This action allows short overload transient pulses to pass through the device without tripping the circuit. At the same time, the OC_TIMER is reset so that it is at its default state before the next overcurrent event. This ensures the full blanking timer interval is provided for every overcurrent event.

If the overcurrent condition persists, the OC_TIMER continues to run and after it expires, the circuit-breaker action turns off the FET immediately.

Equation 6 can be used to calculate the R_{IMON} value for the desired overcurrent threshold.

$$R_{IMON} = \frac{V_{IREF}}{G_{IMON} \times I_{OCP}} \quad (6)$$

The duration for which transients are allowed can be programmed using OC_TIMER register setting through PMBus® writes.

Figure 6-4 illustrates the overcurrent response for TPS1689 eFuse. After the part shuts down due to a circuit-breaker fault, it either stays latched off or restarts automatically based on the RETRY_CONFIG register setting.

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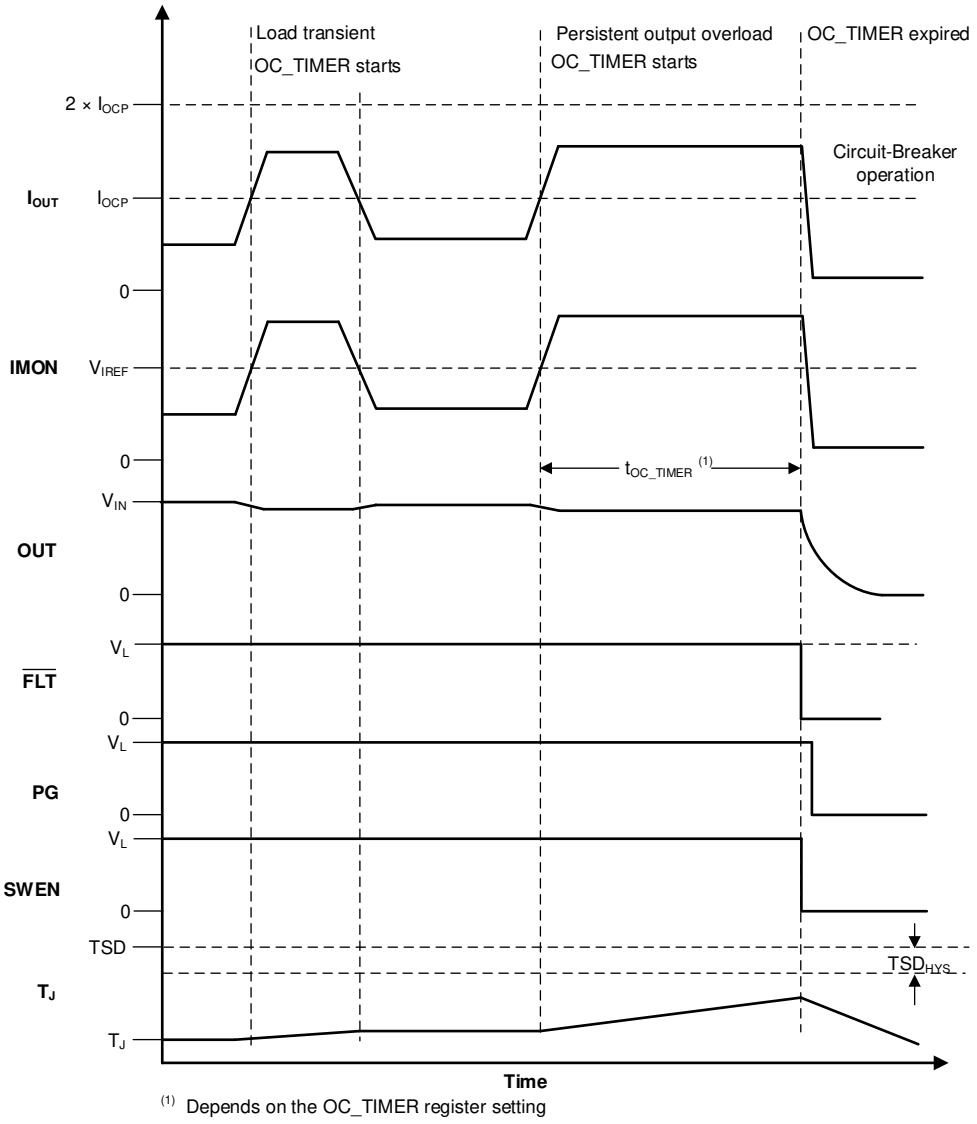

Figure 6-4. Steady-state Overcurrent (Circuit-Breaker) Response

When a transient overcurrent condition (the load current exceeds the programmed current limit threshold but the OC_TIMER does not expire) is detected, the device:

- sets the OC_DET bit in the STATUS_MFR_SPECIFIC_2 register
- fills-up one of the Blackbox RAM registers (if available to write) writing the event identifier as OC_DET and relative time stamp information
- increases the Blackbox RAM address pointer in the BB_TIMER register by one (1) if it was previously less than six (6), otherwise resets to zero (0).

Note

It is assumed that the VIN_UV_WARN , VIN_OV_WARN, and VOUT_UV_WARN events are not triggered because of a step load transient.

When a persistent overcurrent condition (the load current exceeds the programmed current limit threshold and the OC_TIMER expires) is detected, the device:

- sets the FET_OFF and NONE_OF_THE_ABOVE/UNKNOWN bits in the STATUS_BYTE register

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- sets the OUT_STATUS, INPUT_STATUS, PGOODB, and NONE_OF_THE_ABOVE/UNKNOWN bits in the upper byte of the STATUS_WORD register
- sets the VOUT_UV_WARN bit in the STATUS_OUT register
- sets the OC_FLT bit in the STATUS_INPUT register
- sets the PGOODB bit in the STATUS_MFR_SPECIFIC_2 register
- notifies the host by asserting $\overline{\text{SMBA}}$, if it is not masked setting the STATUS_IN, PGOODB, and STATUS_OUT bits in the ALERT_MASK register.
- deasserts the external PG signal.
- asserts the $\overline{\text{FLT}}$ signal, if it is not masked setting the OC_FLT bit high in the FAULT_MASK register.

Note

It is assumed that the VIN_UV_WARN and VIN_OV_WARN events are not triggered because of a step load transient.

6.3.4.3 Active Current Limiting During Start-Up

The TPS1689 responds to output overcurrent conditions during start-up by actively limiting the current. The start-up current limit is internally fixed to $I_{start\text{-}up}$. The device constantly senses the current flowing through the device (I_{DEVICE}) and provides an analog current output (I_{ILIM}) on the ILIM pin, which in turn produces a proportional voltage (V_{ILIM}) across the ILIM pin resistor (R_{ILIM}) as per Equation 7.

$$V_{ILIM} = I_{DEVICE} \times G_{ILIM} \times R_{ILIM} \quad (7)$$

Where G_{ILIM} is the current monitor gain (I_{ILIM} : I_{DEVICE})

During current regulation, the output voltage drops, resulting in increased device power dissipation across the FET. If the device internal temperature (T_J) exceeds the thermal shutdown threshold, the FET is turned off. After the part shuts down due to a TSD fault, then the part either stays latched off or restarts automatically after a delay based on the RETRY_CONFIG register setting. See *Overtemperature protection* section for more details on device response to overtemperature.

Note

The active current limit block employs a foldback mechanism during start-up based on the output voltage (V_{OUT}). When V_{OUT} is below the foldback threshold (V_{FB}), the current limit threshold is further lowered.

6.3.4.4 Short-Circuit Protection

During an output short-circuit event, the current through the device increases very rapidly. When an output short-circuit is detected, the internal fast-trip comparator triggers a fast protection sequence to prevent the current from building up further and causing any damage or excessive input supply droop. This action enables the user to adjust the fast-trip threshold as per system rating, rather than using a high fixed threshold which may not be suitable for all systems. The fast-trip comparator employs a scalable threshold (I_{SFT}) which is a function of the circuit-breaker threshold (I_{OCP}) and a digitally programmable scaling factor. The default fast-trip threshold is equal to 2 × I_{OCP} during steady-state and 2 × $I_{Startup}$ during inrush. The scaling factor for steady-state fast-trip threshold can be programmed to a different value using the DEVICE_CONFIG[12:11] register bits. Available programming options are 1.5 ×, 2 ×, 2.5 × and 8 ×. After the current exceeds the fast-trip threshold, the TPS1689 turns off the FET within t_{SFT}.

The device also employs a higher fixed fast-trip threshold (I_{FFT}) to provide fast protection against hard short-circuits during steady-state (FET in linear region). After the current exceeds I_{FFT}, the FET is turned off completely within t_{FFT}.

The device response after a fast-trip event can be configured using the SC_RETRY bit in the DEVICE_CONFIG register through PMBus® register writes or non-volatile configuration memory. There are 2 programming options available:

1. **SC_RETRY = 0 (Default setting):** The device latches a fault and remains off till a restart is triggered either externally or through internal auto-retry mechanism as per the RETRY_CONFIG register setting.

   When a short-circuit fault occurs with the SC_RETRY bit in the DEVICE_CONFIG register low, the device:

   - sets the FET_OFF and NONE_OF_THE_ABOVE/UNKNOWN bits in the STATUS_BYTE register
   - sets the OUT_STATUS, PGOODB, and NONE_OF_THE_ABOVE/UNKNOWN bits in the upper byte of the STATUS_WORD register
   - sets the VOUT_UV_WARN bit in the STATUS_OUT register
   - sets the PGOODB and SC_FLT bits in the STATUS_MFR_SPECIFIC_2 register
   - notifies the host by asserting SMBA#, if it is not masked setting the PGOODB and STATUS_OUT bits in the ALERT_MASK register.
   - deasserts the external PG signal.
   - asserts the $\overline{\text{FLT}}$ signal, if it is not masked setting the SC_FLT bit high in the FAULT_MASK register.
2. **SC_RETRY = 1:** The device attempts to turn the FET back ON fully after a short de-glitch interval (30 µs). This allows the FET to try and recover quickly after a transient overcurrent event and minimizes the output voltage droop. However, if the fault is persistent, the device enters current limit causing the junction temperature to rise and eventually enter thermal shutdown. The device latches a fault and remains off till a restart is triggered either externally or through internal auto-retry mechanism as per the RETRY_CONFIG register setting. See *Overtemperature Protection* section for details on the device response to overtemperature.

   When a short-circuit fault occurs with the SC_RETRY bit in the DEVICE_CONFIG register high, the device:

   - sets the FET_OFF, STATUS_TEMP, and NONE_OF_THE_ABOVE/UNKNOWN bits in the STATUS_BYTE register
   - sets the OUT_STATUS, MFR_STATUS, PGOODB, and NONE_OF_THE_ABOVE/UNKNOWN bits in the upper byte of the STATUS_WORD register
   - sets the VOUT_UV_WARN bit in the STATUS_OUT register
   - sets the OT_FLT bit in the STATUS_TEMP register
   - sets the SOA_FLT bit in the STATUS_MFR_SPECIFIC register
   - sets the PGOODB bit in the STATUS_MFR_SPECIFIC_2 register
   - notifies the host by asserting SMBA#, if it is not masked setting the PGOODB, MFR_STATUS, STATUS_TEMP, and STATUS_OUT bits in the ALERT_MASK register.
   - deasserts the external PG signal.
   - asserts the $\overline{\text{FLT}}$ signal, if it is not masked setting the SOA_FLT and TEMP_FLT bits high in the FAULT_MASK register.

Figure 6-5 illustrates the short-circuit response for TPS1689 eFuse.

In some of the systems, for example blade servers and telecom equipment which house multiple hot-pluggable blades or line cards connected to a common supply backplane, there can be transients on the supply due to switching of large currents through the inductive backplane. This can result in current spikes on adjacent cards which can potentially be large enough to trigger the fast-trip comparator of the eFuse. The TPS1689 uses a proprietary algorithm to avoid nuisance tripping in such cases thereby facilitating uninterrupted system operation.

Note

- The VIN_TRAN status bit in STATUS_MFR_SPECIFIC_2 register is set to indicate if an input line transient event was detected and masked.

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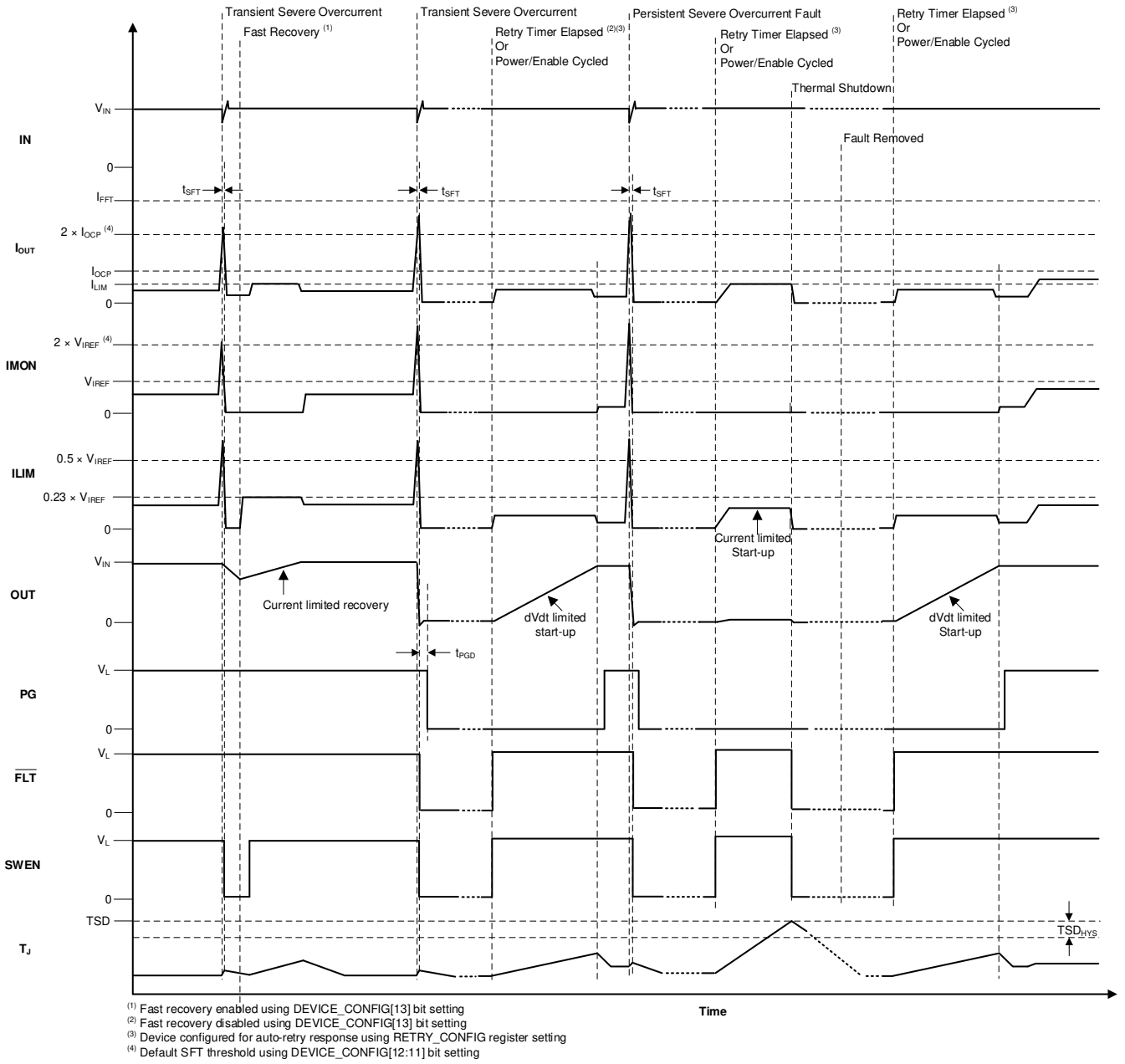

Figure 6-5. Short-Circuit Response

6.3.5 Analog Load Current Monitor (IMON)

The TPS1689 allows the system to monitor the output load current accurately by providing an analog current on the IMON pin which is proportional to the current through the FET. The benefit of having a current output is that the signal can be routed across a board without adding significant errors due to voltage drop or noise coupling from adjacent traces. The current output also allows the IMON pins of multiple eFuse devices (TPS1689 or TPS1685x) to be tied together to get the total current in a parallel configuration. The IMON signal can be converted to a voltage by dropping it across a resistor at the point of monitoring. The user can sense the voltage (V_{IMON}) across the R_{IMON} to get a measure of the output load current using Equation 8.

$$I_{OUT} = \frac{V_{IMON}}{G_{IMON} \times R_{IMON}} \quad (8)$$

The TPS1689 IMON circuit is designed to provide high bandwidth and high accuracy across load and temperature conditions, irrespective of board layout and other system operating conditions. This design allows the IMON signal to be used for advanced dynamic platform power management techniques such as Intel PSYS or PROCHOT to maximize system power usage and platform throughput without sacrificing safety or reliability.

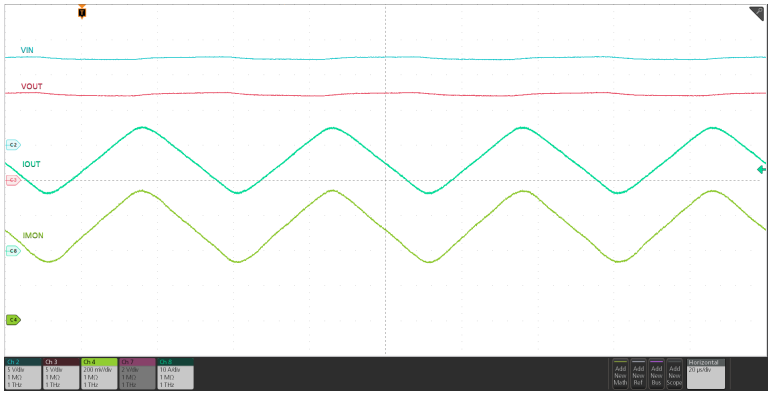

Figure 6-6. Analog Load Current Monitor Response

Note

1. The IMON pin provides load current monitoring information only during steady-state. During inrush, the IMON pin reports zero load current.
2. The ILIM pin reports the individual device load current at all times and can also be used as an analog load current monitor for each individual device.
3. TI recommends adding a 22 pF capacitor from IMON pin to GND for noise filtering purposes.
4. Care must be taken to minimize parasitic capacitance on the ILIM pin to avoid any impact on the overcurrent and short-circuit protection timing during start-up.

6.3.6 Overtemperature Protection

The TPS1689 employs an internal thermal shutdown mechanism to protect itself when the internal FET becomes too hot to operate safely. When the TPS1689 detects thermal overload, the device shuts down. Thereafter the device either remains latched-off until the device is power cycled or re-enabled, or restarts automatically after delay based on the device Auto-retry configuration.

The overtemperature threshold has a default threshold (TSD) which can be digitally programmed to a lower value using the OT_FLT register based on system needs.

Table 6-1. Overtemperature Protection Summary

Auto-Retry Configuration	Enter TSD	Exit TSD
Latch-Off	V_{TEMP} ≥ OT_FLT threshold or T_J ≥ TSD	V_{TEMP} < OT_FLT - OT_{Hys} or T_J < TSD – TSD_{HYS} VDD cycled to 0V and then above $V_{UVP(R)}$ or EN/UVLO toggled below $V_{SD(F)}$
Auto-Retry	V_{TEMP} ≥ OT_FLT threshold or T_J ≥ TSD	V_{TEMP} < OT_FLT - OT_{Hys} or T_J < TSD – TSD_{HYS} Retry Timer expired or VDD cycled to 0V and then above $V_{UVP(R)}$ or EN/UVLO toggled below $V_{SD(F)}$

6.3.7 Analog Junction Temperature Monitor (TEMP)

The TPS1689 allows the system to monitor the junction temperature (T_J) accurately by providing an analog voltage on the TEMP pin which is proportional to the temperature of the die. This voltage is sensed by an ADC input and reported using the READ_TEMPERATURE_1 PMBus® command for digital telemetry. In a

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multi-device parallel configuration involving TPS1689 and TPS1685x , the TEMP outputs of all devices can be tied together. In this configuration, the TEMP signal reports the temperature of the hottest device in the chain.

Note

1. The TEMP pin voltage is used only for external monitoring and does not interfere with the overtemperature protection scheme of each individual device which is based purely on the internal temperature monitor.
2. TI recommends to add a capacitance of 22 pF on the TEMP pin to filter out glitches during system transients.

6.3.8 FET Health Monitoring

The TPS1689 can detect and report certain conditions which are indicative of a failure of the power path FET. If undetected or unreported, these conditions can compromise system performance either by not providing power to the load correctly or the necessary level of protection. After a FET failure is detected, the TPS1689 tries to turn off the internal FET by pulling the gate low and asserts the $\overline{FLT}$ pin. The specific FET fault type is also reported in the STATUS_MFR_SPECIFIC status register.

- **D-S short:** D-S short can result in a constant uncontrolled power delivery path formed from source to load, either due to a board assembly defect or due to internal FET failure. This condition is detected at start-up by checking if $V_{IN-OUT} < V_{DSFLT}$ before the FET is turned ON. If yes, the device engages the internal output discharge to try and discharge the output. If the V_{OUT} doesn't discharge below V_{FB} within a certain allowed interval, the device asserts the $\overline{FLT}$ pin and sets the FET_FAULT_DS bit in the STATUS_MFR_SPECIFIC status register.

Note

There is an option to disable the D-S fault detection digitally by setting the DIS_VDSFLT bit in the DEVICE_CONFIG register. This allows the device start-up into a pre-charged output without triggering the D-S fault.

- **G-D short:** The TPS1689 detects this kind of FET failure at all times by checking if the gate voltage is close to V_{IN} even when the internal control logic is trying to hold the FET in OFF condition. If this condition is detected, the device asserts the $\overline{FLT}$ pin and sets the FET_FAULT_GD bit in the STATUS_MFR_SPECIFIC status register.
- **G-S short:** The TPS1689 detects this kind of FET failure during start-up by checking if the FET G-S voltage fails to reach the necessary overdrive voltage within a certain timeout period (t_{SU_TMR}) after the gate driver is turned ON. While in steady-state, if the G-S voltage becomes low before the controller logic has signaled to the gate driver to turn off the FET, it is latched as a fault. If this condition is detected, the device asserts the $\overline{FLT}$ pin and sets the FET_FAULT_GS bit in the STATUS_MFR_SPECIFIC status register.

6.3.9 Single Point Failure Mitigation

The TPS1689 relies on the proper component connections and biasing on the IMON, ILIM and IREF pins along with the appropriate threshold digital configurations to provide overcurrent and short-circuit protection under all circumstances. As an added safety measure, the device uses the following mechanisms to ensure that the device provides some form of overcurrent protection even if any of these pins are not connected correctly in the system or the associated components have a failure in the field or if the configuration registers are not programmed correctly.

6.3.9.1 IMON Pin Single Point Failure

- **IMON pin open:** In this case, the IMON pin voltage is internally pulled up to a higher voltage and exceeds the threshold (V_{IREF}), causing the part to perform a circuit-breaker action even if there is no significant current flowing through the device.
- **IMON pin shorted to GND directly or through a very low resistance:** In this case, the IMON pin voltage is held at a low voltage and is not allowed to exceed the threshold (V_{IREF}) even if there is significant current

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flowing through the device, thereby rendering the primary overcurrent protection mechanism ineffective. The device relies on an internal overcurrent sense mechanism to provide some protection as a backup. If the device detects that the backup current sense threshold (I_{OC_BKP}) is exceeded but at the same time the primary overcurrent detection on IMON pin fails, it triggers single point failure detection and latches a fault. The FET is turned off and the $\overline{FLT}$ pin is asserted. At the same time, the SPFAIL status bit in STATUS_MFR_SPECIFIC_2 register is set and the SMBA# signal is asserted.

6.3.9.2 IREF Pin Single Point Failure

- **IREF DAC set incorrectly or externally forced to higher voltage:** In this case, the IREF pin (V_{IREF}) is pulled up internally or externally to a voltage which is higher than the target value as per the recommended I_{OCP} or I_{LIM} calculations, preventing the primary circuit-breaker, active current limit, and short-circuit protection from getting triggered even if there is significant current flowing through the device. The device relies on an internal overcurrent detection mechanism to provide some protection as a backup. If the device detects that the load current exceeds backup overcurrent threshold (I_{OC_BKP}) but at the same the primary overcurrent or short-circuit detection on ILIM or IMON pin fails, it triggers single point failure detection and latches a fault. The FET is turned off and the $\overline{FLT}$ pin is asserted. At the same time, the SPFAIL status bit in STATUS_MFR_SPECIFIC_2 register is set and the SMBA# signal is asserted.
- **IREF pin shorted to GND:** In this case, the V_{IREF} threshold is set to 0 V, causing the part to perform active current limit or circuit-breaker action even if there is no significant current flowing through the device.

6.3.10 General Purpose Digital Input/Output Pins

The TPS1689 has two (2) general purpose digital input/output pins which can be configured for different functions as per system needs.

1. TEMP/EECLK/GPIO1(General Purpose Digital Output)
2. Aux/EEDATA/GPIO2(General Purpose Digital Output)

These pins can be configured using DEVICE_CONFIG register bits.

6.3.10.1 Fault Response and Indication ($\overline{FLT}$)

Table 6-2 summarizes the device response to various fault conditions.

Table 6-2. Fault Summary

Event or Condition	Device Response	Fault Latched Internally	$\overline{FLT}$ Pin Status	Pin Indication Masking Option	Delay
Steady-state	None	N/A	H	N/A	
Inrush	None	N/A	H	N/A	
Overtemperature	Shutdown	Y	L	Y	
Undervoltage (EN/UVLO)	Shutdown	N	H	N/A	
Undervoltage (VDD UVP)	Shutdown	N	H	N/A	
Undervoltage (VIN UVP)	Shutdown	N	H	N/A	
Overvoltage (VIN OVP)	Shutdown	N	H	N/A	
Transient overcurrent	None	N	H	N/A	
Persistent overcurrent (steady-state)	Circuit-Breaker	Y	L	Y	t_{ITIMER}
Persistent overcurrent (start-up)	Current Limit	N	H	N/A	Post TSD
Output short-circuit	Fast-trip	Y	L	Y	t_{FT}
Output short-circuit (Fast recovery configuration)	Fast-trip followed by current limited Start-up	N	H	N/A	

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Table 6-2. Fault Summary (continued)

Event or Condition	Device Response	Fault Latched Internally	$\overline{FLT}$ Pin Status	Pin Indication Masking Option	Delay
IMON pin open (steady-state)	Shutdown	Y	L	Y	
IMON pin short (steady-state)	Shutdown (If I_{OUT} > I_{OC_BKP})	Y	L	Y	45µs
IREF pin open (start-up)	Shutdown (If I_{OUT} > I_{OC_BKP})	Y	L	Y	
IREF pin open (steady-state)	Shutdown (if I_{OUT} > I_{OC_BKP})	Y	L	Y	t_{ITIMER}
IREF pin short (steady-state)	Shutdown	Y	L	Y	
IREF pin short (start-up)	Shutdown	Y	L	Y	
Start-up timeout	Shutdown	Y	L	N	t_{SU_TMR}
FET health fault (G-S)	Shutdown	Y	L	Y	10µs
FET health fault (G-D)	Shutdown	Y	L	Y	
FET health fault (D-S)	Shutdown	N	L	Y	t_{SU_TMR}
External fault (SWEN pulled low externally while device is not in UV or OV)	Shutdown	Y	L	Y	

The device response after a fault varies based on the RETRY_CONFIG register setting. The device latches a fault as per the table above and thereafter follows an auto-retry or latch-off response. For auto-retry configuration, the latched faults also trigger the start of the Auto-Retry Timer, while keeping the $\overline{FLT}$ pin pulled low. On expiry of the timer period (t_{RETRY}), the $\overline{FLT}$ pin pull-down is released and the device is ready to restart automatically. When the device turns on again, it follows the usual DVDT limited start-up sequence.

The only exception to this is during Short-circuit fault when the device is configured for fast recovery using the SC_RETRY bit in the DEVICE_CONFIG register. In this case, the device turns off quickly and then automatically turns back on in a current limited manner. This allows the system to try and recover quickly from any transient faults. See Short-Circuit Protection section for more details.

For faults that are latched internally, power cycling the part or pulling the EN/UVLO pin voltage below $V_{SD(F)}$ clears the fault and the $\overline{FLT}$ pin is de-asserted. This action also clears the Auto-retry timer. Pulling the EN/UVLO just below the UVLO threshold has no impact on the device in this condition. This is true in case of latch-off and auto-retry configurations.

In a parallel eFuse configuration involving TPS1689 and TPS1685x, the fault response is determined by the TPS1689 as the primary device. However, if the primary device fails to register a fault, there is a fail-safe mechanism in the secondary device to take control and turn off the entire chain by pulling the SWEN pin low and enter a latch-off condition. Thereafter, the device can be turned on again only by power cycling VDD below $V_{UVP(F)}$ or by cycling EN/UVLO pin below $V_{SD(F)}$.

6.3.10.2 Power Good Indication (PG)

Power Good is an active high digital output which is asserted high to indicate when the device is in steady-state and capable of delivering maximum power.

Table 6-3. PG Indication Summary

Event or Condition	FET Status	PG Pin Status	PG Delay
Device disabled (V_{EN} < V_{UVLO})	OFF	L	t_{PGD}

Table 6-3. PG Indication Summary (continued)

Event or Condition	FET Status	PG Pin Status	PG Delay
VIN Undervoltage (V_{IN} < V_{UVP} or V_{IN} < VIN_UV_FLT)	OFF	L	
VDD Undervoltage (V_{DD} < V_{UVP})	OFF	L	
VIN Overvoltage (V_{IN} > VIN_OV_FLT)	OFF	L	t_{PGD}
Steady-state	ON	H	t_{PGA}
Inrush	ON	L	t_{PGA}
Transient overcurrent	ON	H	N/A
Circuit-breaker (persistent overcurrent followed by OC_TIMER expiry)	OFF	L	t_{OC_TIMER} + t_{PGD}
Fast-trip	OFF	L (V_{OUT} < VOUT_PGTH) H (V_{OUT} > VOUT_PGTH)	t_{PGD} N/A
Overtemperature	Shutdown	L	t_{PGD}

After power up, PG is pulled low initially. The device initiates an inrush sequence in which the gate driver circuit starts charging the gate capacitance from the internal charge pump. When the FET gate voltage reaches the full overdrive indicating that the inrush sequence is complete and the device is capable of delivering full power, the PG pin is asserted high after a de-glitch time (t_{PGA}). The PG assertion delay can be optionally increased by setting the PG_DVDT_DLY bit in the DEVICE_CONFIG register.

The PG is de-asserted if the output voltage falls below a threshold at any point during normal operation or the device detects a fault (except short-circuit). The PG de-assertion threshold can be digitally programmed through the VOUT_PGTH register. The PG de-assertion de-glitch time is t_{PGD}.

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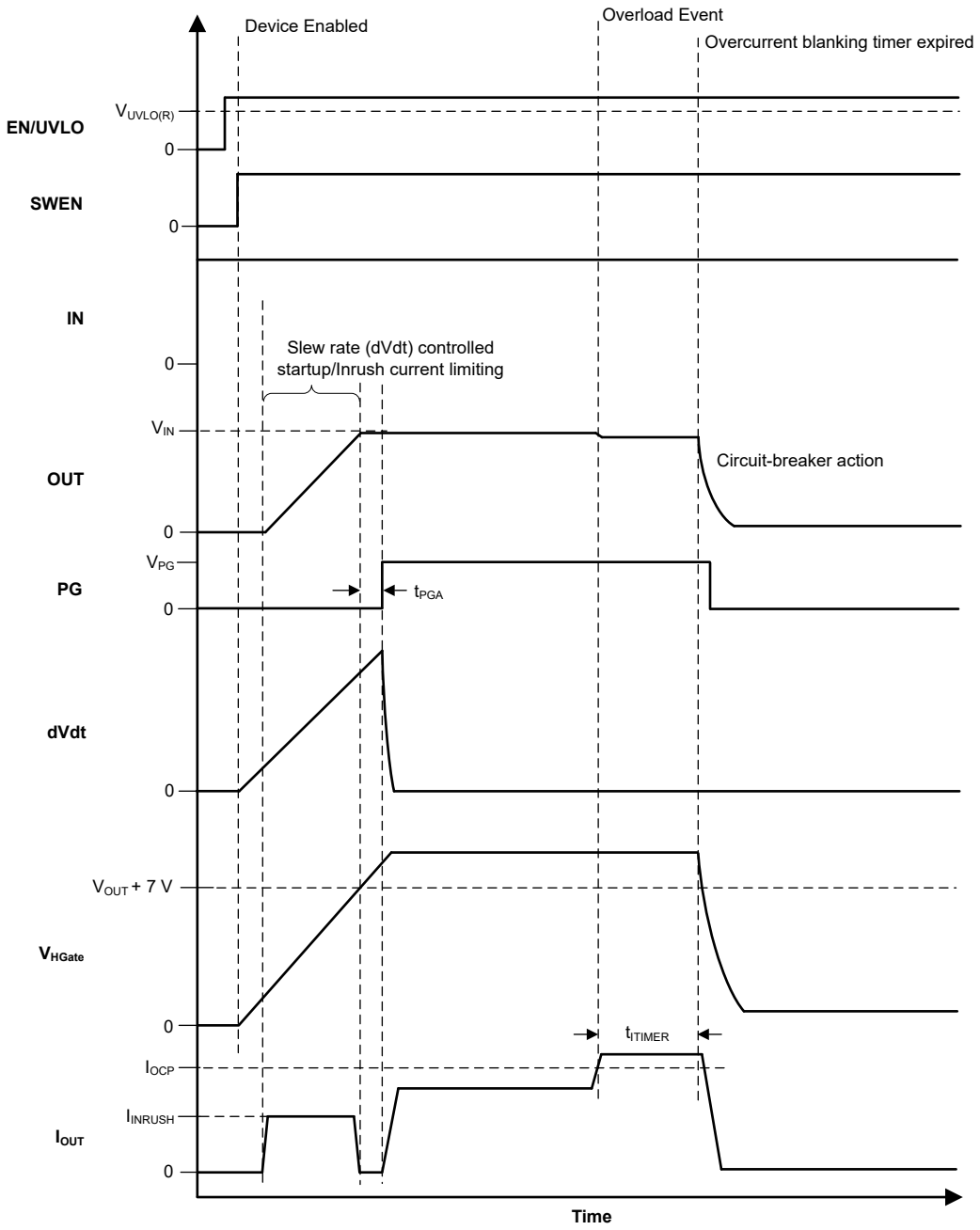

Figure 6-7. TPS1689 PG Timing Diagram

The PG is an open-drain pin and must be pulled up to an external supply.

Note

When there is no supply to the device, the PG pin is expected to stay low. However, there is no active pulldown in this condition to drive this pin all the way down to 0 V. If the PG pin is pulled up to an independent supply which is present even if the device is unpowered, there can be a small voltage seen on this pin depending on the pin sink current, which is a function of the pullup supply voltage and resistor. Minimize the sink current to keep this pin voltage low enough not to be detected as a logic HIGH by associated external circuits in this condition.

6.3.10.3 Parallel Device Synchronization (SWEN)

The SWEN pin is a signal which is driven high when the FET needs to be driven to ON state. When it is driven low (internally or externally), it forces the driver circuit to keep the FET in OFF condition. In a parallel eFuse system, this pin is used by the TPS1689 primary controller to control the other eFuses. It also allows multiple devices in a parallel configuration to synchronize the ON/OFF transitions.

Table 6-4. SWEN Summary

Device State	FET Driver Status	SWEN
Steady-state	ON	H
Inrush	ON	H
Overtemperature shutdown	OFF	L
Auto-retry timer running	OFF	L
Device disabled (V_{EN} < V_{UVLO})	OFF	L
VIN Undervoltage (V_{IN} < V_{UVP} or V_{IN} < VIN_UV_FLT)	OFF	L
VDD Undervoltage (V_{DD} < V_{UVP})	OFF	L
Insertion delay	OFF	L
VIN Overvoltage (V_{IN} > VIN_OV_FLT)	OFF	L
Transient overcurrent	ON	H
Circuit-breaker (persistent overcurrent followed by OC_TIMER expiry)	OFF	L
Fast-trip	OFF	L
Fast-trip response mono-shot running (DEVICE_CONFIG[13] = 1)	OFF	L
Fast-trip response mono-shot expired (DEVICE_CONFIG[13] = 1)	ON	H
FET health fault	OFF	L
External fault (SWEN pulled low by secondary device in parallel chain)	OFF	L (held low by TPS1689 even if secondary device releases the pull down after some time)
Single Point Failure(IMON/IREF)	OFF	L

The SWEN is an open-drain pin and has an internal pull-up to internal power supply.

The SWEN pin has an internal timeout circuit. If the SWEN is held low (internally or externally) for an extended period of time (tSWENTO), it resets the logic (FAST_REC = 0) so that the next time the device starts up after SWEN goes high, it follows the normal inrush sequence. In other cases, it may bypass the inrush sequence and perform a current limited startup for fast recovery.

In a primary and secondary parallel configuration, the SWEN pin is used by the primary device to control the ON and OFF transitions of the secondary devices. At the same time, it allows the secondary devices to communicate any faults or other conditions which can prevent it from turning on the primary device.

To maintain state machine synchronization, the devices rely on SWEN level transitions as well as timing for handshakes. This ensures all the devices turn ON and OFF synchronously and in the same manner (for example, dVdt controlled or current limited start-up). There are also fail-safe mechanisms in the SWEN control and handshake logic to ensure the entire chain is turned off safely even if the primary device is unable to take control in case of a fault.

Note

TI recommends to keep the parasitic loading on the SWEN pin to a minimum to avoid synchronization timing issues.

6.3.11 Stacking Multiple eFuses for Unlimited Scalability

For systems needing higher current than supported by a single TPS1689, it is possible to connect TPS1689 in parallel with one or more TPS1685x devices to deliver the desired total system current. Conventional eFuses do not share current evenly between themselves during steady-state due to mismatches in the path resistances (which includes the individual device R_{DSON} variation from part to part, as well as the parasitic PCB trace resistance). This fact can lead to multiple problems in the system:

1. Some devices always carry higher current as compared to other devices, which can result in accelerated failures in those devices and an overall reduction in system operational lifetime.
2. As a result, thermal hotspots form on the board, devices, traces, and vias carrying higher current, leading to reliability concerns for the PCB. In addition, this problem makes thermal modeling and board thermal management more challenging for designers.
3. The devices carrying higher current can hit their individual circuit-breaker threshold prematurely even while the total system load current is lower than the overall circuit-breaker threshold. This action can lead to false tripping of the eFuse chain during normal operation. This has the effect of lowering the current-carrying capability of the parallel chain. In other words, the current rating of the parallel eFuse chain needs to be de-rated as compared to the sum of the current ratings of the individual eFuses. This de-rating factor is a function of the path resistance mismatch, the number of devices in parallel, and the individual eFuse circuit-breaker accuracy.

The need for de-rating has an adverse impact on the system design. The designer is forced to make one of these trade-offs:

1. Limit the operating load current of the system to below the derated overcurrent threshold of the eFuse chain. Essentially, it means lower platform capabilities than are supported by the power supply (PSU).
2. Increase the overall circuit-breaker threshold to allow the desired system load current to pass through without tripping. As a consequence, the power supply (PSU) must be oversized to deliver higher currents during faults to account for the degradation of the overall circuit-breaker accuracy.

In either case, the system suffers from poor power supply utilization, which can mean sub-optimal system throughput or increased installation and operating costs, or both.

The TPS1689 and TPS1685x devices use a proprietary technique to address these problems and provide unlimited scalability by paralleling as many eFuses as needed. This is incorporated without significant current imbalance or any degradation in accuracy.

For this scheme to work correctly, the devices must be connected in the following manner:

- The SWEN pins of all the devices are connected together.
- The IMON pins of all the devices need to be connected together. The R_{IMON} resistor value on the combined IMON pin can be calculated using Equation 9.

$$R_{IMON} = \frac{V_{IREF}}{G_{IMON} \times I_{OCP(TOTAL)}} \quad (9)$$

- The IREF pins of all the devices need to be connected together. The TPS1689 generates the V_{IREF} reference voltage for the whole chain using its internal DAC which can be programmed using PMBus® writes to the VIREF register. This allows the overcurrent protection thresholds to be dynamically adjusted during system operation. It is also possible to drive the IREF pin using a low impedance external precision voltage reference.
- The start-up current limit and active current sharing threshold for each device is fixed to $I_{start\text{-}up}$. Each device will limit it to this value should the current try to exceed $I_{start\text{-}up}$.

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Note

1. The active current sharing scheme is engaged when the current through any eFuse while in steady-state exceeds the individual current sharing threshold set by the R_{ILIM} based on Equation 10.

$$R_{ILIM} = \frac{1.1 \times V_{IREF}}{3 \times G_{ILIM} \times I_{LIM(ACS)}} \quad (10)$$

2. The active current sharing scheme is disengaged when the total system current exceeds the system overcurrent (circuit-breaker) threshold ($I_{OCP(TOTAL)}$).

6.3.11.1 Current Balancing During Start-Up

The TPS1689 implements a proprietary current balancing mechanism during start-up, which allows TPS1689 and TPS1685x devices connected in parallel to share the inrush current and distribute the thermal stress across all the devices. This feature helps to complete a successful start-up with all the devices and avoid a scenario where some of the eFuses hit thermal shutdown prematurely. This in effect increases the inrush current capability of the parallel chain. The improved inrush performance makes it possible to support very large load capacitors on high current platforms without compromising the inrush time or system reliability.

6.3.12 Quick Output Discharge(QOD)

The TPS1689 has an integrated output discharge function which discharges the capacitors on the OUT pin using an internal constant current (I_{QOD}) sink path to GND. The output discharge function is activated when the EN/UVLO is held low ($V_{SD(F)} < V_{EN} < V_{UVLO(F)}$) for a minimum interval (t_{QOD}). The output discharge function helps to rapidly remove the residual charge left on large output capacitors and prevents the bus from staying at some undefined voltage for extended periods of time. The output discharge is disengaged when $V_{OUT} < V_{FB}$ or if the device detects a fault.

The output discharge function can result in excessive power dissipation inside the device leading to an increase in junction temperature (T_J). The output discharge is disabled if the junction temperature (T_J) crosses the device overtemperature threshold (TSD) to avoid long-term degradation of the part.

Note

In a primary and secondary parallel eFuse configuration, TI recommends to hold EN/UVLO voltage below the $V_{UVLO(F)}$ threshold of the secondary eFuse to activate output discharge for all the eFuses in the chain.

6.3.13 Write Protect Feature(WP#)

WP# allows for pin control to disable PMBUS write access for enhanced protection. In addtion to the software control via PMBUS register MFR_WRITE_PROTECT, this provides a hardware pin control to disable write access to PMBUS. The pin control has higher priority than the MFR_WRITE_PROTECT register. Connecting the WP# pin to ground disables write access to PMBUS registers. If this pin is floating, the MFR_WRITE_PROTECT register controls write access to PMBUS registers.

6.3.14 PMBus® Digital Interface

The TPS1689 is a PMBus® target device with an embedded digital telemetry controller block. This enables bi-directional communication with a host controller using a pre-defined set of commands to control, configure, monitor and debug the system.

The TPS1689 is compliant with PMBus® specifications version 1.3 Part I and Part II.

6.3.14.1 PMBus® Device Addressing

The TPS1689 uses 7-bit I2C device addressing. Up to 25 different addresses can be generated using different pin-strapping combinations on the ADDR0 and ADDR1 pins as shown in Table 6-5. This allows multiple devices to be connected to the same I2C bus.

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Table 6-5. TPS1689 PMBus® Address Decoding

ADDR0 Pin	ADDR1 Pin	PMBus® Device Address
Open	Open	0x40 (Default). Can be overwritten with a user defined address programmed into PMBUS_ADDR register in the Config NVM space.
Open	GND	0x41
Open	75 kΩ to GND	0x42
Open	150 kΩ to GND	0x43
Open	267 kΩ to GND	0x44
GND	Open	0x45
GND	GND	0x46
GND	75 kΩ to GND	0x47
GND	150 kΩ to GND	0x48
GND	267 kΩ to GND	0x49
75 kΩ to GND	Open	0x4A
75 kΩ to GND	GND	0x4B
75 kΩ to GND	75 kΩ to GND	0x4C
75 kΩ to GND	150 kΩ to GND	0x4D
75 kΩ to GND	267 kΩ to GND	0x4E
150 kΩ to GND	Open	0x50
150 kΩ to GND	GND	0x51
150 kΩ to GND	75 kΩ to GND	0x52
150 kΩ to GND	150 kΩ to GND	0x53
150 kΩ to GND	267 kΩ to GND	0x54
267 kΩ to GND	Open	0x55
267 kΩ to GND	GND	0x56
267 kΩ to GND	75 kΩ to GND	0x57
267 kΩ to GND	150 kΩ to GND	0x58
267 kΩ to GND	267 kΩ to GND	0x59

Note

1. TI recommends using low tolerance resistors on ADDR0 and ADDR1 to avoid address decoding errors.
2. TI recommends connecting 10 pF capacitors in parallel with resistors on ADDR0 and ADDR1 pins to improve noise immunity for correct address decoding.

6.3.14.2 SMBus™ Protocol

TPS1689 PMBus® interface is implemented over SMBus protocol using an I2C physical interface (SCL, SDA) for robust link. The following features are supported:

- Fast mode support (up to 1 MHz I2C clock speed)
- Bus timeout
- Support for Byte, Word and Block Read/Write with and without PEC

- Group command support
- SMBus Alert output pin (SMBA#) to alert/interrupt the host during certain system warning/fault events.
- Alert Response Address (ARA) support

6.3.14.3 SMBus™ Message Formats

TPS1689 supports the following SMBus message formats.

Note

All these commands can be used with or without the optional PEC byte.

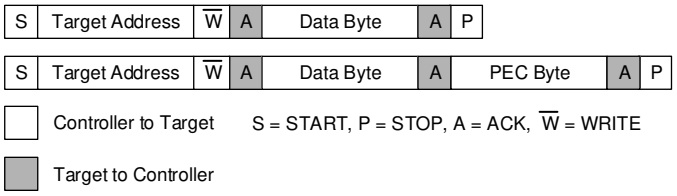

Figure 6-8. Send Byte

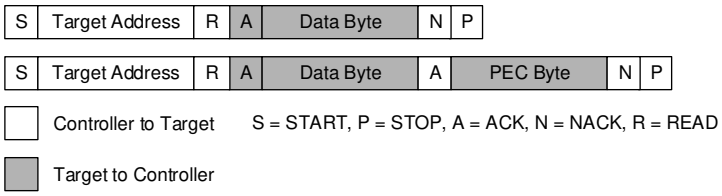

Figure 6-9. Receive Byte

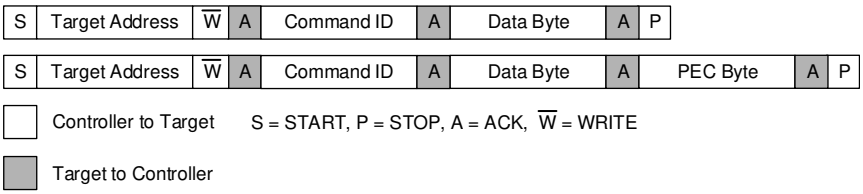

Figure 6-10. Write Byte

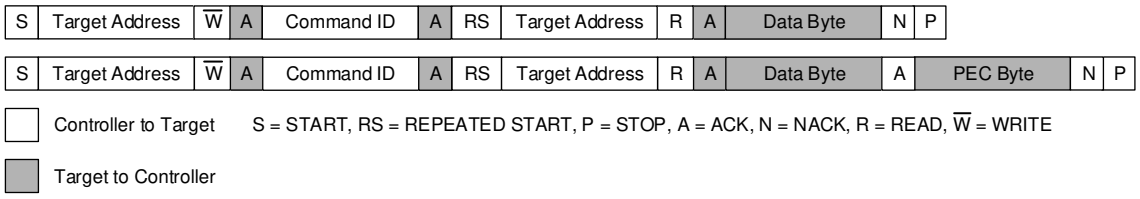

Figure 6-11. Read Byte

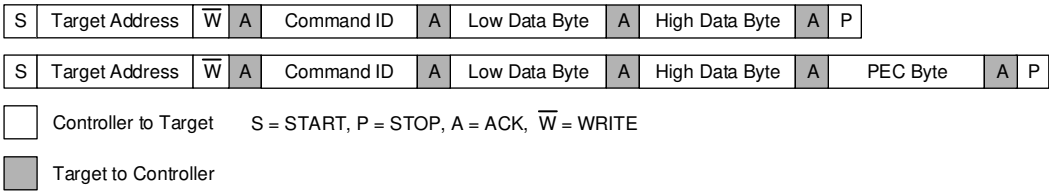

Figure 6-12. Write Word

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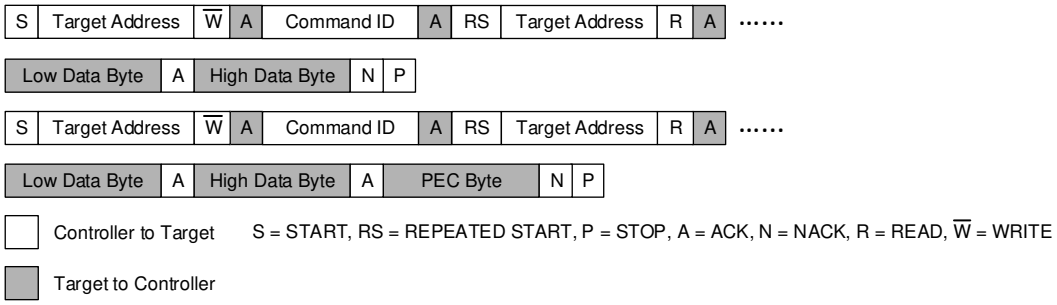

Figure 6-13. Read Word

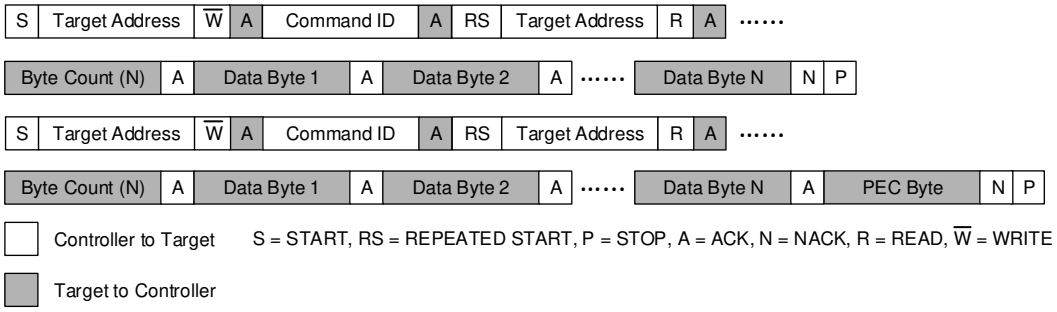

Figure 6-14. Block Read

6.3.14.4 Packet Error Checking

TPS1689 supports optional PEC for all SMBus transactions.

When using packet error checking, an additional byte is added before the stop bit in each transaction.

For reads, the PEC byte is read from the target and the controller compares it to its own PEC byte calculation. For writes, the PEC byte is sent to the target from the controller, and the target compares it to its own PEC byte calculation.

After the comparison, if the PEC bytes differ, the target detects a PEC error. Thereafter, it takes the following actions as per the PMBus® Specification:

- Does not respond to or act upon the command
- Flushes the command code and any received data
- Sets the CML_ERR bit in the STATUS_BYTE register
- Sets the INV_PEC bit in the STATUS_CML register

and

- Notifies the controller of a fault condition by pulling the SMBA# line low

6.3.14.5 Group Commands

As required by PMBus® specification, TPS1689 supports the Group Command Protocol. The Group Command Protocol is used to send commands to more than one PMBus® target device. The commands are sent in one continuous transmission. When the target devices detect the STOP condition that ends the sending of commands, they all begin executing the command they received.

It is not necessary that all target devices receive the same command.

No more than one command can be sent to any one device in one Group Command packet.

The Group Command Protocol must not be used with commands that require the receiving device to respond with data, such as the STATUS_BYTE command.

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The Group Command Protocol uses REPEATED START conditions to separate commands for each device. The Group Command Protocol begins with the START condition, followed by the seven bit address of the first target device to receive a command and then by the write bit zero (0). The secondary device ACKs and the host controller sends a command with the associated data byte or bytes.

After the last data byte is sent to the first device, the host controller does NOT send a STOP condition. Instead, it sends a REPEATED START condition, followed by the seven bit address of the second device to receive a command, a write bit and the command code and the associated data bytes.

If, and only if, this is the last target device to receive a command, the host controller sends a STOP condition. Otherwise, the host controller sends a REPEATED START condition and starts transmitting the address of the third device to receive a command.

This process continues until all target devices have received their command codes, data bytes, and if used and supported, PEC byte. Then when all target devices have received their information, the host controller sends a STOP condition.

If PEC is used, then each target device's sub-packet has its own PEC byte, computed only for that device's sub-packet, including that target device's address.

When the target devices who have received a command through this protocol detect the STOP condition, they are to begin execution immediately of the received command.

When using Packet Error Checking with the Group Command Protocol, the PEC byte is calculated using only the address, command and data bytes for each target device. For example, PEC 1 is calculated using Device Address 1 including the Write bit, Command Code 1, and the data associated with Command Code 1. PEC 1 need only be calculated by the device at Device Address 1.

Similarly, PEC Byte 2 is calculated using Device Address 2 including the Write bit, Command Code 2, and the data associated with Command Code 2. Device 1 must not continue calculating PEC 1 after it sees the Repeated Start.

6.3.14.6 SMBus™ Alert Response Address (ARA)

When there are multiple target devices on the bus with their SMBA# pins also tied together, if one or more target devices assert the SMBA#, the host controller needs a way to identify those target devices on the bus. It does so using the ARA mechanism, which is initiated by sending a read command to the ARA broadcast address 0x0C.

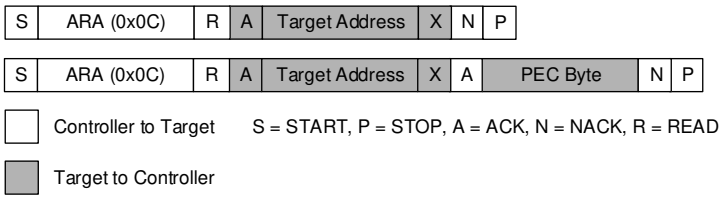

Figure 6-15. ARA Message Protocol

The ARA Automatic Mask is a mask that is set in response to a successful ARA read. An ARA read operation returns the PMBus® address of the lowest addressed target device on the bus that has its SMBA# asserted. A successful ARA read means that this target device was the one that returned its address. When a target device responds to the ARA read, it releases the SMBA# signal. When the last target device on the bus that has an SMBA# set has successfully reported its address, the SMBA# signal will de-asserted.

The way that the TPS1689 releases the SMBA# signal is by setting the ARA Automatic mask bit for all fault conditions present at the time of the ARA read. All status registers will still show the fault condition, but it will not generate an SMBA# alert on that fault again until the ARA Automatic mask is cleared by the host issuing the CLEAR_FAULTS command to this part. This must be done as a routine part of servicing an SMBA# condition on a part, even if the ARA read is not done.

For list of PMBUS commands please refer to the attached accompanying PDF

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6.3.14.7 PMBus® Commands

Table 6-6 shows the list of PMBus® commands supported by the TPS1689 eFuse.

Table 6-6. TPS1689 PMBus® Commands List

Command Name	Code	Type	Description	PMBus®Transaction	Default Value	Stored in On-chip Non-volatile Memory	Stored in EEPROM
OPERATION	01h	Control	eFuse ON/OFF control	Read/Write byte w/ PEC	0x80	N/A	N/A
CLEAR_FAULTS	03h	Control	Clear all fault status bits and Blackbox RAM	Send byte w/ PEC	N/A	N/A	N/A
RESTORE_FACTORY_DEFAULTS	12h	Control	Initialize/Reset all configuration registers to their factory default values	Send byte w/ PEC	N/A	N/A	N/A
STORE_USER_ALL	15h	Control	Store configuration values to NVM/EEPROM	Send byte w/ PEC	N/A	N/A	N/A
RESTORE_USER_ALL	16h	Control	Initialize all configuration registers with the user programmed values stored in NVM/EEPROM	Send byte w/ PEC	N/A	N/A	N/A
BB_ERASE	F5h	Control	Erase Blackbox data in external EEPROM	Send byte w/ PEC	N/A	N/A	N/A
FETCH_BB_EEPROM	F6h	Control	Fetch Blackbox EEPROM contents into internal shadow registers	Send byte w/ PEC	N/A	N/A	N/A
CLEAR_BB_RAM	FCh	Control	Clears the contents of bbox RAM	Send byte w/ PEC	N/A	N/A	N/A
POWER_CYCLE	D9h	Control	Power down output and restart after a delay programmed through the RETRY_CONFIG register	Send byte w/ PEC	N/A	N/A	N/A
MFR_WRITE_PROTECT	F8h	Control	Enable/Disable write protection for OPERATION & POWER_CYCLE commands, configuration registers, NVM, and EEPROM	Read/write byte w/ PEC	0x00	N/A	N/A
CAPABILITY	19h	Telemetry	Supported PMBus® features	Read byte w/ PEC	0xD0	Y	N
STATUS_BYTE	78h	Telemetry	Status register lower byte	Read byte w/ PEC	Undefined	N	N
STATUS_WORD	79h	Telemetry	Status register word	Read word w/ PEC	Undefined	N	Y
STATUS_OUT	7Ah	Telemetry	OUT bus status	Read byte w/ PEC	Undefined	N	N
STATUS_IOUT	7Bh	Telemetry	OUT current status	Read byte w/ PEC	Undefined	N	N
STATUS_INPUT	7Ch	Telemetry	IN bus status	Read byte w/ PEC	Undefined	N	Y
STATUS_TEMP	7Dh	Telemetry	Device temperature status	Read byte w/ PEC	Undefined	N	N
STATUS_CML	7Eh	Telemetry	Communications, Memory, Logic status	Read byte w/ PEC	Undefined	N	N

Table 6-6. TPS1689 PMBus® Commands List (continued)

Command Name	Code	Type	Description	PMBus®Transaction	Default Value	Stored in On-chip Non-volatile Memory	Stored in EEPROM
STATUS_MFR_SPECIFIC	80h	Telemetry	Manufacturer specific fault status	Read byte w/ PEC	Undefined	N	Y
STATUS_MFR_SPECIFIC_2	F3h	Telemetry	Additional manufacturer specific fault status	Read word w/ PEC	Undefined	N	N
PMBUS_REVISION	98h	Telemetry	PMBus® Specifications Part I and II rev 1.3	Read byte w/ PEC	0x33	Y	N
MFR_ID	99h	Telemetry	Manufacturer name	Block read 2 bytes w/ PEC	"TI"	Y	N
MFR_MODEL	9Ah	Telemetry	Device name	Block read 8 bytes w/ PEC	"TPS1689"	Y	N
MFR_REVISION	9Bh	Telemetry	Device revision	Block read 1 byte w/ PEC	0x01	Y	N
READ_VIN	88h	Telemetry	Input voltage	Read word w/ PEC	Undefined	N	N
READ_VOUT	8Bh	Telemetry	Output voltage	Read word w/ PEC	Undefined	N	N
READ_IIN	89h	Telemetry	Input current	Read word w/ PEC	Undefined	N	N
READ_TEMPERATURE_1	8Dh	Telemetry	Device temperature	Read word w/ PEC	Undefined	N	N
READ_VAUX	D0h	Telemetry	Auxiliary analog input voltage	Read word w/ PEC	Undefined	N	N
READ_PIN	97h	Telemetry	Instantaneous input power	Read word w/ PEC	Undefined	N	N
READ_EIN	86h	Telemetry	Accumulated input energy	Block read 6 bytes w/ PEC	Undefined	N	N
READ_VIN_AVG	DCh	Telemetry	Average input voltage	Read word w/ PEC	Undefined	N	N
READ_VIN_MIN	D1h	Telemetry	Minimum input voltage	Read word w/ PEC	Undefined	N	N
READ_VIN_PEAK	D2h	Telemetry	Peak input voltage	Read word w/ PEC	Undefined	N	Y
READ_VOUT_AVG	DDh	Telemetry	Average output voltage	Read word w/ PEC	Undefined	N	N
READ_VOUT_MIN	DAh	Telemetry	Minimum output voltage	Read word w/ PEC	Undefined	N	N
READ_IIN_AVG	DEh	Telemetry	Average input current	Read word w/ PEC	Undefined	N	N
READ_IIN_PEAK	D4h	Telemetry	Peak input current	Read word w/ PEC	Undefined	N	Y
READ_TEMP_AVG	D6h	Telemetry	Average device temperature	Read word w/ PEC	Undefined	N	N
READ_TEMP_PEAK	D7h	Telemetry	Peak device temperature	Read word w/ PEC	Undefined	N	Y
READ_PIN_AVG	DFh	Telemetry	Average input power	Read word w/ PEC	Undefined	N	N
READ_PIN_PEAK	D5h	Telemetry	Peak input power	Read word w/ PEC	Undefined	N	N

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Table 6-6. TPS1689 PMBus® Commands List (continued)

Command Name	Code	Type	Description	PMBus®Transaction	Default Value	Stored in On-chip Non-volatile Memory	Stored in EEPROM
READ_SAMPLE_BUF	D8h	Telemetry	ADC sample buffer	Block read 64 bytes w/ PEC	Undefined	N	N
READ_BB_RAM	FDh	Telemetry	Blackbox RAM registers	Block read 7 bytes w/ PEC	Undefined	N	Y
READ_BB_EEPROM	F4h	Telemetry	Blackbox EEPROM content	Block read 16 bytes w/ PEC	Undefined	N	Y
BB_TIMER	FAh	Telemetry	Blackbox tick timer	Read byte w/ PEC	Undefined	N	Y
PMBUS_ADDR	FBh	Configuration	PMBus® device address for ADDR0 = Open and ADDR1 = Open setting	Read/write byte w/ PEC	0x40	Y	Y
VIN_UV_WARN	58h	Configuration	Input undervoltage warning threshold	Read/write word w/ PEC	0x0095	N	N
VIN_UV_FLT	59h	Configuration	Input undervoltage fault threshold	Read/write word w/ PEC	0x008D	Y	Y
VIN_OV_WARN	57h	Configuration	Input overvoltage warning threshold	Read/write word w/ PEC	0x00A5	N	N
VIN_OV_FLT	55h	Configuration	Input overvoltage fault threshold	Read/write word w/ PEC	0x000E	Y	Y
VOUT_UV_WARN	43h	Configuration	Output undervoltage warning threshold	Read/write word w/ PEC	0x0095	N	N
VOUT_PGTH	5Fh	Configuration	Output threshold for Power Good de-assertion	Read/write word w/ PEC	0x008D	Y	Y
OT_WARN	51h	Configuration	Overtemperature warning threshold	Read/write word w/ PEC	0x007E	N	N
OT_FLT	4Fh	Configuration	Overtemperature fault threshold	Read/write word w/ PEC	0x0085	Y	Y
PIN_OP_WARN	6Bh	Configuration	Input overpower warning threshold	Read/write word w/ PEC	0x00FF	N	N
IIN_OC_WARN	5Dh	Configuration	Input overcurrent warning threshold	Read/write word w/ PEC	0x00FF	N	N
VIREF	E0h	Configuration	Reference voltage for current regulation and protection blocks	Read/write byte w/ PEC	0x32	Y	Y
AUX/TEMP/EEDATA/EECLK/GPIOx configuration	E1h	Configuration	AUX/EEDATA/GPIO2 & AUX/EECLK/GPIO1 pin configuration	Read/write byte w/ PEC	0x00	Y	Y
SMBA_FLTb_CONFIG	E2h	Configuration	SMBA/FLTb pin configuration	Read/write byte w/ PEC	0x00	Y	Y
ALERT_MASK	DBh	Configuration	SMB Alert assertion mask	Read/write word w/ PEC	0x0100	N	N

Table 6-6. TPS1689 PMBus® Commands List (continued)

Command Name	Code	Type	Description	PMBus®Transaction	Default Value	Stored in On-chip Non-volatile Memory	Stored in EEPROM
FAULT_MASK	E3h	Configuration	$\overline{\text{FLT}}$ assertion mask	Read/write word w/ PEC	0x0000	Y	Y
DEVICE_CONFIG	E4h	Configuration	Device configuration	Read/write word w/ PEC	0x1400	Y	Y
BB_CONFIG	E5h	Configuration	Blackbox configuration	Read/write byte w/ PEC	0x00	Y	Y
OC_TIMER	E6h	Configuration	Transient overcurrent blanking timer	Read/write byte w/ PEC	0x14	N	N
RETRY_CONFIG	E7h	Configuration	Auto-retry configuration	Read/write byte w/ PEC	0x84	Y	Y
ADC_CONFIG_1	E8h	Configuration	ADC Configuration	Read/write byte w/ PEC	0x00	N	N
ADC_CONFIG_2	E9h	Configuration	ADC Configuration	Read/write byte w/ PEC	0x00	N	N
PK_MIN_AVG	EAh	Configuration	Peak/Min/Average configuration	Read/write byte w/ PEC	0x00	N	N
PSU_VOLTAGE	ECh	Configuration	PSU nominal voltage	Read/write byte w/ PEC	0x9D	N	N
INS_DLY	F9h	Configuration	Insertion delay	Read/write byte w/ PEC	0x00	Y	Y
IMON OFFSET CALIBRATION	F2h	Configuration	Configuration for IMON offset	Read/write byte	0x00	Y	Y
LOAD_IMON_OFFSET	CAh		NA		0x00	Y	Y
USER DATA	F7h	Configuration	User stored generic data		0x00	Y	Y

6.3.14.8 Analog-to-digital Converter

The TPS1689 integrates a 10-bit, 460 KSPS SAR ADC preceded by an analog MUX. The following signals are available for sampling by the ADC:

1. VIN
2. VOUT
3. VIMON
4. VTEMP
5. VAUX
6. ADDR0
7. ADDR1

The ADC uses a 5kHz low-pass filter at the input to suppress high frequency noise (outside the ADC Nyquist bandwidth) and prevent aliasing.

Note

The ADC also supports a high performance mode wherein the sampling rate is traded off in favor of improved DNL and INL. In this mode, the sampling rate is reduced to 270 KSPS. This mode can be selected by setting the ADC_HI_PERF bit in the DEVICE_CONFIG register.

During normal operation, the ADC automatically sequences the channels. The ADC channel sequencer manages MUX channel selection for sampling.

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Note

- The ADDR0 and ADDR1 signals are sampled only at startup to decode the PMBus® target address.
- The ADC implements background self-calibration to eliminate offset and gain errors inherent to the ADC.

The device also supports buffering of multiple samples of a selected parameter in RAM, which can be read by the host using the ADC_SAMPLE_BUF block read command. This allows the system designer to reconstruct the time domain profile/waveform of that parameter in a given interval. This can be useful during design/debugging by functioning like an in-built "digital oscilloscope". The ADC channel to sample for buffering and the decimation rate/sample skip count can be user configured using PMBus® writes to the ADC_CONFIG_2 register.

The TPS1689 can post-process raw ADC sampled data to compute the following derived parameters:

1. VIN Average
2. VIN Peak
3. VIN Min
4. VOUT Average
5. VOUT Min
6. IIN Average
7. IIN Peak
8. PIN
9. PIN Average
10. PIN Peak
11. EIN
12. Temperature Average
13. Temperature Peak

A single ADC sample can have higher errors due to internal noise. It’s possible to improve the ADC SNR and the telemetry accuracy by averaging higher number of samples. The number of samples to be averaged is user-programmable using the PK_MIN_AVG register. The minimum, maximum, and average values can also be reset using the PK_MIN_AVG register.

The TPS1689 performs digital comparison on the ADC sampled data to detect the following system events.

1. VIN UV WARN
2. VIN UV FAULT
3. VIN OV WARN
4. VOUT PGOOD
5. IIN OC WARN
6. OT WARN
7. OT FAULT
8. PIN OP WARN

The results of the comparisons are reflected in the PMBus® status registers and can be configured to trigger other actions e.g. FET turn OFF (protection response) and $\overline{\text{FLT}}$ output assertion for faults, SMBA# signal assertion for faults/warnings and Blackbox RAM/EEPROM update.

6.3.14.9 Digital-to-analog Converters

The TPS1689 integrates multiple DACs which are used to set the thresholds or gains of various blocks:

1. **VIREF:** This is a 6-bit buffered voltage output DAC which provides a programmable threshold for overcurrent protection, short-circuit protection and active current sharing blocks. This can be programmed using the VIREF register. This signal is available internally always for these blocks, and optionally can be brought on the IREF pin to drive other devices in a parallel chain.
2. **IDVDT:** This is a 2-bit current output DAC which sources current on the DVDT pin to provide output Slew Rate (DVDT) control. This can be programmed using the DEVICE_CONFIG[10:9] register bits.

3. **VOV:** This is a 8-bit DAC which provides a programmable threshold for the VIN overvoltage protection comparator. This can be programmed using the VIN_OV_FLT register.

6.3.14.10 DIRECT format Conversion

For telemetry and configuration parameters, the TPS1689 supports DIRECT format. Digital codes for telemetry or configuration parameters can be converted to their equivalent real world units using Equation 11 and Equation 12.

- **Interpreting received values:**

  The host system uses Equation 11 to convert the value received from the PMBus® device into a reading of V, A, °C, or W:

$$X = \frac{1}{m}\left(Y \times 10^{-R} - b\right) \quad (11)$$

  Where:

  – X, is the calculated, “real world” value in the appropriate units (V, A, °C, or W);
  – m, the slope coefficient, is a two byte, two’s complement integer;
  – Y, is a two byte two’s complement integer received from the PMBus® device;
  – b, the offset, is a two byte, two’s complement integer; and
  – R, the exponent, is a one byte, two’s complement integer.

- **Sending a value:**

  To send a value, the host must use Equation 12 to find the value of Y:

$$Y = (mX + b) \times 10^{R} \quad (12)$$

  Where:

  – Y is the two byte two’s complement integer to be sent to the unit;
  – m, the slope coefficient, is the two byte, two’s complement integer;
  – X, a “real world” value, in units such as V, A, °C, or W, to be converted for transmission;
  – b, the offset, is the two byte, two’s complement integer; and
  – R, the exponent, is the decimal value equivalent to the one byte, two’s complement integer.

Table 6-7. TPS1689 PMBus® DIRECT format Conversion Guide

Parameter	Units	Zero Code Analog Value	Full scale Digital Code	Full-scale Analog Value	m	b	R
READ_VIN	V	0	0x3FF	87.75	1166	0	- 2
VIN_UV_FLT	V	0	0xFF	87.75	2906	0	- 3
VIN_UV_WARN	V	0	0xFF	87.75	2906	0	- 3
VIN_OV_WARN	V	16	0xFF	87.75	3554	−56864	- 3
VIN_OV_FLT	V	16	0xFF	80.00	3984	− 63750	- 3
READ_VOUT	V	0	0x3FF	87.75	1166	0	- 2
VOUT_UV_WARN	V	0	0xFF	87.75	2906	0	- 3
VOUT_PGTH	V	0	0xFF	87.75	2906	0	- 3
VAUX	V	0	0x3FF	1.95	5251	0	- 1
READ_VTEMP	°C	− 229.3	0x3FF	501.40	140	32103	- 2
OT_WARN	°C	− 228.7	0xFF	499.80	35	8005	- 2
OT_FLT	°C	− 228.7	0xFF	499.80	35	8005	- 2
VIMON	V	0	0x3FF	1.95	5251	0	- 1

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Table 6-7. TPS1689 PMBus® DIRECT format Conversion Guide (continued)

Parameter	Units	Zero Code Analog Value	Full scale Digital Code	Full-scale Analog Value	m	b	R
READ_IOUT	A	0	0x3FF	42.02	24347	0	- 3
OC_WARN	A	0	0xFF	42.02	6069	0	- 3
VIREF	V	0.3	0x3F	1.19	7111	– 2133	- 2
PSU_VOLTAGE	V	0	0xFF	85.00	3000	0	- 3
READ_PIN	W	0	0x3FF	3687.06	2775	0	- 4
PIN_OP_WARN	W	0	0xFF	3687.06	6916	0	- 5
READ_EIN	J	0	0x7FFF	543.68	60	0	0

6.3.14.11 Blackbox Fault Recording

The Blackbox feature greatly enhances the ability of the system designer to debug power path related issues during design/development and in case of field returns. Along with a snapshot of the parametric data and event information through various status registers, the TPS1689 provides additional information which helps to re-create the sequence of events as they occurred in a certain interval of time. This information is available in both the on-chip volatile memory and the external I2C EEPROM (connected on the EECLK/EEDATA pins) and can be accessed through PMBus®.

Note

The PMBus® engine is up and running as soon as a stable supply is available on VDD, independent of VIN and other related internal nodes. This ensures that the Blackbox contents can be read back from a field return unit by applying power on VDD pin even if there's damage on VIN side or Power FET .

During the operation of the device, the Blackbox information is stored inside the Blackbox buffer RAM which is seven (7) bytes deep. At any point of time, issuing the READ_BB_RAM command will retrieve the most recent seven (7) events in a sequence along with the timestamp relative to each other. Each byte of this buffer RAM holds the following information about a single event:

1. A 3-bit event identifier
2. A 5-bit value which indicates the time lapse because the previous event. The lower 4 bits of the timer value represents a snapshot of the free running Blackbox tick timer at the instant of registering the event in the Blackbox RAM. The 5^{th} bit indicates whether the timer has overflowed at least once since the last event.

The event identifier and relative timer information help the system designer to reconstruct a timeline of events as they occurred, thereby enhancing the debug capabilities as compared to viewing a single snapshot of status registers. The Blackbox tick timer is a free running timer which is reset to zero after every event. The timer update rate can be configured through the BB_CONFIG register. This allows the users to make a tradeoff between fine timing resolution and longer time span as per their debug needs. The BB_TMR_EXP bit in the BB_TIMER register indicates if the Blackbox tick timer has overflowed at least since the last event. This bit indicates whether the event entries in the RAM are relatively recent or old. This bit is latched when the timer overflows and reset to zero along with the free running timer when the next event occurs.

Here are the events which will trigger a write to the Blackbox RAM:

1. VIN_UV_WARN
2. VIN_OV_WARN
3. OC_WARN
4. OT_WARN
5. OC_DET
6. IN_OP_WARN

Once the device encounters a global fault or alert event (based on the ALERT_MASK), the Blackbox RAM contents, along with the status registers, peak input voltage, peak input current, peak device temperature, and Blackbox timer values are written to an external EEPROM through the EECLK/EEDATA pins.

Note

The EEPROM interface is a standard I2C controller and operates at 400 kHz clock speed. TI recommends using an I2C EEPROM with minimum 1 Kbits of capacity and 16-byte page addressing. Examples of compatible EEPROM devices include 24LC04, 24AA04, etc.

The contents of the Blackbox RAM along with some status registers (STATUS_WORD, STATUS_MFR_SPECIFIC, and STATUS_INPUT) and certain parameters (VIN_PEAK, IIN_PEAK, and TEMPERATURE_PEAK) are stored into Page-0 of an external EEPROM when the following conditions are met. At the same time, Blackbox RAM contents and Blackbox tick timer values are locked.

1. An external EEPROM is successfully connected by setting the EXT_EEPROM bit high in the DEVICE_CONFIG register. Make sure those two (2) selected GPIO pins are physically connected to the EEPROM clock and data pins respectively on the board.
2. Any one of the three BB EEPROM write trigger bits is set in the BB_CONFIG register.

Blackbox EEPROM contents:

1. BB_RAM_0 to BB_RAM_6 [Seven (7) bytes]
2. BB_TIMER [One (1) byte]
3. STATUS_WORD [Two (2) bytes]
4. STATUS_MFR_SPECIFIC [One (1) byte]
5. STATUS_INPUT [One (1) byte]
6. VIN_PEAK [One (1) byte, Eight (8) MSBs from the 10-bit ADC output data]
7. IIN_PEAK [One (1) byte, Eight (8) MSBs from the 10-bit ADC output data]
8. TEMPERATURE_PEAK [One (1) byte, Eight (8) MSBs from the 10-bit ADC output data]
9. CHECKSUM [One (1) byte]

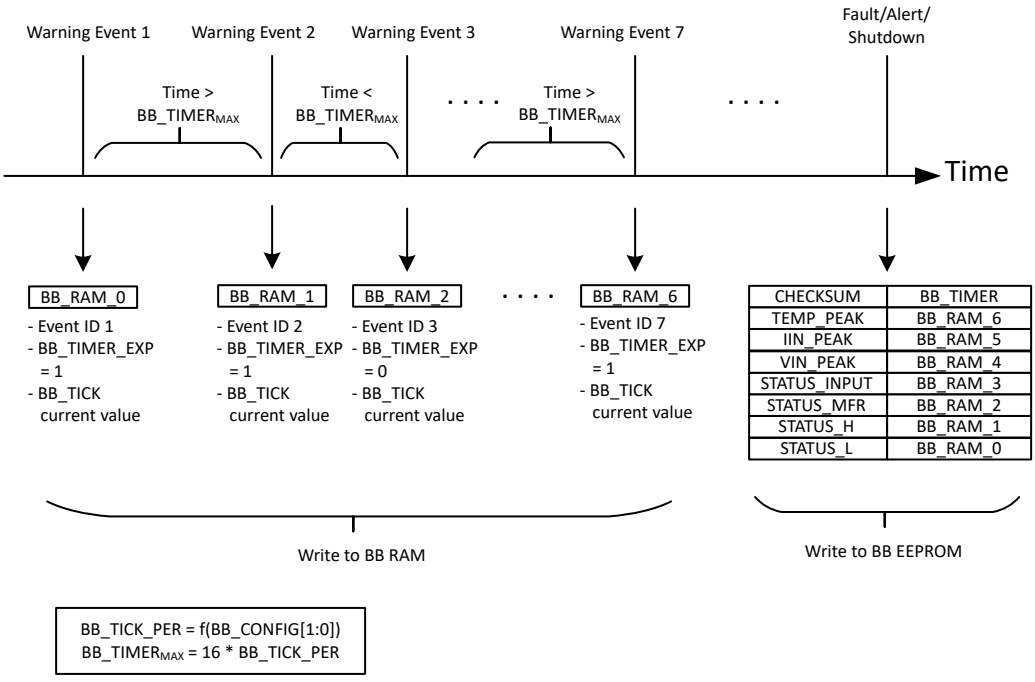

Figure 6-16. Blackbox Operation Example

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6.4 Device Functional Modes

The features of the device depend on the operating mode. Table 6-8 summarizes the device functional modes.

Table 6-8. Device Functional Modes Based on EN/UVLO Pin

Pin Condition	Device State	Output Discharge
EN/UVLO > $V_{UVLO(R)}$	Fully ON	Disabled
$V_{SD(F)}$ < EN/UVLO < $V_{UVLO(F)}$ (time < t_{QOD})	FET OFF	Disabled
$V_{SD(F)}$ < EN/UVLO < $V_{UVLO(F)}$ (time > t_{QOD})	FET OFF	Enabled
EN/UVLO < $V_{SD(F)}$	Shutdown	Disabled

7 Application and Implementation

7.1 Application Information

The TPS1689 is a high-current eFuse that is typically used for input power rail protection and monitoring applications. The device operates from 9V to 80V and supports various user adjustable and programmable protection options. The device provides ability to control inrush current and offers protection against overvoltage, overcurrent, short-circuit and overtemperature conditions. The device can be used in a variety of systems such as server motherboards, add-on cards, graphics cards, accelerator cards, enterprise switches, routers, and so forth. The design procedure explained in the subsequent sections can be used to select the supporting component values based on the application requirements. Additionally, a spreadsheet design tool, *TPS1689x Design Calculator* is available in the web product folder.

7.1.1 Single Device, Standalone Operation

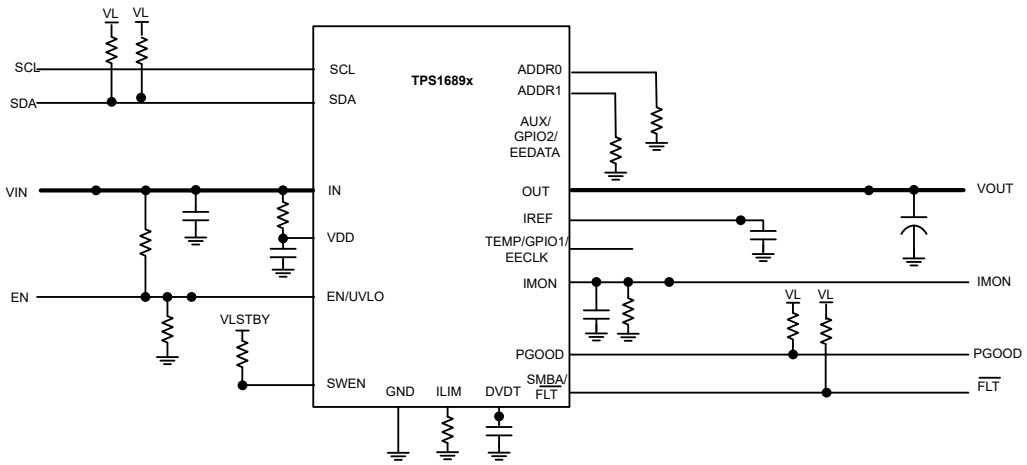

Figure 7-1. Single Device, Standalone Operation

7.1.2 Single TPS1689 and multiple TPS1685 Devices, Parallel Connection

Applications which need higher current input protection along with digital interface for telemetry, control, configurability can use one or more TPS1685 devices in parallel with TPS1689 as shown in Figure 7-2.

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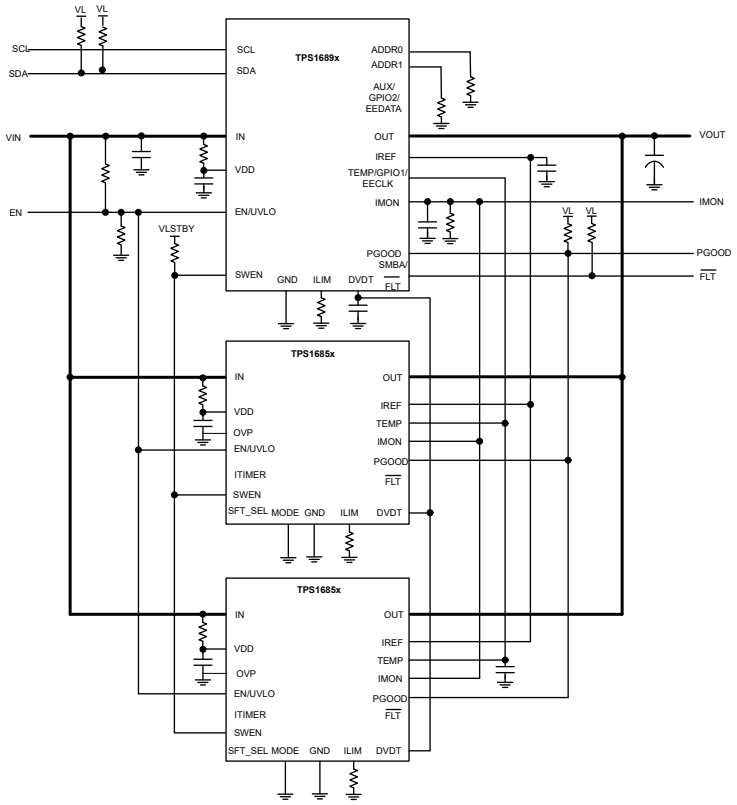

Figure 7-2. TPS1689 Connected in Parallel with TPS1685x For Higher Current Support With PMBus®

In this configuration, the TPS1689 acts as the primary device and controls the other TPS1685x devices in the chain which are designated as secondary devices. This configuration is achieved by connecting the primary device as follows:

1. VDD is connected to IN through an R-C filter.
2. DVDT is connected through capacitor to GND.
3. IREF is connected through capacitor to GND.
4. IMON is connected through resistor to GND.
5. ILIM is connected through resistor to GND.

The secondary devices must be connected in the following manner:

1. VDD is connected to IN through a R-C filter.
2. MODE pin is connected to GND.
3. ITIMER pin is left OPEN.
4. ILIM is connected through resistor to GND.

The following pins of all devices must be connected together:

1. IN
2. OUT
3. EN/UVLO
4. DVDT
5. SWEN
6. PGOOD
7. IMON
8. IREF
9. TEMP

In this configuration, all the devices are powered up and enabled simultaneously.

- The TPS1689 monitors the combined VIN, VOUT, IMON, TEMP and reports it over the PMBus® telemetry interface.
- The OVLO threshold is set to max value in all devices by default. For TPS1685x devices, the OV threshold is fixed in hardware and cannot be changed. The TPS1689 OV threshold can be lowered through PMBus® writes to the VIN_OV_FLT register. In this case, the TPS1689 uses the SWEN pin to turn off the TPS1685x devices during OV conditions.
- The UVLO threshold for all devices is set by the external resistor divider from IN to GND on the EN/UVLO pin. The TPS1689 UV threshold can be changed through PMBus® writes to the VIN_UV_FLT register. In this case, the TPS1689 uses the SWEN pin to turn off the TPS1685x devices during UV conditions.
- During inrush, the output of all the devices are ramped together based on the DVDT capacitor. However, the TPS1689 DVDT sourcing current can be configured through the PMBus® writes to the DEVICE_CONFIG[10:9] register to change the inrush behavior of the whole chain. The TPS1689 controls the DVDT ramp rate for the whole chain and secondary devices simply follow the ramp rate.
- The TPS1689 controls the overall overcurrent threshold of the parallel chain by setting the VIREF threshold voltage using its internal DAC. The VIREF voltage can be programmed through PMBus® to change the overcurrent threshold.
- The TPS1689 controls the transient overcurrent blanking interval (t_{OC_TIMER}) for the whole system through PMBus® writes to the OC_TIMER register. Once the digital timer expires, the TPS1689 pulls the SWEN pin low to signal all devices to break the circuit simultaneously.
- The system Power Good (PGOOD) indication is a combination of all the individual device PGOOD indications. All the devices hold their respective PGOOD pins low till their power FET is fully turned on. Once all devices have reached steady-state, they release their respective PGOOD pin pull-down and the PGOOD signal for the whole chain is asserted high. The TPS1685x secondary devices have control over the system PGOOD assertion only during startup. Once in steady state, only the TPS1689 controls the de-assertion of the PGOOD based on the VOUT_PGTH register setting.
- The fault indication ($\overline{FLT}$) for the whole system is provided by TPS1689. However, each secondary device also asserts its own $\overline{FLT}$ independently.

Power up: After power up or enable, all the eFuse devices initially hold their SWEN low till the internal blocks are biased and initialized correctly. After that, each device releases its own SWEN. After all devices have released their SWEN, the combined SWEN goes high and the devices are ready to turn on their respective FETs at the same time.

Inrush: During inrush, because the DVDT pins are tied together to a single DVDT capacitor all the devices turn on the output with the same slew rate (SR). Choose the common DVDT capacitor (C_{DVDT}) as per Equation 13 and Equation 14.

$$SR\left(\frac{V}{ms}\right) = \frac{I_{INRUSH}\,(mA)}{C_{OUT}\,(\mu F)} \tag{13}$$

$$C_{dVdt}\,(pF) = \frac{50000 \times k}{SR\left(\frac{V}{ms}\right)} \tag{14}$$

Refer to Section 6.3.4.1 section for more details.

The internal balancing circuits ensure that the load current is shared among all devices during start-up. This action prevents a situation where some devices turn on faster than others and experience more thermal stress as compared to other devices. This prevents premature or partial shutdown of the parallel chain, or even SOA damage to the devices. The current balancing scheme ensures the inrush capability of the chain scales according to the number of devices connected in parallel, thereby ensuring successful start-up with larger output capacitances or higher loading during start-up. All devices hold their respective PGOOD signals low during start-up. After the output ramps up fully and reaches steady-state, each device releases its own PGOOD pulldown. Because the DVDT pins of all devices are tied together, the internal gate high detection of all devices is synchronized. There can be some threshold or timing mismatches between devices leading to PGOOD assertion in a staggered manner. However, because the PGOOD pins of all devices are tied together,

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the combined PGOOD signal becomes high only after all devices have released their PGOOD pulldown. This signals the downstream load that it is okay to draw power.

Steady-state: During steady-state, all devices share current nearly equally using the active current sharing mechanism which actively regulates the respective device R_{DSON} to evenly distribute current across all the devices in the parallel chain. Once PGOOD is asserted, de-assertion is controlled only by TPS1689 and based on VOUT_PGTH register setting.

Overcurrent during steady-state: The circuit-breaker threshold for the parallel chain is based on the total system current rather than the current flowing through individual devices. This is done by connecting the IMON pins of all the devices together to a single resistor (R_{IMON}) to GND. Similarly, the IREF pins of all devices are tied together and TPS1689 uses internal programmable DAC (VIREF) to generate a common reference for the overcurrent protection block in all the devices. This action helps minimize the contribution of V_{IREF} variation to the overall mismatch in overcurrent threshold between devices.

In this case, choose the R_{IMON} as per the following equation:

$$R_{IMON} = \frac{V_{IREF}}{G_{IMON} \times I_{OCP(TOTAL)}} \quad (15)$$

The start-up current limit and active current sharing threshold for each device is set independently using the ILIM pin. The R_{ILIM} value for the TPS1689 and TPS1685 must be selected based on the following equation:

$$R_{ILIM} = \frac{1.1 \times N \times R_{IMON}}{3} \quad (16)$$

Where N = Number of devices in parallel chain (1 × TPS1689 + (N - 1) × TPS1685x)

Other variations: The IREF pin can be driven from an external precision voltage reference with low impedance.

During an overcurrent event, the overcurrent detection of all the devices is triggered simultaneously. This in turn triggers the overcurrent blanking timer (OC_TIMER) in TPS1689. The TPS1689 uses the OC_TIMER expiry event as a trigger to pull the SWEN low for all the devices, thereby initiating the circuit-breaker action for the whole chain at the same time. This mechanism ensures that mismatches in the current distribution, overcurrent thresholds and OC_TIMER intervals among the devices do not degrade the accuracy of the circuit-breaker threshold of the complete parallel chain or the overcurrent blanking interval. However, the secondary devices also maintain their backup overcurrent timer and can trigger the shutdown of the whole chain if the primary device fails to do so within a certain interval.

Severe overcurrent (short circuit): If there is a severe fault at the output (for example, output shorted to ground with a low impedance path), the current builds up rapidly to a high value and triggers the fast-trip response in each device. The devices use two thresholds for fast-trip protection – a user-adjustable threshold as well as a fixed threshold (I_{FFT} only during steady-state). After the fast-trip, the TPS1689 relies on the SC_RETRY configuration bit setting in the DEVICE_CONFIG register to determine if the whole chain enters a latched fault or performs a fast recovery by restarting in current limit manner. If it enters a latched fault, the devices remain latched off till the device is power cycled or re-enabled, or auto-retry after a delay based on the RETRY_CONFIG register setting.

7.1.3 Multiple TPS1689 Devices: Parallel Connection With Individual Telemetry

Applications which need higher current support along with separate digital interface for telemetry, control and configurability for each eFuse can use multiple independent TPS1689 if desired instead of 1 TPS1689 and multiple TPS1685x.

Some modifications with respect to TPS1689 in parallel with multiple TPS1685x is needed and shown in Figure 7-3

- IMON pins to be separated. Each device will be configured for its own OCP response. The individual OCP threshold should be set to 1/Nth of system OCP threshold where N is total no of devices in parallel.

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- PMBus address for both devices to be set to different values so that each device can be accessed independently.
- /FLT pins to be kept separate so that it's easy to debug which device encountered a fault.

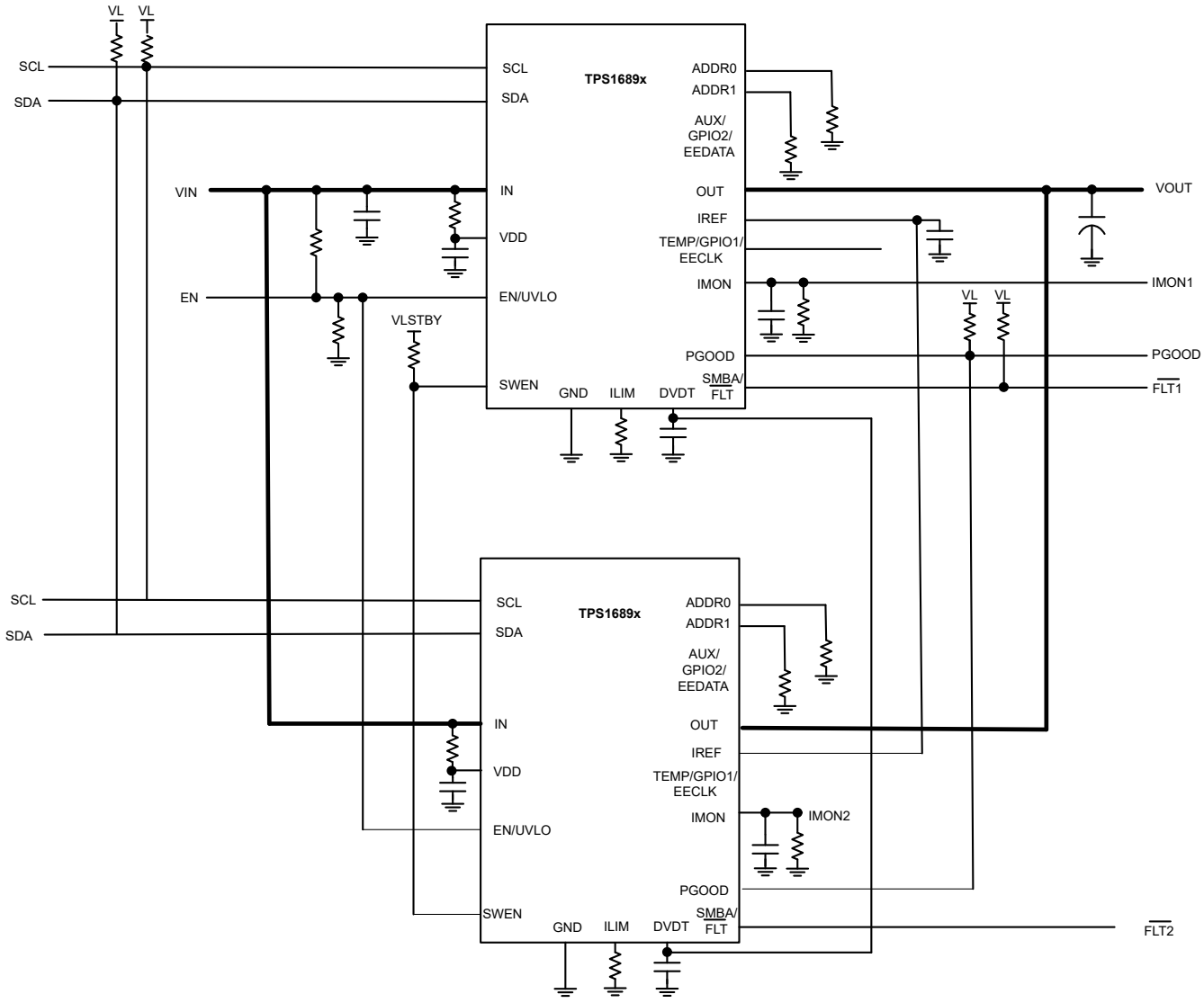

Figure 7-3. Independent Stacking With Multiple TPS1689

7.1.4 Multiple Devices, Independent Operation (Multi-zone)

Systems which need power from a common source to be distributed to different power zones can use multiple TPS1689 devices connected as shown in Figure 7-4 to provide independent monitoring and protection for each zone.

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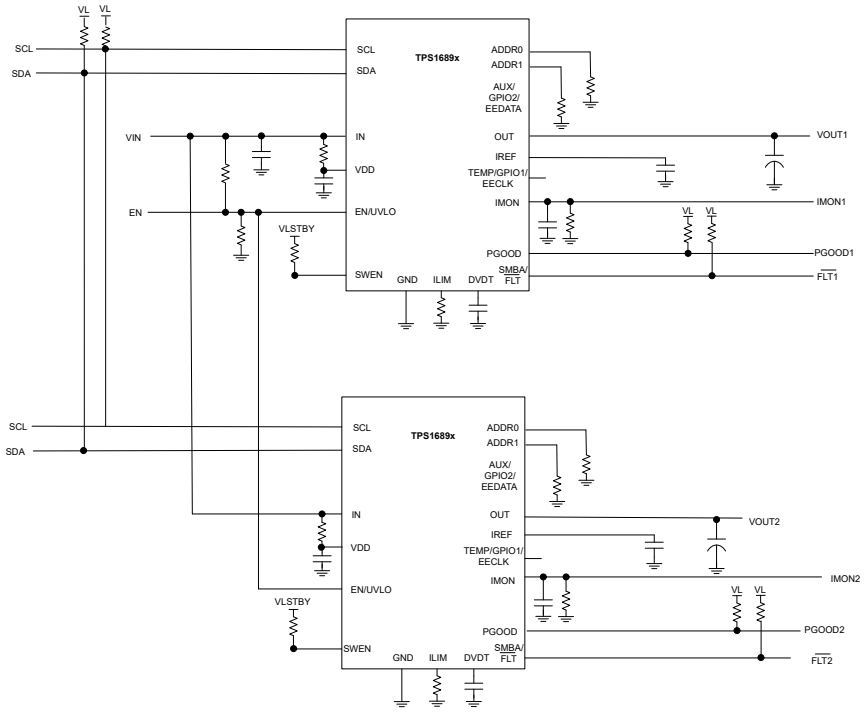

Figure 7-4. Multiple TPS1689 Devices Delivering Power to Different Zones in a System

In this configuration, the following pins of each device are tied to the respective pins on the other devices.

1. IN
2. EN/UVLO
3. SCL
4. SDA

Note

The EN/UVLO pins can be separated if each zone needs to have a different hardware control signal or UVLO threshold.

In this configuration, all the devices are monitored and controlled independently through the PMBus®. Because the devices share the same bus, they must have different device addresses, which can be set using different pin-strapping combinations on the ADDR0 and ADDR1 pins.

7.2 Typical Application: 54-V, 2-kW Power Path Protection with PMBus® Interface in Datacenter Servers

This design example considers a 54V system operating voltage with a tolerance of ±10%. The maximum steady-state load current is 40A. If the load current exceeds 44A, the eFuse circuit must allow transient overload currents up to a 4 ms interval. For persistent overloads lasting longer than that, the eFuse circuit must break the circuit and then latch-off. The eFuse circuit must charge a bulk capacitance of 2mF .Figure 7-5 shows the application schematic for this design example.

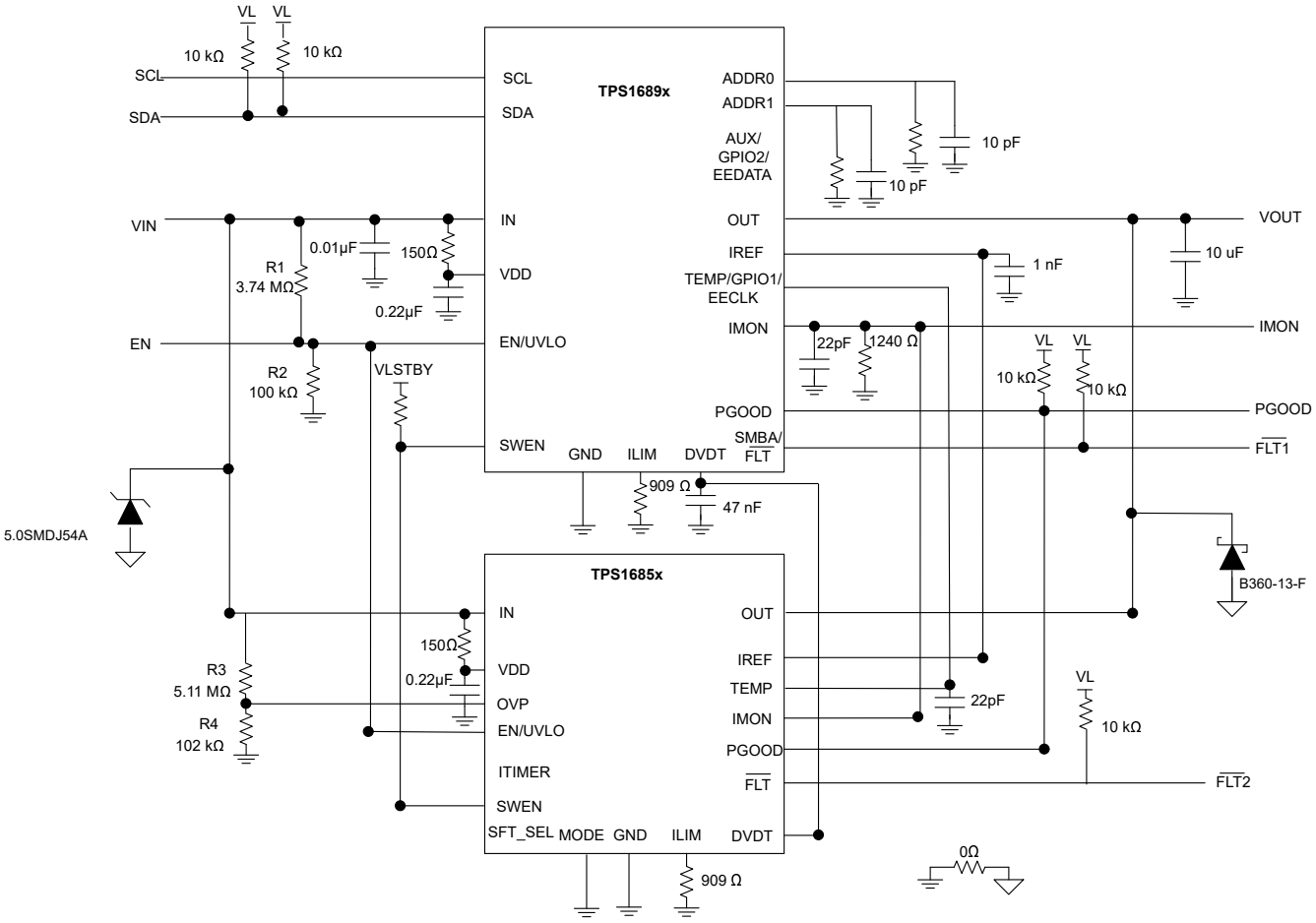

Figure 7-5. Application Schematic for a 54-V, 2-kW Power Path Protection Circuit with PMBus® Interface

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7.2.1 Design Requirements

Table 7-1 shows the design parameters for this application example.

Table 7-1. Design Parameters

PARAMETER	VALUE
Input voltage range (V_{IN})	43 V – 60V
Maximum DC load current ($I_{OUT(max)}$)	40 A
Maximum output capacitance (C_{LOAD})	2 mF
Maximum ambient temperature	55°C
Transient overload blanking timer	4 ms
Need to survive a “hot-short” on output condition?	Yes
Need to survive a “power up into short” condition?	Yes
Can the board be hotplugged in or power cycled?	Yes
Load current monitoring needed?	Yes
Need PMBus® interface for telemetry, control, and configurability?	Yes
Fault response	Latch-off

7.2.2 Detailed Design Procedure

- **Determining the number of eFuse devices to be used in parallel**

  As the design must have PMBus® functionality or interface for telemetry, control, and configuration, the TPS1689 eFuse must be used as a primary device in parallel with TPS1685x eFuse(s) as secondary devices in order to support the required steady-state thermal design current. By factoring in a small variation in the junction to ambient thermal resistance ($R_{\theta JA}$), each TPS1689 eFuse and TPS1685x eFuse is rated at maximum RMS currents of 20A and 20 A respectively with a maximum junction temperature of 125 °C. Therefore, Equation 17 can be used to calculate the number of TPS1685x eFuses (N-1) to be in parallel with a TPS1689 eFuse to support the maximum steady state DC load current ($I_{LOAD(max)}$), for which the solution must be designed.

$$(N-1) \geq \frac{\left(I_{OUT(max)} - 20\right)}{20} \tag{17}$$

  According to Table 7-1, $I_{OUT(max)}$ is 40 A. Therefore, one (1) TPS1689 and one(1) TPS1685x eFuses are connected in parallel to support the desired steady-state load current.

- **Setting up the primary and secondary devices in a parallel combination of TPS1689 and TPS1685x eFuses**

  The TPS1689 functions as a primary device by default. By connecting the MODE pin of all the TPS1685x eFuses to GND, they are configured as secondary devices.

- **Selecting the V_{IREF} to set the reference voltage for overcurrent protection and active current sharing**

  The reference voltage (V_{IREF}) for overcurrent protection and active current sharing will be at 1 V by default. However, it can be programmed via PMBus® using the VIREF register if another reference voltage is needed in the range of 0.3 V to 1.2 V. When the voltage at the IMON pin (V_{IMON}) is used as an input to an ADC to monitor the system current or to implement the Platform Power Control (Intel PSYS) functionality inside the VR controller, V_{IREF} must be set to half of the maximum voltage range of the ISYS_IN input of the controller. This action provides the necessary headroom and dynamic range for the system to accurately monitor the

load current up to the fast-trip threshold (2 × $I_{OCP(TOTAL)}$). For improved noise immunity, place a 1 nF ceramic capacitor from the IREF pin to GND.

Note

Maintain V_{IREF} within the recommended voltage to ensure proper operation of overcurrent detection circuit.

- **Selecting the R_{IMON} resistor to set the overcurrent (circuit-breaker) and fast-trip thresholds during steady-state**

  TPS1689 eFuse responds to the output overcurrent conditions during steady-state by turning off the output after a user-adjustable transient fault blanking interval. This eFuse continuously senses the total system current (I_{OUT}) and produces a proportional analog current output (I_{IMON}) on the IMON pin. This generates a voltage (V_{IMON}) across the IMON pin resistor (R_{IMON}) in response to the load current, which is defined as Equation 18.

$$V_{IMON} = I_{OUT} \times G_{IMON} \times R_{IMON} \quad (18)$$

  G_{IMON} is the current monitor gain (I_{IMON} : I_{OUT}), whose typical value is 18.23 µA/A. The overcurrent condition is detected by comparing the V_{IMON} against the V_{IREF} as a threshold. The circuit-breaker threshold during steady-state ($I_{OCP(TOTAL)}$) can be calculated using Equation 19.

$$I_{OCP(TOTAL)} = \frac{V_{IREF}}{G_{IMON} \times R_{IMON}} \quad (19)$$

  In this design example, $I_{OCP(TOTAL)}$ is considered to be around 44A. Hence, $I_{OCP(TOTAL)}$ is required to be set at 44 A, and R_{IMON} can be calculated to be 1246.6Ω with G_{IMON} as 18.23 µA/A and V_{IREF} as 1 V. The value of R_{IMON} chosen is 1240Ω with 0.1% tolerance and power rating of 100 mW. This results in a circuit-breaker threshold of 44.2A. For noise immunity, place a 22 pF ceramic capacitor from the IMON pin to GND.

Note

The total system output current (I_{OUT}) must be considered when selecting R_{IMON}, not the current carried by each individual device.

- **Selecting the R_{ILIM} resistor to set the active sharing threshold during steady-state**

  R_{ILIM} is used in setting up the active current sharing threshold during steady state among the devices in a parallel chain. Each device continuously monitors the current flowing through it (I_{DEVICE}) and outputs a proportional analog output current on its own ILIM pin. This in turn produces a proportional voltage (V_{ILIM}) across the respective ILIM pin resistor (R_{ILIM}), which is expressed as Equation 20.

$$V_{ILIM} = I_{DEVICE} \times G_{ILIM} \times R_{ILIM} \quad (20)$$

  G_{ILIM} is the current monitor gain (I_{ILIM} : I_{DEVICE}), whose typical value is 18.24 µA/A.

  – ***Active current sharing during steady-state*:** This mechanism operates only after the device reaches steady-state and acts independently by comparing its own load current information (V_{ILIM}) with the Active Current Sharing reference ($CLREF_{LIN}$) threshold, defined as Equation 21.

  – $$CLREF_{LIN} = \frac{1.1 \times V_{IREF}}{3} \quad (21)$$

    Therefore, RILIM must be calculated using Equation 22 to define the active current sharing threshold as IOCP(TOTAL)/N, where N is the number of devices in parallel. Using N = 2, RIMON = 1240Ω, and Equation 22 , RILIM can be calculated to be 909.3 Ω. The closest standard value of 909 Ω with 0.1% tolerance and power rating of 100mW resistances are selected as RILIM for each device.

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$$R_{ILIM} = \frac{1.1 \times N \times R_{IMON}}{3} \quad (22)$$

Note

To determine the value of R_{ILIM}, Equation 23 must be used if a different threshold for active current sharing ($I_{LIM(ACS)}$) is desired.

$$R_{ILIM} = \frac{1.1 \times V_{IREF}}{3 \times G_{ILIM} \times I_{LIM(ACS)}} \quad (23)$$

- **Selecting the overcurrent blanking timer duration (t_{OC_TIMER})**

  The overcurrent blanking timer duration (t_{OC_TIMER}) for the entire parallel chain is controlled by TPS1689 and is set to 2.18 ms by default. However, it can be programmed via PMBus® using the OC_TIMER (E6h) register to a different value . The ITIMER pin for all the secondary TPS1685x devices must be left open.

- **Selecting the resistors to set the undervoltage lockout threshold**

The undervoltage lockout (UVLO) threshold is adjusted by employing the external voltage divider network of R1 and R2 connected between IN, EN/UVLO, and GND pins of the device as described in Section 6.3.1 section. The resistor values required for setting up the UVLO threshold are calculated using Equation 24. To minimize the input current drawn from the power supply, TI recommends using higher resistance values for R1 and R2. From the device electrical specifications, UVLO rising threshold $V_{UVLO(R)}$ = 1.2V. From the design requirements, VIN_{UVLO} = 46V. First choose the value of R1 = 3.74MΩ and use Equation 24 to calculate R2 = 100kΩ. Use the closest standard 1 % resistor values: R1 = 3.74MΩ and R2 = 100kΩ. For noise reduction, place a 100pF ceramic capacitor across the EN/UVLO pin and GND.

- $$V_{IN(UV)} = V_{UVLO(R)} \frac{R_1 + R_2}{R_2} \quad (24)$$

- **Selecting the resistors to set the overvoltage lockout threshold**

  The overvoltage lockout (OVLO) threshold is adjusted by employing the external voltage divider network of R3 and R4 connected between IN, OVLO, and GND pins of the device as described in overvoltage protection section. The resistor values required for setting up the OVLO threshold are calculated using below equation.

- $$V_{IN(OV)} = V_{OVLO(R)} \frac{R_1 + R_2}{R_2} \quad (25)$$

  To minimize the input current drawn from the power supply, TI recommends using higher resistance values for R3 and R4. From the device electrical specifications, OVLO rising threshold V_{OVLO}(R) = 1.164V. From the design requirements, VIN_{OVLO} = 60V. First choose the value of R1 = 5.11MΩ and use Equation 24to calculate R3 = 101kΩ. Use the closest standard 1% resistor values: R3 = 5.11MΩ and R4 = 102kΩ. For noise reduction, place a 10pF ceramic capacitor across the OVLO pin and GND.

- **Selecting the R-C filter between VIN and VDD for TPS1689 and TPS1685x**

  VDD pin is intended to power the internal control circuitry of the eFuse with a filtered and stable supply, not affected by system transients. Therefore, use an R (150 Ω) – C (0.22 µF) filter from the input supply (IN pin) to the VDD pin. This helps to filter out the supply noises and to hold up the controller supply during severe faults such as short-circuit at the output. In a parallel chain, this R-C filter must be employed for each device.

- **Selecting the pullup resistors for PMBus® SCL, SDA, and SMBA# lines**

  The SCL, SDA, and SMBA# lines can be pulled up to potentials less than 5 V in general with pull-up resistors of 10 kΩ. However, to obtain the appropriate values of these pull-up resistors in accordance with the system specifications, please refer to I2C Bus Pullup Resistor Calculation.

- **Configuring the PMBus® target device address**

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Place appropriate resistors across ADDR0 and ADDR1 to GND or leave these pins floating or connect them to GND as described in Section 6.3.14.1 to set the preferred device address. To improve the noise immunity for correct address decoding, connect 10 pF ceramic capacitors in parallel with the resistors on ADDR0 and ADDR1.

- **Selection of TVS diode at input and Schottky diode at output**

  In the case of a short circuit and overload current limit when the device interrupts a large amount of current instantaneously, the input inductance generates a positive voltage spike on the input, whereas the output inductance creates a negative voltage spike on the output. The peak amplitudes of these voltage spikes (transients) are dependent on the value of inductance in series with the input or output of the device. Such transients can exceed the absolute maximum ratings of the device and eventually lead to failures due to electrical overstress (EOS) if appropriate steps are not taken to address this issue. Typical methods for addressing this issue include:

  1. Minimize lead length and inductance into and out of the device.
  2. Use a large PCB GND plane.
  3. Addition of the Transient Voltage Suppressor (TVS) diodes to clamp the positive transient spike at the input.
  4. Using Schottky diodes across the output to absorb negative spikes.

  Refer to *TVS Clamping in Hot-Swap Circuits* and *Selecting TVS Diodes in Hot-Swap and ORing Applications* for details on selecting an appropriate TVS diode and the number of TVS diodes to be in parallel to effectively clamp the positive transients at the input below the absolute maximum ratings of the IN pin (90 V). These TVS diodes also help to limit the transient voltage at the IN pin during the Hot Plug event. 2, SMDJ54A are used in parallel in this design example.

  Note

  Maximum Clamping Voltage V_C specification of the selected TVS diode at I_{pp} (10/1000 µs) (V) must be lower than the absolute maximum rating of the power input (IN) pin for safe operation of the eFuse.

  Selection of the Schottky diodes must be based on the following criteria:

  – The non-repetitive peak forward surge current (I_{FSM}) of the selected diode must be more than the fast-trip threshold . Two or more Schottky diodes in parallel must be used if a single Schottky diode is unable to meet the required I_{FSM} rating. Equation 26 calculates the number of Schottky diodes ($N_{Schottky}$) that must be used in parallel.

  $$N_{Schottky} > \frac{I_{SFT}}{I_{FSM}} \quad (26)$$

  – Forward Voltage Drop (V_F) at near to I_{FSM} must be as small as possible. Ideally, the negative transient voltage at the OUT pin must be clamped within the absolute maximum rating of the OUT pin (-5 V).
  – DC Blocking Voltage (V_{RM}) must be more than the maximum input operating voltage.
  – Leakage current (I_R) must be as small as possible.

  2, B360-13-F are used in parallel in this design example.

- **Selecting C_{IN} and C_{OUT}**

  TI recommends to add ceramic bypass capacitors to help stabilize the voltages on the input and output. The value of C_{IN} must be kept small to minimize the current spike during hot-plug events. For each device, 0.1 µF of C_{IN} is a reasonable target. Because C_{OUT} does not get charged during hot-plug, a larger value such as 2.2 µF can be used at the OUT pin of each device.

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7.2.3 Application Performance Plots

All the waveforms below are captured on an evaluation setup with one (1) TPS1689 eFuse and one(1) TPS1685x eFuse in parallel. All the pullup supplies are derived from a separate standby rail.

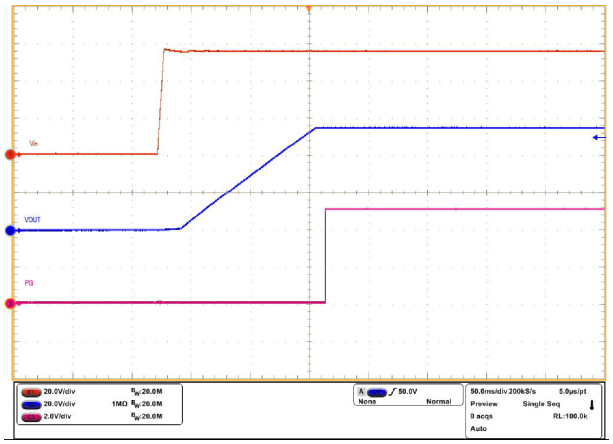


Figure 7-6. VIN Ramped From 0V to 54V

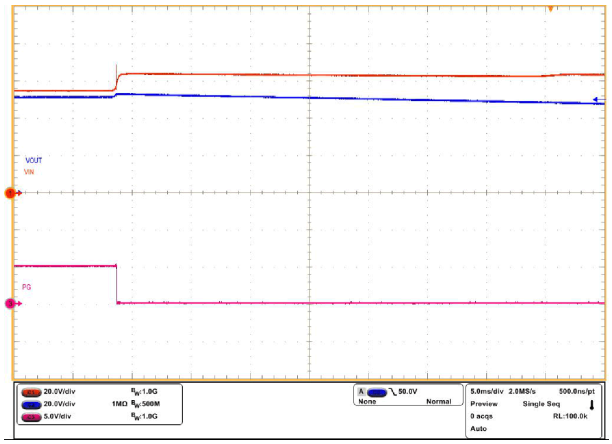


Figure 7-7. Overvoltage protection

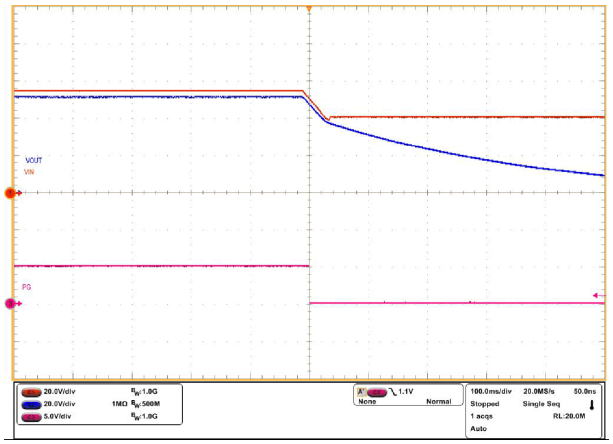


Figure 7-8. Undervoltage protection

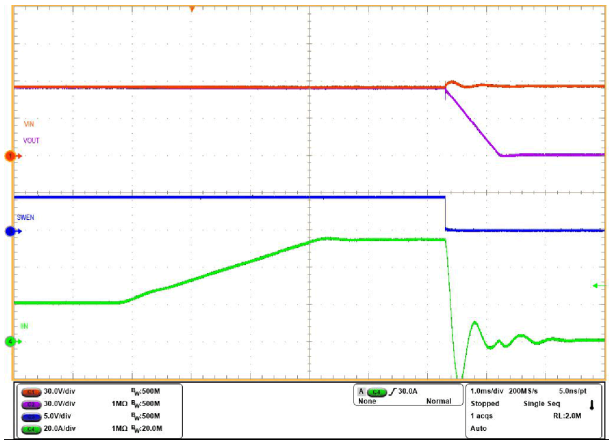


Figure 7-9. Overcurrent protection

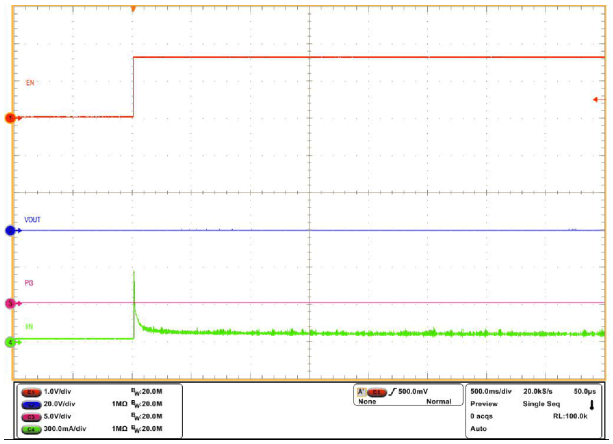


Figure 7-10. Power Up Into Short: VIN = 54V, EN/ UVLO Stepped Up From 0V to 3V

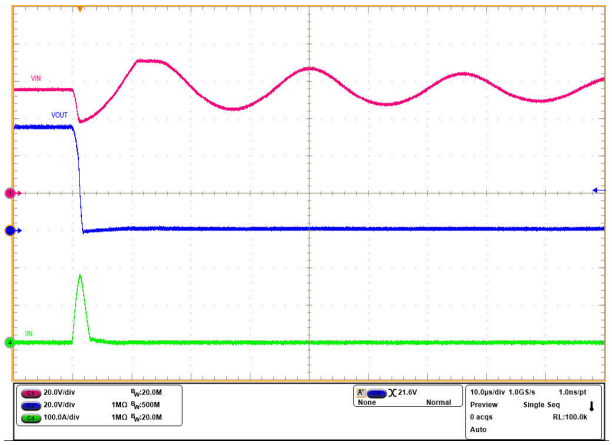


Figure 7-11. Output Hot-Short Response

7.3 Power Supply Recommendations

The TPS1689 devices are designed for a supply voltage in the range of 9V to 80V on the IN pin and 9V to 80V on the VDD pin. TI recommends using a minimum capacitance of 0.1 µF on the IN pin of each device in parallel chain to avoid coupling of high slew rates during hot plug events. TI also recommends using an R-C filter from the IN supply to the VDD pin to filter out supply noise and to hold up the controller supply during severe faults such as short-circuit.

Note

1. If in-system programming of configuration register non-volatile memory is needed, then TI recommends using a minimum supply of 10 V on VDD.

7.3.1 Transient Protection

In the case of a short-circuit or circuit-breaker event, when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Connect a Schottky diode from the OUT pin ground to absorb negative spikes.
- Connect a low ESR capacitor of 2.2 µF or higher at the OUT pin very close to the device.
- Connect a ceramic capacitor C_{IN} = 0.1 µF or higher at the IN pin very close to the device to dampen the rise time of input transients. The capacitor voltage rating must be at least twice the input supply voltage to be able to withstand the positive voltage excursion during inductive ringing.

The approximate value of input capacitance can be estimated with Equation 27.

$$V_{SPIKE(Absolute)} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (27)$$

V_{IN} is the nominal supply voltage.

I_{LOAD} is the load current.

L_{IN} equals the effective inductance seen looking into the source.

C_{IN} is the capacitance present at the input.

- Some applications can require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device. In some cases, even if the maximum amplitude of the transients is below the absolute maximum rating of the device, a TVS can help to absorb the excessive energy dump and prevent it from creating very fast transient voltages on the input supply pin of the IC, which can couple to the internal control circuits and cause unexpected behavior.

The circuit implementation with optional protection components is shown in Figure 7-12.

ADVANCE INFORMATION

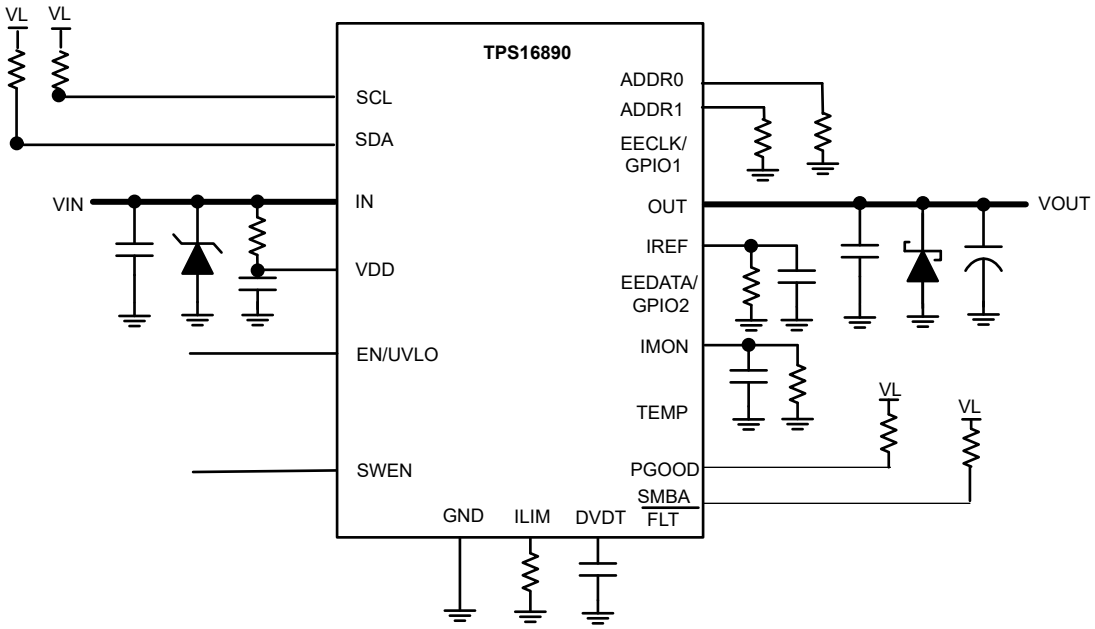


Figure 7-12. Circuit Implementation with Optional Protection Components

7.3.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. The following contribute to variation in results:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

7.4 Layout

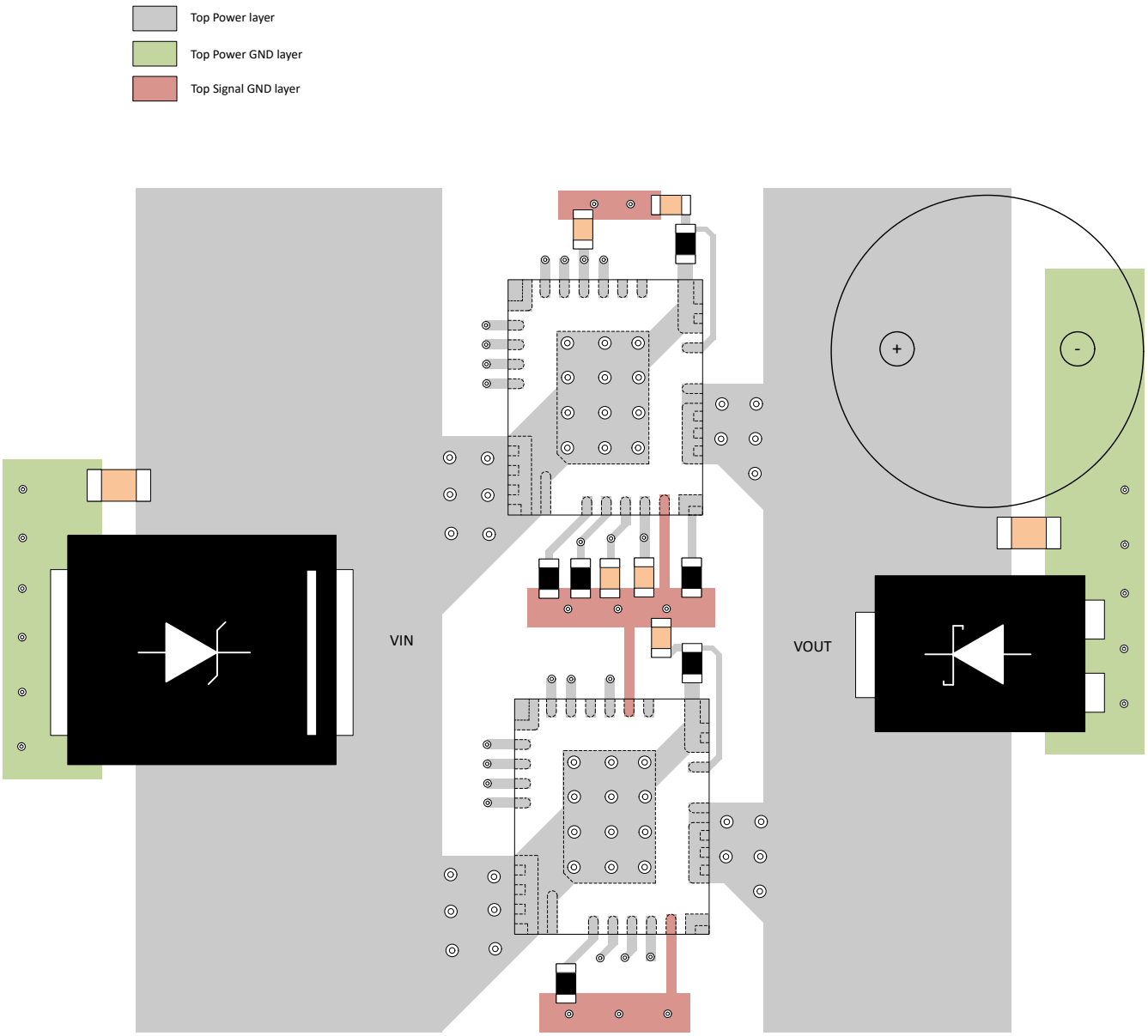
7.4.1 Layout Guidelines

- For all applications, TI recommends a ceramic decoupling capacitor of 0.1 µF or greater between the IN terminal and GND terminal.
- For all applications, TI recommends a ceramic decoupling capacitor of 2.2 µF or greater between the OUT terminal and GND terminal.
- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See Figure below for a PCB layout example.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC. The PCB ground must be a copper plane or island on the board.
- The IN and OUT pins are used for Heat Dissipation. Connect to as much copper area as possible with thermal vias.
- Locate the following support components close to their connection pins:
  - C_{IN}

ADVANCE INFORMATION

  - C_{OUT}
  - C_{VDD}
  - C_{TEMP}
  - R_{ILIM}
  - R_{IMON}
  - C_{IREF}
  - C_{DVDT}
  - Resistors for the EN/UVLO pin
  - Resistors for the ADDR0, ADDR1 pins
- Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the ADDR0, ADDR1, C_{IN}, C_{OUT}, C_{VDD}, C_{IREF}, R_{ILIM}, R_{IMON}, C_{TEMP} and C_{DVDT} components to the device must be as short as possible to reduce parasitic effects on the current limit and soft-start timing. These traces must not have any coupling to switching signals on the board.
- Because the IMON, ILIM and IREF pins directly control the overcurrent protection behavior of the device, the PCB routing of these nodes must be kept away from any noisy (switching) signals.
- TI recommends to keep the parasitic loading on SWEN pin to a minimum to avoid synchronization issues.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, TI recommends a protection Schottky diode to address negative transients due to switching of inductive loads, and it must be physically close to the OUT pins.

7.4.2 Layout Example



ADVANCE INFORMATION

8 Application Limitation and Errata

The following are the application limitation of the device and the workarounds.

- **OVP threshold configuration behaviour**

  OVP Threshold register default value at powerup takes only the lower 4 bits of stored register value from NVM. This may lead to system not powering up with OVP threhsold burnt in NVM.

  Devices affected: All variants.

  Suggested workaround:

  To overwrite the OVP threhsold register upon powerup with desired value
- **Polarity reversed for SMBA pin**

  SMBA polarity is reversed. It is low by default and goes high when there is an alert. This may lead to system reading the SMBA status incorrectly.

  Devices affected: All variants where pin 13 is configured as SMBA alert pin

  Suggested workaround:

  Flip the polarity of SMBA pin status when reading.
- **Unavailability of EEPROM data in shadow register**

  EEPROM data read back is not stored in shadow register. The system may be unable to read the EEPROM data stored through PMBUS.

  Devices affected: All variants.

  Suggested workaround:

  Read the EEPROM data directly through the MCU via I2C.
- **Device behaviour when there is EEPROM timeout when attempting to read**

  The expected behaviour is for the device to attempt communication with the EEPROM device for 100ms when it is unable to establish communication in one go, post that the device is supposed to flag EEPROM timeout alert. The device currently waits only a few us before attemping communication and flags EEPROM timeout error.

  Devices affected: All variants.
- **Device behaviour when EN is low but supply is present**

  There is considerable leakage on VOUT pin when supply is present but EN pin is low. The system may see the VOUT pin voltage slowly rise due to output capacitor being charged by leakage, if there is no load draining it.

  Devices affected: All variants.

  Suggested workaround :

  Add a appropriate bleeder resistor on Vout to ensure that the leakage current does not lead to rise of output voltage beyond the desired value.
- **Incorrect NVM data loading after multiple power cycles**

  An error is sometimes detected during NVM read at powerup leading to checksum error and device reverts to factory default settings instead of the programmed configuration. It flags a NVM error.

  Devices affected: All variants.

  Suggested workaround:

  Configure the PMBUS registers at every powerup via the PMBUS to override the default settings.

All the above limitations are planned to be addressed in the final silicon revision.

ADVANCE INFORMATION

ADVANCE INFORMATION

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS1689EVM eFuse Evaluation Board*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

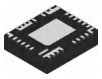
DATE	REVISION	NOTES
March 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Mechanical Data

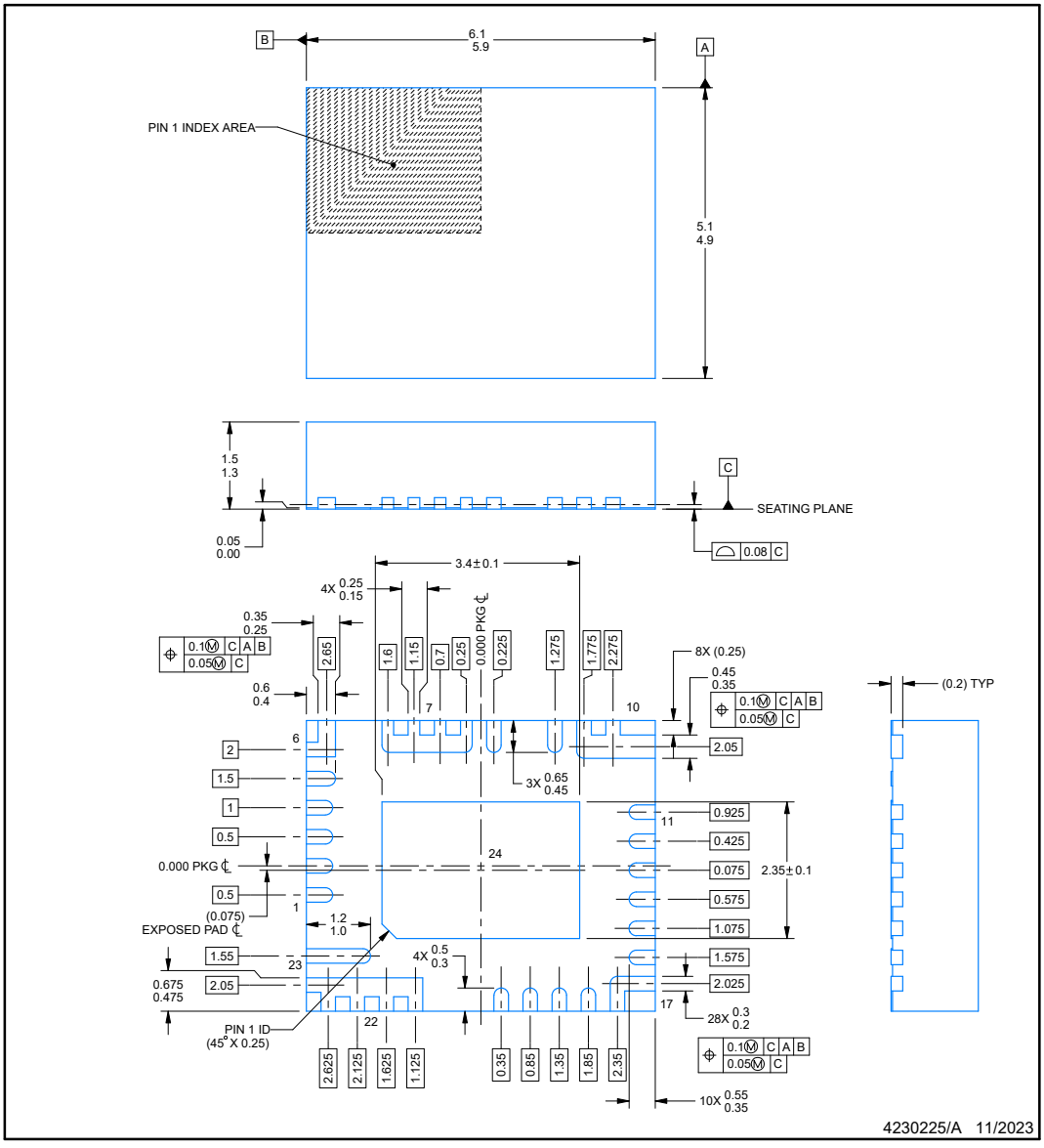
VMA0023A



PACKAGE OUTLINE

LQFN-CLIP - 1.5 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

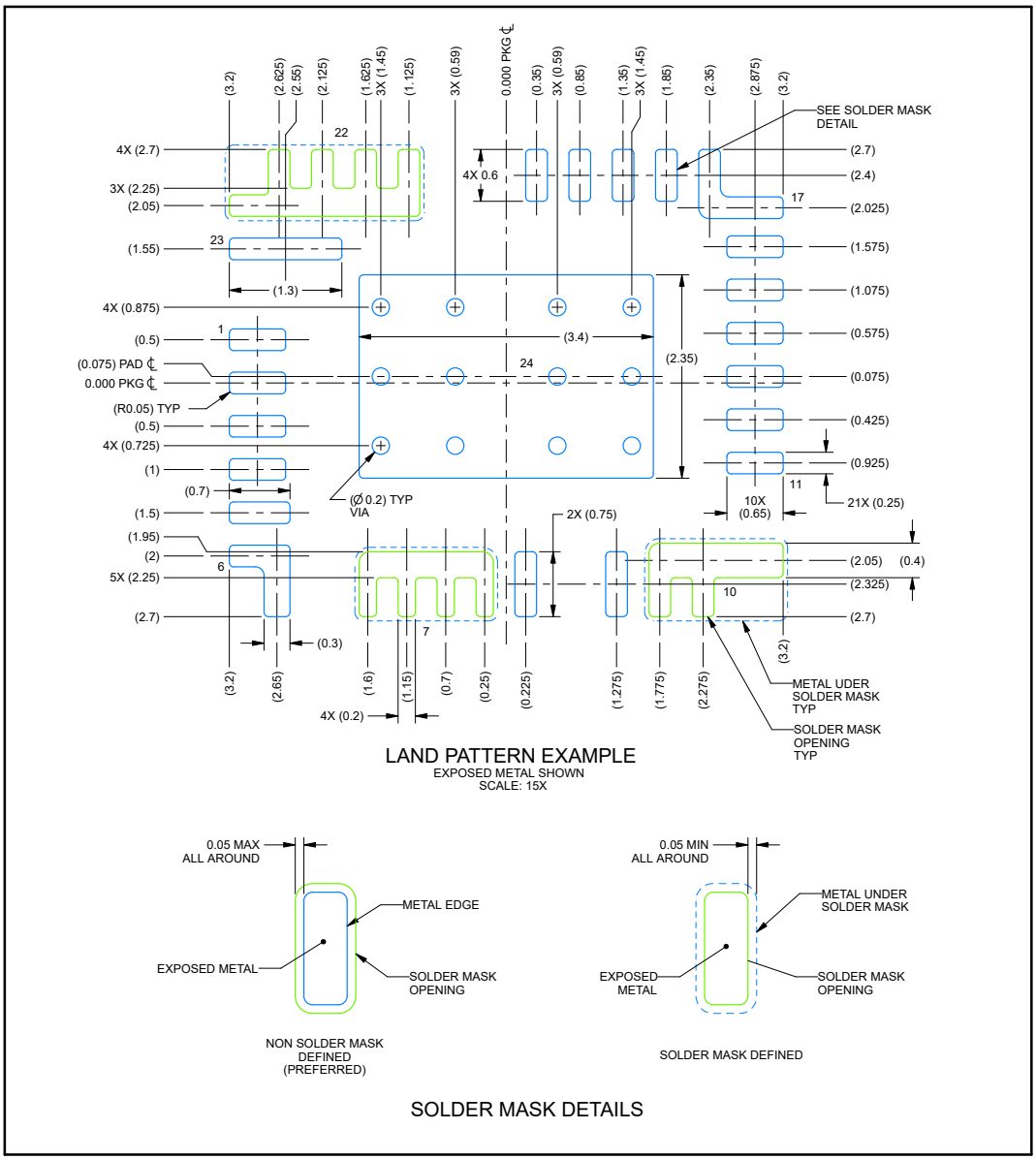
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

VMA0023A

LQFN-CLIP - 1.5 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



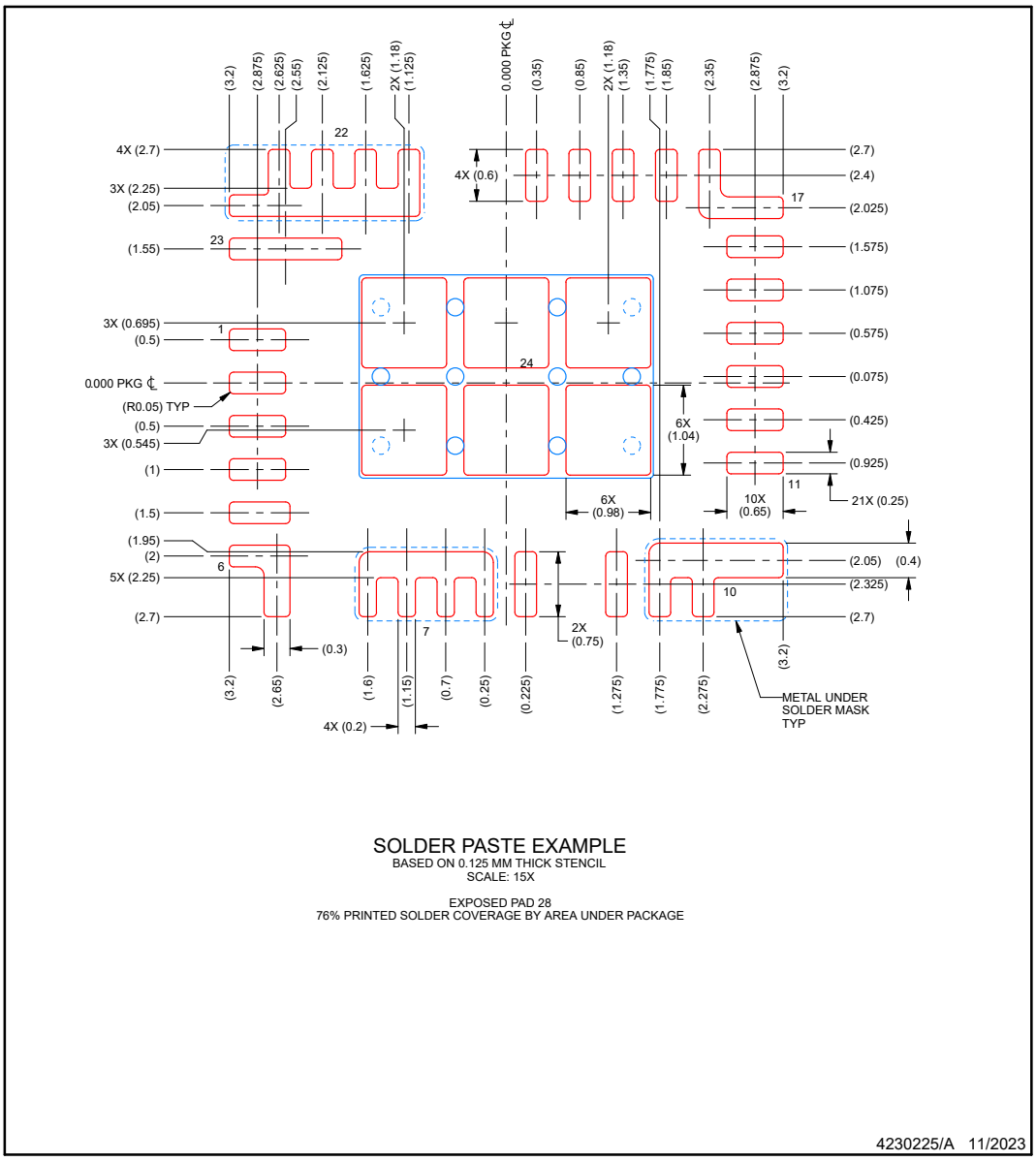
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

VMA0023A — **LQFN-CLIP - 1.5 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 28
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4230225/A 11/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS16890VMAR	Active	Preproduction	LQFN-CLIP (VMA) | 23	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPS16890VMAR.Z	Active	Preproduction	LQFN-CLIP (VMA) | 23	2500 | LARGE T&R	-	Call TI	Call TI	See PTPS16890VMAR	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

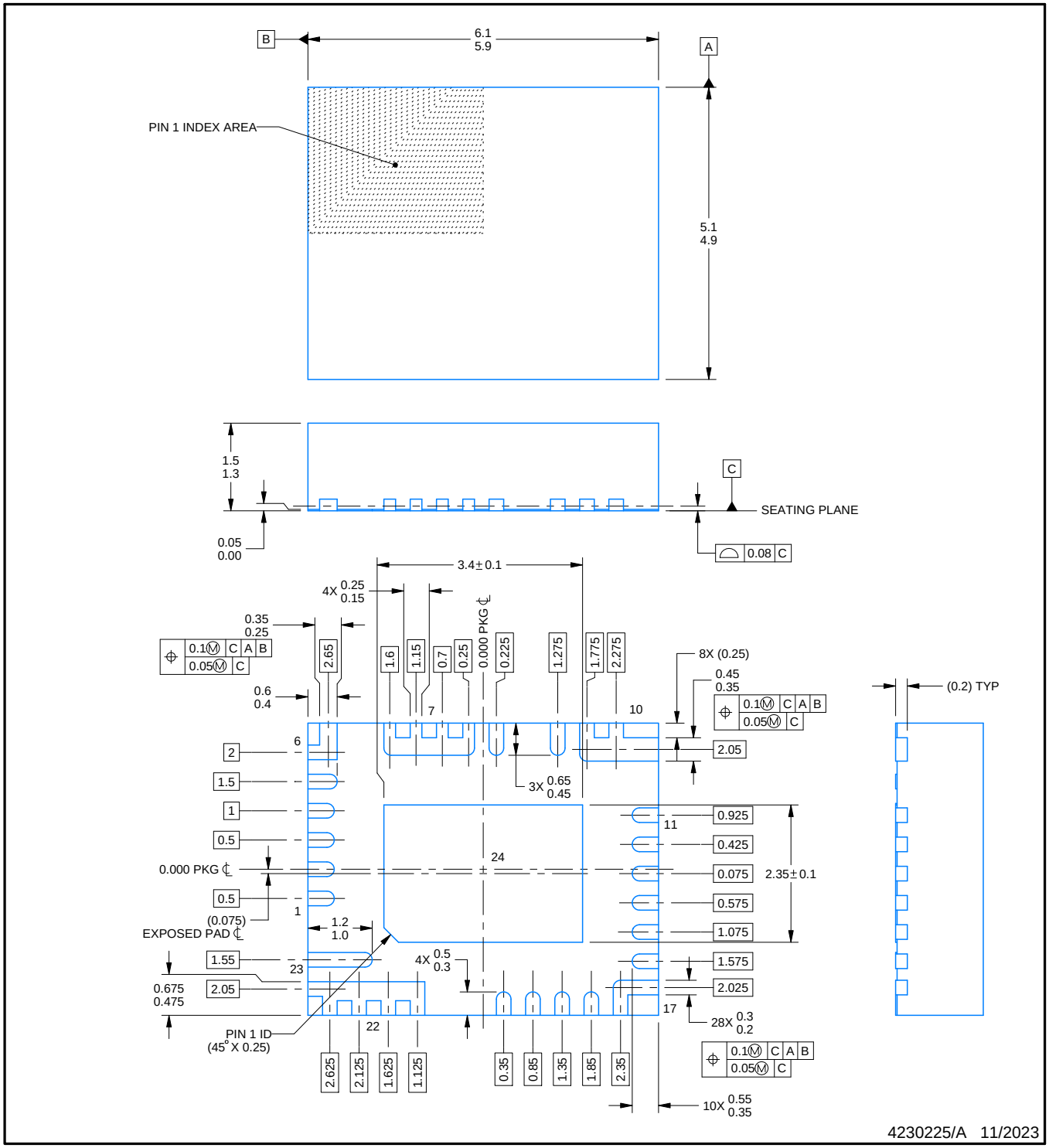
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

VMA0023A

PACKAGE OUTLINE

LQFN-CLIP - 1.5 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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EXAMPLE BOARD LAYOUT

VMA0023A

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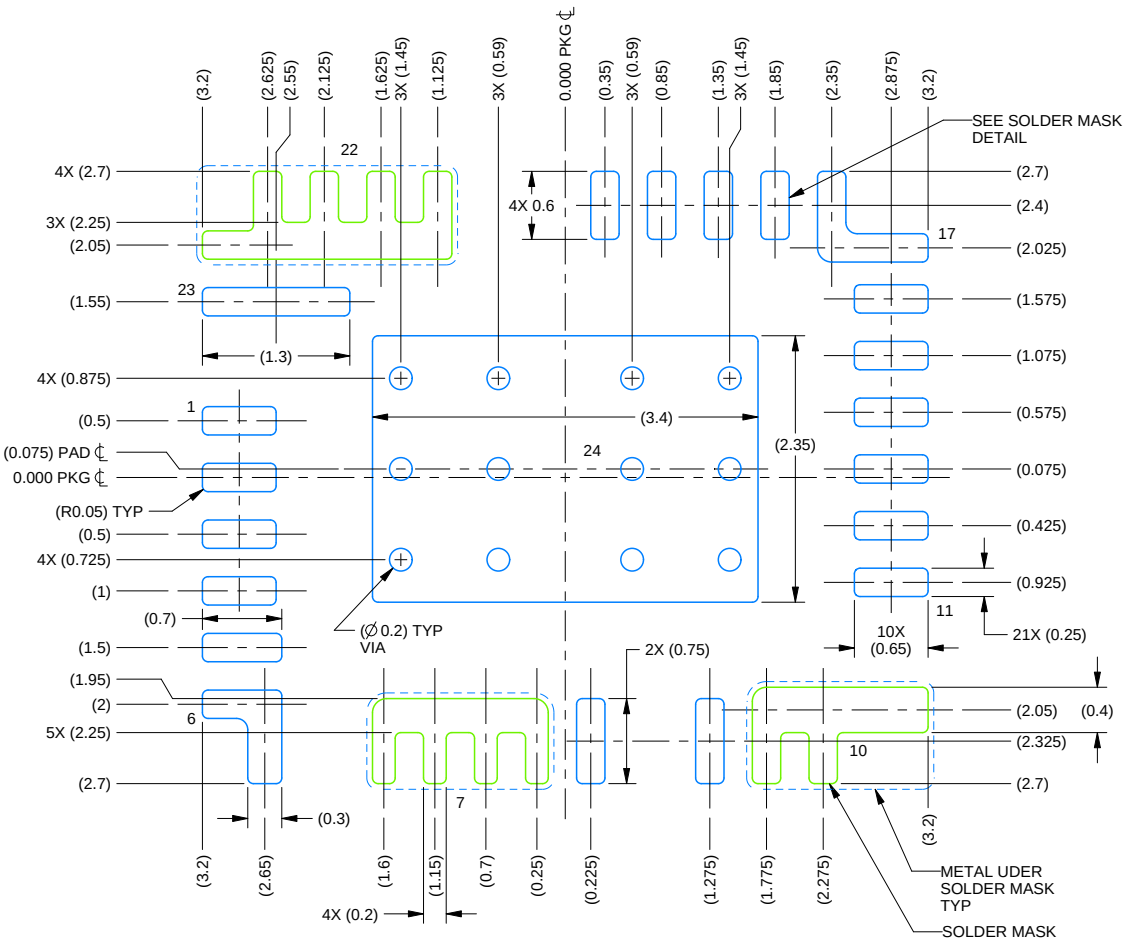
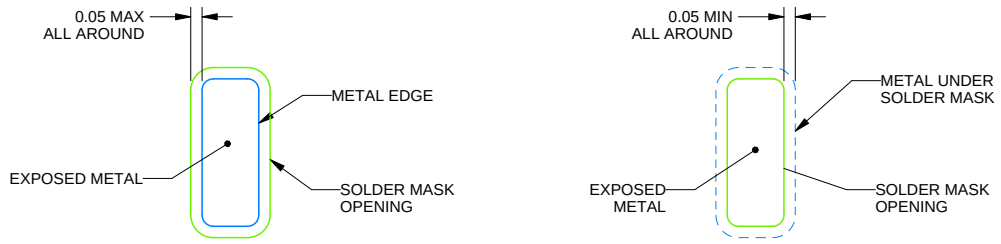
PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

VMA0023A

LQFN-CLIP - 1.5 mm max height

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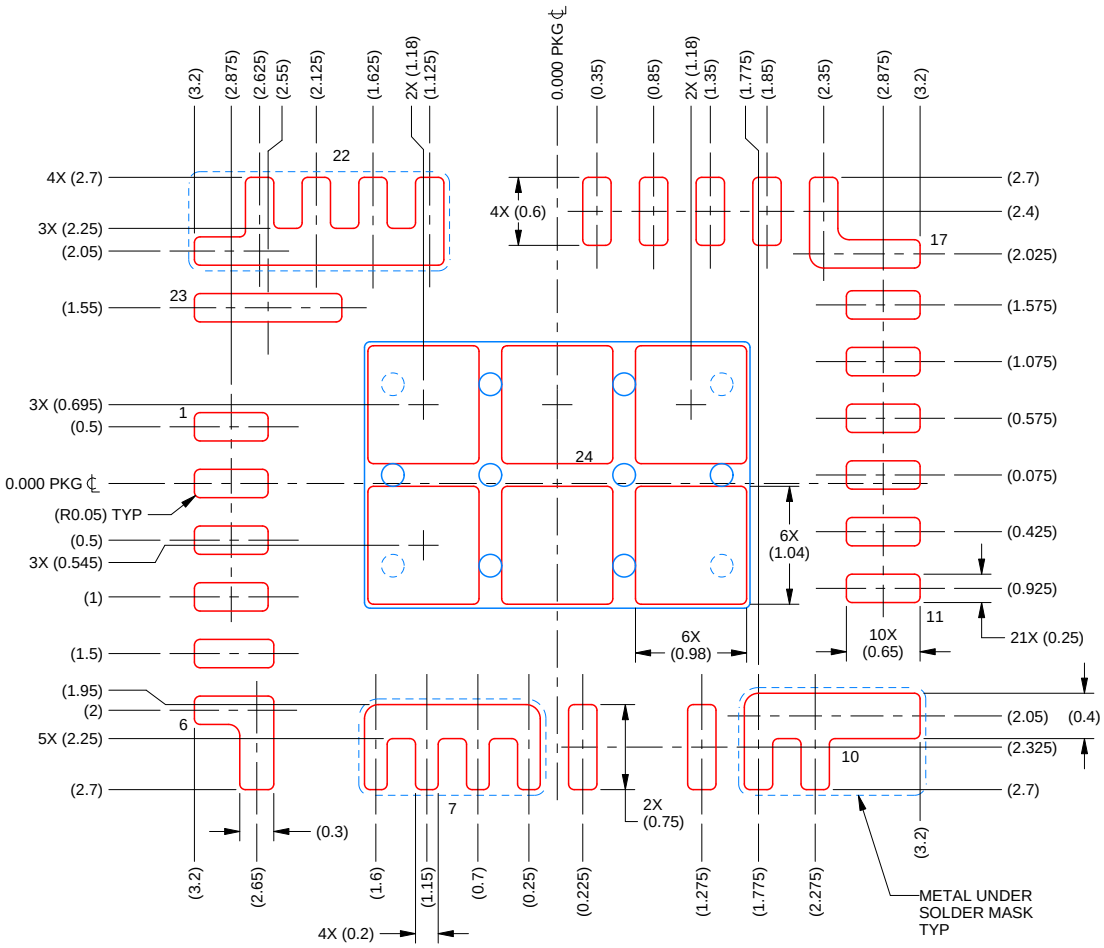

SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 28
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4230225/A 11/2023

NOTES: (continued)

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