1 Features

- Integrated Dual Channel Load Switch
- Input Voltage Range: 0.8 V to 5.5 V
- VBIAS Voltage Range: 2.5 V to 5.5 V
  - Ideal for 1S Battery Configuration
- Ultra-Low R\text{ON} Resistance
  - R\text{ON} = 27 mΩ at V\text{IN} = 5 V (V\text{BIAS} = 5 V)
  - R\text{ON} = 25 mΩ at V\text{IN} = 3.3 V (V\text{BIAS} = 5 V)
  - R\text{ON} = 25 mΩ at V\text{IN} = 1.8 V (V\text{BIAS} = 5 V)
- 4-A Maximum Continuous Switch Current per Channel
- Low Quiescent Current
  - 55 μA at V\text{BIAS} = 5 V (Both Channels)
  - 55 μA at V\text{BIAS} = 5 V (Single Channel)
- Low Control Input Threshold Enables Use of 1.2-, 1.8-, 2.5-, 3.3-V Logic
- Configurable Rise Time\(^{(1)}\)
- Quick Output Discharge (QOD)\(^{(2)}\) (Optional)
- SON 14-Pin Package with Thermal Pad
- ESD Performance Tested per JEDEC Standard
  - 2-kV HBM and 1-kV CDM
- Latch-Up Performance Exceeds 100 mA per JESD 78, Class II
- GPIO Enable – Active High
- TPS22968N: Product Preview Only

\(^{(1)}\) See the Application Information section for CT value vs. rise time
\(^{(2)}\) This feature discharges the output of the switch to GND through a 270-Ω resistor, preventing the output from floating.

2 Applications

- Ultrabook™
- Notebooks and Netbooks
- Tablets
- Consumer Electronics
- Set-Top Boxes
- Telecom Systems

3 Description

The TPS22968x is a small, ultra-low R\text{ON}, dual-channel load switch with controlled turn on. The device contains two N-channel MOSFETs that can operate over an input voltage range of 0.8 to 5.5 V and can support a maximum continuous current of 4 A per channel. Each switch is independently controlled by an on and off input (ON1 and ON2), which is capable of interfacing directly with low-voltage control signals. In TPS22968, a 270-Ω on-chip load resistor is added for output quick discharge when switch is turned off.

The TPS22968x is available in a small, space-saving package (DPU) with integrated thermal pad allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of –40 to +105°C.

Device Information \(^{(1)}\)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS22968</td>
<td>WSON (14)</td>
<td>3.00 mm × 2.00 mm</td>
</tr>
<tr>
<td>TPS22968N</td>
<td>WSON (14)</td>
<td>3.00 mm × 2.00 mm</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For all available packages, see the orderable addendum at the end of the data sheet.
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4 Revision History

Changes from Revision D (March 2016) to Revision E Page

• Changed QOD description from (TPS22968 only) to (Optional) in Features section ........................................ 1

Changes from Revision E (July 2016) to Revision F Page

• Changed Functional Block Diagram .......................................................... 1

Changes from Revision C (October 2015) to Revision D Page

• Made Changes to Thermal Considerations .................................................. 22

Changes from Revision B (June 2015) to Revision C Page

• Updated information for TPS22968N release. ............................................. 1
• Updated “TEST CONDITIONS” for RON. .................................................. 6
• Updated “TEST CONDITIONS” for RON. .................................................. 7

Changes from Revision A (July 2014) to Revision B Page

• Updated Typical Characteristics graphs. ................................................... 8

Changes from Original (January 2014) to Revision A Page

• Added Handling Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section .................................................. 1
5 Device Comparison

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>Ron (typ) at VIN = 3.3 V, VBIAS = 5 V</th>
<th>QUICK OUTPUT DISCHARGE</th>
<th>MAXIMUM OUTPUT CURRENT</th>
<th>ENABLE</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS22968</td>
<td>25 mΩ</td>
<td>Yes</td>
<td>4 A</td>
<td>Active High</td>
</tr>
<tr>
<td>TPS22968N</td>
<td>25 mΩ</td>
<td>No</td>
<td>4 A</td>
<td>Active High</td>
</tr>
</tbody>
</table>

6 Pin Configuration and Functions

Pin Functions

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>PIN NAME</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VIN1</td>
<td>I</td>
<td>Switch 1 input. Bypass this input with a ceramic capacitor to GND</td>
</tr>
<tr>
<td>2</td>
<td>ON1</td>
<td>I</td>
<td>Active-high switch 1 control input. Do not leave floating</td>
</tr>
<tr>
<td>4</td>
<td>VBIAS</td>
<td>I</td>
<td>Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5 V to 5.5 V. See the VIN and VBIAS Voltage Range section</td>
</tr>
<tr>
<td>5</td>
<td>ON2</td>
<td>I</td>
<td>Active-high switch 2 control input. Do not leave floating</td>
</tr>
<tr>
<td>6</td>
<td>VIN2</td>
<td>I</td>
<td>Switch 2 input. Bypass this input with a ceramic capacitor to GND</td>
</tr>
<tr>
<td>9</td>
<td>VOUT2</td>
<td>O</td>
<td>Switch 2 output</td>
</tr>
<tr>
<td>10</td>
<td>CT2</td>
<td>O</td>
<td>Switch 2 slew rate control. Can be left floating</td>
</tr>
<tr>
<td>11</td>
<td>GND</td>
<td>—</td>
<td>Ground</td>
</tr>
<tr>
<td>12</td>
<td>CT1</td>
<td>O</td>
<td>Switch 1 slew rate control. Can be left floating</td>
</tr>
<tr>
<td>13</td>
<td>VOUT1</td>
<td>O</td>
<td>Switch 2 output</td>
</tr>
<tr>
<td>15</td>
<td>Thermal Pad</td>
<td>—</td>
<td>Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See the Application Information section for layout guidelines</td>
</tr>
</tbody>
</table>

---

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature (unless otherwise noted)(1)

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
<th>(2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN1,2}$</td>
<td>Input voltage</td>
<td>$-0.3$</td>
<td>$6$</td>
</tr>
<tr>
<td>$V_{BIAS}$</td>
<td>Bias voltage</td>
<td>$-0.3$</td>
<td>$6$</td>
</tr>
<tr>
<td>$V_{OUT1,2}$</td>
<td>Output voltage</td>
<td>$-0.3$</td>
<td>$6$</td>
</tr>
<tr>
<td>$V_{ON1,2}$</td>
<td>ON voltage</td>
<td>$-0.3$</td>
<td>$6$</td>
</tr>
<tr>
<td>$I_{MAX}$</td>
<td>Maximum continuous switch current per channel, $T_A = 30 , ^\circ C$</td>
<td>$4$</td>
<td>A</td>
</tr>
<tr>
<td>$I_{PLS}$</td>
<td>Maximum pulsed switch current, pulse &lt; 300 $\mu s$, 2% duty cycle</td>
<td>$6$</td>
<td>A</td>
</tr>
<tr>
<td>$T_J$</td>
<td>Maximum junction temperature</td>
<td>$125$</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{stg}$</td>
<td>Storage temperature</td>
<td>$-65$</td>
<td>$150$</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{(ESD)}$</td>
<td>Electrostatic discharge</td>
</tr>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)</td>
<td>±2000</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)</td>
<td>±1000</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN1,2}$</td>
<td>Input voltage</td>
<td>$0.8$</td>
</tr>
<tr>
<td>$V_{BIAS}$</td>
<td>Bias voltage</td>
<td>$2.5$</td>
</tr>
<tr>
<td>$V_{ON1,2}$</td>
<td>ON voltage</td>
<td>$0$</td>
</tr>
<tr>
<td>$V_{OUT1,2}$</td>
<td>Output voltage</td>
<td>$V_{IN}$</td>
</tr>
<tr>
<td>$V_{IH, ON1,2}$</td>
<td>High-level input voltage, ON1,2</td>
<td>$V_{BIAS} = 2.5 , V$ to $5.5 , V$</td>
</tr>
<tr>
<td>$V_{IL, ON1,2}$</td>
<td>Low-level input voltage, ON1,2</td>
<td>$V_{BIAS} = 2.5 , V$ to $5.5 , V$</td>
</tr>
<tr>
<td>$C_{IN1,2}$</td>
<td>Input capacitor</td>
<td>$1^{(1)}$</td>
</tr>
<tr>
<td>$T_A$</td>
<td>Operating free-air temperature (2)</td>
<td>$-40$</td>
</tr>
</tbody>
</table>

(1) See the Application Information section.

(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{UA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} - (R_{UA} \times P_{D(max)})$.

7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC (1) (2)</th>
<th>TPS22968</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{UA}$</td>
<td>Junction-to-ambient thermal resistance</td>
</tr>
<tr>
<td>$R_{UJC(top)}$</td>
<td>Junction-to-case (top) thermal resistance</td>
</tr>
<tr>
<td>$R_{UB}$</td>
<td>Junction-to-board thermal resistance</td>
</tr>
<tr>
<td>$\psi_{JT}$</td>
<td>Junction-to-top characterization parameter</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.
## Thermal Information (continued)

<table>
<thead>
<tr>
<th>THERMAL METRIC (1) (2)</th>
<th>TPS22968</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\psi$JB</td>
<td>Junction-to-board characterization parameter</td>
<td></td>
</tr>
<tr>
<td>$R_{\theta JC(bot)}$</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td></td>
</tr>
</tbody>
</table>

### 7.5 Electrical Characteristics ($V_{BIAS} = 5 \text{ V}$)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$ (full) and $V_{BIAS} = 5 \text{ V}$. Typical values are for $T_A = 25^\circ\text{C}$ (unless otherwise noted).

#### POWER SUPPLIES AND CURRENTS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$T_A$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{Q, VBIAS}$</td>
<td>$V_{BIAS}$ quiescent current (both channels)</td>
<td>–40°C to +105°C</td>
<td>55</td>
<td>70</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{Q, VBIAS}$ quiescent current (single channel)</td>
<td>–40°C to +105°C</td>
<td>55</td>
<td>68</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{SD, VBIAS}$</td>
<td>$V_{BIAS}$ shutdown current</td>
<td>–40°C to +105°C</td>
<td>1</td>
<td>2</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{SD, VIN1,2}$</td>
<td>$V_{IN1,2}$ shutdown current (per channel)</td>
<td>$V_{ON1,2} = 0 \text{ V}, V_{OUT1,2} = 0 \text{ V}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN1,2} = 5 \text{ V}$</td>
<td>–40°C to +85°C</td>
<td>0.5</td>
<td>8</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–40°C to +105°C</td>
<td>10</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN1,2} = 3.3 \text{ V}$</td>
<td>–40°C to +85°C</td>
<td>0.1</td>
<td>3</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–40°C to +105°C</td>
<td>4</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN1,2} = 1.8 \text{ V}$</td>
<td>–40°C to +85°C</td>
<td>0.07</td>
<td>2</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–40°C to +105°C</td>
<td>3</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN1,2} = 1.2 \text{ V}$</td>
<td>–40°C to +85°C</td>
<td>0.05</td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–40°C to +105°C</td>
<td>2</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN1,2} = 0.8 \text{ V}$</td>
<td>–40°C to +85°C</td>
<td>0.04</td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–40°C to +105°C</td>
<td>2</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{ON1,2}$</td>
<td>ON pin input leakage current</td>
<td>$V_{ON} = 5.5 \text{ V}$</td>
<td>–40°C to +105°C</td>
<td>0.1</td>
<td></td>
<td>µA</td>
</tr>
</tbody>
</table>

#### RESISTANCE CHARACTERISTICS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$T_A$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{ON}$</td>
<td>On-state resistance</td>
<td>$I_{OUT} = -200 \text{ mA}, V_{BIAS} = 5 \text{ V}$</td>
<td>$V_{ON1,2} = 5 \text{ V}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} = 5 \text{ V}$</td>
<td>25°C</td>
<td>27</td>
<td>36</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–40°C to +85°C</td>
<td>40</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–40°C to +105°C</td>
<td>42</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} = 3.3 \text{ V}$</td>
<td>25°C</td>
<td>25</td>
<td>34</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–40°C to +85°C</td>
<td>38</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–40°C to +105°C</td>
<td>40</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} = 1.8 \text{ V}$</td>
<td>25°C</td>
<td>25</td>
<td>34</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–40°C to +85°C</td>
<td>38</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–40°C to +105°C</td>
<td>40</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} = 1.5 \text{ V}$</td>
<td>25°C</td>
<td>25</td>
<td>34</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–40°C to +85°C</td>
<td>38</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–40°C to +105°C</td>
<td>40</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} = 1.2 \text{ V}$</td>
<td>25°C</td>
<td>25</td>
<td>34</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–40°C to +85°C</td>
<td>38</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–40°C to +105°C</td>
<td>40</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} = 0.8 \text{ V}$</td>
<td>25°C</td>
<td>25</td>
<td>34</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–40°C to +85°C</td>
<td>38</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–40°C to +105°C</td>
<td>40</td>
<td></td>
<td>mΩ</td>
</tr>
</tbody>
</table>

| $R_{PD}$ | Output pulldown resistance | $V_{IN} = 5 \text{ V}, V_{ON} = 0 \text{ V}, I_{OUT} = 10 \text{ mA}$ | –40°C to +105°C | 270 | 320 | Ω |

(1) TPS22968 only.
## 7.6 Electrical Characteristics (V\text{BIAS} = 2.5 V)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature \(-40 \, ^\circ C \leq T_A \leq +105 \, ^\circ C \) (full) and V\text{BIAS} = 2.5 V. Typical values are for \( T_A = 25^\circ C \) (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( T_A )</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{\text{Q, VBIAS}} ) V\text{BIAS} quiescent current (both channels)</td>
<td>( I_{\text{OUT1}} = I_{\text{OUT2}} = 0 ), V\text{IN1,2} = V\text{ON1,2} = V\text{BIAS} = 2.5 V</td>
<td>( -40^\circ C ) to +105°C</td>
<td>18</td>
<td>27</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{Q, VBIAS}} ) V\text{BIAS} quiescent current (single channel)</td>
<td>( I_{\text{OUT1}} = I_{\text{OUT2}} = 0 ), V\text{ON2} = 0 V, V\text{IN1,2} = V\text{ON1} = V\text{BIAS} = 2.5 V</td>
<td>( -40^\circ C ) to +105°C</td>
<td>18</td>
<td>27</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{SD, VBIAS}} ) V\text{BIAS} shutdown current</td>
<td>V\text{ON1,2} = 0 V, V\text{OUT1,2} = 0 V</td>
<td>( -40^\circ C ) to +105°C</td>
<td>0.5</td>
<td>2</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{SD, VIN1,2}} ) V\text{IN1,2} shutdown current (per channel)</td>
<td>V\text{ON1,2} = 0 V, V\text{OUT1,2} = 0 V</td>
<td>V\text{IN1,2} = 2.5 V</td>
<td>( -40^\circ C ) to +85°C</td>
<td>0.1</td>
<td>2</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V\text{IN1,2} = 1.8 V</td>
<td>( -40^\circ C ) to +85°C</td>
<td>0.07</td>
<td>2</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V\text{IN1,2} = 1.2 V</td>
<td>( -40^\circ C ) to +105°C</td>
<td>0.05</td>
<td>1</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V\text{IN1,2} = 0.8 V</td>
<td>( -40^\circ C ) to +105°C</td>
<td>0.04</td>
<td>1</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{\text{ON1,2}} ) ON pin input leakage current</td>
<td>V\text{ON} = 5.5 V</td>
<td>( -40^\circ C ) to +85°C</td>
<td>0.1</td>
<td>( \mu A )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Resistance Characteristics

| \( R_{\text{ON}} \) | On-state resistance | \( I_{\text{OUT}} = -200 \, mA \), V\text{BIAS} = 2.5 V | V\text{IN1,2} = 5 V | V\text{IN} = 2.5 V | \( -40^\circ C \) to +85°C | 30 | 39 | m\( \Omega \) |
| | | | | \( -40^\circ C \) to +105°C | 44 | 46 | m\( \Omega \) |
| | | | | V\text{IN} = 1.8 V | \( -40^\circ C \) to +85°C | 28 | 36 | m\( \Omega \) |
| | | | | \( -40^\circ C \) to +105°C | 41 | 43 | m\( \Omega \) |
| | | | | V\text{IN} = 1.5 V | \( -40^\circ C \) to +85°C | 28 | 36 | m\( \Omega \) |
| | | | | \( -40^\circ C \) to +105°C | 41 | 43 | m\( \Omega \) |
| | | | | V\text{IN} = 1.2 V | \( -40^\circ C \) to +85°C | 25 | 37 | 36 | m\( \Omega \) |
| | | | | \( -40^\circ C \) to +105°C | 41 | 43 | m\( \Omega \) |
| | | | | V\text{IN} = 0.8 V | \( -40^\circ C \) to +85°C | 25 | 28 | 35 | m\( \Omega \) |
| | | | | \( -40^\circ C \) to +105°C | 39 | 41 | m\( \Omega \) |
| \( R_{\text{PD}} \) (1) | Output pulldown resistance | V\text{IN} = 2.5 V, V\text{ON} = 0 V, \( I_{\text{OUT}} = 10 \, mA \) | \( -40^\circ C \) to +105°C | 270 | 320 | \( \Omega \)

(1) TPS22968 only.
# 7.7 Switching Characteristics

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{\text{ON}})</td>
<td>Turnon time</td>
<td>(R_L = 10 \ \Omega, \ C_L = 0.1 \ \mu F, \ CT = 1000 \ \text{pF})</td>
<td>1128</td>
<td>(\mu s)</td>
<td></td>
</tr>
<tr>
<td>(t_{\text{OFF}})</td>
<td>Turnoff time</td>
<td>(R_L = 10 \ \Omega, \ C_L = 0.1 \ \mu F, \ CT = 1000 \ \text{pF})</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{\text{R}})</td>
<td>(V_{\text{OUT}}) rise time</td>
<td>(R_L = 10 \ \Omega, \ C_L = 0.1 \ \mu F, \ CT = 1000 \ \text{pF})</td>
<td>1387</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{\text{F}})</td>
<td>(V_{\text{OUT}}) fall time</td>
<td>(R_L = 10 \ \Omega, \ C_L = 0.1 \ \mu F, \ CT = 1000 \ \text{pF})</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{\text{D}})</td>
<td>ON delay time</td>
<td>(R_L = 10 \ \Omega, \ C_L = 0.1 \ \mu F, \ CT = 1000 \ \text{pF})</td>
<td>455</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(V_{\text{IN}} = V_{\text{ON}} = V_{\text{BIAS}} = 5 \ \text{V}, \ TA = 25 ^\circ \text{C}\) (unless otherwise noted)

\(V_{\text{IN}} = 0.8 \ \text{V}, \ V_{\text{ON}} = V_{\text{BIAS}} = 5 \ \text{V}, \ TA = 25 ^\circ \text{C}\) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{\text{ON}})</td>
<td>Turnon time</td>
<td>(R_L = 10 \ \Omega, \ C_L = 0.1 \ \mu F, \ CT = 1000 \ \text{pF})</td>
<td>508</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{\text{OFF}})</td>
<td>Turnoff time</td>
<td>(R_L = 10 \ \Omega, \ C_L = 0.1 \ \mu F, \ CT = 1000 \ \text{pF})</td>
<td>33</td>
<td>(\mu s)</td>
<td></td>
</tr>
<tr>
<td>(t_{\text{R}})</td>
<td>(V_{\text{OUT}}) rise time</td>
<td>(R_L = 10 \ \Omega, \ C_L = 0.1 \ \mu F, \ CT = 1000 \ \text{pF})</td>
<td>273</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{\text{F}})</td>
<td>(V_{\text{OUT}}) fall time</td>
<td>(R_L = 10 \ \Omega, \ C_L = 0.1 \ \mu F, \ CT = 1000 \ \text{pF})</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{\text{D}})</td>
<td>ON delay time</td>
<td>(R_L = 10 \ \Omega, \ C_L = 0.1 \ \mu F, \ CT = 1000 \ \text{pF})</td>
<td>377</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(V_{\text{IN}} = 2.5 \ \text{V}, \ V_{\text{ON}} = V_{\text{BIAS}} = 2.5 \ \text{V}, \ TA = 25 ^\circ \text{C}\) (unless otherwise noted)

\(V_{\text{IN}} = 0.8 \ \text{V}, \ V_{\text{ON}} = V_{\text{BIAS}} = 2.5 \ \text{V}, \ TA = 25 ^\circ \text{C}\) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{\text{ON}})</td>
<td>Turnon time</td>
<td>(R_L = 10 \ \Omega, \ C_L = 0.1 \ \mu F, \ CT = 1000 \ \text{pF})</td>
<td>1718</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{\text{OFF}})</td>
<td>Turnoff time</td>
<td>(R_L = 10 \ \Omega, \ C_L = 0.1 \ \mu F, \ CT = 1000 \ \text{pF})</td>
<td>7</td>
<td>(\mu s)</td>
<td></td>
</tr>
<tr>
<td>(t_{\text{R}})</td>
<td>(V_{\text{OUT}}) rise time</td>
<td>(R_L = 10 \ \Omega, \ C_L = 0.1 \ \mu F, \ CT = 1000 \ \text{pF})</td>
<td>1701</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{\text{F}})</td>
<td>(V_{\text{OUT}}) fall time</td>
<td>(R_L = 10 \ \Omega, \ C_L = 0.1 \ \mu F, \ CT = 1000 \ \text{pF})</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{\text{D}})</td>
<td>ON delay time</td>
<td>(R_L = 10 \ \Omega, \ C_L = 0.1 \ \mu F, \ CT = 1000 \ \text{pF})</td>
<td>859</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

# 7.8 Typical DC Characteristics

![Figure 1: Bias Voltage vs Quiescent Current (Both Channels)](image1)

![Figure 2: Bias Voltage vs Quiescent Current (Single Channel)](image2)
Typical DC Characteristics (continued)

Figure 3. Bias Voltage vs Shutdown Current (Both Channels)

Figure 4. Input Voltage vs Shutdown Current

Figure 5. Temperature vs On-Resistance

Figure 6. Temperature vs On-Resistance

Figure 7. Input Voltage vs On-Resistance

Figure 8. Input Voltage vs On-Resistance
Typical DC Characteristics (continued)

![Graph showing Pulldown Resistance vs Input Voltage](image1)

**Figure 9.** Input Voltage vs Pulldown Resistance (TPS22968 Only)

![Graph showing Output Voltage vs ON Voltage](image2)

**Figure 10.** ON Voltage vs Output Voltage

![Graph showing Delay Time vs Input Voltage](image3)

**Figure 11.** Input Voltage vs Delay Time

![Graph showing Fall Time vs Input Voltage](image4)

**Figure 12.** Input Voltage vs Fall Time

**V_{\text{BIAS}} = 2.5\ V**

CT = 1 nF

**V_{\text{BIAS}} = 5\ V**

CT = 1 nF

**V_{\text{BIAS}} = 5\ V**

CT = 1 nF

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Typical DC Characteristics (continued)

- **Figure 15.** Input Voltage vs Turnoff Time
  - $V_{\text{BIAS}} = 2.5\, \text{V}$
  - $CT = 1\, \text{nF}$

- **Figure 16.** Input Voltage vs Turnoff Time
  - $V_{\text{BIAS}} = 5\, \text{V}$
  - $CT = 1\, \text{nF}$

- **Figure 17.** Input Voltage vs Turnon Time
  - $V_{\text{BIAS}} = 2.5\, \text{V}$
  - $CT = 1\, \text{nF}$

- **Figure 18.** Input Voltage vs Turnon Time
  - $V_{\text{BIAS}} = 5\, \text{V}$
  - $CT = 1\, \text{nF}$

- **Figure 19.** Input Voltage vs Rise Time
  - $V_{\text{BIAS}} = 2.5\, \text{V}$
  - $CT = 1\, \text{nF}$

- **Figure 20.** Input Voltage vs Rise Time
  - $V_{\text{BIAS}} = 5\, \text{V}$
  - $CT = 1\, \text{nF}$
7.9  Typical AC Characteristics

**Figure 21. Turnon Response Time**
- $V_{IN} = 0.8$ V
- $V_{BIAS} = 2.5$ V
- $C_{IN} = 1$ µF
- $R_L = 10$ Ω
- $C_L = 0.1$ µF

**Figure 22. Turnon Response Time**
- $V_{IN} = 0.8$ V
- $V_{BIAS} = 5$ V
- $C_{IN} = 1$ µF
- $R_L = 10$ Ω
- $C_L = 0.1$ µF

**Figure 23. Turnon Response Time**
- $V_{IN} = 2.5$ V
- $V_{BIAS} = 2.5$ V
- $C_{IN} = 1$ µF
- $R_L = 10$ Ω
- $C_L = 0.1$ µF

**Figure 24. Turnon Response Time**
- $V_{IN} = 5$ V
- $V_{BIAS} = 5$ V
- $C_{IN} = 1$ µF
- $R_L = 10$ Ω
- $C_L = 0.1$ µF

**Figure 25. TurnOff Response Time**
- $V_{IN} = 0.8$ V
- $V_{BIAS} = 2.5$ V
- $C_{IN} = 1$ µF
- $R_L = 10$ Ω
- $C_L = 0.1$ µF

**Figure 26. Turnoff Response Time**
- $V_{IN} = 0.8$ V
- $V_{BIAS} = 5$ V
- $C_{IN} = 1$ µF
- $R_L = 10$ Ω
- $C_L = 0.1$ µF
Typical AC Characteristics (continued)

Figure 27. Turnoff Response Time

- $V_{IN} = 2.5 \, \text{V}$
- $V_{BIAS} = 2.5 \, \text{V}$
- $C_{IN} = 1 \, \mu\text{F}$
- $R_L = 10 \, \Omega$

Figure 28. Turnon Response Time

- $V_{IN} = 5 \, \text{V}$
- $V_{BIAS} = 5 \, \text{V}$
- $C_{IN} = 1 \, \mu\text{F}$
- $R_L = 10 \, \Omega$

- $C_L = 0.1 \, \mu\text{F}$

$$\text{Figure 27. Turnoff Response Time}$$

$$\text{Figure 28. Turnon Response Time}$$
8 Parameter Measurement Information

![Test Circuit Diagram]

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TEST CIRCUIT

![Timing Diagrams]

A. Rise and fall times of the control signal is 100 ns.

Figure 29. Test Circuit and Timing Waveforms
9 Detailed Description

9.1 Overview

The TPS22968 is a 5.5-V, 4-A, dual-channel ultra-low $R_{ON}$ load switch with controlled turnon. The device contains two N-channel MOSFETs. Each channel can support a maximum continuous current of 4 A and is controlled by an on and off GPIO-compatible input. The ON pin must be connected and cannot be left floating. The device is designed to control the turnon rate and therefore the inrush current. By controlling the inrush current, power supply sag can be reduced during turnon. The slew rate for each channel is set by connecting a capacitor to GND on the CT pins.

The slew rate is proportional to the capacitor on the CT pin. See the Adjustable Rise Time section to determine the correct CT value for a desired rise time.

The internal circuitry is powered by the VBIAS pin, which supports voltages from 2.5 V to 5.5 V. This circuitry includes the charge pump, QOD (optional), and control logic. For these internal blocks to function correctly, a voltage between 2.5 V and 5.5 V must be supplied to VBIAS.

When a voltage is supplied to VBIAS, the ON1 pin goes low, and the ON2 pins go low, the QOD turns on. This connects VOUT1 and VOUT2 to GND through an on-chip resistor. The typical pulldown resistance ($R_{PD}$) is 270 $\Omega$.

9.2 Functional Block Diagram

![Functional Block Diagram](image-url)
9.3 Feature Description

9.3.1 ON and OFF Control

The ON pins control the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be tied either high or low for proper functionality.

9.3.2 Input Capacitor (Optional)

When the switch turns on into a discharged load capacitor or short-circuit, a capacitor must be placed between VIN and GND to limit the voltage drop on the input supply caused by transient inrush currents. A 1-µF ceramic capacitor (C\text{IN}), placed close to the pins, is sufficient. Higher values of C\text{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, TI recommends having an input capacitor 10x higher than the output capacitor to avoid excessive voltage drop.

9.3.3 Output Capacitor (Optional)

TI highly recommends a C\text{IN} greater than C\text{L}, because of the integrated body diode in the NMOS switch. A C\text{L} greater than C\text{IN} can cause the voltage on VOUT to exceed VIN when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. TI recommends a C\text{IN} to C\text{L} ratio of 10 to 1 for minimizing V\text{IN} dip caused by inrush currents during startup.

9.3.4 QOD (Optional)

The TPS22968 includes a QOD feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 270 Ω and prevents the output from floating while the switch is disabled.

9.3.5 VIN and VBIAS Voltage Range

For optimal R\text{ON} performance, make sure V\text{IN} ≤ V\text{BIAS}. The device is still functional if V\text{IN} > V\text{BIAS}, but it exhibits R\text{ON} greater than what is listed in the Electrical Characteristics (V\text{BIAS} = 5 V) and Electrical Characteristics (V\text{BIAS} = 2.5 V) table. See Figure 30 for an example of a typical device. Notice the increasing R\text{ON} as V\text{IN} exceeds V\text{BIAS} voltage. Be sure to never exceed the maximum voltage rating for V\text{IN} and V\text{BIAS}.

Temperature = 25°C

\[ I_{\text{OUT}} = 200 \text{ mA} \]

![Figure 30. On-Resistance vs Input Voltage](image)

Temperature = 25°C

\[ I_{\text{OUT}} = 200 \text{ mA} \]
Feature Description (continued)

9.3.6 Adjustable Rise Time

A capacitor to GND on the CT pins sets the slew rate for each channel. The capacitor to GND on the CT pins must be rated for 25 V and above. An approximate formula for the relationship between CT and slew rate with \( V_{BIAS} = 5 \) V is shown in Equation 1.

\[
SR = 0.32 \times CT + 13.7
\]

where

- \( SR \) is the slew rate (in \( \mu \)s/V)
- \( CT \) is the capacitance value on the CT pin (in pF)
- The units for the constant 13.7 is in \( \mu \)s/V.  \( (1) \)

Rise time can be calculated by multiplying the input voltage by the slew rate. Table 1 contains rise time values measured on a typical device.

<table>
<thead>
<tr>
<th>CTx (pF)</th>
<th>VIN = 5 V</th>
<th>VIN = 3.3 V</th>
<th>VIN = 2.5 V</th>
<th>VIN = 1.8 V</th>
<th>VIN = 1.5 V</th>
<th>VIN = 1.2 V</th>
<th>VIN = 0.8 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>65</td>
<td>48</td>
<td>41</td>
<td>35</td>
<td>31</td>
<td>29</td>
<td>24</td>
</tr>
<tr>
<td>220</td>
<td>378</td>
<td>253</td>
<td>197</td>
<td>152</td>
<td>131</td>
<td>111</td>
<td>83</td>
</tr>
<tr>
<td>470</td>
<td>704</td>
<td>474</td>
<td>363</td>
<td>272</td>
<td>234</td>
<td>192</td>
<td>140</td>
</tr>
<tr>
<td>1000</td>
<td>1387</td>
<td>931</td>
<td>717</td>
<td>544</td>
<td>449</td>
<td>372</td>
<td>273</td>
</tr>
<tr>
<td>2200</td>
<td>3062</td>
<td>2021</td>
<td>1536</td>
<td>1173</td>
<td>991</td>
<td>825</td>
<td>595</td>
</tr>
<tr>
<td>4700</td>
<td>7091</td>
<td>4643</td>
<td>3547</td>
<td>2643</td>
<td>2213</td>
<td>1828</td>
<td>1349</td>
</tr>
<tr>
<td>10000</td>
<td>14781</td>
<td>9856</td>
<td>7330</td>
<td>5507</td>
<td>4600</td>
<td>3841</td>
<td>2805</td>
</tr>
</tbody>
</table>

(1) RISE TIME (\( \mu \)s) 10% - 90%, \( C_L = 0.1 \) \( \mu \)F, \( C_{IN} = 1 \) \( \mu \)F, \( R_L = 10 \) \( \Omega \), \( V_{BIAS} = 5 \) V

9.4 Device Functional Modes

Table 2 lists the device function table.

<table>
<thead>
<tr>
<th>ONx</th>
<th>VINx to VOUTx</th>
<th>VOUTx to GND</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>Off</td>
<td>On</td>
</tr>
<tr>
<td>H</td>
<td>On</td>
<td>Off</td>
</tr>
</tbody>
</table>
10 Application and Implementation

**NOTE**
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

This section highlights some of the design considerations for implementing this device in various applications. A PSPICE model for this device is also available on the product page for additional information.

10.1.1 Parallel Configuration

To increase the current capabilities and lower the $R_{ON}$ by approximately 50%, both channels can be placed in parallel as shown in Figure 31 (parallel configuration). With this configuration, the CT1 and CT2 pins can be tied together to use one capacitor, CT, as shown in Figure 31. With a single CT capacitor, the rise time is half of the typical rise-time value. Refer to the Table 1 for typical timing values.

![Figure 31. Parallel Configuration](image-url)
Application Information (continued)

10.1.2 Standby Power Reduction

Any end equipment that is powered from the battery has a need to reduce current consumption to keep the battery charged for a longer time. TPS22968 helps to accomplish this by turning off the supply to the modules that are in standby state, and therefore, significantly reduces the leakage current overhead of the standby modules. See Figure 32.

Figure 32. Standby Power Reduction

10.1.3 Power Supply Sequencing Without a GPIO Input

In many end equipments, there is a need to power up various modules in a predetermined manner. The TPS22968 can solve the problem of power sequencing without adding any complexity to the overall system. See Figure 33.

VIN1 must be greater than \( V_{IH} \).

Figure 33. Power Sequencing Without a GPIO Input
Application Information (continued)

10.1.4 Reverse Current Blocking

In certain applications, it may be desirable to have reverse current blocking. Reverse current blocking prevents current from flowing from the output to the input of the load switch when the device is disabled. With the following configuration, the TPS22968 can be converted into a single-channel switch with reverse current blocking. In this configuration, VIN1 or VIN2 can be used as the input and VIN2 or VIN1 is the output. See Figure 34.

![Figure 34. Reverse Current Blocking](image-url)
10.2 Typical Application

This application demonstrates how the TPS22968 can be used to power downstream modules with large capacitances. The example in Figure 35 TPS22968 is powering a 100-µF capacitive output load.

![Typical Application Schematic for Powering a Downstream Module](image)

Figure 35. Typical Application Schematic for Powering a Downstream Module

10.2.1 Design Requirements

For this design example, use the following Table 3 as the input parameters.

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{IN}} )</td>
<td>3.3 V</td>
</tr>
<tr>
<td>( V_{\text{BIAS}} )</td>
<td>5 V</td>
</tr>
<tr>
<td>Load current</td>
<td>4 A</td>
</tr>
<tr>
<td>Output capacitance ( (C_L) )</td>
<td>22 ( \mu \text{F} )</td>
</tr>
<tr>
<td>Allowable inrush current on VOUT due to ( C_L ) capacitor</td>
<td>0.33 A</td>
</tr>
</tbody>
</table>

10.2.2 Detailed Design Procedure

To begin the design process, the designer must know the following:

- \( V_{\text{IN}} \) voltage
- \( V_{\text{BIAS}} \) Voltage
- Load current
- Allowable inrush current on VOUT due to \( C_L \) capacitor

10.2.2.1 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the \( R_{\text{ON}} \) of the device and the load current. The \( R_{\text{ON}} \) of the device depends upon the \( V_{\text{IN}} \) and \( V_{\text{BIAS}} \) conditions of the device. Refer to the \( R_{\text{ON}} \) specification of the device in the Electrical Characteristics \( (V_{\text{BIAS}} = 5 \text{ V}) \) and Electrical Characteristics \( (V_{\text{BIAS}} = 2.5 \text{ V}) \). After the \( R_{\text{ON}} \) of the device is determined based upon the \( V_{\text{IN}} \) and \( V_{\text{BIAS}} \) conditions, use Equation 2 to calculate the VIN to VOUT voltage drop:

\[
\Delta V = I_{\text{LOAD}} \times R_{\text{ON}}
\]

where

- \( \Delta V \) is the voltage drop from VIN to VOUT
- \( I_{\text{LOAD}} \) is the load current
- \( R_{\text{ON}} \) is the On-resistance of the device for a specific \( V_{\text{IN}} \) and \( V_{\text{BIAS}} \) combination

An appropriate \( I_{\text{LOAD}} \) must be chosen such that the \( I_{\text{MAX}} \) specification of the device is not violated.

10.2.2.2 Inrush Current

To determine how much inrush current is caused by the \( C_L \) capacitor, use Equation 3.

\[
I_{\text{INRUSH}} = C_L \times \frac{dV_{\text{OUT}}}{dt}
\]

where
- $I_{\text{INRUSH}}$ is the amount of inrush caused by $C_L$
- $C_L$ is the capacitance on VOUT
- $dt$ is the time it takes for change in $V_{\text{OUT}}$ during the ramp up of VOUT when the device is enabled
- $dV_{\text{OUT}}$ is the change in $V_{\text{OUT}}$ during the ramp up of VOUT when the device is enabled

The device offers adjustable rise time for VOUT. This feature allows the user to control the inrush current during turnon through the CTx pins. The appropriate rise time can be calculated using the design requirements and the inrush current equation (Equation 3). See Equation 4 and Equation 5.

\[330 \text{ mA} = 22 \mu \text{F} \times 3.3 \text{ V} / dt\]  
\[dt = 220 \mu \text{s}\]

To ensure an inrush current of less than 330 mA, choose a CT based on Table 1 or Equation 1 value that yields a rise time of more than 220 μs. See the oscilloscope captures in the Application Curves for an example of how the CT capacitor can be used to reduce inrush current. See Table 1 for correlation between rise times and CT values.

An appropriate $C_L$ value must be placed on VOUT such that the $I_{\text{MAX}}$ and $I_{\text{PLS}}$ specifications of the device are not violated.

10.2.2.3 Thermal Considerations

The maximum IC junction temperature must be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{\text{D(max)}}$, for a given output current and ambient temperature, use Equation 6.

\[P_{\text{D(max)}} = \frac{T_{\text{j(max)}} - T_A}{R_{\theta JA}}\]

where
- $P_{\text{D(max)}}$ is the maximum allowable power dissipation
- $T_{\text{j(max)}}$ is the maximum allowable junction temperature (125°C for the TPS22968)
- $T_A$ is the ambient temperature of the device
- $R_{\theta JA}$ is the junction to air thermal impedance. See the Thermal Information table. This parameter is highly dependent upon board layout.

Equation 7 to Equation 10 and Equation 11 to Equation 13 show two examples to determine how to use this information correctly:

For $V_{\text{BIAS}} = 5 \text{ V}$, $V_{\text{IN}} = 5 \text{ V}$, the maximum ambient temperature with a 4-A load through each channel can be determined by using Equation 7 to Equation 10:

\[P_D = I^2 \times R \times 2 \text{ (multiplied by 2 because there are two channels)}\]  
\[2 \times I^2 \times R = \frac{T_{\text{j(max)}} - T_A}{R_{\theta JA}}\]  
\[T_A = T_{\text{j(max)}} - R_{\theta JA} \times 2 \times I^2 \times R\]  
\[T_A = 125^\circ \text{C} - 62.5^\circ \text{C/W} \times 2 \times (4 \text{ A})^2 \times 27 \text{ m}\Omega = 71^\circ \text{C}\]

For $V_{\text{BIAS}} = 5 \text{ V}$, $V_{\text{IN}} = 5 \text{ V}$, the maximum continuous current for an ambient temperature of 85°C with the same current flowing through each channel can be determined by using Equation 11 to Equation 13:

\[2 \times I^2 \times R = \frac{T_{\text{MAX}} - T_A}{R_{\theta JA}}\]
\[ I = \sqrt{\frac{T_{J \text{MAX}} - T_A}{2 \times R \times R_{\text{J/A}}}} \]  

(12)

\[ I = \sqrt{\frac{125^\circ C - 105^\circ C}{2 \times 27 \text{m}\Omega \times 62.5^\circ C/\text{W}}} = 3.44 \text{ A per channel} \]  

(13)

### 10.2.3 Application Curves

The two scope captures show the usage of a CT capacitor in conjunction with the device. A higher CT value results in a slower rise and a lower inrush current.

![Scope Capture 1](image1.png)

**Figure 36. Inrush Current Without CT Capacitor**

![Scope Capture 2](image2.png)

**Figure 37. Inrush Current With CT = 220 pF**
11 Power Supply Recommendations

The device is designed to operate from a $V_{\text{BIAS}}$ range of 2.5 V to 5.5 V and $V_{\text{IN}}$ range of 0.8 V to 5.5 V. This supply must be well regulated and placed as close to the device pin as possible with the recommended 1-µF bypass capacitor. If the supply is located more than a few inches from the device pins, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10 µF may be sufficient.

12 Layout

12.1 Layout Guidelines

- VIN and VOUT traces must be as short and wide as possible to accommodate for high current.
- Use vias under the exposed thermal pad for thermal relief for high current operation.
- VINx pins must be bypassed to ground with low-ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1-µF ceramic with X5R or X7R dielectric. This capacitor must be placed as close to the device pins as possible.
- VOUTx pins must be bypassed to ground with low-ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the VINx bypass capacitor of X5R or X7R dielectric rating. This capacitor must be placed as close to the device pins as possible.
- The VBIAS pin must be bypassed to ground with low-ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 0.1-µF ceramic with X5R or X7R dielectric.
- The CTx capacitors must be placed as close to the device pins as possible. The typical recommended CTx capacitance is a capacitor of X5R or X7R dielectric rating with a rating of 25 V or higher.

12.2 Layout Example
13 Device and Documentation Support

13.1 Device Support

13.1.1 Development Support
For the TPS22968 and TPS22968-Q1 PSpice Transient Model, see SLVMA29.
For the TPS22968 and TPS22968N-Q1 PSpice Transient Model, see SLVMB9.

13.2 Documentation Support

13.2.1 Related Documentation
For related documentation see the following:
• Managing Inrush Current, SLVA670A
• Quiescent Current vs Shutdown Current for Load Switch Power Consumption, SLVA757
• TPS22968EVM-007 Dual 4A Load Switch, SLVUA30
• Load Switch Thermal Considerations, SLVUA74
• TPS22968/68N-Q1 Dual-Channel 5.5-V 4-A 27-Ω Load Switch EVM User's Guide, SLVUAE2A
• TPS22968NEVM Dual 4 A Load Switch, SLVUAL0

13.3 Related Links
The table below lists quick access links. Categories include technical documents, support and community
resources, tools and software, and quick access to sample or buy.

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<tr>
<th>PARTS</th>
<th>PRODUCT FOLDER</th>
<th>SAMPLE &amp; BUY</th>
<th>TECHNICAL DOCUMENTS</th>
<th>TOOLS &amp; SOFTWARE</th>
<th>SUPPORT &amp; COMMUNITY</th>
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</thead>
<tbody>
<tr>
<td>TPS22968</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
<tr>
<td>TPS22968N</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
</tbody>
</table>

13.4 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper
right corner, click on Alert me to register and receive a weekly digest of any product information that has
changed. For change details, review the revision history included in any revised document.

13.5 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective
contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of
Use.

TI E2E™ Online Community **TI's Engineer-to-Engineer (E2E) Community.** Created to foster collaboration
among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help
solve problems with fellow engineers.

Design Support **TI's Design Support** Quickly find helpful E2E forums along with design support tools and
contact information for technical support.

13.6 Trademarks
E2E is a trademark of Texas Instruments.
Ultrabook is a trademark of Intel.
13.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.8 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
### PACKAGING INFORMATION

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<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
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<td>ACTIVE</td>
<td>WSON</td>
<td>DPU</td>
<td>14</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 105</td>
<td>RB968</td>
<td>Samples</td>
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<td>Samples</td>
</tr>
</tbody>
</table>

1. **The marketing status values are defined as follows:**
   - **ACTIVE:** Product device recommended for new designs.
   - **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
   - **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
   - **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
   - **OBSOLETE:** TI has discontinued the production of the device.

2. **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
   - **RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
   - **Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

3. **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

4. **There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.**

5. **Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.**

6. **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS22968:

- Automotive: TPS22968-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
### TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

#### PACKAGE MATERIALS INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin Quadrant</th>
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*All dimensions are nominal.*
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<td>35.0</td>
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</table>

*All dimensions are nominal*
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
F. This package is Pb–free.
THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

NOTE: All linear dimensions are in millimeters.
NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com [http://www.ti.com].
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
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