INTEGRATED 100-V IEEE 802.3af PD AND DC/DC CONTROLLER

FEATURES

- **Complete 802.3af PoE Interface**
  - **Features derived from the TPS2375**
  - **100 V, 0.6 Ω Internal Pass MOSFET**
  - **Standard and Legacy UVLO Choices**
  - **Fixed 140 mA Inrush Limit**
- **Primary Side DC/DC Converter Control**
  - **Minimum External Component Count**
  - **Current Mode Control**
  - **Isolated and Non-Isolated Topologies**
  - **Programmable Operating Frequency**
  - **Current Sense Leading-edge Blanking**
  - **50% Duty Cycle Limiting**
  - **Voltage Output Error Amplifier**
- **Internal PoE and Converter Sequencing**
- **Industry-Standard 20 Lead Package**
- **Industrial Temperature Range: –40°C to 85°C**

APPLICATIONS

- **All PoE PD Devices Including:**
  - **Wireless Access Points**
  - **VoIP Phones**
  - **Security Cameras**

DESCRIPTION

The TPS23750 integrates the functionality of the TPS2375 with a primary-side dc/dc PWM controller. The designer can create a front-end solution for PoE-PD applications with minimum external components. The TPS23770 is identical to the TPS23750 with the exception of the undervoltage lockout turn-on voltage, which is compatible with legacy systems.

The PoE front end has all the necessary IEEE 802.3af functions including detection, classification, undervoltage lockout and inrush control. The PoE input switch is integrated within the TPS23750.

The dc/dc controller section is designed to support flyback, forward, and nonsynchronous low-side switch buck topologies.

The external switching MOSFET and current sense resistor provide flexibility in topology, power level, and current limit. The full-featured dc/dc controller includes programmable soft start, hiccup type fault limiting, 50% maximum duty cycle, programmable constant switching frequency, and a true voltage-output error amplifier. Additional protection features provide for robust designs.

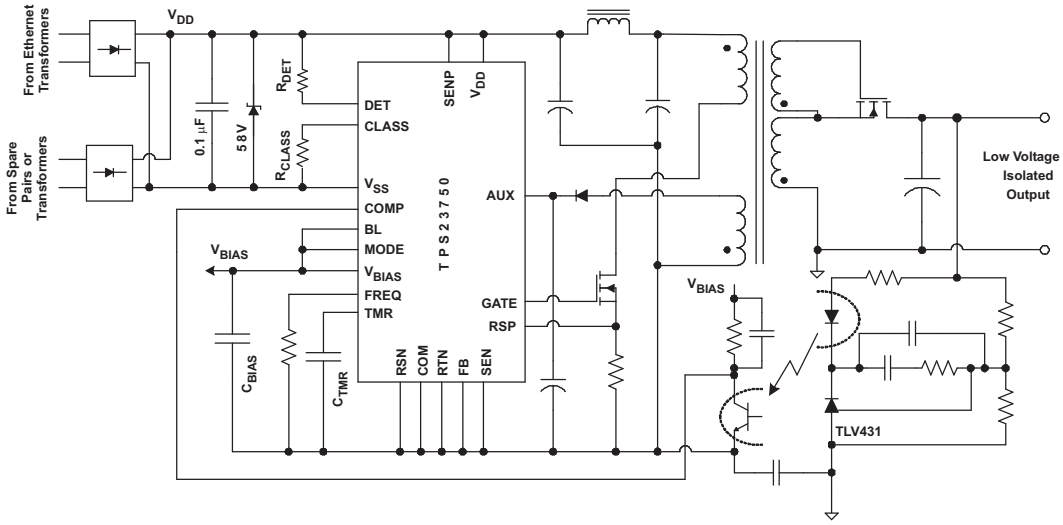


Figure 1. Typical Application

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	UVLO THRESHOLDS			PACKAGE(2)	MARKING
	TYPE	LOW	HIGH	TSSOP-20 PowerPAD™	
–40°C to 85°C	Standard	30.5 V	39.3 V	TPS23750PWP	TPS23750
	Legacy	30.5 V	35.1 V	TPS23770PWP	TPS23770

(1) Add an R suffix to the device type for tape and reel.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range and with respect to V_{SS} unless otherwise noted(1)

			UNIT
	Input voltage range(2)	RSN, COM, RTN, SEN	–0.7 V to 100 V
	Input voltage range	AUX, VDD, DET, SENP	–0.3 V to 100 V
	Input voltage range(3)	[V_{BIAS}, BL, TMR, FB, COMP, FREQ, RSP, MODE] to RTN	–0.3 V to 6.5 V
	Input voltage range	[GATE or AUX] to COM	–0.3 V to 20 V
	Input voltage range	[RSN to RTN] and [COM to RTN]	–0.3 V to 0.3 V
		SENP to SEN	–0.3 V to 100 V
	Input voltage range(3)	CLASS	–0.3 V to 12 V
	Sourcing current	AUX	Internally limited
V_{BIAS}	Sourcing current		Internally limited
	Sourcing or sinking current, COMP		Internally limited
	Average sourcing or sinking current, GATE		25 mA_{rms}
	HBM ESD rating		2 kV
	ESD – system level (contact/air) at RJ-45 (4)		8 kV / 15 kV
	Continuous total power dissipation		See Dissipation Rating Table
T_J	Maximum operating junction temperature		Internally limited
T_{stg}	Storage temperature range		–65°C to 150°C
	Lead temperature 1.6mm (1/16-inch) from case for 10 seconds		260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) I_{RTN} = 0 for V_{RTN} > 80 V. Maximum I_{RTN} = 500 mA at 80 V.
(3) Do not apply external voltage sources to CLASS, DET, GATE, FREQ, V_{BIAS}, and TMR.
(4) Surges applied to RJ-45 of TPS23750EVM-107 between pins of RJ-45, and between pins and output voltage rails per EN61000-4-2, 1999 with no device failure.

RECOMMENDED OPERATING CONDITIONS(1) (2)

All voltage values are with respect to V_{SS} unless otherwise noted.

			MIN	NOM	MAX	UNIT
V_{DD}	Input voltage range(3)	COM, SEN, SENP	0		67	V
	Input voltage range	FB, COMP, MODE, BL	0		V_{BIAS}	V
		AUX to COM	0		16	
		RSP to RSN	0		1	
	Sourcing current	AUX	0		2	mA
		V_{BIAS}	0		2	
		COMP	0		2	
Q_G	GATE loading				20	nC
	AUX load capacitance		0.8		25	µF
	V_{BIAS} load capacitance		0.08		1.5	µF
	R_{FREQ}		30		300	kΩ
T_J	Operating junction temperature range		-40		125	°C
T_A	Operating ambient temperature range		-40		85	°C

(1) RSN, COM, and RTN should be tied together. SENP should be tied to V_{DD} except for the buck configuration, where it should be tied to the output positive rail.
(2) TMR, FREQ, CLASS, DET, V_{BIAS}, and GATE should not be externally driven.
(3) Junction temperature may be a constraining factor for high bias power designs.

DISSIPATION RATINGS TABLE

PACKAGE	θ_{JP} °C/W(1)	θ_{JC} °C/W	θ_{JA} °C/W(2)	θ_{JA} °C/W(3)	θ_{JA} °C/W(4)	MAXIMUM POWER RATING (W)(5)
PWP (TSSOP-20)	1.4	26.62	32.6	151.9	73.8	1.2

(1) Thermal resistance junction to pad.
(2) See TI document SLMA002 for recommended layout. This is a best case, zero airflow number.
(3) JEDEC method with low-k board (2 signal layers) and power pad not soldered (worst case).
(4) JEDEC method with high-k board (4 layers, 2 signal and 2 planes) and power pad not soldered.
(5) Based on TI recommended layout and 85°C ambient.

ELECTRICAL CHARACTERISTICS

Characteristics are for: –40°C ≤ T_J ≤ 125°C; $V_{DD} – V_{SS}$ = 48 V. V_{DD}, CLASS, and DET referenced to V_{SS}, and all other pin voltages are referenced to RSN, COM, and RTN shorted together unless otherwise noted. SEN=MODE=BL=RSP=RTN, FB=V_{BIAS}, SENP=V_{DD}, C_{TMR} = 1000 pF, C_{VBIAS} = 0.1 µF, C_{VAUX} = 0.1 µF, R_{FREQ} = 150 kΩ, R_{DET} = 24.9 kΩ, R_{CLASS} = 255 Ω, GATE is unloaded, and V_{BIAS} and AUX have no external loads unless otherwise noted.

DC/DC CONTROLLER SECTION

RTN = V_{SS} for this section only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS SUPPLY (VBIAS)						
V_{BIAS}	Output voltage	0 ≤ I_{LOAD} ≤ 5 mA	4.60	5.1	5.5	V
AUX SUPPLY (AUX)						
V_{AUX}	Supply output voltage	18 V ≤ $V_{VDD – COM}$ ≤ 57 V, 0 mA ≤ I_{AUX} ≤ 10 mA	9	10	11	V
	Current limit	V_{AUX} = 0 V	12	23.5	28	mA
OSCILLATOR (FREQ)						
D_{MAX}	Maximum duty cycle	R_{FREQ} = 30 kΩ, V_{COMP} = 3.9 V, MODE = V_{BIAS}, Measure GATE voltage at 50% rising to 50% falling	48.8	49.2	49.5	%
f_{OSC}	Oscillator frequency	MODE = V_{BIAS}, V_{COMP} = 3 V, Measure at GATE				kHz
		R_{FREQ} = 30 kΩ	435	487	565	
		R_{FREQ} = 150 kΩ	90	100	110	
ERROR AMPLIFIER (FB, COMP)						
	COMP source current	0 ≤ V_{COMP} ≤ 4 V, FB = RTN, V_{TMR} = 2.5 V	2.5			mA
	COMP sink current	1.2 V ≤ V_{COMP} ≤ V_{BIAS}, V_{TMR} = 2.5 V	2.4			mA
V_{REF}	FB regulation voltage	V_{COMP} = 2.5 V, V_{TMR} = 2.5 V	1.47	1.50	1.53	V
	Open loop voltage gain	1.2 V ≤ V_{COMP} ≤ 4 V, V_{TMR} = 2.5 V	80			dB
	Small signal unity gain bandwidth	V_{COMP} = 2.5 V, V_{TMR} = 2.5 V	1.5	2		MHz
	COMP input resistance	MODE = V_{BIAS}, 1.1 ≤ V_{COMP} ≤ 4.4, V_{TMR} = 2.5 V	70	100	130	kΩ
	FB leakage (source or sink)	0 ≤ V_{FB} ≤ V_{BIAS}, V_{TMR} = 2.5 V			1	µA
SOFT START TIMER (TMR)						
	Source current	TMR charging, V_{TMR} between lower threshold and clamp	38	50	62	µA
	Ratio of source/sink current		9	10	11	-
	ON duty cycle	MODE = V_{BIAS}, V_{COMP} = 4.4 V, Second cycle and beyond	8	9.1	10	%
CURRENT SENSE (RSP, RSN, BL)						
	Current limit threshold	MODE = V_{BIAS}, V_{COMP} = 4.2 V, V_{TMR} = 2.5 V, Increase $V_{RSP-RSN}$ until the duty cycle switches from 50% to the minimum	0.46	0.5	0.54	V
	Fault current threshold	MODE = V_{BIAS}, V_{COMP} = 4.2 V, V_{TMR} = 2.5 V, Increase $V_{RSP-RSN}$ until no gate pulses occur	0.70	0.765	0.83	V
t_{BLNK}	Current limit delay	$V_{RSP – RSN}$ = 0.6 V, V_{AUX} = 12 V, MODE = V_{BIAS}, V_{COMP} = 4.2 V, V_{TMR} = 2.5 V. Measure 50% of V_{GATE} ↑ to 50% V_{GATE} ↓				ns
		Minimum propagation delay, BL floating	40	60	90	
		Blanking period (pulse width above minimum), BL connected to RSN	45	70	95	
		Blanking period (pulse width above minimum), BL connected to V_{BIAS}	70	105	140	
	RSP current	FREQ = V_{BIAS}, MODE = V_{BIAS}, V_{COMP} = 4 V, $V_{RSP-RSN}$ = 0.4 V, I_{RSP} sourcing	2.5	4	8	µA
GATE DRIVER (GATE)						
	Output voltage swing	5 mA source, V_{AUX} = 12 V	11.9			V
		5 mA sink, V_{AUX} = 12 V			0.05	
	Peak source current	V_{AUX} = 12 V, pulse test	0.33	0.58	0.8	A
	Peak sink current	V_{AUX} = 12 V, AC test or pulse test with TMR = RSN	0.7	1.0	1.3	A
VOLTAGE TRANSLATOR (SEN, SENP)						
	(SENP - SEN) regulation voltage	V_{TMR} = 2.5 V, Measure with servo loop that includes the error amplifier	1.456	1.492	1.526	V

DC/DC CONTROLLER SECTION (continued)

RTN = V_{SS} for this section only.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Translator output resistance	$V_{SENP-SEN}$ = 1.5 V, TMR = RSN, I_{FB} = 0 µA and 10 µA, $R_{FB} = \Delta V_{FB} / \Delta I_{FB}$		11.25	15	18.75	kΩ
	SEN sinking current	$V_{SENP-SEN}$ = 1.50 V, V_{TMR} = RSN				1	µA
	SENP sinking current	$V_{SENP-SEN}$ = 1.50 V, V_{TMR} = RSN		17	22.5	28	µA

PoE SECTION

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DETECTION (DET)							
	Offset current	DET open, $V_{DD} = V_{RTN}$ = 1.9 V, Measure $I_{VDD} + I_{RTN} + I_{SENP}$			0.45	4	µA
	Sleep current	DET open, $V_{DD} = V_{RTN}$ = 10.1 V, Measure $I_{VDD} + I_{RTN} + I_{SENP}$			5.6	12	µA
	DET leakage current	$V_{DET} = V_{DD}$ = 57 V, Measure I_{DET}			0.3	5	µA
	Detection current	RTN = V_{DD}, Measure $I_{VDD} + I_{RTN} + I_{DET} + I_{SENP}$	V_{DD} = 1.4 V	51.5	55	58.7	µA
			V_{DD} = 10.1 V	395	411	417	
CLASSIFICATION (CLASS)							
I_{CLASS}	Classification current	RTN = V_{DD}, Measure $I_{VDD} + I_{RTN} + I_{DET} + I_{SENP}$					mA
		R_{CLASS} = 4420 Ω, 13 ≤ V_{DD} ≤ 21 V		2.2	2.5	2.8	
		R_{CLASS} = 953 Ω, 13 ≤ V_{DD} ≤ 21 V		10.3	10.6	11.3	
		R_{CLASS} = 549 Ω, 13 ≤ V_{DD} ≤ 21 V		17.7	18.3	19.5	
		R_{CLASS} = 357 Ω, 13 ≤ V_{DD} ≤ 21 V		27.1	28.0	29.5	
		R_{CLASS} = 255 Ω, 13 ≤ V_{DD} ≤ 21 V		38.0	39.4	41.2	
V_{CL_ON}	Classification lower threshold	Regulator turns on, V_{DD} rising		10.2	11.3	13.0	V
V_{CL_H}		Hysteresis		1	1.75	3	
V_{CU_OFF}	Classification upper threshold	Regulator turns off, V_{DD} rising		21	21.9	23	V
V_{CU_H}		Hysteresis		0.5	0.83	1	
PASS DEVICE (RTN)							
	On resistance	I_{RTN} = 300 mA			0.60	1	Ω
	Current limit	V_{RTN} = 1 V		405	450	515	mA
I_{INR}	Inrush limit	V_{RTN} = 1.6 V		100	140	180	mA
CONTROL							
	Inrush current state termination	I_{RTN} falling from I_{INR}, I_{RTN}/I_{INR}		0.85		1.00	
UVLO							
V_{UVLO_R}	Standard UVLO threshold	V_{DD} rising, monitor I_{RTN}		38.4	39.3	40.4	V
V_{UVLO_F}		V_{DD} falling, monitor I_{RTN}		29.6	30.5	31.5	
		Hysteresis		8.3	8.8	9.1	
V_{UVLO_R}	Legacy UVLO threshold	V_{DD} rising, monitor I_{RTN}		34.1	35.1	36.0	V
V_{UVLO_F}		V_{DD} falling, monitor I_{RTN}		29.7	30.5	31.4	
		Hysteresis		4.3	4.5	4.8	

ELECTRICAL CHARACTERISTICS – COMBINED

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CURRENT						
I_{VDDQ}	Quiescent current			1	1.3	mA
	Operational current	COMP = FB		1.1	1.4	mA
		COMP = FB, R_{FREQ} = 30 kΩ		1.3	1.75	
	Off state current	RTN = COM = RSN = V_{DD}, V_{DD} = 33 V		0.18	0.5	mA
THERMAL SHUTDOWN						
	Shutdown temperature	Temperature rising		140		°C
	Hysteresis			17		°C

DEVICE INFORMATION

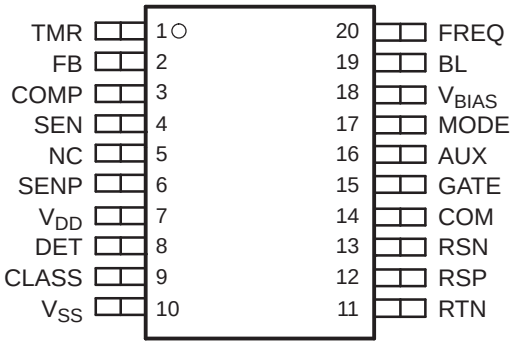
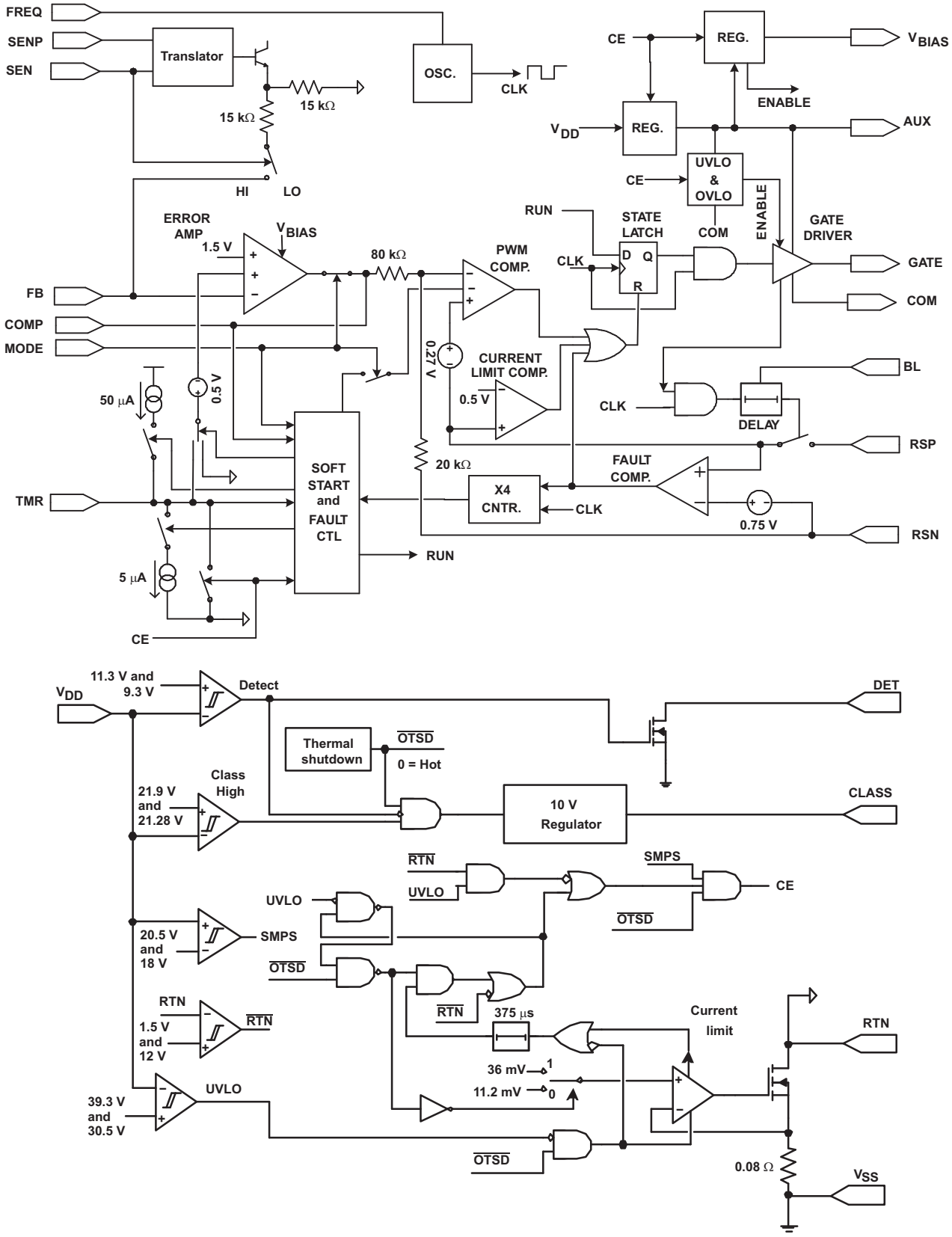


Figure 2. Pinout

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
TMR	1	O	Multifunction pin, serves as a converter soft start and a hiccup timer. A capacitor to RTN determines the softstart and hiccup timing.
FB	2	I	Converter error amplifier inverting input. Tie to RTN when not used.
COMP	3	I/O	Converter error amplifier output and PWM block input. COMP is used for loop compensation or PWM control with an external error amplifier and opto-isolator.
SEN	4	I	Voltage-level translator's sense input and enable; connect to RTN to disable. SEN is regulated to 1.5 V below SENP by the control loop when the translator is used. Typically used in a low-side switch buck converter.
NC	5	-	No connect. There are no internal connections.
SENP	6	I	Voltage-level translator's positive reference voltage (sense positive) used in conjunction with SEN. Tie to the regulated voltage positive rail when the translator is used, and V_{DD} otherwise.
V_{DD}	7	PWR	Positive supply input.
DET	8	O	PoE detection pin; a 24.9 kΩ resistor to V_{DD} establishes a valid signature. It is pulled to V_{SS} during detection.
CLASS	9	O	Classification pin for PoE. A resistor to V_{SS} sets the PoE device class. This pin is driven to 10 V during classification.
V_{SS}	10	PWR	Negative supply input from the PoE feed (after required ORing bridges).
RTN	11	I	The switched PoE negative output. RTN is the converter's negative input rail. COM and RSN should be tied to RTN.
RSP	12	I	Connect to the converter switching MOSFET current-sense resistor (current Sense Resistor Positive end).
RSN	13	I	Converter switching MOSFET current-sense reference (current Sense Resistor Negative end) and quiet analog return (ground). Connect to RTN.
COM	14	I	Converter MOSFET gate driver circuit return. Connect to RTN.
GATE	15	O	Converter switching MOSFET gate drive.
AUX	16	I/O	Converter gate driver supply; outputs 10 V and can accept inputs up to 16 V. Connect a bypass capacitor to COM.
MODE	17	I	Connect to V_{BIAS} to disable the error amplifier, otherwise to RTN.
V_{BIAS}	18	O	Converter internal 5 V bias supply output, also used to bias external optocoupler. A bypass capacitor to RTN is required.
BL	19	I	Converter current sense blanking selector. Leave floating for minimum blanking, tie BL to RTN for a short period, and to V_{BIAS} for a long period.
FREQ	20	I	Connect a resistor to RTN to program the switching frequency.
PowerPAD	-	PWR	Internally connected to V_{SS}; used to heatsink the part to the circuit board traces. Must be connected to the V_{SS} pin.

BLOCK DIAGRAM



DETAILED DESCRIPTION

AUX – This pin is the junction between the internal 10 V converter-bias regulator, the gate driver supply, and the 5-V regulator that powers the rest of the converter control circuit. Voltage may be applied to this pin during normal converter operation to improve efficiency and reduce the TPS23750 temperature rise. A UVLO of about 8 V monitors $V_{AUX-COM}$ to prevent operation with inadequate or weak bias. A converter overvoltage lockout protects the IC when a bias winding is used and V_{AUX} rises above 17.5 V.

A low ESR bypass capacitor of at least 0.8 µF must be connected from AUX to COM.

BL – This pin selects the desired blanking operation. The blanking function prevents the sensed MOSFET current from tripping the PWM and current limit comparators for a predetermined period after the GATE switches high. This prevents the comparators from being falsely triggered by the gate drive current and recovery currents in the external power rectifiers. The recovery currents are strongly influenced by the topology, device selection, and device parasitics. The current limit comparator, logic, and gate driver account for the minimum delay which is obtained with the BL pin open. There are two preset delay choices, as shown below. Shorter periods may be obtained by leaving BL open and using an RC filter.

Table 1. BL Connections

BL CONNECTION	BLANKING OPERATION
Open	None (Minimum current-sense loop delay)
RSN	Minimum plus 70 ns
V_{BIAS}	Minimum plus 105 ns

CLASS – Classification is a PoE function implemented by means of an external resistor, R_{CLASS}, connected between CLASS and V_{SS}. Current is drawn from V_{DD} through R_{CLASS} for input voltages between 13 V and 21 V. Classification allows the PD to indicate the required average power requirements to the PSE as shown in Table 2.

Table 2. Classification

CLASS	PD POWER (W)	R_{CLASS} (Ω)	802.3af CLASS CURRENT LIMITS (mA)	NOTE
0	0.44 – 12.95	4420 ±1%	0 – 4	Default class
1	0.44 – 3.84	953 ±1%	9 – 12	
2	3.84 – 6.49	549 ±1%	17 – 20	
3	6.49 – 12.95	357 ±1%	26 – 30	
4	Reserved	255 ±1%	36 – 44	Treated like class 0

Approximately 10 V is applied to the CLASS resistor for up to 75 ms. The resistor's wattage rating need only be based on this transient condition.

The CLASS pin must not be shorted to ground. The recommended CLASS 0 resistor serves as a bleeder for capacitance connected around the TPS23750 after power is removed.

COM – Switching regulator gate driver return. This signal is internally separated from RTN and RSN to minimize noise coupling, but it should always be connected to RSN and RTN on the circuit board.

COMP – The TPS23750 is a traditional current-mode controller. The COMP pin represents the junction between the voltage control loop's error amplifier output and the current control loop's reference input. The name refers to the traditional connection of loop compensation components, which are connected between COMP and FB.

MODE alters the function of COMP. If MODE is tied to RTN, the internal error amplifier is enabled. If MODE is tied to V_{BIAS}, the internal amplifier disconnects from COMP, allowing an optocoupler to be fed directly into the PWM comparator circuit. The COMP pin should only be driven between RTN and V_{BIAS} when in this mode. Tie FB to RTN when the amplifier is disabled.

The current-mode control range includes COMP voltages between 1.35 V and just under 4 V. Converter switching is inhibited for COMP voltages below 1.35 V. COMP voltages higher than of 4.1 V cause the TMR circuit to begin hiccup operation. COMP is forced low during a hiccup-cycle off period when the internal error amplifier is used.

The COMP output should not be over-driven when the internal error amplifier is active. The amplifier can source and sink significant currents which will greatly increase power dissipation. TMR may be pulled low to turn the converter off when the internal error amplifier is used. The error amplifier will source current when COMP is pulled below its saturated low voltage due to the nature of the class AB amplifier stage.

DET – Connect a 24.9 kΩ, ±1% resistor (R_{DET}), between DET and V_{DD}. R_{DET} is connected across the input line when V_{DD} lies between 1.4 V and 10.1 V, and is disconnected when the line voltage exceeds 12 V to conserve power. R_{DET} may be adjusted to compensate for input diode characteristics.

FB – This is the internal dc/dc converter error amplifier's inverting input. FB is used for output voltage feedback and loop compensation. FB equals 1.5 V when the feedback loop is in regulation. FB should be tied to RTN when the error amplifier is disabled using MODE. The internal level translator drives this pin with a source impedance of about 15 kΩ when it is enabled using SEN.

FREQ – A resistor connected from FREQ to RTN programs the converter switching frequency. This feature allows an existing design to be easily upgraded to use the TPS23750 without requiring redesign of the magnetics and filtering. While the oscillator is characterized between 100 kHz and 500 kHz, it operates properly down to a frequency of a few kilohertz.

$$R_{FREQ}(k\Omega) = \frac{15000}{Switching\_Frequency\ (kHz)} \quad (1)$$

Although this expression is reasonably accurate, the frequency will be slightly lower than predicted at higher frequencies.

FREQ must not be shorted to ground or have voltage applied.

GATE – DC/DC converter's switching MOSFET driver output. This pin has an internal pull-down to keep the external switching MOSFET off when the converter is inactive.

MODE – This pin disables the converter error amplifier, allowing an optocoupler to drive the PWM comparator directly from COMP. Connecting MODE to RTN enables the error amplifier, and to V_{BIAS} disables it. MODE should not be left floating.

RSN – This pin is the current-mode controller's quiet "ground" reference for current sensing and other low-level signals. RTN, RSN, and COM should be tied together.

RSP – This pin is the current-mode controller's current-sense input. Current-mode control monitors the switching MOSFET peak current, which is sensed as voltage between RSP and RSN, to set the PWM duty cycle. The peak current limit is established by limiting the maximum sense voltage to about 0.5 V.

MOSFET current may rise to high levels during the blanking period when there is a short in the power circuit. If the RSP peak voltage exceeds 0.75 V on four successive switching cycles, the converter is turned off and a hiccup cycle is started.

If the blanking is sufficient to eliminate the need for an input RC filter, this pin may be directly connected to the sense resistor.

RTN – An internal MOSFET connects this pin to V_{SS}. This MOSFET is controlled by the PoE section UVLO, inrush limit, current limit, thermal limit, and fault voltage limiting.

Most applications connect RSN, COM, and RTN together through a ground plane.

SEN – SEN is the negative input for the level translator. It can be used in buck converters as demonstrated in Figure 40. The translator is enabled by connecting SEN above 1 V with respect to RTN. The level translator applies $V_{SENP-SEN}$ to the FB pin through an internal 15 kΩ resistor. This feature simplifies feedback voltage sensing above RTN. Connect SEN to RSN if the level translator is not used.

SENP – SENP is the positive input for the level translator. It is used in conjunction with SEN as demonstrated in Figure 40. The presence of this pin allows a filter inductor to be placed in the positive power rail between V_{DD} and the output. Connect SENP to V_{DD} when the level translator is disabled. The voltage on SENP should always be greater than the voltage on SEN.

TMR – Connect a capacitor from TMR to RTN to program the softstart and hiccup timer functions. Pull this pin to RTN to disable the converter.

TMR controls softstart, overload time-out, and automatic restart on overload, which is referred to as a hiccup function.

V_{BIAS} – This 5-V bias supply powers the bulk of the converter functions. V_{BIAS} can be used to power the feedback optocoupler in isolated applications. External loading should be minimized to avoid excessive power dissipation. V_{BIAS} has a UVLO function that inhibits converter operation at outputs of less than 4.6 V. V_{BIAS} should be bypassed with a capacitor between 0.08 µF and 1.5 µF. Do not apply external bias to this pin.

V_{DD} – This is the positive power pin to the IC.

V_{SS} – Common ground for the internal PoE circuits. This pin is connected to the low side of the rectified PoE voltage. An internal power MOSFET connects RTN to V_{SS} under control of the PoE section. The PowerPAD on the bottom of the package is internally connected to V_{SS}. The PowerPAD is used to remove heat from the die through the PCB.

TYPICAL CHARACTERISTICS

V_{BIAS} VS LOAD CURRENT

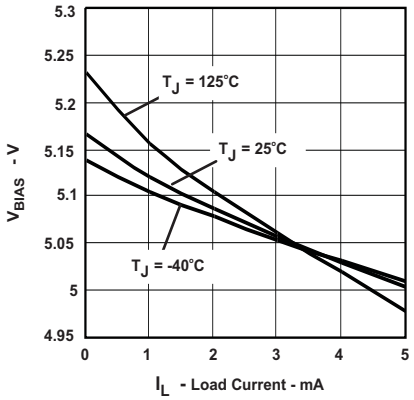


Figure 3.

V_{BIAS} CURRENT LIMIT VS JUNCTION TEMPERATURE

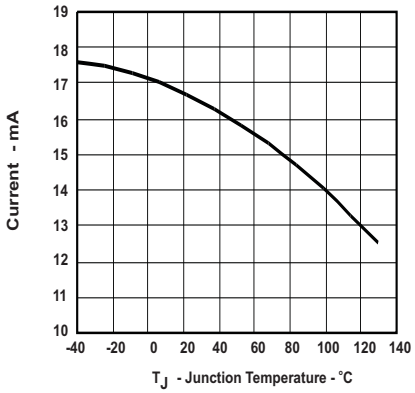


Figure 4.

AUX VOLTAGE VS LOAD CURRENT

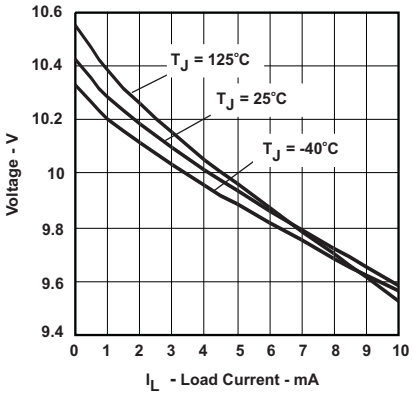


Figure 5.

AUX CURRENT LIMIT VS JUNCTION TEMPERATURE

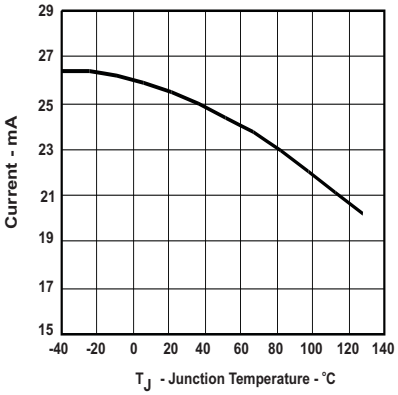


Figure 6.

ERROR AMPLIFIER SOURCE CURRENT VS V_{COMP}

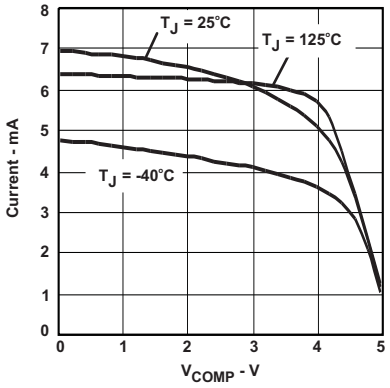


Figure 7.

ERROR AMPLIFIER SINK CURRENT VS V_{COMP}

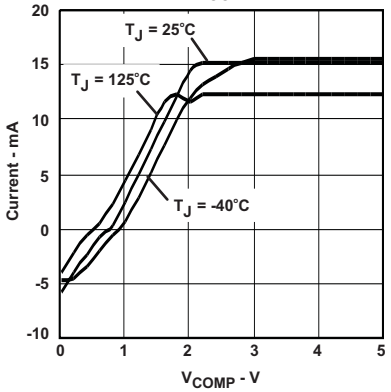


Figure 8.

ERROR AMPLIFIER GAIN AND PHASE VS FREQUENCY

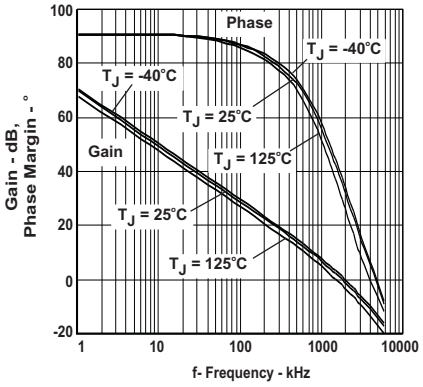


Figure 9.

FB REGULATION VOLTAGE VS JUNCTION TEMPERATURE

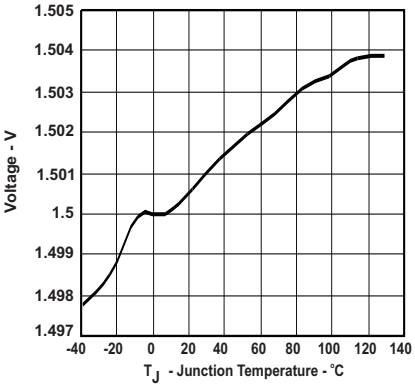


Figure 10.

TMR SOURCE CURRENT VS JUNCTION TEMPERATURE

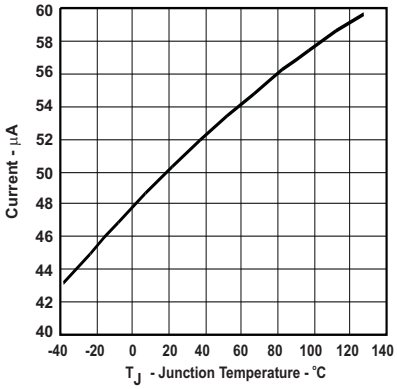


Figure 11.

TYPICAL CHARACTERISTICS (continued)

TMR SOURCE/SINK CURRENT RATIO vs JUNCTION TEMPERATURE

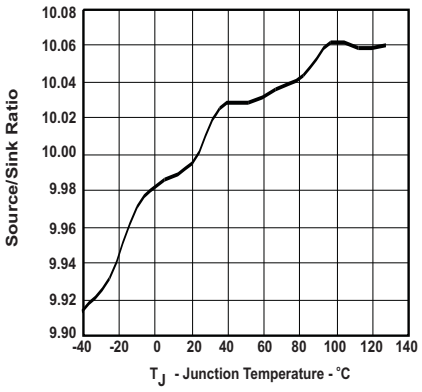


Figure 12.

CONVERTER CURRENT LIMIT THRESHOLD (V_{RSP}) vs JUNCTION TEMPERATURE

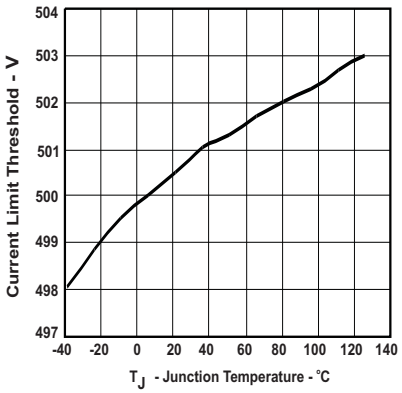


Figure 13.

RSP SOURCE CURRENT vs JUNCTION TEMPERATURE

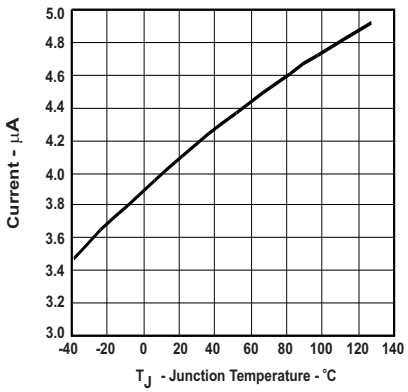


Figure 14.

GATE OUTPUT RESISTANCE vs JUNCTION TEMPERATURE

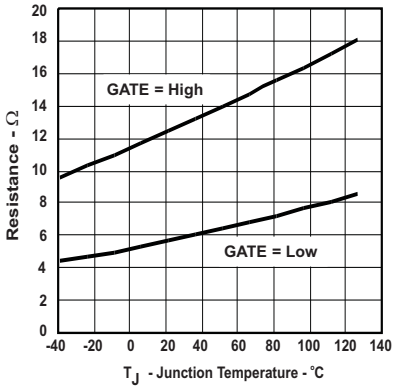


Figure 15.

GATE PEAK DRIVE CURRENT vs JUNCTION TEMPERATURE

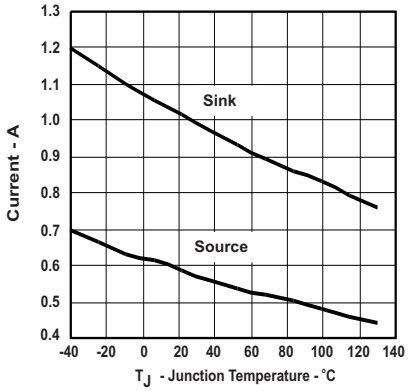


Figure 16.

SENP SINKING CURRENT vs JUNCTION TEMPERATURE

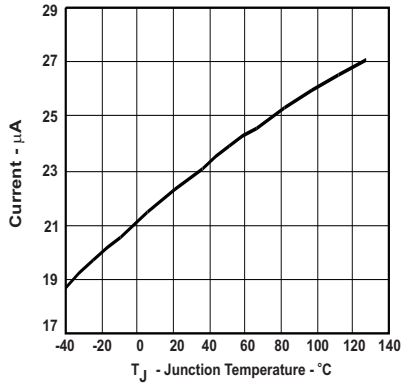


Figure 17.

SEN SINKING CURRENT vs JUNCTION TEMPERATURE

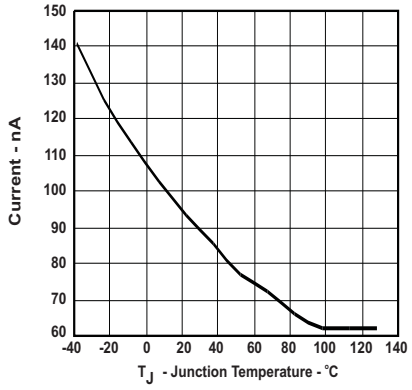


Figure 18.

(SENP - SEN) REGULATION VOLTAGE vs JUNCTION TEMPERATURE

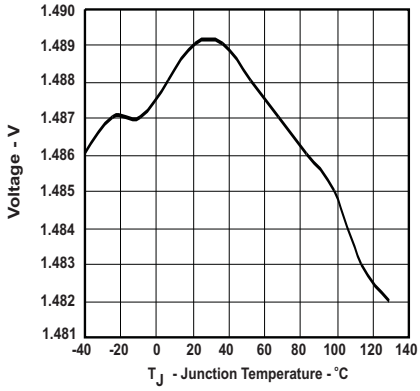


Figure 19.

TRANSLATOR OUTPUT RESISTANCE vs JUNCTION TEMPERATURE

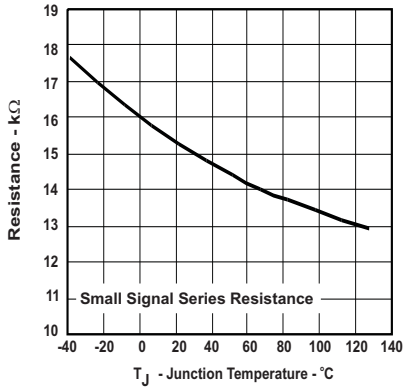


Figure 20.

TYPICAL CHARACTERISTICS (continued)

(V_{DD} + RTN + SENP) DETECTION CURRENT vs SUPPLY VOLTAGE

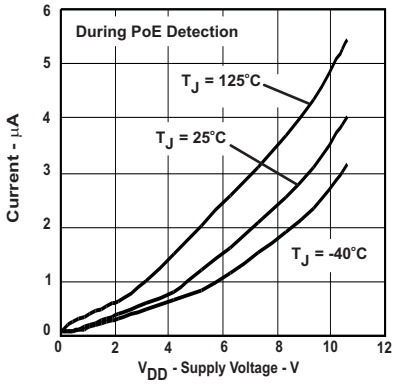


Figure 21.

PoE CURRENT LIMIT vs JUNCTION TEMPERATURE

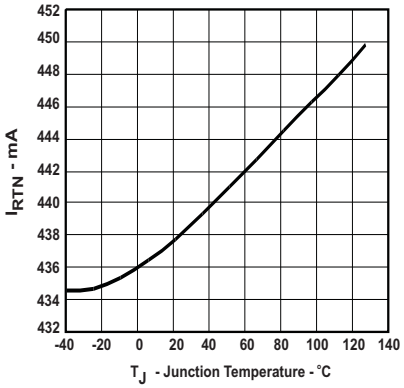


Figure 22.

MAXIMUM DUTY CYCLE vs OSCILLATOR FREQUENCY

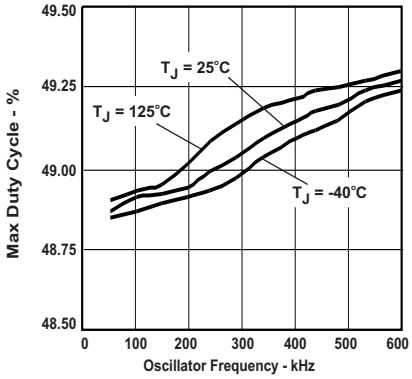


Figure 23.

CONVERTER CURRENT LIMIT RESPONSE TIME vs JUNCTION TEMPERATURE

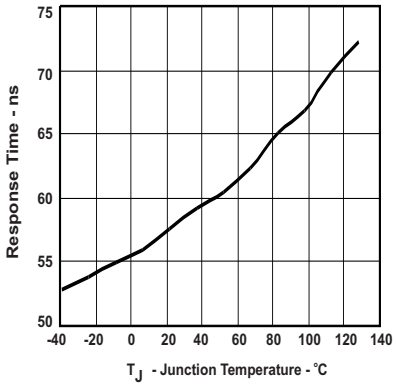


Figure 24.

BLANKING TIME vs JUNCTION TEMPERATURE

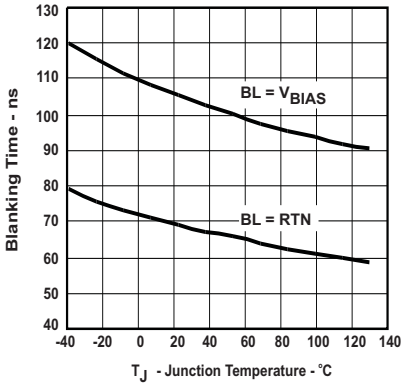


Figure 25.

OSCILLATOR FREQUENCY vs 15000/R_{FREQ}

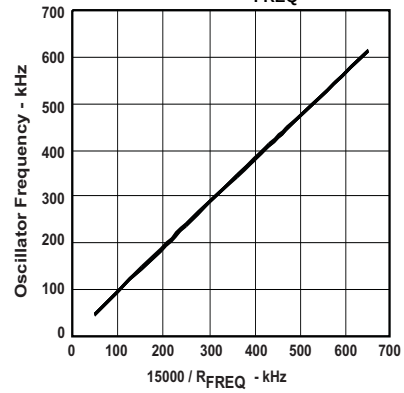


Figure 26.

PD DETECTION RESISTANCE vs VOLTAGE, V_{PI}

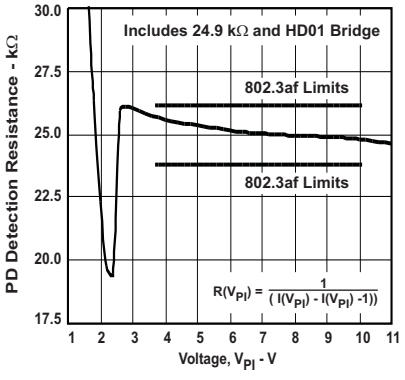


Figure 27.

OPERATING CURRENT (I_{VDD}) vs JUNCTION TEMPERATURE

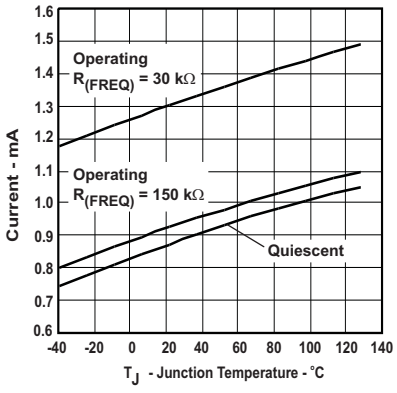


Figure 28.

APPLICATION INFORMATION

PoE OVERVIEW

The following text is intended as an aid in understanding the operation of the TPS23750 but not as a substitute for the actual IEEE 802.3af standard. Standards change and should always be referenced when making design decisions.

The IEEE 802.3af specification defines a method of safely powering a PD over a cable, and then removing power if a PD is disconnected. The process proceeds through the three operational states of detection, classification, and operation. The PSE leaves the cable unpowered while it periodically looks to see if something has been plugged in; this is referred to as detection. The low power levels used during detection are unlikely to damage devices not designed for PoE. If a valid PD signature is present, then the PSE may optionally inquire how much power the PD requires; this is referred to as classification. The PD may return a default full-power signature, or one of four other choices. The PSE may then power the PD if it has adequate capacity. Once started, the PD must present the maintain power signature (MPS) to assure the PSE that it is still there. The PSE monitors its output for a valid MPS, and turns the port off if it loses the MPS. Loss of the MPS returns the PSE to the initial state of detection. Figure 29 shows the operational states as a function of PD input voltage.

The PD input is typically an RJ-45 eight-lead connector which is referred to as the power interface (PI). PD input requirements differ from PSE output requirements to account for voltage drops in the cable and operating margin. The specification uses a cable resistance of 20 Ω to derive the voltage limits at the PD from the PSE output requirements. Although the standard specifies an output power of 15.4 W at the PSE output, only 12.95 W is available at the input of the PD due to the worst-case power loss in the cable.

The PSE can apply voltage either between the RX and TX pairs (pins 1–2 and 3–6), or between the two spare pairs (4–5 and 7–8). The applied voltage can be of either polarity and can only be applied to one set of pairs at a time. The PD uses input diode bridges to accept power from any of the possible PSE configurations. The voltage drops associated with the input bridges create a difference between the IEEE 802.3af limits at the PI and the TPS23750 specifications.

The PSE is required to current limit at an average of between 350 mA and 400 mA during normal operation, and it must disconnect the PD if it draws this current for more than 75 ms. Class 0 and 3 PDs may draw up to 400 mA peak currents. The PSE may set lower output current limits based on the PD's declared power requirements, as discussed below.

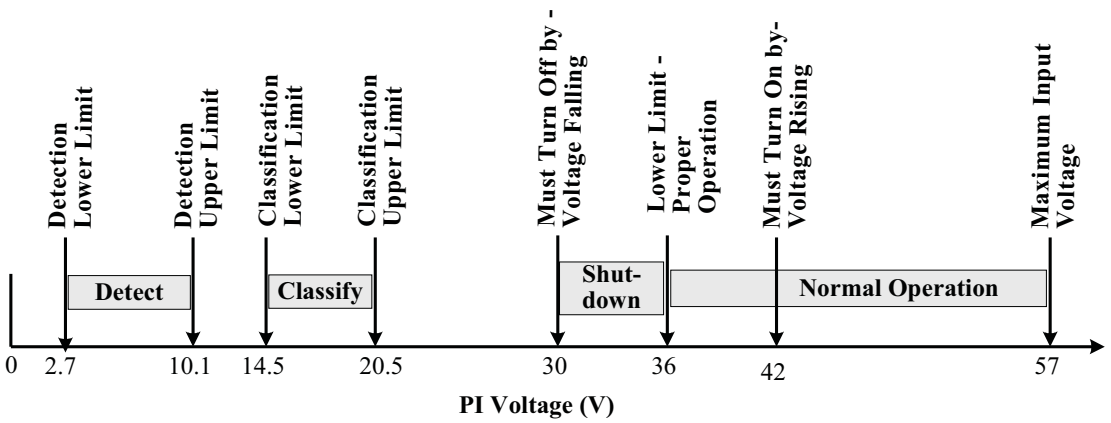


Figure 29. IEEE 802.3 PD Limits

PoE THRESHOLDS

The TPS23750 has a number of internal comparators with hysteresis for stable switching between the various states as shown in Figure 29. Figure 30 relates the parameters in the Electrical Characteristics section to the PoE states. The mode labeled *idle* between classification and operation implies that the DET, CLASS, and RTN pins are all high impedance.

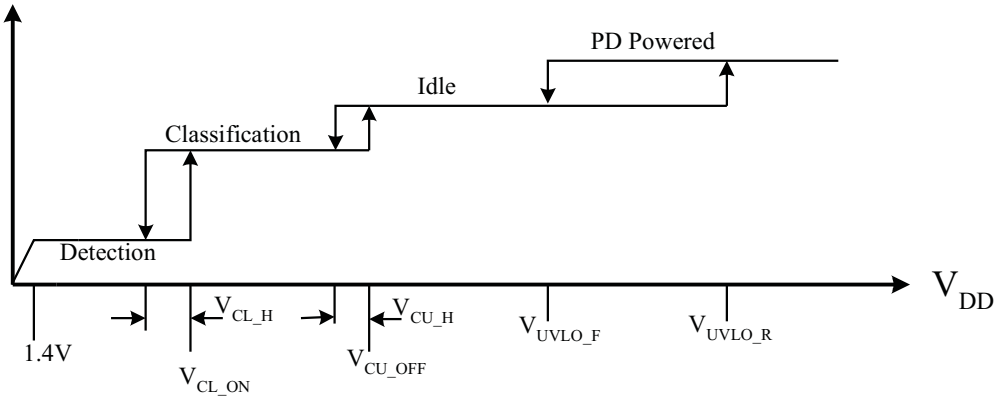


Figure 30. Threshold Voltages

DETECTION

This feature of IEEE 802.3af reduces the risk of damaging Ethernet devices not intended for application of 48 V. When a voltage in the range of 2.7 V to 10.1 V is applied to the PI, an incremental resistance of 25 kΩ signals the PSE that the PD is both capable of, and ready to, accept power. The incremental resistance is measured by applying at least two different voltages to the PI and measuring the current it draws. These two test voltages must be within the specified range and be at least 1 V apart. The incremental resistance equals the difference between the voltages divided by the difference between the currents. The allowed range of resistance is 23.75 kΩ to 26.25 kΩ.

The TPS23750 is in detection mode whenever the supply voltage is below the lower classification threshold. The TPS23750 draws a minimum of bias power in this condition, while RTN is high impedance and almost all the internal circuits are disabled. The DET pin is pulled to ground during detection, so a 24.9 kΩ, 1% resistor from V_{DD} to DET presents the correct signature. R_{DET} may be a small, low-power resistor since it only sees a stress of about 5 mW. When the input voltage rises above the 11.3 V upper detection comparator threshold, the DET pin goes to an open-drain condition to conserve power.

The input diode bridge's incremental resistance may be hundreds of Ohms at the very low currents seen at 2.7 V on the PI. The bridge's resistance is in series with R_{DET} and increases the total resistance seen by the PSE. The nonlinearity in the detection signature of Figure 29 is caused by the diode bridge. This varies with the type of diode selected by the designer, and it is not usually specified on the diode data sheet. The value of R_{DET} may be adjusted downwards to accommodate a particular diode type.

CLASSIFICATION

Once the PSE has detected a PD, it may optionally classify the PD. Classification allows a PSE to determine a PD's power requirements rather than assuming every PD requires 15.4 W, which allows the PSE to power the maximum number of PDs from its 48-V power supply. This step is optional because some PSEs can afford to allot the full power to every powered port.

The classification process applies a voltage between 14.5 V and 20.5 V to the input of the PD, which in turn draws a fixed current set by R_{CLASS}. The PSE measures the PD current to determine which of the five available classes (see Table 2) that the PD falls into. The total current drawn from the PSE during classification is the sum of bias currents and current through R_{CLASS}. The TPS23750 disconnects R_{CLASS} at voltages above the classification range to avoid excessive power dissipation (see Figure 29 and Figure 30).

The value of R_{CLASS} should be chosen from the values listed in Table 2 based on the average power requirements of the PD. The power rating of this resistor should be chosen so that it is not overstressed for the required 75 ms classification period, during which 10 V is applied. The PD could be in classification for extended periods during bench test conditions, or if an auxiliary power source with voltage within the classification range is connected to the PD front end. Thermal protection may activate and turn classification off if it continues for more than 75 ms, but the design must not rely on this function to protect the resistor.

NORMAL OPERATION AND PoE UNDERVOLTAGE LOCKOUT (UVLO)

The TPS23750 incorporates an undervoltage lockout (UVLO) circuit that monitors PoE input voltage to determine when to apply power to the converter, allowing the PD to power up and run. The IEEE 802.3af specification dictates a maximum PD turn-on voltage of 42 V and a minimum turn-off voltage of 30 V (see Figure 30). The IEEE 802.3af standard assumes an 8 V drop in the cabling based on a 20 Ω feed resistance and a 400 mA maximum inrush limit. Because the minimum PSE output voltage is 44 V, the PD must continue to operate properly with input voltages as low as 36 V. The TPS23750 allows an input diode drop of 1.5 V and sets its nominal turn-on at 39.3 V and its turn-off at 30.5 V, while the TPS23770 turns on at 35 V with the same turn-off.

The TPS23770 UVLO limits are designed to support legacy systems whose minimum output voltage is less than 44 V. These systems required a lower turn-on voltage and smaller hysteresis. Although the TPS23770 works with compliant PSEs, it could potentially exhibit startup instabilities if the PSE output voltage rises slowly. The TPS23750 is recommended for applications with compliant PSEs.

The MPS is an electrical signature presented by the PD to assure the PSE that it is still present. A valid MPS consists of a minimum dc current of 10 mA and an ac impedance lower than a series 26.25 kΩ and 0.05 µF load. The ac impedance is usually overshadowed by the minimum capacitance requirement of 5 µF.

PD STATE MACHINE AND CONVERTER OPERATION

The TPS23750 incorporates a state machine that controls the inrush and operational current limit states. When V_{DD} is below the lower UVLO limit, the pass MOSFET is off. Consequently, the RTN pin is high impedance, and at V_{DD} once the output capacitor is discharged by the converter. When V_{DD} rises above the UVLO turn-on threshold with RTN high, the TPS23750 enables the internal power MOSFET with the current limit set to 140 mA. The converter is disabled while the output capacitor charges and V_{RTN} falls from V_{DD} to nearly V_{SS}. Once the inrush current falls about 10% below the programmed limit, the current limit switches to the internal 450 mA operational level after a 375 µs delay. The converter section is enabled once the current limit is switched and the converter begins a softstart cycle. If the input voltage drops below the lower UVLO, the PoE MOSFET turns off, but the converter is allowed to operate to a (V_{VDD}- V_{SS}) of about 18 V.

The internal pass MOSFET is protected against output faults with a current limit and a form of foldback when it is operating in the full current limit state. The PSE output cannot be relied on to protect the PD MOSFET against transient conditions, so the PD implements its own output protection. High stress conditions include converter output shorts, shorts from V_{DD} to RTN, or transients on the input line. An overload on the pass MOSFET engages the current limit, with (V_{RTN} - V_{SS}) rising as a result. If V_{RTN} rises above 12 V, the current limit state machine resets to the 140 mA inrush current limit, and turns off the converter. The thermal shutdown activates to protect the device if the power dissipation from current limit overheats the TPS23750 as described in the thermal protection section below. The RTN comparator is capable of detecting even short excursions of RTN over 12 V that can be caused during overloads and input transients. If the fault that caused the overload disappears, the TPS23750 goes through a normal startup cycle as discussed above. This form of protection limits the peak dissipation in the MOSFET, prevents lockup of the converter in current limit, protects the load from a harmful voltage droop, and allows an orderly recovery from a known state if the problem disappears.

The TPS23750 allows startup and operation from a 24 V to 48 V adapter when it is connected from V_{DD} to RTN without PoE power available. Converter operation is enabled if

- The PoE section is not in inrush, and
- V_{DD} - V_{SS} has exceeded 20.5 V with RTN less than 1.5 V, and
- V_{DD} - V_{SS} is greater than 18 V.

The thresholds are defined in terms of V_{DD} - V_{SS} even though the converter really operates from V_{DD} to RTN. The internal PoE pass MOSFET has a reverse diode which clamps V_{SS} to one diode drop above RTN when the device is powered from the output side.

PoE STARTUP EXAMPLE

Figure 31 demonstrates detection, classification, and startup. The PSE controls the voltage on the PI, while the PD controls the current. The waveforms presented are the PI voltage, PI current, and dc/dc converter output voltage. Testing with different PSEs may result in waveforms that are not exactly the same because the IEEE 802.3af standard allows for different implementations.

The first event is detection. Two voltage levels of about 4 V and 8 V are seen, but the detection current levels are not seen because of the current scale. The second event is classification. The PD draws about 28 mA while the PI voltage is about 17 V, indicating it is a class 3 device. The third event is startup. The PI voltage ramps to about 46 V and the PD draws an inrush current between 120 mA and 140 mA as the downstream bulk capacitor is charged. The PI current drops once the bulk capacitor is charged, allowing the inrush state to terminate and the converter to enable. The final event is converter startup into a fixed 1-Ω load. The converter output voltage ramps to 3.3 V with a corresponding PI current draw. The PI current increases to a steady-state value of 260 mA with only a small overshoot as the output capacitor is charged. The PD is powered, and the applications circuits are operational at the end of startup.

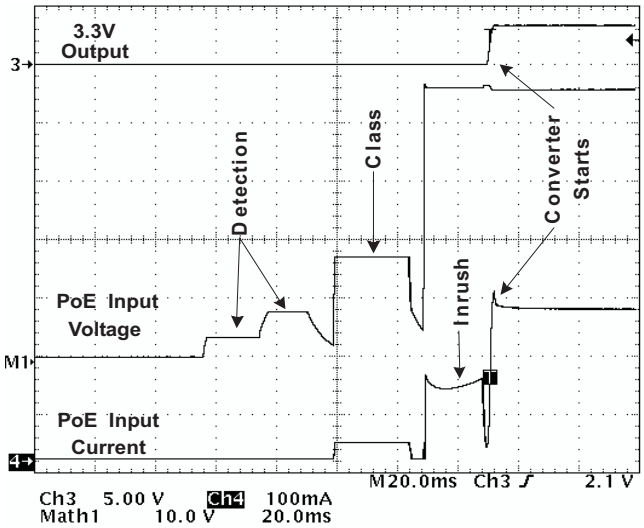


Figure 31. Typical Startup Waveforms

THERMAL PROTECTION

The TPS23750 enters a low-power mode if the die temperature exceeds 140°C. The pass MOSFET, dc/dc converter, AUX regulator, and CLASS regulator are turned off when this occurs. Sources of internal dissipation include bias currents, the pass MOSFET, and the AUX, V_{BIAS}, and CLASS regulators. Loading on AUX and V_{BIAS} is a dominant contributor when the AUX rail is not externally biased. The TPS23750 automatically restarts when the die temperature has fallen approximately 17°C with the pass MOSFET set in the inrush state, the converter disabled, and the TMR capacitor discharged.

The TPS23750 is built using a PowerPAD package to provide a low thermal resistance from the junction to the circuit board. The PowerPAD should be soldered to a large copper area on the circuit board to provide good thermal performance.

Other sources of local PCB heating should be considered during the thermal design. Typical calculations assume that the TPS23750 is the only heat source contributing to the PCB temperature rise.

CONVERTER CONTROLLER OVERVIEW

The TPS23750 dc/dc controller implements a typical current-mode control topology reminiscent of the UC3844, but with a number of enhancements.

A class AB inverting error amplifier, with a 1.5 V fixed reference, connects between input FB and output COMP. The error amplifier has a 1.5 MHz gain-bandwidth product and can source or sink several milliamps. This amplifier can be disabled to allow an optocoupler feedback circuit to drive the PWM section

COMP is also the input to the current-mode PWM section. A 1/5 divider scales the COMP input to the current comparators. Offsets built into the comparator assure that the duty cycle can be driven to 0%. The current limit comparator threshold of 0.5 V on the RSP pin provides a regulated current limit. The fault comparator detects a runaway condition when the peak voltage on RSP is greater than 0.75 V. This can occur with a shorted transformer winding, a short on the switching MOSFET drain, or a shorted buck converter inductor. The TPS23750 shuts down immediately after four consecutive fault comparator trips and enters a TMR-based hiccup cycle.

The duty cycle is limited to 50% based on typical circuits used in PoE, providing a number of benefits. First, it eliminates the complexity of a stabilizing current ramp. Second, it gives an assured reset period for the magnetics. Third, many forward converters with a 1:1 reset winding require a 50% or less duty cycle. Most applications that use a transformer or buck-mode converter prefer this lower duty cycle.

User-programmable current sense blanking eliminates the need for an RC filter. A 70 ns blanking period is provided to serve higher-frequency switching circuits with low output-rectifier recovery periods. A 115 ns blanking period is provided to serve medium-to-slow frequency circuits that have significant gate drive and recovery requirements. The minimum blanking option is provided to allow short period RC filters to be used.

The TMR pin provides a closed-loop softstart when the error amplifier is used. An open-loop softstart is provided if the internal error amplifier is disabled. TMR also implements a synthesized hiccup, or pause and restart, to limit average power dissipation when there is a fault in the converter. Cascading failures are avoided during a fault because the converter operates only about 9% of the time, allowing the power components to cool. A hiccup can be triggered when the COMP pin is railed high for a programmed period, which occurs when there is an overload, or the input voltage is too low.

The internal bias regulators eliminate external bootstrap resistors and startup regulators. The internal regulators allow the converter to start and run as soon as inrush completes. This avoids the pitfalls associated with the bootstrap-startup topology including failure to start and excessive startup delay.

Some PD designs use a 24 V wall adapter to operate when PoE is not available. The converter control allows startup with at least 20.5 V applied V_{DD} - RTN, and operation down to about 18 V.

ERROR AMPLIFIER CONNECTIONS

The TPS23750 accommodates many types of converters and feedback methods. A level translator supports a simple low-side switch buck converter, a class-AB voltage error amplifier supports non-isolated converters, and an error amplifier disable supports optocoupler feedback.

Some PD designers prefer to create multi-output power supplies using a flyback or forward topology, but do not require metallic isolation between the PoE front end and the application circuits. Figure 32 shows a configuration that enables the internal error amplifier and disables the level shifter. A standard output voltage divider and compensation scheme utilizes the FB and COMP pins. The control loop design should account for a 0.2 V/V attenuation factor from the error amplifier to the PWM comparator. The TMR pin ramps the reference voltage to the error amplifier giving a closed-loop softstart.

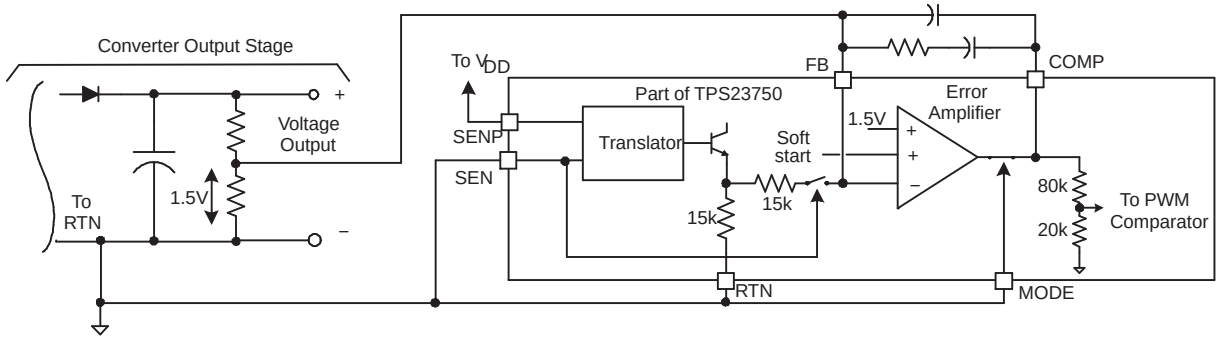


Figure 32. Nonisolated Converter Configuration

Isolated PD converters that use an optocoupler, such as TL431-based circuits, should use the configuration of Figure 33. The MODE connection disables the internal error amplifier, rendering its output high impedance. A primary-side PWM softstart is internally implemented when the error amplifier is disabled. The same gain of 0.2 V/V appears before the PWM comparator. The COMP pin is still monitored to implement hiccup in this configuration.

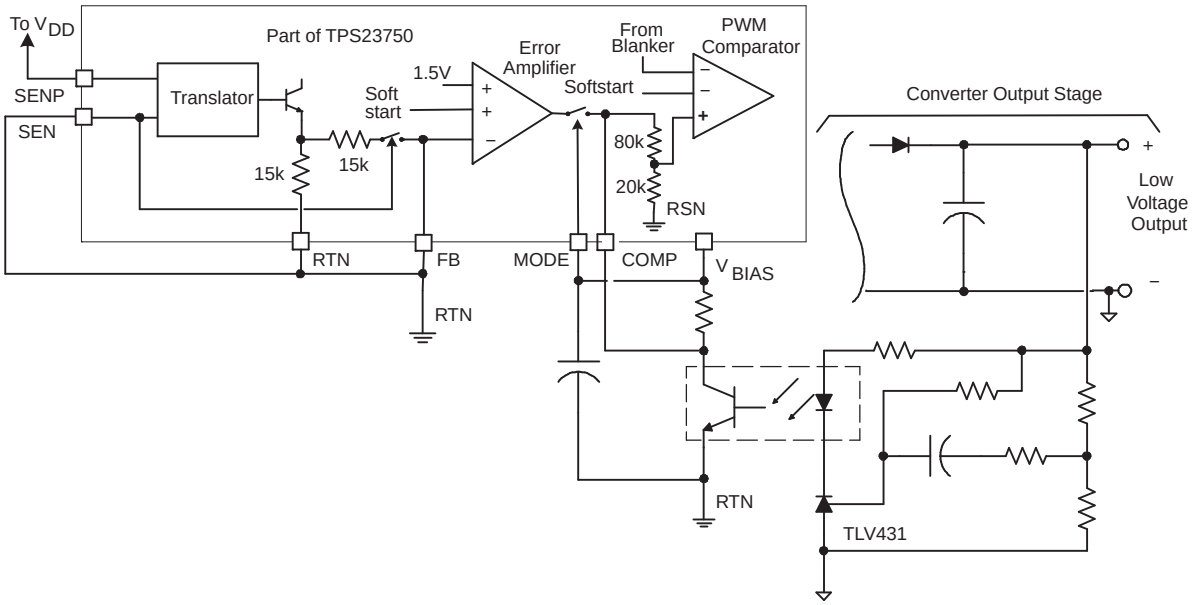


Figure 33. Isolated Converter Configuration

The buck converter configuration is shown in Figure 34. The loop regulates the voltage across R_{LO} to 1.5 V. The translator topology provides a gain of 1 V/V from $V_{SENP-SEN}$ to the 15 kΩ internal series resistor. The error amplifier gain expression is ($Z_{COMP-FB}$ / 15 kΩ). The output divider and translator attenuate both the ac and dc components, unlike the configuration of Figure 32 where the ac signal is not divided because the virtual ground at the amplifier input cancels the effect of R_{LO}. Addition of C_{BYP} across R_{HI} applies the full ac signal to the error amplifier. The $R_{HI}C_{BYP}$ corner frequency should be at least an octave lower than the R_ZC_Z zero frequency. This method assures C_{BYP} has little effect on standard loop design practices.

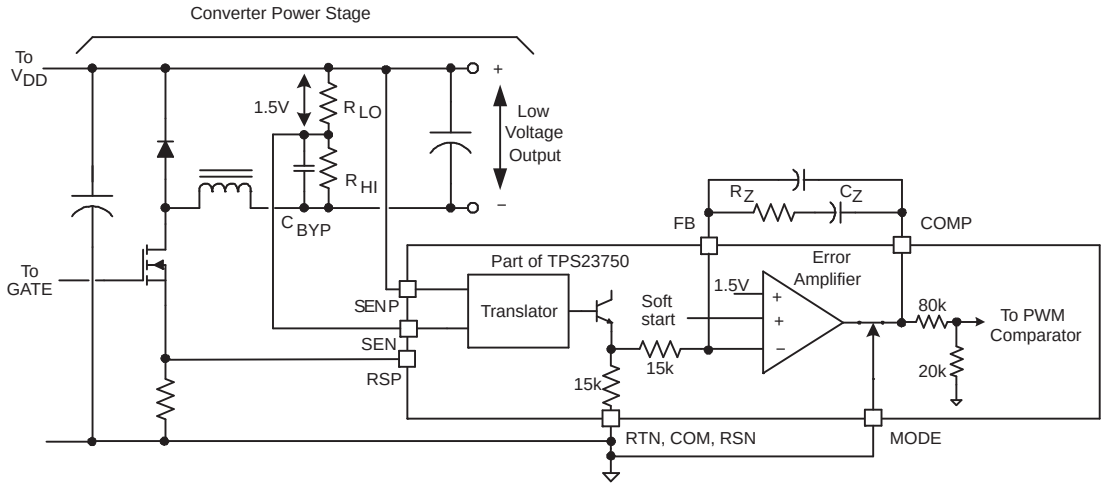


Figure 34. Buck Converter Configuration

ADDITIONAL USES OF SENP AND SEN

The level translator inputs, SENP and SEN, are not limited to the buck application shown in Figure 34. They may

be used at voltages above V_{DD}, but within their recommended voltage range with respect to V_{SS}. SENP draws about 22.5 μA of current, while the SEN pin draws less than 1 μA. The SENP current can cause a small offset in the output voltage if connected to the center tap of an output voltage divider. If necessary, the offset can be minimized or compensated. The following example shows a method of creating a voltage greater than V_{DD} for a telecom application that requires a voltage greater than battery ground.

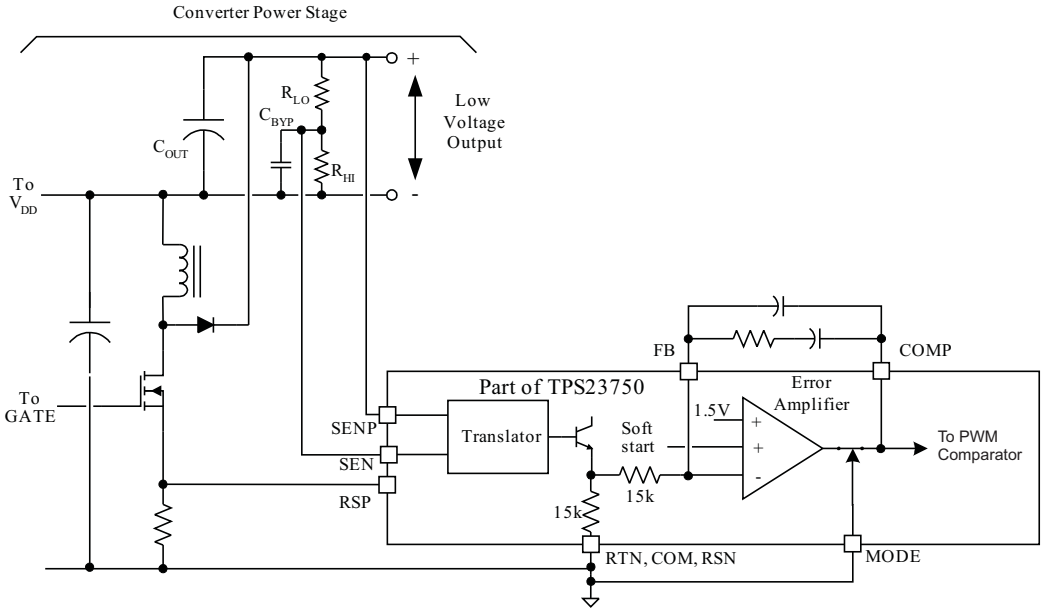


Figure 35. Buck-Boost Configuration Example

Bias Supplies

The TPS23750 has two bias supplies, the AUX input/output and the V_{BIAS} supply, each with its own UVLO.

The AUX supply is a current-limited, 10 V regulator that draws its current from V_{DD}. It may be overridden by feeding a higher external voltage into this pin to improve efficiency. The gate driver draws large current pulses from this rail. It requires low-impedance bypass capacitors, such as a 1 µF ceramic capacitor, located next to the TPS23750 and connected by low-impedance connections. A UVLO prevents gate drive if the voltage is less than 8 V. A 17.5 V overvoltage lockout (OVLO) on AUX prevents an open-loop converter, such as the one in Figure 1, from damaging the part by inhibiting gate drive. The V_{BIAS} regulator draws its power from the AUX pin.

The V_{BIAS} regulator is a current-limited, 5.1 V regulator that requires a capacitor between 0.08 µF–1.5 µF from its output to RTN. An optocoupler can be powered from this rail. Current drawn from the V_{BIAS} pin should not exceed 5 mA. This regulator also has a UVLO that turns the converter off if it is pulled below 4.6 V.

BLANKING CONSIDERATIONS AND RSP

Programmable blanking typically eliminates the need for the traditional RC filter on the RSP input. Blanking prevents the current-mode and current-limit comparators from reacting to the current spike that occurs as the converter's switching MOSFET turns on. This current spike consists of the MOSFET gate current, parasitic drain capacitance current, and output rectifier recovery current. The required blanking period is highly dependent on the specific design. Having too short a blanking time causes the converter to current limit, or switch erratically at less than full load. A longer blanking time increases the minimum load required before cycle skipping occurs. The power required to run an Ethernet link should provide most PDs adequate load to prevent cycle skipping.

Starting recommendations for the BL setting are:

- Use the long blanking period for transformer-based designs operating below about 150 kHz or using synchronous rectifiers.
- Use the short blanking period for transformer-based designs operating above 150 kHz or using Schottky output diodes.
- Use the short blanking period for buck or boost converter topologies.

BL pin connections to achieve each blanking length are listed below.

BL CONNECTION	BLANKING OPERATION
Open	None (Minimum current-sense loop delay)
RSN	Minimum plus 70 ns
V_{BIAS}	Minimum plus 105 ns

An RC filter may be used on the RSP pin should the need arise. A bias current of less than 8 µA flows out of the RSP pin.

The blanking period is specified as an increase in observable minimum gate on-time. The blanking circuit, current limit or PWM comparator, control logic, and loaded gate driver contribute to the observable current-sense loop delay. The PWM and current limit comparators do not respond to signals shorter than 20 ns, providing some inherent blanking within the current-sense loop delay measurement. The blanking circuit contributes almost negligible loop delay when the BL pin is open. The blanking periods are measured as the difference between the observed gate on-time with BL open, and its period with the BL pin connected high or low. The blanking periods shown do not include the comparator delays.

While many converter designs do not require a resistor in series with RSP, there may be instances where one is required to protect the pin from harmful currents. Even though the RSP pin has an absolute maximum voltage rating of –0.3 V, the ESD clamp can withstand occasional negative current pulses, provided they are limited to less than 100 mA. Some supply topologies, such as the self-driven synchronous rectifier circuit of Figure 38, have the ability to drive energy back through the transformer. This causes negative voltages on RSP and currents that can exceed the 100 mA. A small series protection resistor on RSP protects the device without requiring a Schottky diode clamp.

CONVERTER STARTUP

An imbalance between converter output capacitance, converter current limit, input bulk capacitance, and softstart time causes the converter to hiccup when attempting to start. The converter has a hard input current limit enforced by either the internal hotswap MOSFET or the PSE. If this current is exceeded, the converter meets its energy demands by drawing down the voltage on the bulk capacitor. As the capacitor voltage falls, the voltage across the internal MOSFET increases. If the voltage across the TPS23750's MOSFET reaches 12 V, it turns the converter off, falls back into inrush, and tries to restart.

To successfully start up, the design should balance the output capacitance, converter current limit, input bulk capacitance, and softstart time. Minimize the output capacitance and converter current limit. Use a long softstart period to control the output capacitor charge current. Finally, use a larger input capacitor that provides an energy store to get over this peak demand. The input bulk capacitor voltage droop should generally not exceed 5 V.

TMR OPERATION

TMR provides both a softstart and fault protection by means of a hiccup mode. Each cycle of hiccup operation consists of time-limited overload, followed by an enforced quiescent period, and an automatic restart. The benefits of hiccup operation include reduction of average thermal stress during faults and an automatic restart if a transient condition shuts the converter down.

During softstart, the converter is enabled and C_{TMR} charges at 50 µA from a low voltage towards 3 V. If V_{COMP} is less than 4.2 V when V_{TMR} reaches 3 V, C_{TMR} continues to charge towards the 3.5 V clamp level and the converter remains enabled. Internal scaling assures that a V_{COMP} less than 4 V will yield the maximum peak current limit. A V_{COMP} of less than 4.2 V means that the voltage loop is in regulation. A high V_{COMP} is an indication that there is a problem, with the most likely problem being an output overload. If V_{COMP} is above 4.2 V when V_{TMR} reaches 3.0 V, the converter disables and C_{TMR} discharges at 5 µA. A new softstart cycle begins when TMR reaches 0.3 V.

If the converter is operating normally, and V_{COMP} exceeds 4.2 V, C_{TMR} begins to discharge at 5 µA towards 3 V. If TMR reaches 3 V, the converter shuts off and a hiccup cycle begins. If V_{COMP} falls below 4.2 V before TMR reaches 3 V, C_{TMR} recharges at 50 µA and converter operation continues uninterrupted. Brief transients does not cause a hiccup due to the inherent filtering set by the value of C_{TMR}.

Softstart behaves differently when the internal error amplifier is used or disabled. The error amplifier, if used, regulates the voltage on FB to equal the voltage on TMR minus 0.5 V during softstart. The output voltage rises slowly and is in regulation when FB equals 1.5 V. If the error amplifier is disabled, the PWM comparator trip point ramps from 0 V to 0.5 V as V_{TMR} transitions from 0.54 V to 1.54 V.

TMR is discharged with a 1 kΩ pull down resistance when the converter is disabled.

Several other conditions interact with TMR:

- TMR is held low when the PoE control disables the converter.
- TMR is held low if converter UVLOs are not satisfied.
- TMR is held low in thermal shutdown.
- TMR hiccups after four consecutive fault comparator trips. Switching is suspended immediately while a hiccup cycle occurs.

Figure 36 illustrates the operation of the TMR pin. These waveforms were obtained using the circuits of Figure 38 and Figure 40. The buck converter shows softstart with the internal error amplifier and the flyback example shows operation when an optocoupler circuit is used. The flyback example shows COMP voltage droops due to the secondary-side softstart rather than from the internal error amplifier.

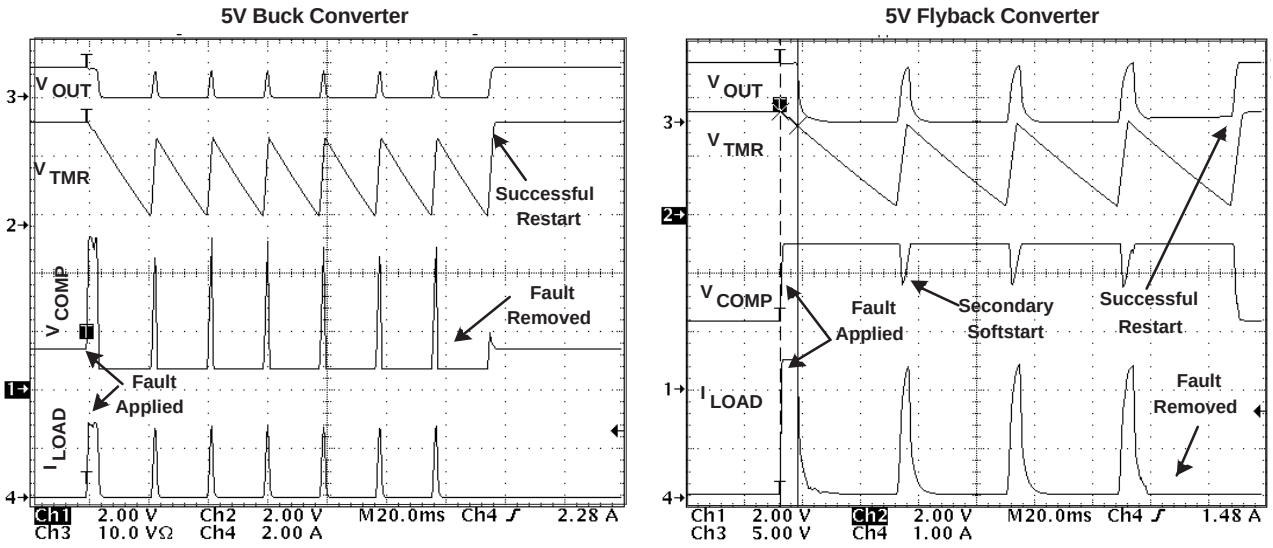


Figure 36. TMR Pin Operation

AUXILIARY SUPPLY ORing

Many PoE-capable devices are designed to operate from either a wall adapter or PoE power. A local power solution adds cost and complexity, but allows a product to be used regardless of PoE availability. Forcing one input or the other to dominate results in complex solutions. However, designs which run from the highest source are simple. Most applications only require that the two sources coexist in a predictable manner. Figure 37 illustrates three options for diode ORing external power into a PD. Option 1 applies power to the TPS23750's PoE input, option 2 inserts power between the TPS23750's PoE section and the converter, and option 3 applies power to the output side of the PoE power converter. Each of these options has advantages and disadvantages. The wall adapter must meet a minimum 1500 Vac dielectric withstand test voltage between the output and all other connections for options 1 and 2. The adapter only needs 1500 V isolation for option 3 if it is not provided by the converter.

Adapter input ORing diodes are shown for all the options to protect against a reverse input voltage, a short on the input pins, and to allow a natural ORing of PoE and auxiliary voltage. ORing is sometimes accomplished with a MOSFET in option 3.

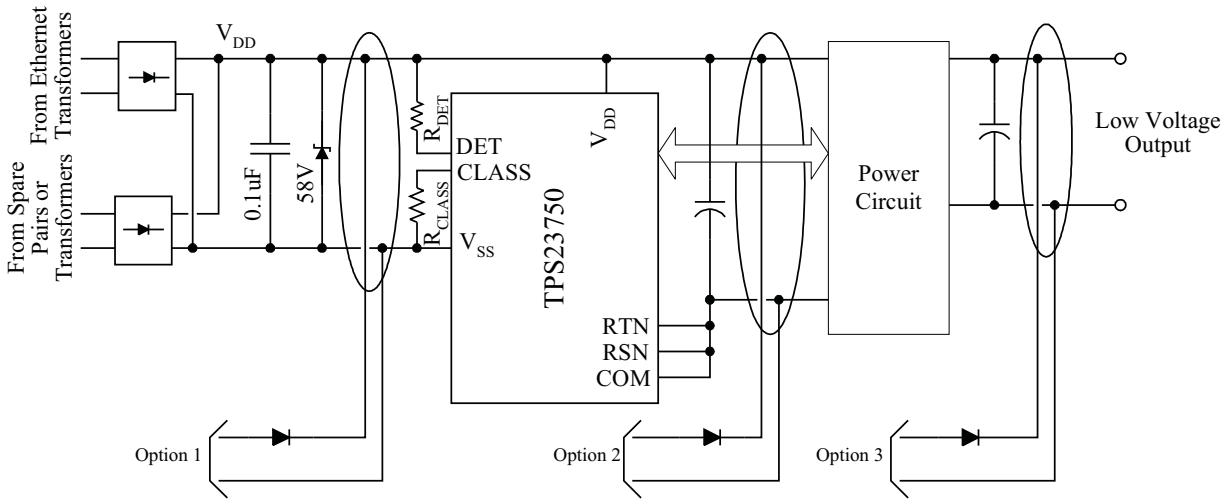


Figure 37. Auxiliary Power ORing

Option 1 inserts power before the TPS23750. A 48-V adapter that meets the TPS23750 UVLO is needed. If the adapter supply applies power to the PD before the PSE, it prevents the PSE from detecting the PD. This occurs because the input bridges are reverse biased and the Ethernet power path looks open. If the PSE is already powering the PD when the auxiliary source is plugged in, priority is given to the higher supply voltage.

Option 2 has the benefit that the adapter voltage may be lower than the PoE operating range. The TPS23750 was designed to operate from 24-V adapters. The bulk capacitor connected from V_{DD} to RTN should be large enough to control voltage transients that occur when plugging an adapter in. Usually at least several microfarads minimum are required. Once the PD is powered from the adapter, the PSE does not successfully detect the PD. This occurs because the internal MOSFET body diode establishes reverse bias voltage across the input bridges. Once the PD is powered from the PSE, the auxiliary source only takes over if its voltage is higher than the PSE output.

In some cases it may be desirable to make one power input dominant when using option 1 or 2. This can be accomplished for some configurations by using switches in the appropriate power path to allow one source to turn the other one off. These solutions require a number of additional components. In order for the PSE to disconnect, the dc current must be dropped below 5 mA, and the ac impedance must be greater than 2 MΩ at 500 Hz.

Option 3 consists of ORing power to the output of the PoE dc/dc converter. This option is often used in cases where PoE is added to an existing design that uses a low-voltage wall adapter. The relatively large PD output capacitance reduces the potential for transients when the adapter is plugged in. The adapter output may be grounded if the PD incorporates an isolated converter. The highest voltage source will dominate. Simple circuits using P-channel MOSFETs can be designed that force the auxiliary power source off. The auxiliary source can force the TPS23750 converter to stop switching by forcing the feedback node above its regulated value. This results in the converter shutting down.

ESD

The TPS23750 has been tested to EN61000-4-2 using the TPS23750EVM-107. The levels used were 8 kV contact discharge and 15 kV air discharge. Surges were applied between the RJ-45 and the dc EVM outputs, and between an auxiliary power input jack and the dc outputs. No failures were observed.

ESD requirements for a unit that incorporates the TPS23750 have a much broader scope and operational implications than are used in TI's testing. Unit-level requirements should not be confused with reference design testing that only validates the ruggedness of the TPS23750.

COMPONENT SELECTION

Converter Section Bypass Capacitors

The converter section's AUX and V_{BIAS} pins should be bypassed with high-quality ceramic capacitors. The V_{BIAS} supply provides a quiet source of power for internal and external circuits. The V_{BIAS} regulator is stable for output capacitances of 0.08 µF to 1.5 µF. A 1 µF capacitor is recommended, and this should be located as close to the TPS23750 as practical. The AUX supply is the source of the GATE drive current pulses. It requires a minimum 0.8 µF of ceramic bypass capacitor. The AUX capacitor must be located as close as possible to the TPS23750. The AUX regulator can be loaded with much larger capacitance.

PoE Data Transformer

Ethernet interfaces running on twisted pair commonly use an isolation transformer (see Figure 1) per long-standing IEEE 802.3 requirements. The transformer must include a center tap on the media (cable) side and be rated to handle the dc current and imbalance of IEEE 802.3af.

Input Diodes or Diode Bridges

IEEE 802.3af requires the PD to accept power on either set of input pairs with either polarity. This requirement is satisfied by using two full-wave input bridge rectifiers as shown in Figure 1. Silicon p-n diodes with a 1 A or 1.5 A rating and a minimum breakdown of 100 V are recommended. Diodes exhibit large dynamic resistance under low-current operating conditions such as in detection. The diodes should be tested for their behavior under this condition. The diode forward drops must be less than 1.5 V at 500 µA at the lowest operating temperature.

PoE Input Capacitor

IEEE 802.3af requires a PD input capacitance between 0.05 µF and 0.12 µF during detection. This capacitor should be located directly adjacent to the TPS23750 as shown in Figure 1. A 100 V, 10%, X7R ceramic capacitor meets the specification over a wide temperature range.

Input Transient Voltage Suppressor (TVS)

A TVS across the rectified PoE voltage per Figure 1 must be used. An SMAJ58A, or a part with equal to or better performance, is recommended. If an auxiliary supply is connected from V_{DD} - RTN, voltage transients caused by the input cable inductance ringing with the internal PD capacitance can occur. Adequate capacitive filtering or a TVS must limit this voltage to be within the absolute maximum ratings.

Converter Bulk Capacitor

IEEE 802.3af requires a PD input capacitance of 5 µF minimum while in the powered state. More capacitance is generally required to meet conducted emissions such as CISPR22 or those implied by IEEE 802.3af sections 33.3.4 and 33.3.5. At least several microfarads should appear directly between V_{DD} and RTN to aid in control of transients.

TMR Capacitor

C_{TMR} plays a major role in controlling the turn-on profile and input current drawn when the internal error amplifier is used. The nominal expression for this capacitor is

$$C_{TMR} = 33 \times 10^{-6} \times t$$

where t is the desired softstart period and C_{TMR} is in Farads. The softstart period may vary by 50% due to variation in TMR currents and capacitor tolerance. The capacitor should be oversized accordingly. Typical softstart periods are on the order of several milliseconds. The delay between output fault and converter shutdown (hiccup start) is

$$t_{DELAY} = 95 \times 10^{3} \times C_{TMR}$$

where t_{DELAY} is in seconds and C_{TMR} is in Farads.

The softstart capacitor also assists an isolated design that does not use the internal error amplifier in limiting the peak input current. The output error amplifier still has to swing from saturation to regulation during startup, so a secondary-side softstart may be required as well.

Thermal Considerations and MOSFET Q_G

The AUX internal regulator may dissipate a large amount of heat. This occurs when high AUX rail currents are drawn from the V_{DD} rail rather than an external source. When an external supply powers AUX, the internal dissipation remains low. AUX supplies internal bias currents as well as external loads such as the switching MOSFET and optocoupler.

Applications that use a transformer-coupled circuit can override the internal AUX regulator by means of an additional winding as shown in Figure 38. Under a fault condition, such as an output short, the AUX regulator is active. Significant instantaneous power can be dissipated based on the gate drive loading, however the optocoupler does not draw power when this occurs. TMR limits the average operating duty cycle to less than 10%, which greatly reduces internal power dissipation.

Applications that do not override the internal AUX regulator should minimize the loading on AUX. The primary source of loading is the converter's switching-MOSFET gate capacitance. Q_G is the MOSFET data sheet parameter that defines the charge required to switch the transistor on or off. The switching MOSFET should be chosen to balance the $r_{DS(on)}$-related MOSFET loss with the amount of gate-drive current it requires. Suitable devices are available with a Q_G in the region of 5 nC for many applications, and it is not recommended that devices larger than 20 nC be used. An approximate expression for the internal power dissipated due to gate drive is:

$$P_{DISS\_GATE\_DRV} = [V_{DD} \times Q_G \times f\,].$$

The PowerPAD provides a low thermal resistance path for heat removal, enabling applications where high dissipation can't be avoided.

Four major contributors to internal heat dissipation are the internal (hotswap) MOSFET I^2R, the gate drive load, the internal bias power, and the optocoupler load. These four contributors form a template for the loss approximations of the common configurations shown in Table 3 . The total loss under low, medium, and high input voltages should be checked. I^2R dominant designs fare worse at low input voltage, while an AUX-load loss driven design may be worse at high input voltage.

Table 3. Power Dissipation

	INTERNAL DISSIPATION MODEL
Isolated converter with AUX override	$P = \left[\left(\frac{P_{IN}}{V_{DD}}\right)^2 \times R_{DSON}\right] + \left[V_{AUX} \times Q_G \times f\right] + \left[V_{AUX} \times I_{INTERNAL}\right] + \left[\left(V_{AUX} - V_{BIAS}\right) \times I_{OPTO}\right]$
Isolated converter without AUX override	$P = \left[\left(\frac{P_{IN}}{V_{DD}}\right)^2 \times R_{DSON}\right] + \left[V_{DD} \times Q_G \times f\right] + \left[V_{DD} \times I_{INTERNAL}\right] + \left[\left(V_{DD} - V_{BIAS}\right) \times I_{OPTO}\right]$
Nonisolated converter with AUX override	$P = \left[\left(\frac{P_{IN}}{V_{DD}}\right)^2 \times R_{DSON}\right] + \left[V_{AUX} \times Q_G \times f\right] + \left[V_{AUX} \times I_{INTERNAL}\right]$
Nonisolated converter without AUX override	$P = \left[\left(\frac{P_{IN}}{V_{DD}}\right)^2 \times R_{DSON}\right] + \left[V_{DD} \times Q_G \times f\right] + \left[V_{DD} \times I_{INTERNAL}\right]$

- $I_{INTERNAL}$ represents the operational current from the Electrical Characteristics table. Approximate that all the current is due to the controller.
- P_{IN} is the converter input power (P_{OUT}/efficiency), not the power at the PI.
- f is the converter switching frequency, and I_{OPTO} is the optocoupler bias current.
- V_{DD} can be calculated as

$$V_{DD} = \frac{\left(V_{PSE} - 2 \times V_D\right) + \sqrt{\left(V_{PSE} - 2V_D\right)^2 - 4 \times P_{IN} \times R_{LOOP}}}{2}$$

where V_D is an input diode drop (0.75 V), R_{LOOP} is 0 Ω to 20 Ω plus the MOSFET resistance, and P_{IN} as above. V_{PSE} is 44 V for cases where the MOSFET loss dominates.

- R_{DSON} is the internal pass MOSFET resistor, 0.6 Ω typical and 1 Ω maximum.
- The loss should be checked at different PI voltages to determine the worst case, especially where AUX override is not used.

A simple thermal model for the junction temperature is:

$$T_J = T_A + (P \times \theta_{JA})$$

where T_J is the junction temperature, T_A is the ambient temperature, P is the total power dissipated in the TPS23750, and θ_{JA} is the thermal resistance from the junction to ambient. θ_{JA} includes heat paths from the die through the package directly to air, through the leads to the circuit board, from the PowerPAD to the circuit board, and from the circuit board to air. The long-term steady-state junction temperature should be kept below 125°C.

Consider the case of a buck converter to demonstrate a thermal design:

- The output is 5 V at 1.5 A, with estimated efficiency of 85%.
- The chosen switching MOSFET has a Q_G of 10 nC, and a switching frequency of 200 kHz.
- Use the worst-case internal MOSFET resistance of 1 Ω.
- Assume an ambient air temperature of 65°C.
- Assume a thermal resistance of 45°C/W, because the PowerPAD has been connected to a large copper fill, but is not exactly as shown in SLMA002.
- Use the worst-case combinations of input voltage and loop resistance per Table 4.

$$P_{IN} = 5\ V \times 1.5\ A/0.85 = 8.82\ W$$

$$V_{DD} = \frac{(44\ V - 2 \times 0.75\ V) + \sqrt{(44\ V - 2 \times 0.75\ V)^2 - 4 \times 8.82\ W \times 20\ \Omega}}{2} = 37.84\ V$$

$$P = \left[\left(\frac{8.82\ W}{37.84\ V}\right)^2 \times 1\ \Omega\right] + [37.84\ V \times 10\ nC \times 200\ kHz] + [37.84\ V \times 2.2\ mA] = 0.213\ W$$

$$T_J = 65^oC + (0.213\ W \times 45^oC/W) = 74.6^oC$$

Table 4. Temperature Rise Calculator Summary

V_{PSE}	R_{LOOP} (Ω)	V_{DD} (V)	P (W)	T_J (°C)
44	20	37.84	0.213	74.6
50.5	10	47.13	0.233	75.5
57	0	55.5	0.258	76.6

Three conditions were calculated to determine which resulted in the higher junction temperature. The I^2R loss and bias loss variation with input voltage almost cancelled in this case. The resulting junction temperature is quite low due in part to the good circuit selections, moderate ambient temperature, and low thermal resistance.

LAYOUT

The layout of the PoE front end must use good practice for power and EMI/ESD. A basic set of recommendations include:

1. The parts placement must be driven by the power flow in a point-to-point manner such as RJ-45 → Ethernet transformer → diode bridges → TVS and 0.1 µF capacitor → TPS23750 → bulk capacitor → converter input.
2. There should not be any crossovers of signals from one part of the flow to another.
3. All power leads should be as short as possible with wide power traces and paired signal and return.
4. Spacings consistent with standards such as IEC60950 or IPC2221A should be observed between the 48 V input voltage rails and between the input and an isolated converter's output.
5. The TPS23750 should be positioned over split local ground planes referenced to V_{SS} for the PoE input, and to RTN for the converter. While the PoE side may operate without a ground plane, the converter side must have one. The PowerPAD must be tied to the V_{SS} plane or fill area, especially if power dissipation is a concern. Logic ground and logic power layers should not be present under the Ethernet input or the converter primary side.
6. Large copper fills and traces should be used on SMT power dissipating devices, and wide traces or overlay copper fills should be used in the power path.
7. The converter layout can benefit from basic rules such as:
   a. Pair signals to reduce emissions and noise, especially the paths that carry high-current pulses through the power semiconductors and magnetics.
   b. Minimize the length of all the traces that carry high-current pulses.
   c. Where possible, use vertical pairing rather than side-side pairing.
   d. Keep the high-current and high-voltage switching traces from low-level analog circuits including those outside the power supply. Pay special attention to FB, COMP, FREQ, and TMR.
   e. The current sensing lead to RSP is the most critical, noise-sensitive, signal. It must be protected as in d), paying attention to exposure to the gate drive signal.
   f. Follow adequate spacing around the high voltage sections of the converter.

Two evaluation modules (EVM) which demonstrate these principals have been created for this part. Documentation, including PCB layouts, are available on-line.

CONCEPT SCHEMATICS

The TPS23750 will work with almost any conventional circuit. Figure 38, Figure 39, and Figure 40 demonstrate the TPS23750's use. Figure 38 is an isolated synchronous flyback, Figure 39 is a non-isolated flyback, and Figure 40 is a buck converter variant. Each of these circuits provides a single output. Multiple outputs can be created by use of techniques such as multi-secondary transformers and combinations of linear and switching regulators. These three circuits form the basis of the two EVMs available for this product.

Isolated Flyback Example

The isolated synchronous flyback of Figure 38 is appropriate where the PD has a non-isolated metallic interface such as RS-232 or USB, or cannot pass 1500V hipot per IEC60950 section 6.2. A forward converter can also be used for this application.

This example includes provision for an external wall adapter with the voltage applied directly to the converter input, after the PoE output. Adapter inputs from 24 V to 48 V (nominal) can be connected and the converter starts up, although this particular converter is designed to run from 48 V. Sequencing between the PoE input, adapter input, and converter operation is internally handled.

The standard PoE front end, starting with the RJ-45 connector, includes the diode bridges, capacitor, and TVS. The TPS23750 forms the heart of the control circuit, performing the basic PoE and dc/dc converter functions. R1 implements detection. R4 sets the PD as a Class 3 (full power) device. An internal MOSFET isolates the converter from the input during PoE detection and classification, while performing inrush limit and current limit under fault conditions. Input energy storage and EMI filtering are performed by the π filter consisting of C4, L1, C1, and C2. The converter startup bias is handled by internal regulators, eliminating the need for several external components.

The internal error amplifier and buck regulator sense circuitry are disabled by setting MODE to V_{BIAS} and SEN to RTN. Disabling the internal error amplifier allows the external optocoupler U3 to drive COMP as a high impedance pin. BL is tied to V_{BIAS} to select the longer blanking period which allows for the output synchronous rectifier (Q1) recovery. C16 sets the softstart and hiccup period, while R23 sets a 100 kHz switching frequency. In this design, the switching frequency was set to 100 kHz to help reduce the switching losses. C11 and C12 provide bypass for the internal regulators, and D6 and R6 provide AUX bias power from the transformer to improve efficiency. D5, R2, and C3 form a voltage clamp to protect switching MOSFET Q2 from voltage spikes as it turns off. The current-sense resistor, R8, feeds the current-mode control comparator through RSP, and sets the current limit. R9 is present to protect the RSP pin's ESD clamp from excessive current caused by negative voltage across R8. This is an unusual condition that arises when this synchronous converter topology stops switching with voltage remaining on the output, causing the output energy to be recycled to the input.

In this 5-V output example, the transformer primary inductance is 150 µH with turns ratios of PRI:BIAS:OUTPUT:GATE of 5:2.22:1:1.56. Winding 7–8 provides gate drive for the synchronous rectifier Q1. The design operates in continuous conduction down to no load due to the synchronous rectifier operation. An output π-filter is formed by C5, C6, C7, L2, and C8. This filter, which provides very low output ripple, may be simplified for some applications. The feedback is driven by a conventional TL431 error amplifier, U2, driving an optocoupler, U3. Components D9, C18, and R13 act as a softstart that limits turn-on overshoot while U2 swings its cathode several volts to regulate. C17 serves to compensate the inner feedback loop caused by biasing the optocoupler from the output. C10 aids in EMI control, and has a high voltage rating to meet the 1500 V isolation test required in the standard.

Nonisolated Flyback Example

The nonisolated flyback of Figure 39 resembles the isolated version. This converter is sometimes used to generate multiple outputs in applications where there are no metallic interfaces and the PD can meet the IEEE802.3af 1500 V hipot without isolation. Multiple outputs can be provided by adding secondary windings to T2 along with diodes and capacitors. The synchronous rectifier has been replaced by a diode for demonstration purposes. While the diode is simpler and cheaper, the synchronous rectifier's lower power loss improves efficiency for low-voltage, high-current outputs. T2 winding 7-8 is not needed for a production design. The TL431 based error amplifier and optocoupler have been removed, and the TPS23750 internal error amplifier has been enabled by tying MODE to RTN. FB and COMP are used in a standard error amplifier topology for control and compensation.

Buck Converter Example

Figure 40 illustrates a particular form of buck converter where the output is derived with respect to the positive input rail. The application circuits are connected across the output, shown on J4, with terminal 2 as the application circuit ground reference. This type of circuit is applicable to those PDs that don't have outside connections other than the Ethernet cable, and where the load requirements can be met with lower efficiency.

This form of buck converter places the switch in the low side instead of the high side, with the output referenced to the positive rail. It allows a low-side control section to drive a step-down topology. The load operates properly from the differential output voltage because PoE is a floating power delivery method. There is no absolute ground reference. This is situation analogous to an ungrounded adapter output. The level translator allows use of this topology without the penalty of external components for accurately sensing an output voltage that doesn't have the same ground reference.

The error amplifier and level translator are configured by tying MODE low and SEN to the high-side referenced output. Tying BL low selects the short blanking because the reverse recovery of the free-wheeling diode, D4, is relatively short.

The PoE front end is the same as the isolated flyback example. The input π-filter is formed by C2, L1, C4, and C5, and provides bulk energy storage and EMI filtering. The buck topology consists of inductor L2, switch Q2, and diode D4. The output voltage is sensed by R7, R6, and R5, with the fed back voltage across R5. C3 allows the feedback-signal ac component through the translator, reducing the required ac gain of the compensation. The TPS23750 level translator, behind pins SENP and SEN, reflects the voltage across R5 to the error amplifier, which is referenced to RTN. The level translator provides a precision method of sensing the output voltage without requiring external components, and is automatically engaged when SEN is connected to the high side. The internal 15 kΩ resistor between the translator output and FB, in conjunction with the feedback between COMP and FB, completes the control loop error amplifier. The compensation components are C7, R2, and C6. A maximum 50% duty cycle limit makes output voltages to 15 V possible

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2. Current Mode Control of Switching Power Supplies, Lloyd H. Dixon Jr., TI (SLUP075)
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6. PowerPAD™ Thermally Enhanced Package Application Report, TI (SLMA002)
7. Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs, TI (SZZA017A)
8. Digital Designer's Guide to Linear Voltage Regulators and Thermal Management, Bruce Hunter and Patrick Rowland, TI (SLVA118)

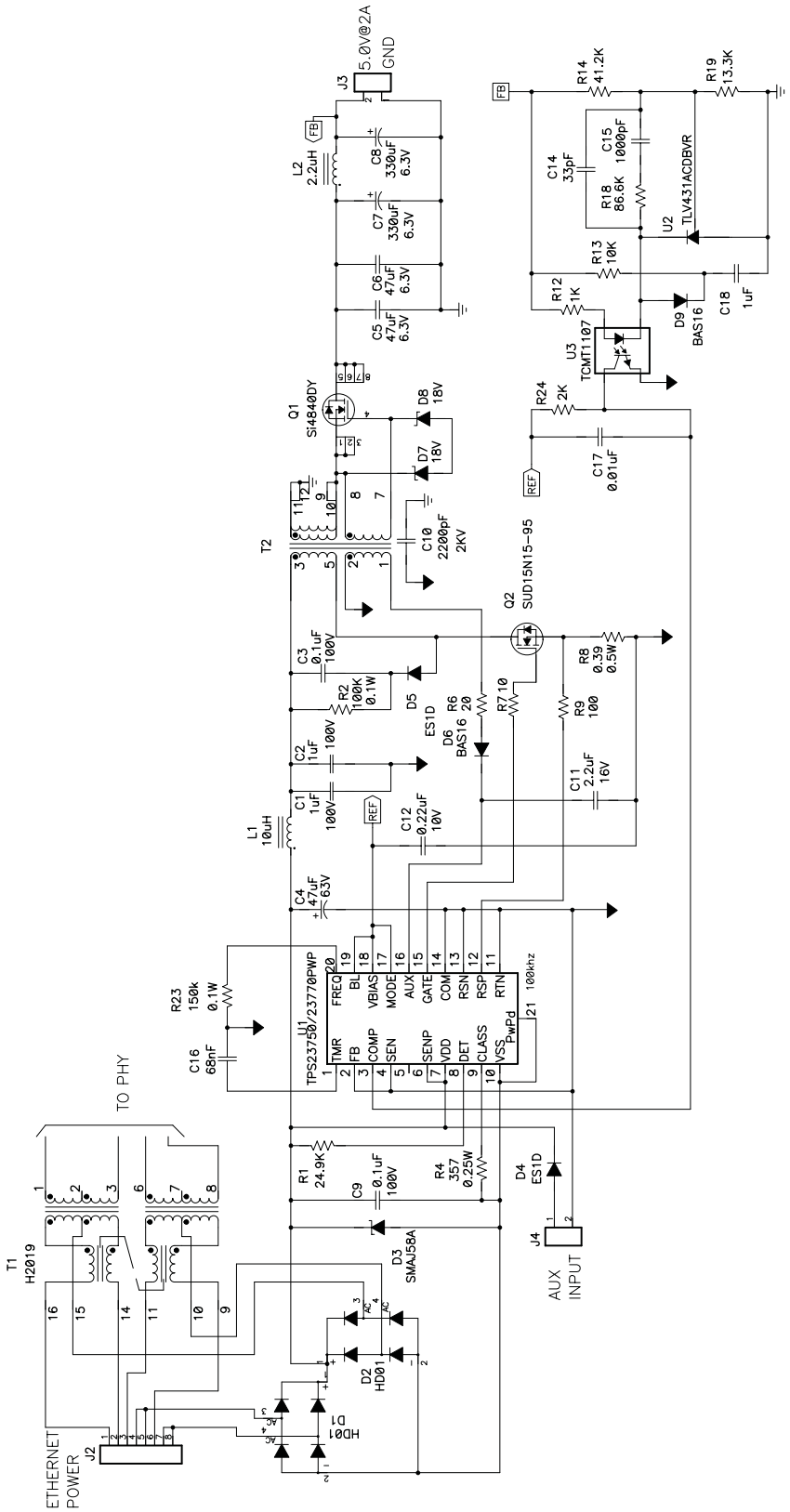


Figure 38. Isolated Flyback Example

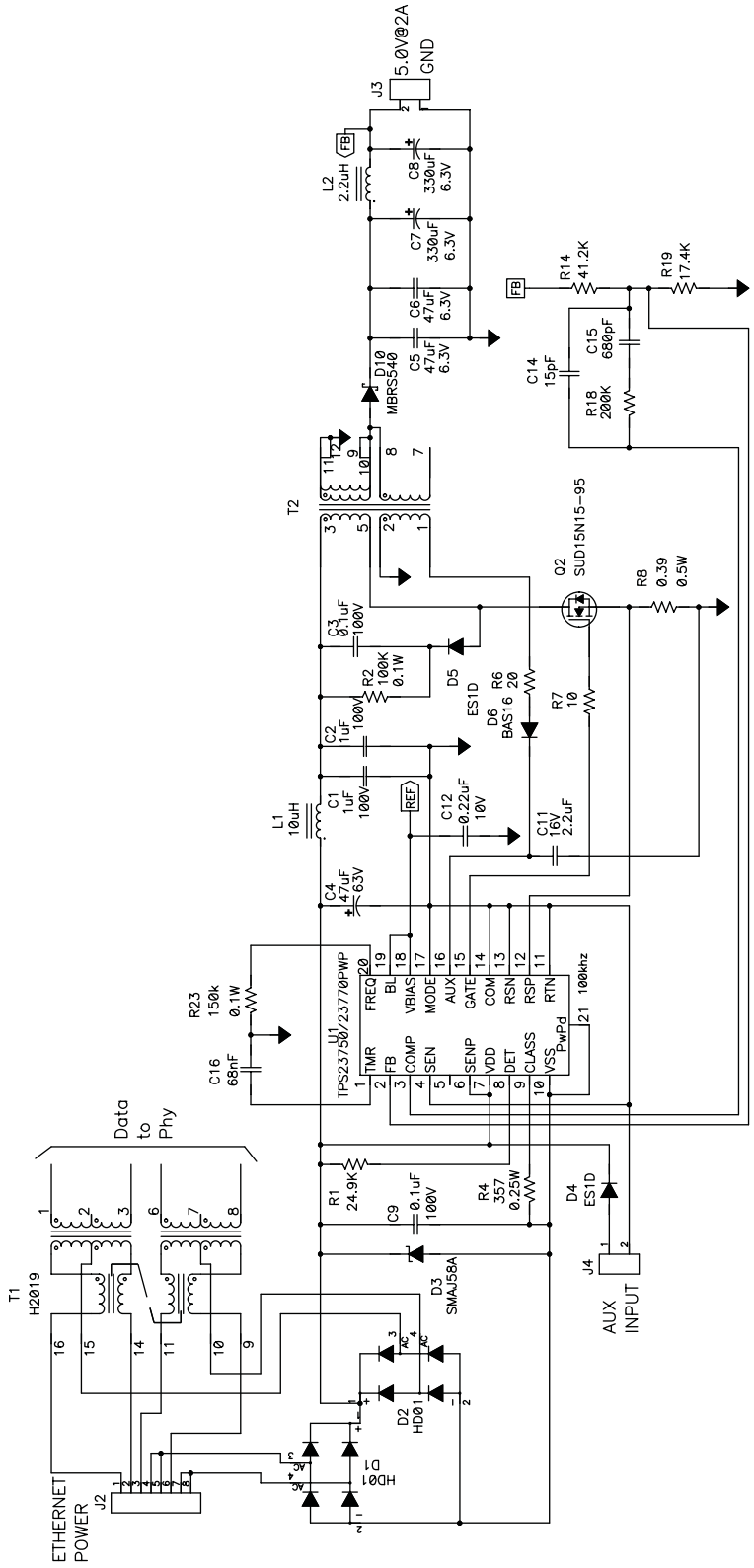


Figure 39. Non-Isolated Flyback

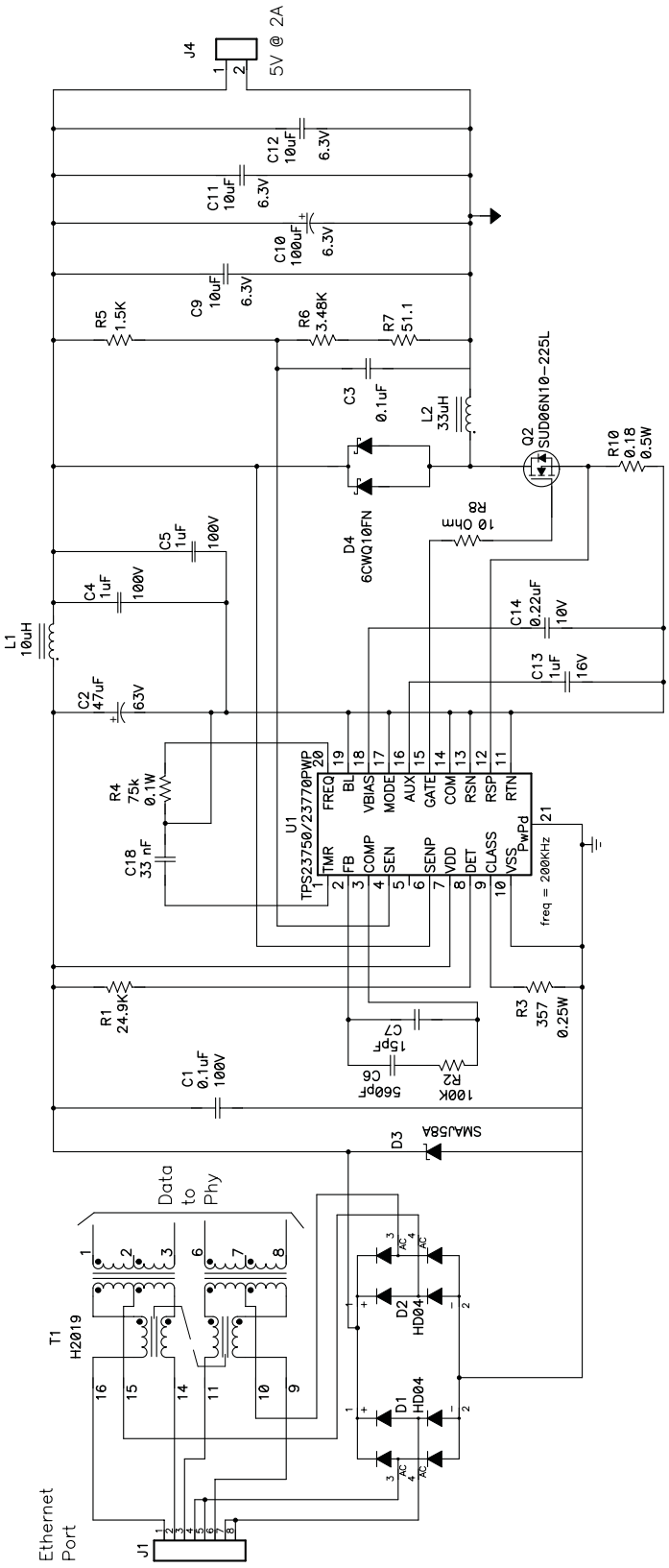


Figure 40. Buck Converter Example

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS23750PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU | NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS23750
TPS23750PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS23750
TPS23770PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS23770
TPS23770PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS23770

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

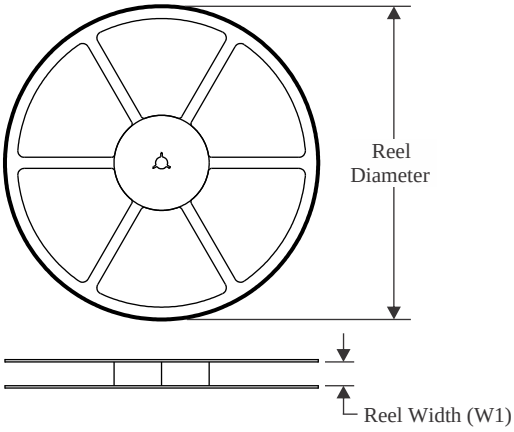
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

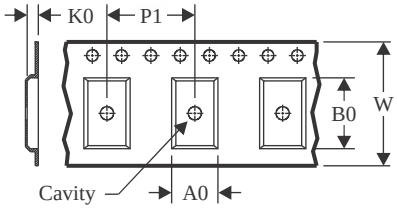
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

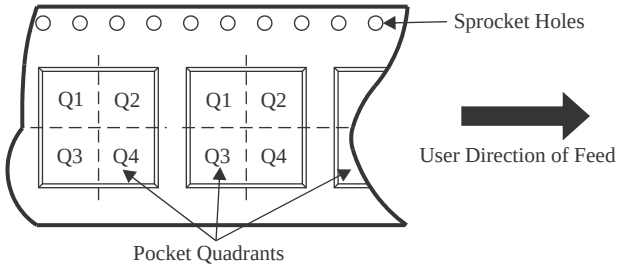


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

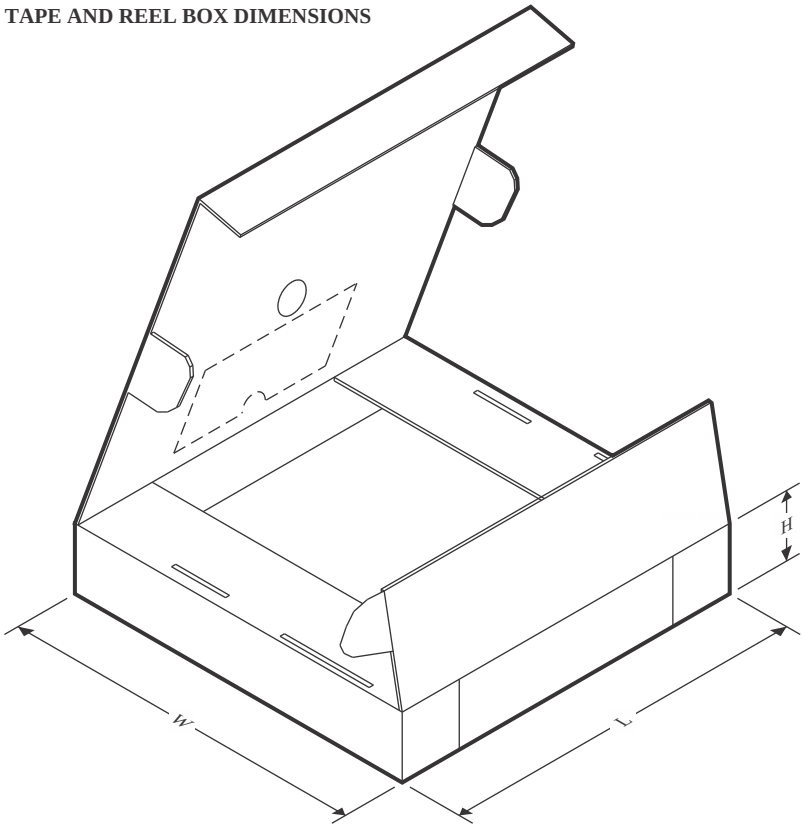
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS23750PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS23750PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS23770PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

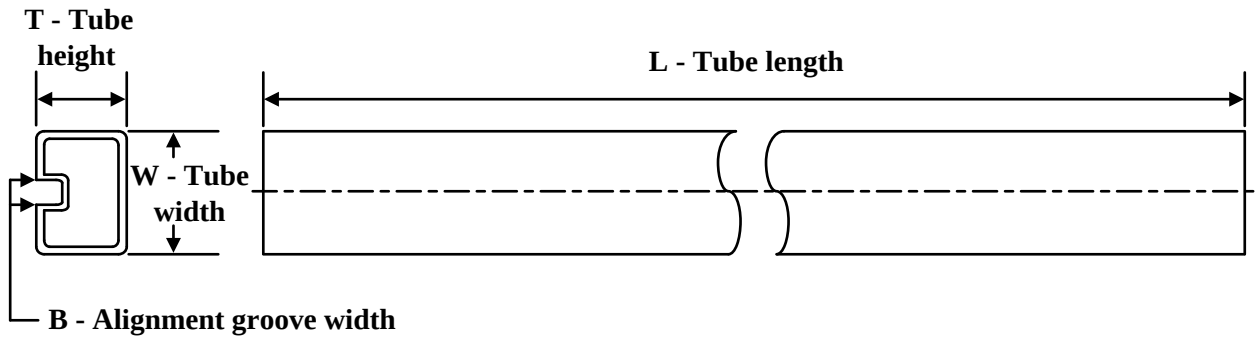
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS23750PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS23750PWPR	HTSSOP	PWP	20	2000	367.0	367.0	38.0
TPS23770PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS23750PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS23750PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS23770PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

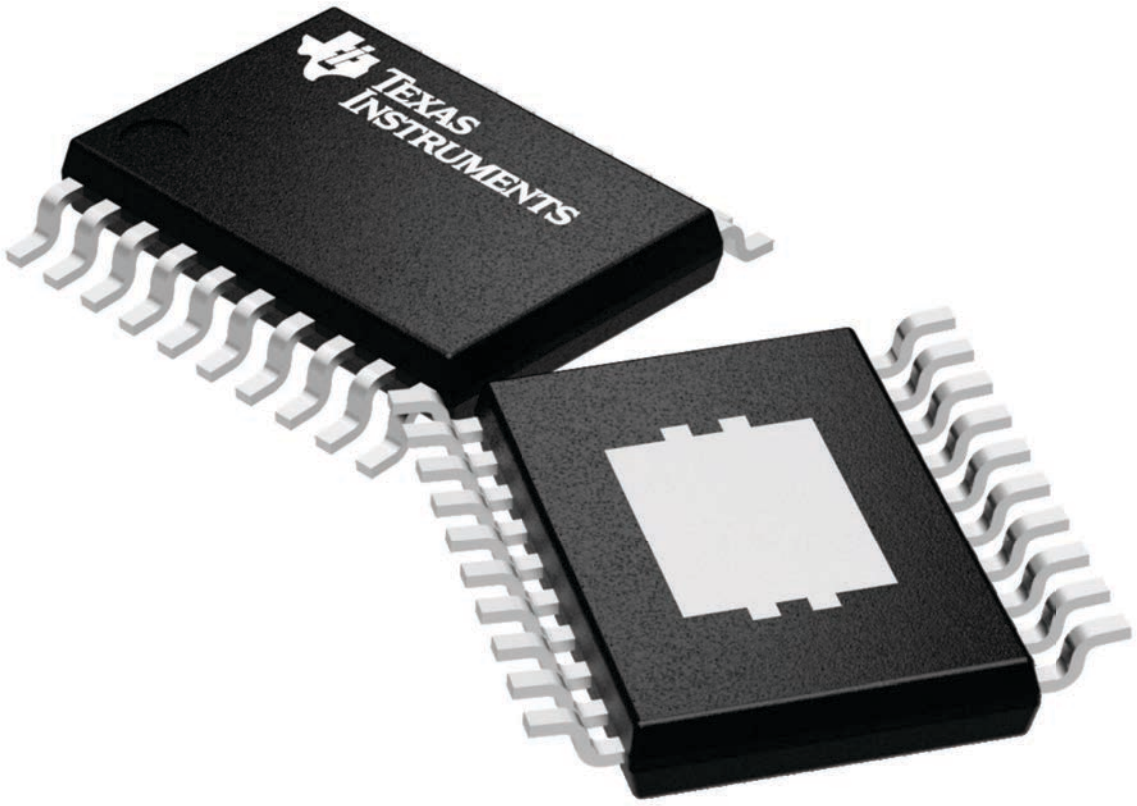
PWP 20

HTSSOP - 1.2 mm max height

6.5 x 4.4, 0.65 mm pitch

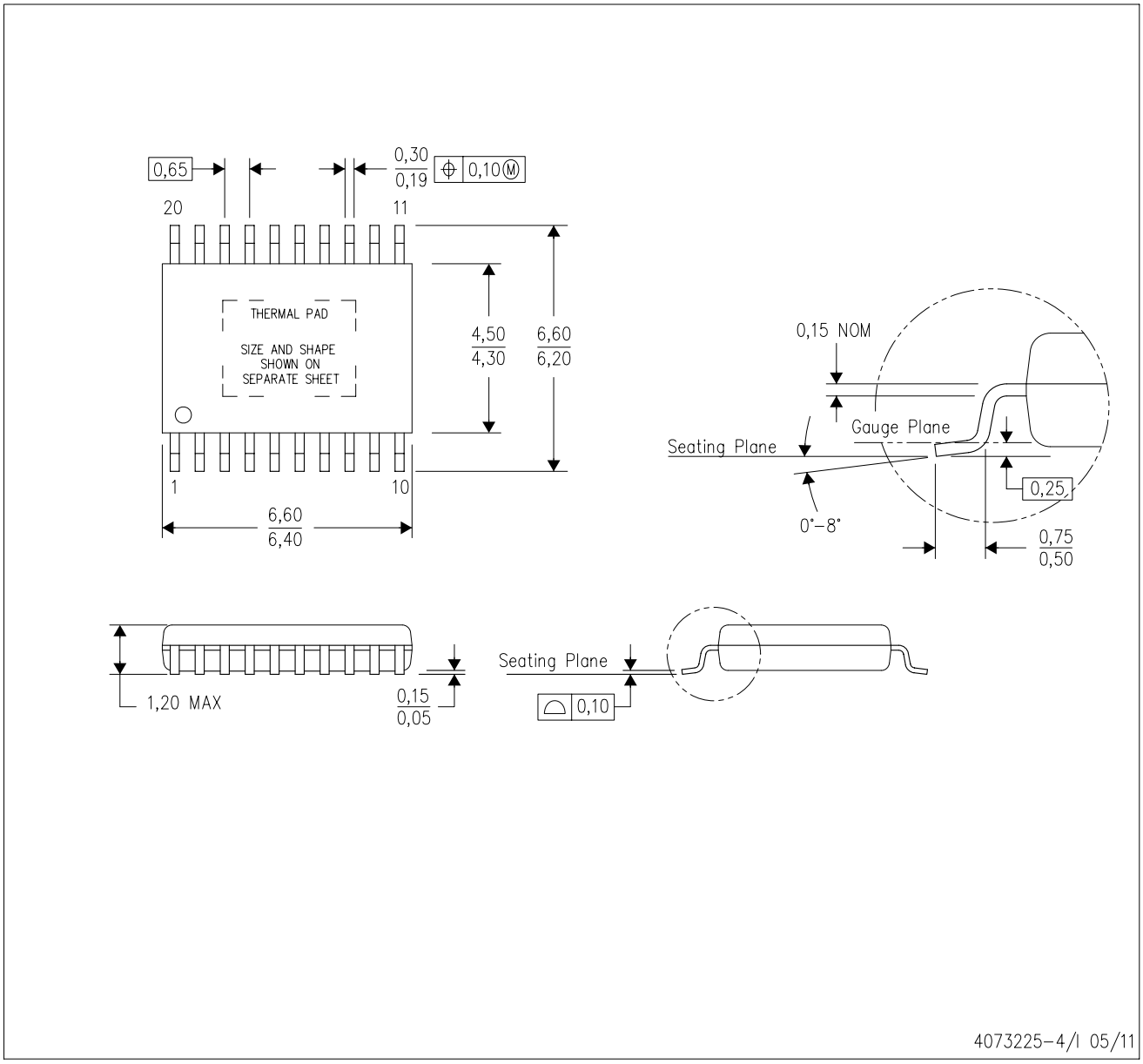
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

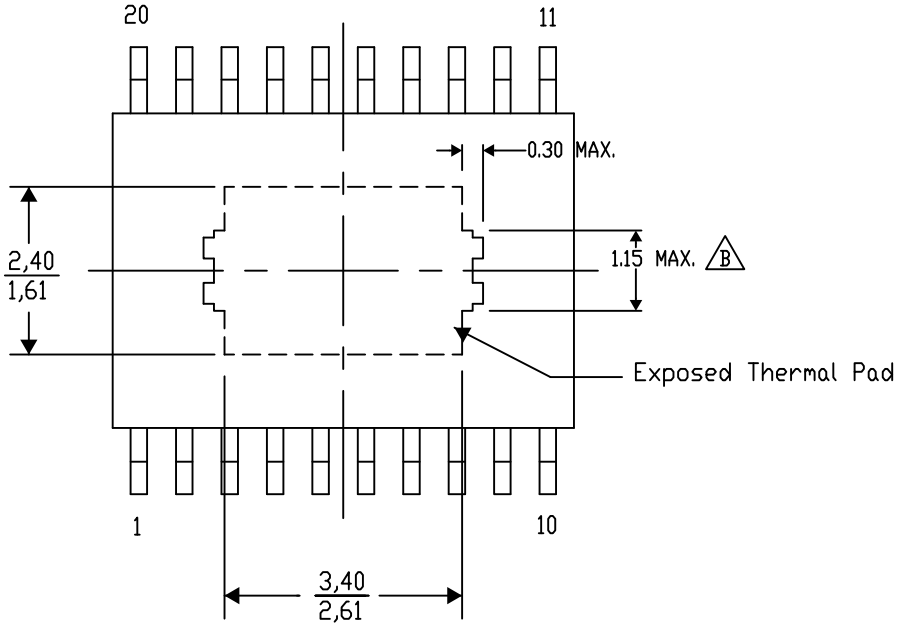
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

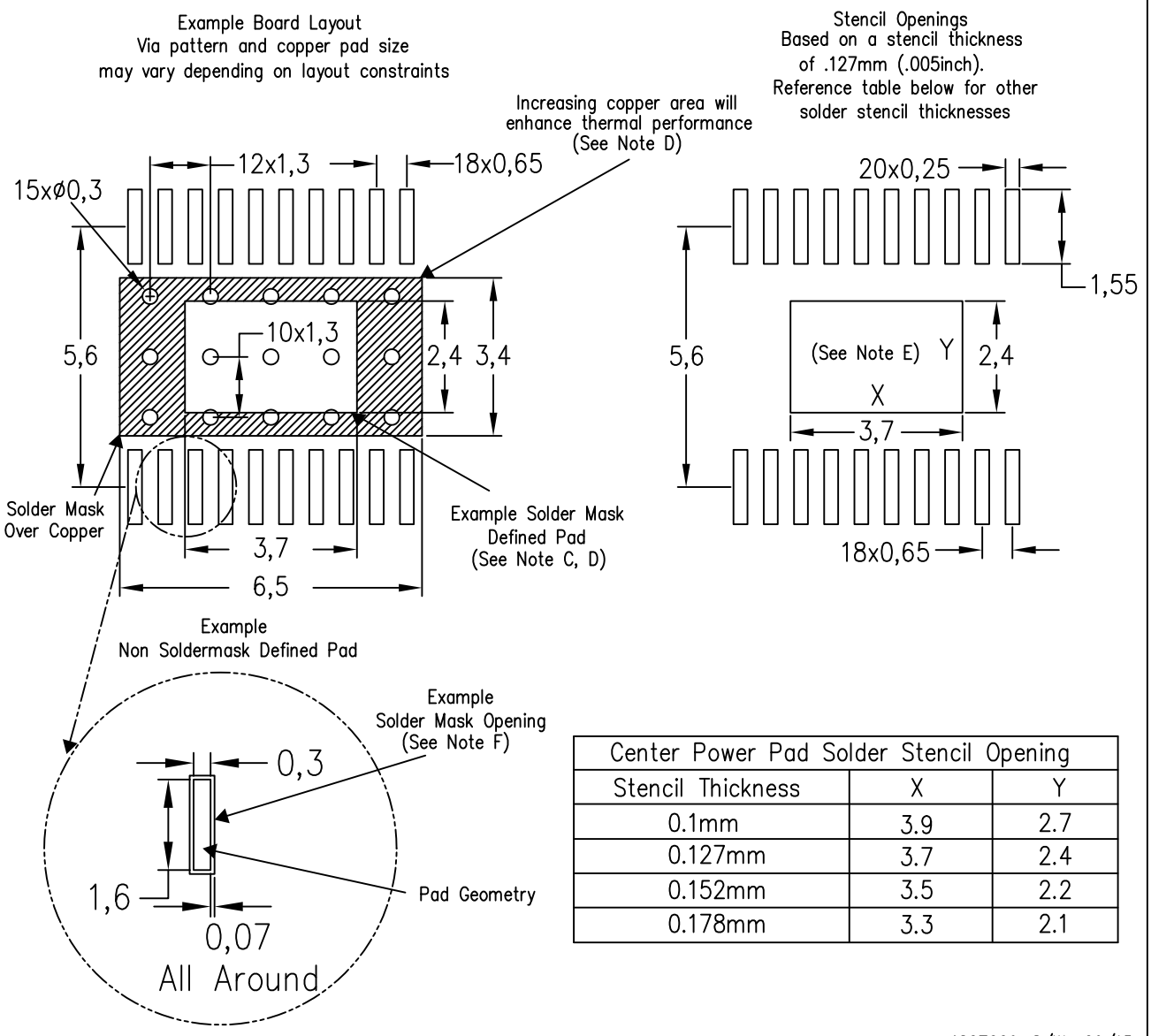
4206332–15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–8/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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