TPS25772-Q1 Automotive Dual USB Type-C® Power Delivery Controller with Buck-Boost Regulator

1 Features

- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C2b
  - Enhanced connector pin ESD protection
- USB Power Delivery (PD) controller with Programmable Power Supply (PPS) support
  - Wide V_{IN}: 5.5 V to 18 V (40-V maximum)
  - Integrated buck-boost 4 power switches supporting up to 65-W USB PD output power
  - V_{BUS} output: 3–21 V with ±20-mV step size
  - I_{BUS} output: 0–3 A with ±50-mA current limit step size
  - V_{BUS} short circuit to V_{BAT} and GND protection
  - V_{BUS} cable droop compensation
  - MFi overcurrent protection
  - Switching frequency: 300, 400, 450 kHz
  - DC/DC sync in/out with dithering
- USB port configurations options
  - 1 USB-PD Port (TPS25762-Q1)
  - 2 USB-PD Ports (TPS25772-Q1)
- Compliant to USB
  - USB Type-C® Power Delivery Rev 3.1
    - TPS25762-Q1: USB–IF certification with PPS, TID: 9509
    - TPS25772-Q1: USB–IF certification with PPS, TID: 9161
    - CC logic, V_{CONN} source and discharge
    - USB cable polarity detection
  - Battery charging specification rev 1.2
    - DCP: Dedicated Charging Port
- Legacy Fast Charging
  - 2.7-V divider-3 mode
  - 1.2-V divider mode
  - High Voltage DCP Protocol
- Microcontroller core allows
  - Firmware updates
  - Intelligent power sharing across charging ports
  - Supply voltage and temperature-dependent power management
- Short to V_{BUS} and V_{BAT} protection
  - V_{BUS}
  - Px_ DP and Px_DM
  - Px_CC1 and Px_CC2
- HotRod™ QFN package with wettable flank

2 Applications

- Automotive USB Charge
- Automotive Media Hub
- Automotive Head Unit
- Automotive Rear Seat Entertainment

3 Description

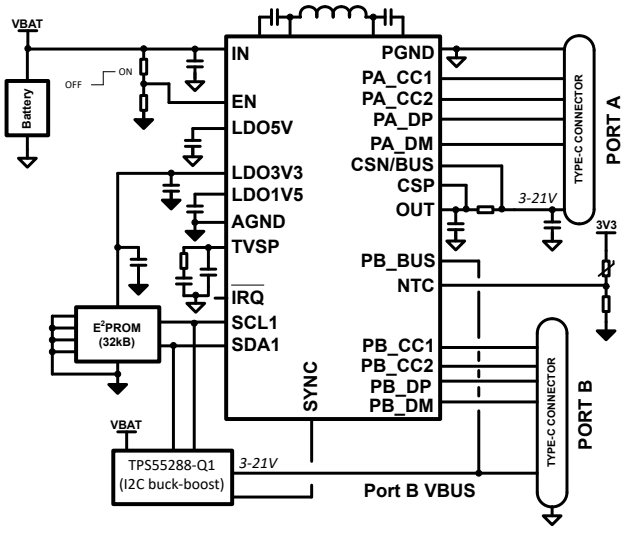
The TPS25772-Q1 is a fully integrated dual-port USB Type-C® Power Delivery (PD) solution with integrated buck-boost converter for automotive dual USB port applications. Functionality includes: integrated Buck-Boost converter with 4 power switches; an ARM® Cortex®-M0; USB port controller with Type-C cable plug and orientation detection; USB Battery Charging Specification Version 1.2 (BC1.2) detection; USB Endpoint PHY; device power management and supervisory circuitry; and connector pin protection over-voltage and short-circuit protection;

An intelligent System Policy Manager maximizes delivered USB power while protecting the system from automotive battery transient and over-temperature conditions.

Device configuration settings are selected through an intuitive graphical user interface (GUI).

Device Information

PART NUMBER	PACKAGE	BODY SIZE
TPS25772-Q1	RQL (QFN-29)	6 mm x 5 mm



TPS25772-Q1

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2022) to Revision A (September 2023)	Page
• Added TPS25762-Q1 and TPS25772-Q1 USB–IF certification TID	1
• Added wettable flank package information	1
• Added TPS25762CAQRQLRQ1, TPS25772CAQRQLRQ1, TPS25762CQRQLRQ1, TPS25772CQRQLRQ1 comparison in Device Comparison Table	3
• Added TPS25762CAQRQLRQ1 and TPS25762CAQRQLRQ1 R_{TVSP} configuration settings	36
• Added R_{TVSP} Circuit Configuration for applications requiring a configuration other than TVSP Index 0 (R_{TVSP} open)	36

5 Device Comparison Table

PART NUMBER	Orderable Device	Port A	Port B	Port A Output Power	Port B Output Power	Astable VIN Boot Support	Configurable Boot Mode(2)
TPS25762-Q1	TPS25762CQRQLRQ1	USB-PD	n/a	65 W	n/a	VIN-dependent(1)	Yes
	TPS25762CAQRQLRQ1					Yes	No
TPS25772-Q1	TPS25772CQRQLRQ1		USB-PD		65 W	VIN-dependent(1)	Yes
	TPS25772CAQRQLRQ1					Yes	No

1. Assured device boot up during astable VIN (e.g. cold crank) conditions when VIN oscillation minimum voltage is ≧7.6V until boot is completed. Refer to application brief TPS257x2-Q1 Startup with an Astable Supply Voltage.
2. Refer to Section 9.3.2.

6 Pin Configuration and Functions

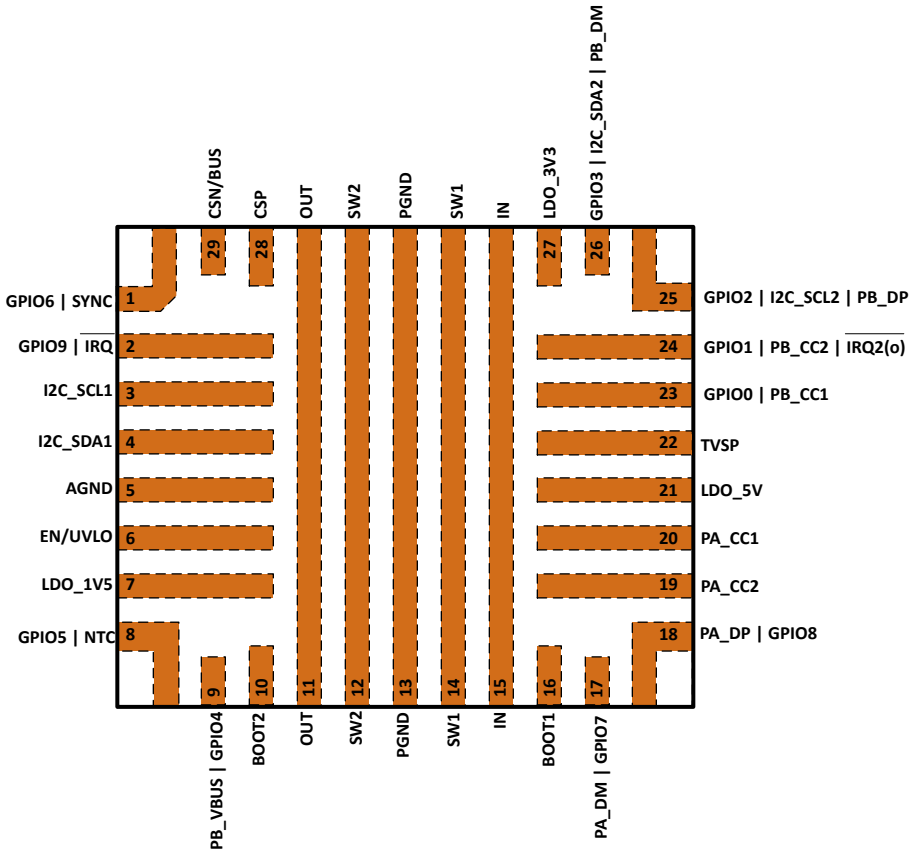


Figure 6-1. RQL Package 29-Pin (VQFN) Top View

Table 6-1. Pin Descriptions

PIN		DESCRIPTION
NAME	NO.	
EN/UVLO	6	Enable pin. For EN/UVLO < 0.3 V, the TPS25772-Q1 is in a low current shutdown mode. For EN/UVLO > 1.3 V, the full functionality is enabled, provided LDO_5V exceeds the LDO_5V UVLO threshold.
IN	15	The input supply pin to the IC. Connect V_{IN} to a supply voltage between 5.5 V and 18 V (40-V ABS MAX transient).
PGND	13	Power ground of the IC. The high current ground connection to the low-side gate drivers.
SW1	14	The buck side switching node.
SW2	12	The boost side switching node.
BOOT1	16	An external capacitor is required between the BOOT1 and the SW1 pins to provide bias to the high-side MOSFET gate drivers.
BOOT2	10	An external capacitor is required between the BOOT2 and the SW2 pins to provide bias to the high-side MOSFET gate drivers.
AGND	5	Analog ground of the IC.
OUT	11	Output of the buck-boost regulator. Connect to bulk capacitance.
CSP	28	Positive input of the current sense amplifier.
CSN/BUS	29	Negative input of the current sense amplifier. This is the PA_VBUS supply.
LDO_5V	21	Output of internal 5 V LDO for buck-boost low-side FET drivers, and Px_VCONN supply. Connect bypass capacitor to PGND. May be overdriven from external 5-V supply.
LDO_3V3	27	Output of internal 3.3-V LDO for analog circuitry and GPIO drivers. Connect bypass capacitor to AGND.
LDO_1V5	7	Output of internal 1.5-V LDO for digital circuitry. Connect bypass capacitor to AGND.
I2C_SCL1	3	Controller I2C Clock Input/Output.
I2C_SDA1	4	Controller I2C Data Input/Output.
GPIO2 (I2C_SCL2 or PB_DP)	25	Multifunction pin. GPIO; target I2C Clock Input; or Port B USB data line DP input depending upon firmware configuration.
GPIO3 (I2C_SDA2 or PB_DM)	26	Multifunction pin. GPIO; target I2C Data Input; or Port B USB data line DM input depending upon firmware configuration.
$\overline{\text{IRQ}}$ (GPIO9)	2	Multifunction pin. Interrupt I/O and fault flag for I2C1 or I2C2; or GPIO depending upon firmware configuration. Reports fault conditions set by application configuration firmware.
PA_CC1	20	Analog input/output. Port A Type-C current advertisement, VCONN, and USB PD modem. Connect to Port A Type-C connector CC1 pin.
PA_CC2	19	Analog input/output. Port A Type-C current advertisement, VCONN, and USB PD modem. Connect to Port A Type-C connector CC2 pin.
PA_DP (GPIO8)	18	Multifunction pin. BC1.2 USB 2.0 D+ data line input/output. Connect to Port A Type-C USB data line DP connector pins. May also be used as GPIO depending upon firmware configuration.
PA_DM (GPIO7)	17	Multifunction pin. BC1.2 USB 2.0 D- data line input/output. Connect to Port A Type-C USB data line DM connector pins. May also be used as GPIO depending upon firmware configuration.
PB_CC1 (GPIO0)	23	Multifunction pin. Port B Type-C current advertisement, VCONN, and USB PD modem. Connect to Port B Type-C connector CC1 pin; May also be used as GPIO when port B is disabled in firmware configuration.
PB_CC2 (GPIO1 or $\overline{\text{IRQ2(o)}}$)	24	Multifunction pin. Port B Type-C current advertisement, VCONN, and USB PD modem. Connect to Port B Type-C connector CC2 pin; May also be used as GPIO or Interrupt I/O when port B is disabled in firmware configuration.
GPIO5 (NTC)	8	Multifunction pin. GPIO; thermistor input (can use either negative temperature coefficient resistor or positive temperature coefficient resistor).
GPIO6 (SYNC)	1	Multifunction pin. GPIO; SYNC(o) - clock out to synchronize slave DC/DC regulators to internal DC/DC switching frequency; SYNC(i) - clock input to synchronize internal DC/DC to an external clock.
PB_VBUS (GPIO4)	9	Multifunction pin. PB_VBUS voltage monitor; or GPIO when port B is disabled in firmware configuration

Table 6-1. Pin Descriptions (continued)

PIN		DESCRIPTION
NAME	NO.	
TVSP	22	Transient voltage protection and firmware setting pin. See *Table 9-4* for boot configuration. See *Table 9-3* for R-C network component values.

7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of -40°C to 150°C and AGND = PGND (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Input voltage range	IN (3) (4) to PGND	–0.3	40	V
Input voltage range	IN with respect to SW1	–0.3	25	V
Input voltage range	EN/UVLO (5) to AGND	–0.3	internally limited	V
Input voltage range	BOOT1 with respect to SW1	–0.3	6	V
Input voltage range	BOOT2 with respect to SW2 (6)	–0.3	6	V
Input voltage range	SW1 (7) to PGND	–0.3	24	V
Input voltage range	SW2 (8) to PGND	–0.3	24	V
Input voltage range	SW2 to OUT		17.5	V
Input voltage range	CSP to PGND	–0.3	24	V
Input voltage range	CSN/BUS to PGND	–0.3	24	V
Input voltage range	CSP to CSN	-0.3	0.3	V
Input voltage range	AGND to PGND	–0.3	0.3	V
Output voltage range	OUT to PGND	–0.3	24	V
Output voltage range	LDO_5V to PGND	–0.3	6	V
Output voltage range	LDO_3V3 to AGND	–0.3	6	V
Output voltage range	LDO_1V5 to AGND	–0.3	2	V
I/O voltage range	TVSP to PGND	–0.3	30	V
I/O voltage range	I2C_SCL1 to AGND	–0.3	6	V
I/O voltage range	I2C_SDA1 to AGND	–0.3	6	V
I/O voltage range	GPIO9, $\overline{\text{IRQ1}}$ to AGND	–0.3	6	V
I/O voltage range	PA_CC1 to AGND	–0.3	30	V
I/O voltage range	PA_CC2 to AGND	–0.3	30	V
I/O voltage range	PA_DM to AGND	–0.3	30	V
I/O voltage range	GPIO7 to AGND	–0.3	6	V
I/O voltage range	PA_DP to AGND	–0.3	30	V
I/O voltage range	GPIO8 to AGND	–0.3	6	V
I/O voltage range	PB_CC1 to AGND	–0.3	30	V
I/O voltage range	GPIO0 to AGND	–0.3	6	V
I/O voltage range	PB_CC2 to AGND	–0.3	30	V
I/O voltage range	GPIO1, $\overline{\text{IRQ2}}$ to AGND	–0.3	6	V
I/O voltage range	PB_DP to AGND	–0.3	30	V
I/O voltage range	GPIO2, I2C_SCL2 to AGND	–0.3	6	V
I/O voltage range	PB_DM to AGND	–0.3	30	V
I/O voltage range	GPIO3, I2C_SDA2 to AGND	–0.3	6	V
I/O voltage range	PB_BUS to AGND	–0.3	30	V
I/O voltage range	GPIO4	–0.3	6	V
I/O voltage range	GPIO5, NTC to AGND	–0.3	6	V
I/O voltage range	GPIO6, SYNC to AGND	–0.3	6	V

7.1 Absolute Maximum Ratings (continued)

Over the recommended operating junction temperature range of -40°C to 150°C and AGND = PGND (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Input current	EN/UVLO	0	2	mA
Output current	Positive source current on PA_CC1, PA_CC2, PB_CC1, PB_CC2		internally limited	A
Output current	GPIO 2, 3, 5, 6, 7, 8		0.0010	A
Output current	GPIO 0, 1, 4, 9		0.005	A
Output current	positive sink current for I2C_SDA1, I2C_SCL1, I2C_SDA2, I2C2_SCL2		internally limited	A
Output current	positive source current for LDO_5V, LDO_3V3, LDO_1V5		internally limited	A
T_A Operating ambient temperature		–40	125	°C
T_J Operating junction temperature		–40	150	°C
T_{STG} Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to PGND or AGND. Connect the PGND pin directly to the Ground plane of the board. The PGND and AGND traces can be connected near the AGND pin.
(3) When the buck-boost is operating and V_{IN} exceeds 18 V, the positive slew rate dV_{IN}/dt must not exceed 200V/ms.
(4) When applying V_{IN}, the time from V_{IN} exceeding 5 V to V_{IN} exceeding 25 V must not be less than 2 µs. This is normally achieved by properly sizing the input EMI filter.
(5) EN/UVLO pin is internally clamped to 10V. Ensure input current rating is not exceeded by connecting current limit resistor.
(6) BOOT2 with respect to SW2 during OUT overvoltage conditions can be -15 V due to internal clamp.
(7) SW1 can undershoot PGND by -1 V during negative switching transients as up to 10A (peak) may flow through the body diode. Typical duration ~20 ns. SW1 can overshoot OUT by 1 V during positive transients. Typical duration ~ 20 ns.
(8) SW2 can undershoot PGND by -2 V during switching transients as up to 10A (peak) may flow through the body diode. Typical duration ~20 ns. SW2 can overshoot OUT by 1 V during positive transients. Typical duration ~20 ns.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002		±2000(1)	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011		±750(2)	V
$V_{(ESD)}$	Electrostatic discharge	IEC61000-4-2 Air-gap discharge 150 pF, 330 Ω.	OUT, CSP, CSN/BUS, PA_CC1, PA_CC2, PA_DP, PA_DM, PB_CC1, PB_CC2, PB_DP, PB_DM, PB_BUS	±2000(4)	V
$V_{(ESD)}$	Electrostatic discharge	IEC61000-4-2 Contact discharge 150 pF, 330 Ω.	OUT, CSP, CSN/BUS, PA_CC1, PA_CC2, PA_DP, PA_DM, PB_CC1, PB_CC2, PB_DP, PB_DM, PB_BUS	±2000(4)	V
$V_{(ESD)}$	Electrostatic discharge	ISO 10605 Contact discharge 330 pF, 330 Ω.	OUT, CSP, CSN/BUS, PA_CC1, PA_CC2, PA_DP, PA_DM, PB_CC1, PB_CC2, PB_DP, PB_DM, PB_BUS	±2000(3)	V
$V_{(ESD)}$	Electrostatic discharge	ISO 10605 Air-gap discharge 330 pF, 330 Ω.	OUT, CSP, CSN/BUS, PA_CC1, PA_CC2, PA_DP, PA_DM, PB_CC1, PB_CC2, PB_DP, PB_DM, PB_BUS	±2000(3)	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordancewith the ANSI/ESDA/JEDEC JS-001 specification.
(2) The passing level per AEC-Q100 Classification C2b.
(3) Test conducted on Texas Instruments evaluation board.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of -40°C to 150°C (unless otherwise noted)

			MIN	MAX	UNIT
V_I	Input voltage range (up to 65W output)	IN	6.8	18	V
V_I	Input voltage range (up to 30W output)	IN	5.5	18	V
V_I	Input voltage range	EN/UVLO	0	7 (2)	V
I_I	Input current	EN/UVLO	0	1	mA
V_I	Input voltage range	LDO_5V when overdriven by external supply	4.75	5.5	V
V_I	Input voltage range	CSP, CSN/BUS	0	22	V
V_I	Input voltage range	PB_VBUS (GPIO4 when configured as PB_VBUS)	3	22	V
V_O	Output voltage range	OUT	0	21	V
V_{IO}	I/O voltage range	PA_CC1, PA_CC2, PB_CC1, PB_CC2	0	5.5	V
V_{IO}	I/O voltage range	PA_DP, PA_DM, PB_DP, PB_DM	0	3.6	V
V_{IO}	I/O voltage range	I2C_SDAn, I2C_SCLn, $\overline{IRQn}$ (n=1 or 2)	0	5.5	V
V_{IO}	I/O voltage range	GPIOn (n = 0 - 9)	0	3.6	V
V_{IO}	I/O voltage range	NTC monitor (GPIO5), SYNC (GPIO6)	0	3.6	V
I_O	Output current(1)	IOUT		5	A
I_O	Output current	PA_CC1, PA_CC2, PB_CC1, PB_CC2		225	mA
I_O	Output current (from LDO_3V3)	GPIOn (n = 0 - 9)		10	mA
fsw	Buck-boost converter switching frequency driven from SYNC pin		250	500	kHz
T_A	Ambient operating temperature		–40	125	°C
T_J	Operating junction temperature		–40	150	°C

(1) Average LC filtered output current from buck-boost power stage. Operation with I_{OUT} > 3A with V_{OUT} > 10 V may result in thermal shutdown.
(2) EN/UVLO MAX specification specification applies when current into pin is not externally limited.

7.4 Recommended Components

over operating free-air temperature range (unless otherwise noted)

PARAMETER (1)		VOLTAGE RATING	MIN	TYP	MAX	UNIT
C_{IN}	Capacitance on VIN	40 V	22	47		µF
C_{LDO_5V}	Capacitance on LDO_5V (supplied internally)	10 V	4.7		10	µF
C_{LDO_5V}	Capacitance on LDO_5V (supplied externally)	10 V	10	47	100	µF
C_{LDO_3V3}	Capacitance on LDO_3V3	6.3 V	4.7		10	µF
C_{LDO_1V5}	Capacitance on LDO_1V5	6.3 V	4.7		10	µF
C_{Px_CCy}	Capacitance on Px_CCy pins(2)	6.3 V	200	330	480	pF
C_{BOOT1}, C_{BOOT2}	Boot charge capacitance	10 V	0.08	0.1	0.3	µF
$R_{Snubber\_SW1}$	RC snubber resistor on SW1	35 V, 0.25 W		1.1		Ω
$C_{Snubber\_SW1}$	RC snubber capacitor on SW1	35 V		1		nF
$R_{Snubber\_SW2}$	RC snubber resistor on SW2	35 V, 0.25 W		1.1		Ω
$C_{Snubber\_SW2}$	RC snubber capacitor on SW2	35 V		3.3		nF

over operating free-air temperature range (unless otherwise noted)

PARAMETER (1)		VOLTAGE RATING	MIN	TYP	MAX	UNIT
C_{OUT}	Capacitance on OUT (4)	35 V	30	33	40	µF
C_{BUS}	Capacitance on PA_VBUS	35 V	100	120	150	µF
L	Inductor (4)		3.3	4.7	5.6	µH
NTC	Thermistor		47		100	kΩ
$R_{EN/UVLO}$	Enable/UVLO pull up resistance		47			kΩ
TVPS pin components (C_{TVSP} || ($Damper_{R+C}$))	C_{TVSP} Capacitance on TVSP pin href	40 V	0.08	0.1	0.12	µF
TVPS pin components (C_{TVSP} || ($Damper_{R+C}$))	Damper resistor R of R + C network in Parallel with C_{TVSP}	0.25W	8	10	12	Ω
TVPS pin components (C_{TVSP} || ($Damper_{R+C}$))	Damper capacitor C of R + C network in Parallel with C_{TVSP}	40 V	0.376	0.47	0.564	µF
ESR_{CTVSP}	TVSP Capacitor ESR (eq series resistance)			10		mΩ
ESL_{CTVSP}	TVSP Capacitor ESL (eq series inductance)			1		nH

(1) Capacitance values do not include any derating factors. For example, if 5.0 µF is required and the external capacitor value reduces by 50% at the required operating voltage, then the required external capacitor value would be 10 µF.
(2) This includes all capacitance to the Type-C receptacle.
(3) Maximum capacitance allowed on TVSP pin to ensure proper decode of device configuration during boot.
(4) See applications section for recommended L and C_{OUT} combinations.

7.5 Thermal Information

THERMAL METRIC(1)		TPS25772-Q1 Hot Rod 29 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	7.3	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	7.2	

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.6 Buck-Boost Regulator

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 150°C junction temperature range unless otherwise stated.V_{IN} = 13.5 V, $V_{EN/UVLO}$ = 2V unless otherwise stated. (1)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN)						
I_Q	V_{IN} shutdown current	$V_{EN/UVLO}$ = 0 V			130	µA
I_Q	V_{IN} operating current	$V_{EN/UVLO}$ = 2V, V_{OUT} = 5 V, I_{OUT} = 0 A		8		mA
I_Q	V_{IN} operating current	$V_{EN/UVLO}$ = 1V, V_{OUT} = 0 V, I_{OUT} = 0 A			4.5	mA
I_Q	V_{IN} operating current	$V_{EN/UVLO}$ = 2V, V_{OUT} = 0 V, I_{OUT} = 0 A			8	mA
$V_{IN(OVP\_R)}$	V_{IN} rising overvoltage threshold	V_{IN} rising.	18.4	19.2	20	V
$V_{IN(OVP\_F)}$	V_{IN} falling overvoltage threshold	V_{IN} falling.	18.0	18.8	19.6	V
	hysteresis			0.4		V
$V_{IN(UVLO\_R)}$	V_{IN} undervoltage lockout rising	V_{IN} rising.	5.14	5.30	5.46	V
$V_{IN(UVLO\_F)}$	V_{IN} undervoltage lockout falling	V_{IN} falling.	5.04	5.20	5.36	V
	hysteresis			0.1		V

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 150°C junction temperature range unless otherwise stated.V_{IN} = 13.5 V, $V_{EN/UVLO}$ = 2V unless otherwise stated. (1)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
LDO_5V OUTPUT						
V_{LDO_5V}	LDO_5V Output Regulation voltage	7V ≤ V_{IN} ≤ 18 V, 0 < I_{LDO_5V} < 125mA, V_{EN} = 2 V.	4.5	4.63	4.75	V
$V_{LDO\_5V(UVLO\_R)}$	LDO_5V Undervoltage lockout rising		4.29	4.4	4.51	V
$V_{LDO\_5V(UVLO\_F)}$	LDO_5V Undervoltage lockout falling		4.09	4.2	4.31	V
	Undervoltage hysteresis			200		mV
$V_{LDO\_5V\_DO}$	drop out voltage	V_{IN} = 5.5 V; I_{LDO_5V} = 125mA	4.3			V
$I_{LDO\_5V(ILIMIT)}$	LDO_5V current limit	V_{LDO_V5V} = 0 to 3.5 V, $R_{LDO\_V5V\_LOAD}$ = 1 Ω	125	200	400	mA
LDO_3V3 OUTPUT						
V_{LDO_3V3}	LDO_3V3 Output regulation voltage	7V ≤ V_{IN} ≤ 18 V, V_{EN} = 2 V, $V_{LDO\_5V(UVLO)}$ < V_{LDO_5V} < 5.5 V, 0 < I_{LDO_3V3} < 25mA	3.4	3.5	3.6	V
$V_{LDO\_3V3(UVLO\_R)}$	LDO_3V3 Undervoltage lockout rising		3.2	3.3	3.4	V
$V_{LDO\_3V3(UVLO\_F)}$	LDO_3V3 Undervoltage lockout falling		3.05	3.15	3.25	V
	Undervoltage hysteresis			150		mV
$V_{LDO\_3V3\_DO}$	drop out voltage	VIN = 4.5 V, I_{LDO_3V3} = 30mA	3.3			V
$I_{LDO\_3V3(ILIMIT)}$	LDO_3V3 current limit	V_{LDO_3V3} = 0 to 2.5 V, $R_{LDO\_3V3\_LOAD}$ = 1 Ω	35	50	80	mA
LDO_1V5 OUTPUT						
V_{LDO_1V5}	LDO_1V5 Output Regulation voltage	4.5 < V_{LDO_5V} < 5.5V, 0 < I_{LDO_1V5} < 10 mA	1.49	1.55	1.65	V
$V_{LDO\_1V5(UVLO\_R)}$	LDO_1V5 Undervoltage lockout rising		1.44	1.49	1.54	V
$V_{LDO\_1V5(UVLO\_F)}$	LDO_1V5 Undervoltage lockout falling		1.37	1.42	1.47	V
	Undervoltage hysteresis			70		mV
$I_{LDO\_1V5(ILIMIT)}$	LDO_1V5 current limit	V_{LDO_1V5} = 0 to 1.2 V, $R_{LDO\_1V5\_LOAD}$ = 1 Ω	15	20	28	mA
EN/UVLO						
$V_{EN(LDO\_V5V\_R)}$	EN input level required to turn on internal LDOs	EN/UVLO rising			1.05	V
$V_{EN(LDO\_V5V\_F)}$	EN input level required to turn off internal LDOs	EN/UVLO falling	0.3			V
$V_{EN(OPER)}$	EN input level required to start operation	EN/UVLO rising Precision EN	1.2	1.25	1.3	V
$V_{EN(STBY)}$	EN input level required to stop operation	EN/UVLO falling	1.1	1.15	1.2	V
$V_{EN(HYS)}$	Hysteresis			100		mV
$V_{EN(CLAMP)}$	EN input clamp voltage	$V_{EN/UVLO}$ > $V_{EN(CLAMP)}$, 10 µA < $I_{EN/UVLO}$ < 1 mA	6	9	12	V
$I_{EN(LEAK)}$	Leakage current into EN pin	0 V < V_{EN} < 6 V			1	µA
OUTPUT VOLTAGE						
$V_{CSN/BUS(3V)}$	$V_{CNS/BUS}$ regulation accuracy at 3V	0 ≤ I_{OUT} ≤ 3A	2.9	3	3.1	V
$V_{CSN/BUS(5V)}$	$V_{CNS/BUS}$ regulation accuracy at 5V	0 ≤ I_{OUT} ≤ 3A	4.85	5	5.15	V
$V_{CSN/BUS(21V)}$	$V_{CNS/BUS}$ regulation accuracy at 21V	0 ≤ I_{OUT} ≤ 3A	20.48	21	21.53	V
V_{CSN/BUS_STP}	Output voltage step size (12-bit DAC)			10		mV
VDAC Resolution	Resolution of V_{BUS} DAC			12		Bits
I_{DISCHG}	CSN/BUS discharge current when transitioning to VSafe0V	V_{CSP} = $V_{CSN/BUS}$. $V_{CSN/BUS}$ = 3V. Measure current into BUS.	40			mA

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 150°C junction temperature range unless otherwise stated.V_{IN} = 13.5 V, $V_{EN/UVLO}$ = 2V unless otherwise stated. (1)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{DISCHG}	CSN/BUS discharge time when transitioning to VSafe5V	V_{BUS} = 21 V (max), CBULK = 220 µF, time to discharge BUS to < 5.5 V (per USB PD specification)			275	ms
t_{DISCHG}	CSN/BUS discharge time when transitioning to VSafe0V	V_{BUS} = 21 V (max), CBULK = 220 µF, time to discharge BUS to < 0.8 V (per USB PD specification)			650	ms
R_{DISCHG}	Weak discharge resistance on BUS pin when not sourcing VBUS	EN = 2V; measure BUS to PGND resistance.	60		135	kΩ
$R_{BUS-GND(PWR)}$	BUS to GND resistance, R_{DISCH} disabled, not sourcing VBUS	EN = 2V measure BUS to PGND resistance.	120		500	kΩ
$R_{BUS-GND(UNPWR)}$	BUS to GND resistance, unpowered	VIN = EN = 0V measure BUS to PGND resistance.		2		kΩ
CABLE VOLTAGE DROP COMPENSATION						
V_{OUT_CDC}	ΔV_{OUT} increase vs I_{OUT}	Gain setting = 0.1V/A: V_{CSP} - $V_{CSN/BUS}$ = 50 mV	465	500	535	mV
V_{OUT_CDC}	ΔV_{OUT} increase vs I_{OUT}	Gain setting = 0.1V/A: V_{CSP} - $V_{CSN/BUS}$ = 10 mV	85	100	115	mV
V_{OUT_CDC}	ΔV_{OUT} increase vs I_{OUT}	Gain stetting = 0.075V/A: V_{CSP} - $V_{CSN/BUS}$ = 50 mV	346	375	404	mV
V_{OUT_CDC}	ΔV_{OUT} increase vs I_{OUT}	Gain setting = 0.075V/A: V_{CSP} - $V_{CSN/BUS}$ = 10 mV	61	75	89	mV
V_{OUT_CDC}	ΔV_{OUT} increase vs I_{OUT}	Gain setting = 0.05V/A: V_{CSP} - $V_{CSN/BUS}$ = 50 mV	227	250	273	mV
V_{OUT_CDC}	ΔV_{OUT} increase vs I_{OUT}	Gain setting = 0.05V/A: V_{CSP} - $V_{CSN/BUS}$ = 10 mV	37	50	63	mV
V_{OUT_CDC}	ΔV_{OUT} increase vs I_{OUT}	Gain setting = 0.025V/A: V_{CSP} - $V_{CSN/BUS}$ = 50 mV	109	125	141	mV
V_{OUT_CDC}	ΔV_{OUT} increase vs I_{OUT}	Gain setting = 0.025V/A: V_{CSP} - $V_{CSN/BUS}$ = 10 mV	14	25	36	mV
V_{OUT_CDC}	ΔV_{OUT} increase vs I_{OUT}	Gain setting = 0V/A: 0 mV ≤ V_{CSP} - $V_{CSN/BUS}$ ≤ 50 mV	-5		20	mV
BUCK-BOOST PEAK CURRENT LIMITS						
$I_{PEAK(BOOST)}$	Boost peak current limit (in boost mode)		12.3	14.5	16.7	A
$I_{PEAK(BOOST)}$	Boost peak current limit (in boost mode)		10.8	12.8	14.7	A
$I_{PEAK(BOOST)}$	Boost peak current limit (in boost mode)		9.3	11.0	12.6	A
$I_{PEAK(BOOST)}$	Boost peak current limit (in boost mode)		7.9	9.3	10.6	A
$I_{PEAK(BOOST)}$	Boost peak current limit (in boost mode)		6.3	7.5	8.6	A
$I_{PEAK(BOOST)}$	Boost peak current limit (in boost mode)		4.8	5.7	6.5	A
$I_{PEAK(BUCK)}$	Buck peak current limit (in buck mode)		8.2	9.7	11.2	A
$I_{PEAK(BUCK)}$	Buck peak current limit (in buck mode)		9.0	10.6	12.1	A
$I_{PEAK(BUCK)}$	Buck peak current limit (in buck mode)		9.7	11.4	13.1	A
$I_{PEAK(BUCK)}$	Buck peak current limit (in buck mode)		10.4	12.3	14.1	A
$I_{PEAK(BUCK)}$	Buck peak current limit (in buck mode)		5.3	6.2	7.2	A
$I_{PEAK(BUCK)}$	Buck peak current limit (in buck mode)		6	7.1	8.2	A
$I_{PEAK(BUCK)}$	Buck peak current limit (in buck mode)		6.8	8.0	9.1	A

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 150°C junction temperature range unless otherwise stated.V_{IN} = 13.5 V, $V_{EN/UVLO}$ = 2V unless otherwise stated. (1)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$I_{PEAK(BUCK)}$	Buck peak current limit (in buck mode)		7.5	8.8	10.1	A
$I_{NEG(BUCK)}$	Buck negative current limit (in buck mode)		-4.6	- 3.8	-3	A
OUT CURRENT DAC						
IDAC_Resolution				8		Bits
CURRENT LIMIT						
I_{LIMIT_LO}	Current limit accuracy	1 A ≤ I_{OUT} ≤ 3 A, $V_{CSN/BUS}$ < 2.5 V; R_S = 10 mΩ.	-250		250	mA
I_{LIMIT_LO}	Current limit accuracy < 1 A	1 A ≤ I_{OUT} ≤ 3 A, $V_{CSN/BUS}$ ≥ 2.5 V; R_S = 10 mΩ	-150		150	mA
I_{LIMIT_HI}	Current limit accuracy > 3 A	I_{OUT} > 3 A, $V_{CSN/BUS}$ < 2.5 V; R_S = 10 mΩ	-20		20	%
I_{LIMIT_HI}	Current limit accuracy > 3 A	I_{OUT} > 3 A, $V_{CSN/BUS}$ ≥ 2.5 V; R_S = 10 mΩ	-5		5	%
I_{LIMIT_MIN}	Minimum programmable current limit		1			A
I_{CL_STEP}	Current limit step size	1 A ≤ I_{OUT} ≤ 5 A; R_S = 10 mΩ		50		mA
FREQUENCY						
$f_{SW(1)}$	Switching Frequency 1		285	300	315	kHz
$f_{SW(2)}$	Switching Frequency 2		380	400	420	kHz
$f_{SW(3)}$	Switching Frequency 3		428	450	473	kHz
FREQUENCY DITHER						
FS_{SS}	Positive frequency deviation during dither		8	10	12	%
	Negative frequency deviation during dither		-12	-10	-8	%
FS_{SS_MOD}	Modulation frequency of dither	DITHER_FREQ = 0	9	10	11	kHz
FS_{SS_MOD}	Modulation frequency of dither	DITHER_FREQ = 1	22.5	25	27.5	kHz
OVERVOLTAGE PROTECTION						
V_{CSN/BUS_OVP_R}	Fixed output overvoltage threshold at CSN/BUS pin		22.0	23	24	V
V_{CSN/BUS_OVP_F}	Falling		20.5	21.5	22.5	V
	Hysteresis			1.5		V
POWER SWITCHES						
$R_{DS(ON)}$	M1	V_{IN} = 12V; (V_{BOOT1} - V_{SW1}) = 4.5V; I_{SW1} = -1 A		4.5		mΩ
$R_{DS(ON)}$	M2	V_{IN} = 12V; I_{SW1} = 1 A		20		mΩ
$R_{DS(ON)}$	M4	V_{IN} = 12V; I_{SW2} = 1 A		6		mΩ
$R_{DS(ON)}$	M3 + M5	V_{IN} = V_{OUT} = 12V: (V_{BOOT2} - V_{SW2}) = 4.5V, I_{SW2} = -1 A		18		mΩ
$V_{UV\_BOOT1\_R}$	BOOT1 to SW1 rising UVLO threshold		3.5	4	4.4	V
$V_{UV\_BOOT1\_F}$	BOOT1 to SW1 falling UVLO threshold		2.9	3.4	3.7	V
	BOOT1 to SW1 UVLO hysteresis			680		mV
$V_{OV\_BOOT1\_R}$	BOOT1 to SW1 rising OVP threshold		4.6	5.3	5.9	V
$V_{OV\_BOOT1\_F}$	BOOT1 to SW1 falling OVP threshold		4.3	5	5.6	V
	BOOT 1 OVP hysteresis		250	300	350	mV
$V_{UV\_BOOT2\_R}$	BOOT2 to SW2 rising UVLO threshold		3.5	4	4.4	V
$V_{UV\_BOOT2\_F}$	BOOT2 to SW2 falling UVLO threshold		2.9	3.4	3.7	V
	BOOT2 to SW2 UVLO hysteresis			680		mV

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 150°C junction temperature range unless otherwise stated.V_{IN} = 13.5 V, $V_{EN/UVLO}$ = 2V unless otherwise stated. (1)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{OV\_BOOT2\_R}$	BOOT2 to SW2 rising OVP threshold		4.6	5.3	5.9	V
$V_{OV\_BOOT2\_F}$	BOOT2 to SW2 falling OVP threshold		4.3	5	5.6	V
	BOOT2 OVP hysteresis		250	300	350	mV
BUCK-BOOST CHARACTERISTICS						
t_{SS}	Soft-start time			6		ms

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

7.7 CC Cable Detection Parameters

Typical values correspond to TJ = 25°C. Minimum and maximum limits apply over the –40°C to 150°C junction temperature range unless otherwise stated.V_{IN} = 13.5 V, EN =2 V, unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Type-C Source (Rp pull-up)						
$V_{OC\_3.3}$	Unattached Px_CCy open circuit voltage while Rp enabled, no load	R_{CC} = 47 kΩ	1.85			V
V_{OC_5}	Attached Px_CCy open circuit voltage while Rp enabled, no load	R_{CC} = 47 kΩ	2.95			V
I_{Rev}	Unattached reverse current on Px_CCy	V_{CCy} = 5.5V, V_{CCx} = 0V, measure current into CCy			10	µA
I_{RpStd}	current source - Standard	0 < V_{CCy} < 1.0 V, measure I_{CCy}	64	80	96	µA
$I_{Rp1.5}$	current source - 1.5A	0 < V_{CCy} < 1.5 V, measure I_{CCy}	166	180	194	µA
$I_{Rp3.0}$	current source - 3.0A	0 < V_{CCy} < 2.45 V, measure I_{CCy}	304	330	356	µA
Type-C Sink (Rd pull-down)						
R_{SNK}	Rd pulldown resistance	0V ≤ V_{Px_CCy} ≤ 2.1 V, measure resistance on Px_CCy	4.6		5.6	kΩ
R_{VCONN_DIS}	VCONN discharge resistance	0V ≤ V_{Px_CCy} ≤ 5.5 V, measure resistance on Px_CCy	4.0		6.6	kΩ
Common (Source and Sink)						
t_{CC}	deglitch time for comparators on Px_CCy, this applies for V_{SRC1}, V_{SRC2}, V_{SRC3}, V_{SNK1}, V_{SNK2}, V_{SNK3}, and V_{SNK4}.			2.56		ms

7.8 CC VCONN Parameters

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 150°C junction temperature range unless otherwise stated.V_{IN} = 13.5 V, EN = 2 V unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PP_CABLE}	Rdson of the VCONN path	V_{LDO_5V} = 5V, I_L = 200 mA, measure resistance from LDO_5V to Px_CCy			1.2	Ω
I_{LIMVC}	short circuit current limit	setting 0, V_{LDO_5V} = 5V, R_L=10mΩ , measure I_{Px_CCy}	30	50	70	mA
		setting 1, V_{LDO_5V} = 5V, R_L=10mΩ , measure I_{Px_CCy}	235	275	315	
I_{CCyLKG}	Leakage current into Px_Cy pins	VCONN disabled, T_J ≤ 125 ºC, V_{Px_CCy} = 5.5 V, measure I_{Px_CCy}	-1	0	10	µA
V_{VC_OVP}	Over-voltage protection threshold for Px_CCy	V_{LDO_5V} rising	5.6	5.9	6.2	V

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 150°C junction temperature range unless otherwise stated.V_{IN} = 13.5 V, EN = 2 V unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VC_RCP}	Reverse current protection threshold for Px_CCy, sourcing VCONN through CCx	V_{LDO_5V} = 5 V, V_{CCx} rising, setting 1.	230	310	390	mV
V_{VC_RCP}	Reverse current protection threshold for Px_CCy, sourcing VCONN through CCx	V_{LDO_5V} = 5 V, V_{CCx} rising, setting 2.	60	155	250	mV
$t_{PP\_CABLE\_FSD}$	Time to disable Px_Cy VCONN after V_{LDO_5V} > V_{VC_OVP} or V_{CCx} - V_{LDO_5V} > V_{VC_RCP}	C_L=0		1.5		µs
$t_{PP\_CABLE\_off}$	from disable signal to Px_CCy at 10% of final value	I_L = 200 mA, V_{LDO_5V} = 5V, C_L=0	100	225	300	µs
$t_{iOS\_PP\_CABLE}$	response time to short circuit	External V_{LDO_5V} = 5V, for short circuit R_L = 10mΩ. Set VCONILIM = 1.			2	µs
$t_{iOS\_PP\_CABLE}$	response time to short circuit	Internal V_{LDO_5V} = 5V, for short circuit R_L = 10mΩ. Set VCONILIM = 0.			0.3	µs

7.9 CC PHY Parameters

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 150°C junction temperature range unless otherwise stated.V_{IN} = 13.5 V, EN = 2V unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmitter						
V_{TXHI}	Transmit high voltage on Px_CCy	Standard External load	1.05	1.125	1.2	V
V_{TXLO}	Transmit low voltage on Px_CCy	Standard External load	-75		75	mV
Z_{DRIVER}	Transmit output impedance while driving the CC line using Px_CCy	measured at 750 kHz	33		75	Ω
t_{Rise}	Rise time. 10 % to 90 % amplitude points on Px_CCy, minimum is under an unloaded condition. Maximum set by TX mask	C_{Px_CCy}= 520 pF	300			ns
t_{Fall}	Fall time. 90 % to 10 % amplitude points on Px_CCy, minimum is under an unloaded condition. Maximum set by TX mask	C_{Px_CCy}= 520 pF	300			ns
V_{PHY_OVP}	OVP detection threshold for USB PD PHY.	Initially V_{CC1} ≤ 5.5 V and V_{CC2} ≤ 5.5 V, then V_{CCx} rises.	5.5		8.5	V
Receiver						
Z_{BMCRX} (2)	Receiver input impedance on Px_CCy	Does not include pull-up or pulldown resistance from cable detect. Transmitter is Hi-Z.	1			MΩ
C_{CC}	Receiver capacitance on Px_CCy(1)	Capacitance looking into the CC pin when in receiver mode			120	pF

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 150°C junction temperature range unless otherwise stated.V_{IN} = 13.5 V, EN = 2V unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{RX\_SNK\_R}$	Rising threshold on Px_CCy for receiver comparator	sink mode (rising)	499	525	551	mV
$V_{RX\_SRC\_R}$	Rising threshold on Px_CCy for receiver comparator	source mode (rising)	784	825	866	mV
$V_{RX\_SNK\_F}$	Falling threshold on Px_CCy for receiver comparator	sink mode (falling)	230	250	270	mV
$V_{RX\_SRC\_F}$	Falling threshold on Px_CCy for receiver comparator	source mode (falling)	523	550	578	mV

(1) C_{CC} includes only the internal capacitance on a Px_CCy pin when the pin is configured to be receiving BMC data. External capacitance is needed to meet the required minimum capacitance per the USB-PD Specifications (cReceiver). Therefore, TI recommends adding C_{Px_CCy} externally.
(2) Guaranteed, but not production tested.

7.10 Thermal Shutdown Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD_BB}	Temperature shutdown threshold	Temperature rising	160	167	175	°C
T_{SD_HYS}	Temperature shutdown hysteresis	hysteresis		18		°C
$T_{SD\_PA\_VCONN}$	Temperature shutdown threshold	Temperature rising	152	166	179	°C
T_{SD_HYS}	Temperature shutdown hysteresis	hysteresis		20		°C
$T_{SD\_PB\_VCONN}$	Temperature shutdown threshold	Temperature rising	152	166	179	°C
T_{SD_HYS}	Temperature shutdown hysteresis	hysteresis		20		°C
$T_{SD\_PA\_VBUS\_DISCH}$	Temperature shutdown threshold	Temperature rising	155	166	177	°C
T_{SD_HYS}	Temperature shutdown hysteresis	hysteresis		20		°C
T_{SD_LDO5V}	Temperature shutdown threshold	Temperature rising	165	177	188	°C
T_{SD_HYS}	Temperature shutdown hysteresis	hysteresis		15		°C

7.11 Oscillator Characteristics

Typical values correspond to TJ = 25°C. Minimum and maximum limits apply over the –40°C to 150°C junction temperature range unless otherwise stated.V_{IN} = 13.5 V, EN =2 V, unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$F_{OSC(100K)}$	100KHz oscillator	Trimmed.	89	103	111	kHz
$F_{OSC(24M)}$	24MHz oscillator	Trimmed. 0 ℃ ≤ T_A ≤ 70 ℃	23.64	24.2	24.36	MHz
$F_{OSC(24M)}$	24MHz oscillator	Trimmed. -40 ℃ ≤ T_A ≤ 150 ℃	23.3	24.2	24.5	MHz

7.12 ADC Characteristics

Typical values correspond to TJ = 25°C. Minimum and maximum limits apply over the –40°C to 150°C junction temperature range unless otherwise stated.V_{IN} = 13.5 V, EN =2 V, unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LSB	least significant bit	3.6V max scaling, voltage divider of 3		14		mV
LSB	least significant bit	25.2V max scaling, voltage divider of 21		98		mV
LSB	least significant bit	(V_{CSP} - $V_{CSN/BUS}$)= 10 mV, 30 mV		27		mA
E_G	Gain error	0 A ≤ I_{TVSP} ≤ 0.9 mA	–2.7		2.7	%
E_G	Gain error	0.05V ≤ V_{GPIOx} ≤ 3.6V, V_{GPIOx} ≤ V_{LDO_3V3}	–2.7		2.7	%
E_G	Gain error	2.7V ≤ V_{LDO_3V3} ≤ 3.6V	–2.4		2.4	%
E_G	Gain error	0.6V ≤ V_{Px_VBUS} ≤ 22V	–2.4		2.4	%
E_G	Gain error, current sense	(V_{CSP} - $V_{CSN/BUS}$)= 10 mV, 30 mV	–2.4		2.4	%
E_G	Gain error	V_{IN}	–2.4		2.4	%
E_G	Gain error	4.3 V ≤ V_{LDO_5V} ≤ 5.5V	–2.4		2.4	%
$V_{OS(E)}$	Offset error(1)	0 A ≤ I_{TVSP} ≤ 0.9 mA	–4.1		15	mV
$V_{OS(E)}$	Offset error(1)	0.05V ≤ V_{GPIOx} ≤ 3.6V, V_{GPIOx} ≤ V_{LDO_3V3}	–4.1		4.1	mV
$V_{OS(E)}$	Offset error(1)	2.7V ≤ V_{LDO_3V3} ≤ 3.6V	-4.1		4.1	mV
$V_{OS(E)}$	Offset error(1)	0.6V ≤ V_{Px_VBUS} ≤ 22V	-4.1		4.1	mV
$V_{OS(E)}$	Offset error(1)	(V_{CSP} - $V_{CSN/BUS}$)= 10 mV, 30 mV	-4.5		4.5	mA
$V_{OS(E)}$	Offset error(1)	V_{IN}	-4.1		4.1	mV
$V_{OS(E)}$	Offset error(1)	4.3 V ≤ V_{LDO_5V} ≤ 5.5V	-4.1		4.1	mV

(1) The offset error is specified after the voltage divider.

7.13 TVS Parameters

VIN = 13.5V, EN = 2V. over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TVSP						
V_{TVSP_PU}	Pull up voltage for configuration (1)	0 < I_{TVSP} < 1 mA	5.3	5.5	5.7	V
Decode 0	Device configuration decode	R_{TVS} = Open			1	µA
Decode 1	Device configuration decode	R_{TVS} = 93.1 kΩ	56.9		61.2	µA
Decode 2	Device configuration decode	R_{TVS} = 47.5 kΩ	111.6		120	µA
Decode 3	Device configuration decode	R_{TVS} = 29.4 kΩ	180.3		193.9	µA
Decode 4	Device configuration decode	R_{TVS} = 20.0 kΩ	265		285	µA
Decode 5	Device configuration decode	R_{TVS} = 14.7 kΩ	360.5		387.8	µA
Decode 6	Device configuration decode	R_{TVS} = 11.0 kΩ	481.8		518.2	µA
Decode 7	Device configuration decode	R_{TVS} = 8.45 kΩ	627.2		674.6	µA
Decode 8	Device configuration decode	R_{TVS} = 6.65 kΩ	797		857.1	µA

VIN = 13.5V, EN = 2V. over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{TVSP(ILIMIT)}$	Current limit when TVSP is sourcing.	C_{TVSP} = open; R_{TVSP} = open. All Px_Dy = 0 V and Px_CCy = 0 V. V_{TVSP} = 0 V. Measure current flowing out of TVSP.	1.1	1.44	1.83	mA

(1) For proper device configuration, V_{IN} must be ≥ 7.6 V at time of configuration read.

7.14 Input/Output (I/O) Characteristics

Typical values correspond to TJ = 25°C. Minimum and maximum limits apply over the –40°C to 150°C junction temperature range unless otherwise stated.V_{IN} = 13.5 V, EN =2 V, unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIO0-9 (Inputs) (1)						
V_{IH}	GPIOx high-Level input voltage		1.3			V
V_{IL}	GPIOx low-level input voltage				0.54	V
	GPIOx input hysteresis voltage		0.09			V
$I_{I(LEAKAGE)}$	GPIOx leakage current	V_{GPIOx} = 5.5 V	–8		8	µA
R_{PU}	GPIOx internal pull-up	pull-up enabled	50	100	150	kΩ
R_{PD}	GPIOx internal pull-down	pull-down enabled	50	100	150	kΩ
t_{DG}	GPIOx input deglitch			20		ns
GPIO 2, 3, 5, 6 (Outputs)						
V_{OH}	GPIOx output high voltage	I_{GPIOx}= -5mA	2.9			V
V_{OL}	GPIOx output low voltage	I_{GPIOx}=5mA			0.4	V
GPIO 0, 1, 4, 7, 8, 9 (Outputs) (2)						
V_{OH}	GPIOx output high voltage	I_{GPIOx}= -2mA	2.9			V
V_{OL}	GPIOx output low voltage	I_{GPIOx}=2mA			0.4	V
SYNC OUT						
ϕ shift_00	GPIOx when configured as phase shifted DC/DC fsw clock output	Phase difference between fsw and GPIO6 when configured as SYNC(O).		0		degrees
ϕ shift_90	GPIOx when configured as phase shifted DC/DC fsw clock output	Phase difference between fsw and GPIO6 when configured as SYNC(O).		90		degrees
ϕ shift_120	GPIOx when configured as phase shifted DC/DC fsw clock output	Phase difference between fsw and GPIO6 when configured as SYNC(O).		120		degrees
ϕ shift_180	GPIOx when configured as phase shifted DC/DC fsw clock output	Phase difference between fsw and GPIO6 when configured as SYNC(O).		180		degrees
SYNC IN						
$f_{SYNC(300kHz)}$	Valid external clock frequency ($f_{SW\_internal}$ = 300kHz)		250		353	kHz
$f_{SYNC(400kHz)}$	Valid external clock frequency ($f_{SW\_internal}$ = 400kHz)		334		470	kHz
$f_{SYNC(450kHz)}$	Valid external clock frequency ($f_{SW\_internal}$ = 450kHz)		376		530	kHz

(1) GPIO9 is normally configured as I2C_IRQ1m (master): input pin. I2C specification requires use of external pullup resistor. Input thresholds (V_{IH}; V_{IL}) leakage current ($I_{I(LEAKAGE)}$)and deglitch timing (t_{DG}) specifications are apply when used as I2C_IRQ1m. Internal pullup and pulldown resistors are not used during this mode of operation.

(2) GPIO9 or GPIO1 may be configured as I2C_IRQ2s (slave): open-drain output pin. I2C specification requires use of external pullup resistor. Output threshold (V_{OL}) applies. Internal pullup and pulldown resistors are not used during this mode of operation.

7.15 BC1.2 Characteristics

Typical values correspond to TJ = 25°C. Minimum and maximumlimits apply over the –40°C to 150°C junction temperature range unless otherwise stated.V_{IN} = 13.5 V, EN =2 V, unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BC1.2 RESISTANCES						
R_{DCP_DAT}	Dedicated Charging Port Resistance between Px_DP and Px_DM	V_{Px_DP} = 0.6 V, V_{Px_DM} = 0V, measure DP to DM shorted resistance			200	Ω
$R_{DM\_DWN\_15k}$	Px_DM line pulldown resistance	V_{Px_DM} = 3.6V	12	15	18	kΩ
$R_{DM\_DWN\_20k}$	Px_DM line pulldown resistance	V_{Px_DM} = 3.6V	14.25	19.53	24.8	kΩ
DIVIDER MODES						
$V_{2.7V}$	Output Voltage on DPy pin	No load on DPy pin	2.57	2.7	2.83	V
$V_{2.7V}$	Output Voltage on DMy pin	No load on DMy pin	2.57	2.7	2.83	V
$R_{2.7V}$	Output Impedance on DPy	5µA pulled from DPy pin	24	30	36	kΩ
$R_{2.7V}$	Output Impedance on DMy	5µA pulled from DMy pin	24	30	36	kΩ
$V_{1.2V}$	Output Voltage on DMy	No load on DMy	1.12	1.2	1.28	V
$R_{1.2V}$	Output Impedance on DMy	5µA pulled from DMy	80	102	130	kΩ
HVDCP THRESHOLD VOLTAGES						
V_{DAT_REF}	Data detection voltage on DP or DM pin		0.25	0.325	0.4	V
V_{SEL_REF}	Output selection voltage DP or DM pin		1.8	2	2.2	V
DP AND DM OVERVOLTAGE PROTECTION						
V_{Dy_OVP}	OVP detection threshold for USB Px_DP and Px_DM pins	Initially $V_{PxDy} \leq 3.6$ V, then V_{Px_Dy} rises.	5.5		8.5	V

7.16 I2C Requirements and Characteristics

Typical values correspond to TJ = 25°C. Minimum and maximumlimits apply over the –40°C to 150°C junction temperature range unless otherwise stated.V_{IN} = 13.5 V, EN =2 V, unless otherwise stated. V_{DD} = I2C pullup voltage (3.3 V or 1.8 V)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{\text{I2C\_IRQ1s}}$, $\overline{\text{I2C\_IRQ2}}$						
$\overline{\text{I2C\_IRQ1m}}$						
SDA and SCL Characteristics (Standard, Fast, Fast-mode Plus)						
V_{IL}	Input low signal				0.54	V
V_{IH}	Input high signal		1.3			V
V_{DD} = 3.3 V INPUT LOGIC THRESHOLDS						
V_{IL}	Input low signal				0.9	V
V_{IH}	Input high signal		2.31			V
V_{HYS}	Input hysteresis		0.165			V
V_{OL}	Output low voltage	V_{DD} = 1.8V, I_{OL}=2 mA			0.36	
V_{OL}	Output low voltage	V_{DD} = 3.3V, I_{OL}=3 mA			0.4	V
I_{OL}	Max output low current	V_{OL}=0.4 V	12			mA
I_{LEAK}	Input leakage current	Voltage on pin = 3.3V	–5		5	µA
C_I	pin capacitance (internal)				10	pF
C_b	Capacitive load for each bus line (external). Applies in Standard-mode and Fast-mode.				400	pF
C_b	Capacitive load for each bus line (external). Applies in Fast-mode Plus.				550	pF
COMMON TIMING						
t_{SP}	I2C pulse width suppressed				50	ns

Typical values correspond to TJ = 25°C. Minimum and maximumlimits apply over the –40°C to 150°C junction temperature range unless otherwise stated.V_{IN} = 13.5 V, EN =2 V, unless otherwise stated. V_{DD} = I2C pullup voltage (3.3 V or 1.8 V)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDA and SCL Characteristics (Standard Mode)						
f_{SCLS}	Clock frequency (slave)	V_{DD} = 1.8V or 3.3V			100	kHz
$t_{HD;STA}$	Start or repeated start condition hold time	V_{DD} = 1.8V or 3.3V	4			µs
t_{LOW}	SCL Clock low time	V_{DD} = 1.8V or 3.3V	4.7			µs
t_{HIGH}	SCL Clock high time	V_{DD} = 1.8V or 3.3V	4			µs
$t_{SU;STA}$	Start or repeated start condition setup time	V_{DD} = 1.8V or 3.3V	4.7			µs
$t_{HD;DAT}$	Serial data hold time (1)	V_{DD} = 1.8V or 3.3V	0 (2)		- (3)	ns
$t_{SU;DAT}$	Serial data setup time	V_{DD} = 1.8V or 3.3V	250			ns
t_r	Rise time of SCL and SDA signals	V_{DD} = 1.8V or 3.3V; R_{PU} = 2.8 kΩ; Cb = 400pF; measure 0.3 × V_{DD} to 0.7 × V_{DD}			1000	ns
t_{of}	Output fall time from $V_{IH(MIN)}$ to $V_{IL(MAX)}$	V_{DD} = 1.8V or 3.3V; measure 0.3 × V_{DD} to 0.7 × V_{DD}			250 (4)	ns
t_f	Fall time of SCL and SDA signals (2) (4) (5)	V_{DD} = 1.8V, R_{PU} = 2.8 kΩ; 10 pF ≤ C_b ≤ 400 pF			300	ns
t_f	Fall time of SCL and SDA signals (2) (4) (5)	V_{DD} = 3.3V, R_{PU} = 2.8 kΩ; 10 pF ≤ C_b ≤ 400 pF			300	ns
$t_{SU;STO}$	Stop condition setup time	V_{DD} = 1.8V or 3.3V	4			µs
t_{BUF}	Bus free time between stop and start	V_{DD} = 1.8V or 3.3V	4.7			µs
$t_{VD;DAT}$	Valid data time (6)	Transmitting Data; V_{DD} = 1.8V or 3.3V, SCL low to SDA output valid			3.45 (3)	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting Data; V_{DD} = 1.8V or 3.3V, ACK signal from SCL low to SDA valid			3.45 (3)	µs
SDA and SCL Characteristics (Fast Mode)						
f_{SCLS}	Clock frequency (slave)	V_{DD} = 1.8V or 3.3V			400	kHz
$t_{HD;STA}$	Start or repeated start condition hold time	V_{DD} = 1.8V or 3.3V	0.6			µs
t_{LOW}	SCL Clock low time	V_{DD} = 1.8V or 3.3V	1.3			µs
t_{HIGH}	SCL Clock high time	V_{DD} = 1.8V or 3.3V	0.6			µs
$t_{SU;STA}$	Start or repeated start condition setup time	V_{DD} = 1.8V or 3.3V	0.6			µs
$t_{HD;DAT}$	Serial data hold time (1)	V_{DD} = 1.8V or 3.3V	0 (2)		- (3)	ns
$t_{SU;DAT}$	Serial data setup time	V_{DD} = 1.8V or 3.3V	100 (7)			ns
t_r	Rise time of SCL and SDA signals	V_{DD} = 1.8V or 3.3V; R_{PU} = 850 Ω; C_b = 400 pF; measure 0.3 × V_{DD} to 0.7 × V_{DD}	20		300	ns
t_{of}	Output fall time from $V_{IH(MIN)}$ to $V_{IL(MAX)}$	V_{DD} = 1.8V; measure 0.3 × V_{DD} to 0.7 × V_{DD}	6.55		250 (4)	ns
t_{of}	Output fall time from $V_{IH(MIN)}$ to $V_{IL(MAX)}$	V_{DD} = 3.3V; measure 0.3 × V_{DD} to 0.7 × V_{DD}	12		250 (4)	ns
t_f	Fall time of SCL and SDA signals (2) (4) (5)	V_{DD} = 1.8V; R_{PU} = 850 Ω; 10 pF ≤ C_b ≤ 400 pF	6.55		300	ns
t_f	Fall time of SCL and SDA signals (2) (4) (5)	V_{DD} = 3.3V; R_{PU} = 850 Ω; 10 pF ≤ C_b ≤ 400 pF	12		300	ns
$t_{SU;STO}$	Stop condition setup time	V_{DD} = 1.8V or 3.3V	0.6			µs
t_{BUF}	Bus free time between stop and start	V_{DD} = 1.8V or 3.3V	1.3			µs

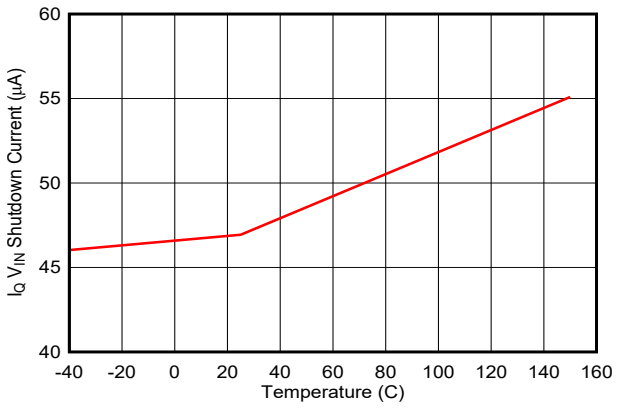
Typical values correspond to TJ = 25°C. Minimum and maximumlimits apply over the –40°C to 150°C junction temperature range unless otherwise stated.V_{IN} = 13.5 V, EN =2 V, unless otherwise stated. V_{DD} = I2C pullup voltage (3.3 V or 1.8 V)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{VD;DAT}$	Valid data time (6)	Transmitting Data; V_{DD} = 1.8V or 3.3V, SCL low to SDA output valid			0.9 (3)	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting Data; V_{DD} = 1.8V or 3.3V, ACK signal from SCL low to SDA (out) low			0.9 (3)	µs

(1) $t_{HD;DAT}$ = the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
(2) A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(3) The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode, but must be less than the maximum $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the setup time before it releases the clock.
(4) The maximum t_f for the SDA and SCL bus lines is stated in these tables as 300 ns is longer than the specified maximum t_{of} for the output stages (250 ns). This allows series protection resistors (R_S) to be connected between the SDA and SCL pins and the SDA and SCL bus lines without exceeding the maximum specified t_f.
(5) In Fast-mode Plus, fall time is specified the same for both ouput stage and bus timing. If series resistors (R_S) are used, designers should allow for this when considering bus timing.
(6) $t_{VD;DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
(7) A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)}$ + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

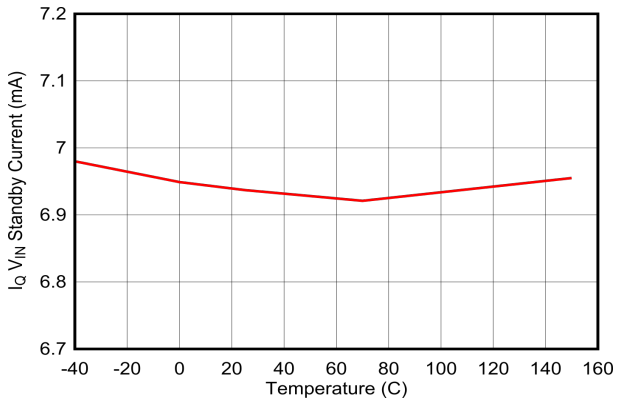
7.17 Typical Characteristics

At V_{IN} = 12 V, f_{sw} = 400 kHz, unless otherwise stated.



EN = 0 V

Figure 7-1. I_Q V_{IN} Shutdown Current vs Temperature



EN = 2 V

USB Port(s) not connected

Figure 7-2. I_Q V_{IN} Standby Current vs Temperature

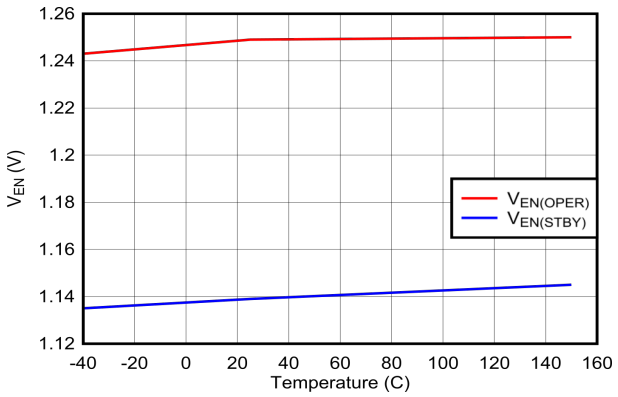


Figure 7-3. ENABLE/UVLO Thresholds vs Temperature

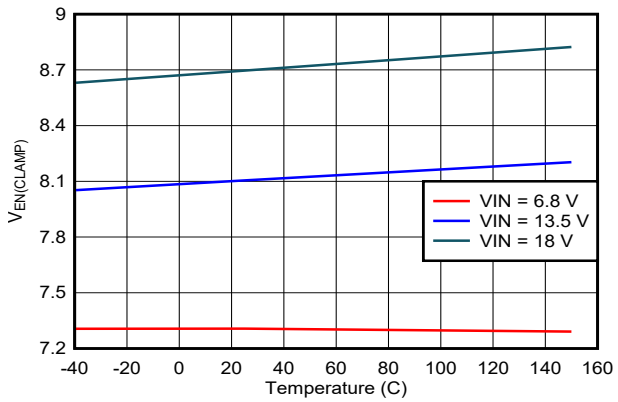


Figure 7-4. EN Clamp Voltage vs Temperature

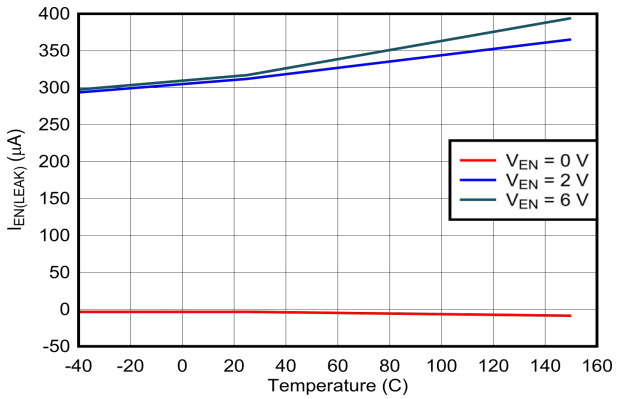


Figure 7-5. EN Leakage Current vs Temperature

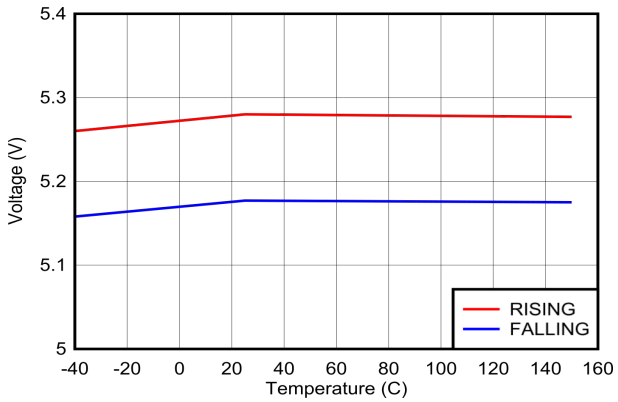


Figure 7-6. $V_{IN(UVLO)}$ vs Temperature

7.17 Typical Characteristics (continued)

At V_{IN} = 12 V, f_{sw} = 400 kHz, unless otherwise stated.

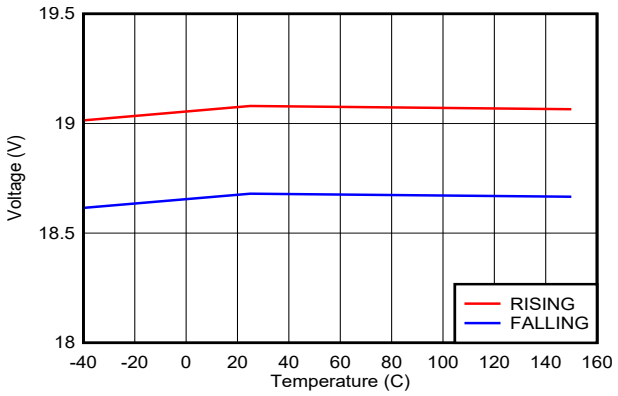


Figure 7-7. $V_{IN(OVP)}$ vs Temperature

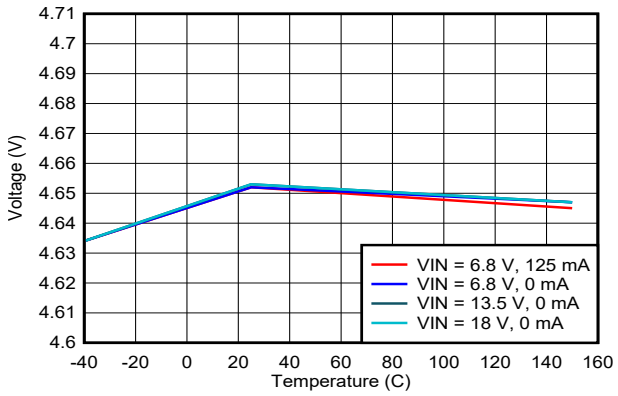


Figure 7-8. LDO_5V vs V_{IN} and Temperature

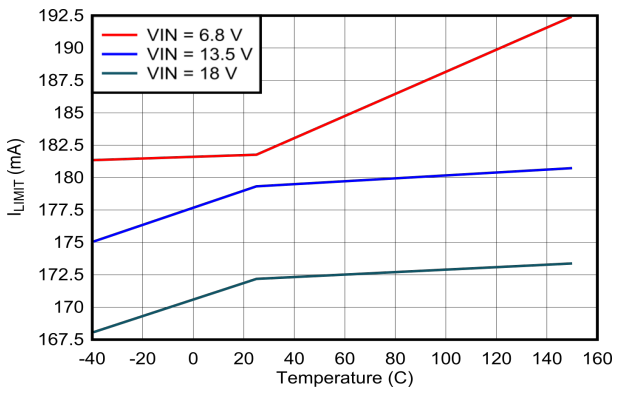


Figure 7-9. LDO_5V Current Limit vs V_{IN} and Temperature

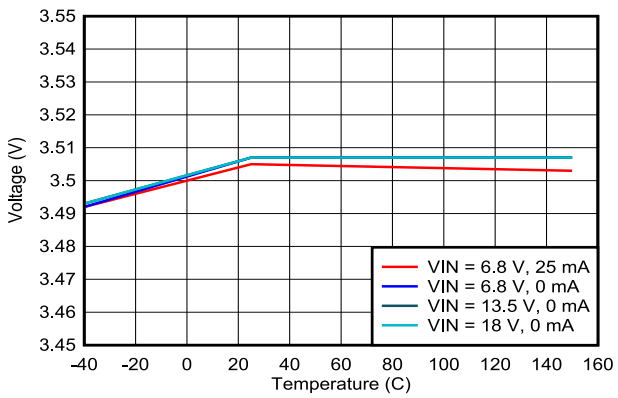


Figure 7-10. LDO_3V3 vs V_{IN} and Temperature

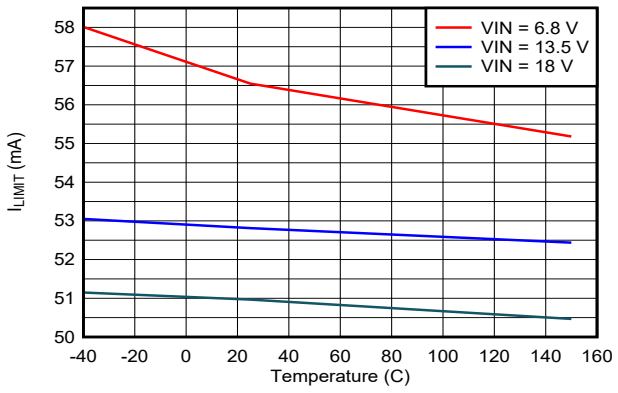


Figure 7-11. LDO_3V3 Current Limit vs V_{IN} and Temperature

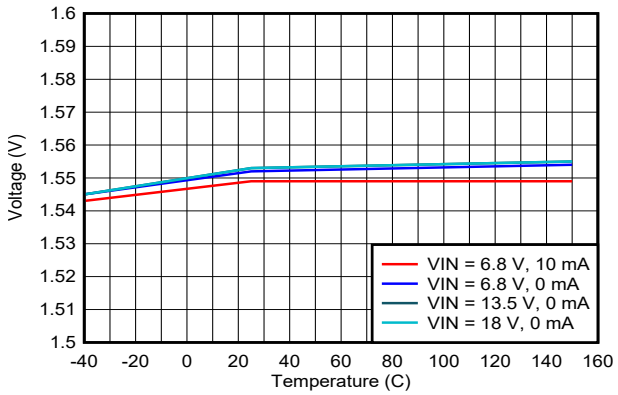


Figure 7-12. LDO_1V5 vs V_{IN} and Temperature

7.17 Typical Characteristics (continued)

At V_{IN} = 12 V, f_{sw} = 400 kHz, unless otherwise stated.

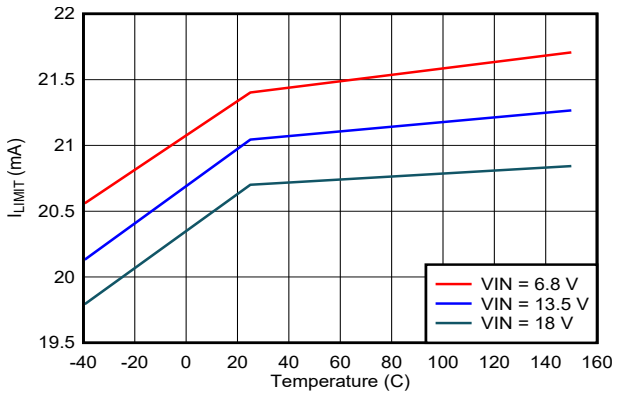


Figure 7-13. LDO_1V5 Current Limit vs V_{IN} and Temperature

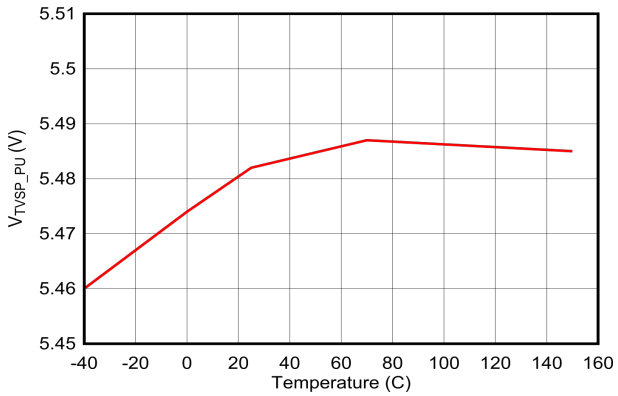


Figure 7-14. V_{TVSP_PU} vs Temperature

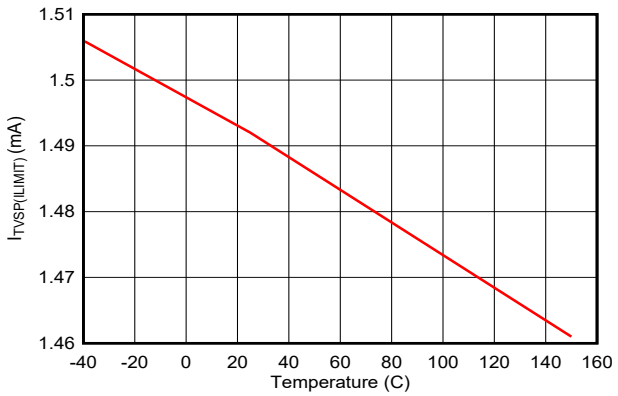


Figure 7-15. $I_{TVSP(ILIMIT)}$ vs Temperature

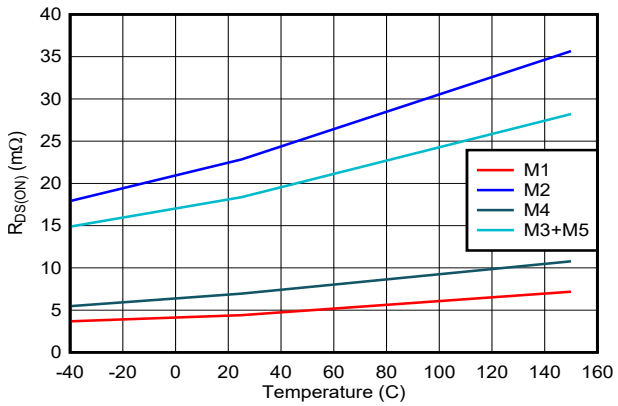


Figure 7-16. Buck-Boost Power FET $RDS_{(ON)}$ vs Temperature

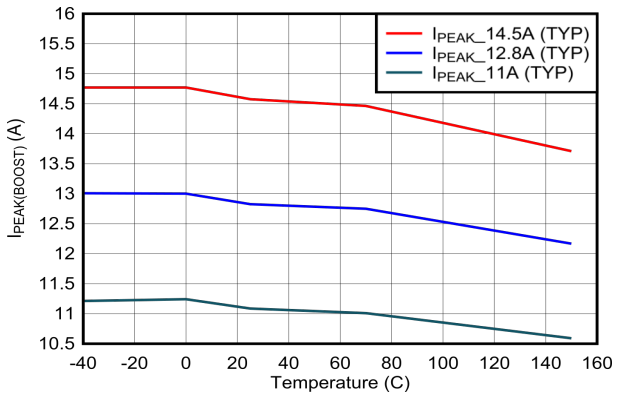


Figure 7-17. Boost Peak Current Limit vs Temperature (upper settings)

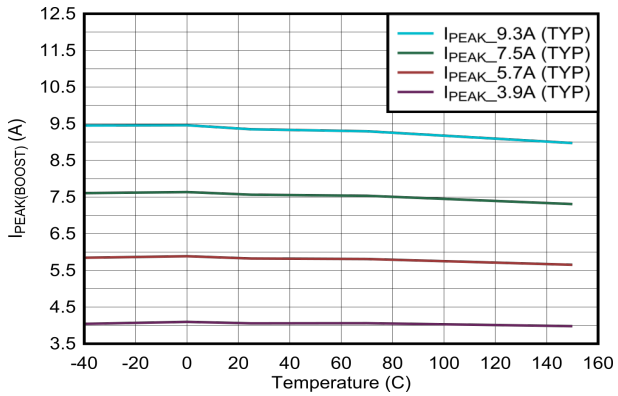


Figure 7-18. Boost Peak Current Limit vs Temperature (lower settings)

7.17 Typical Characteristics (continued)

At V_{IN} = 12 V, f_{sw} = 400 kHz, unless otherwise stated.

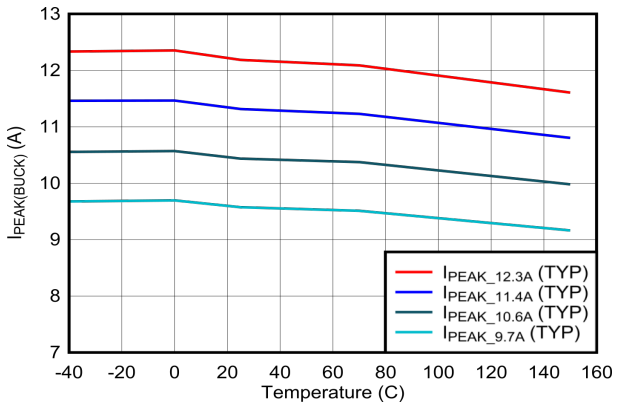


Figure 7-19. Buck Peak Current Limit vs Temperature (upper settings)

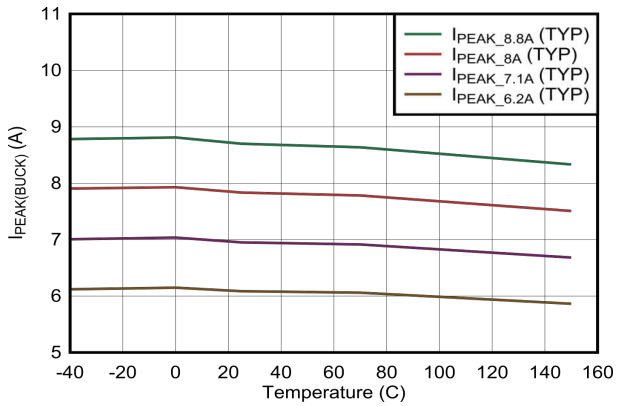


Figure 7-20. Buck Peak Current Limit vs Temperature (lower settings)

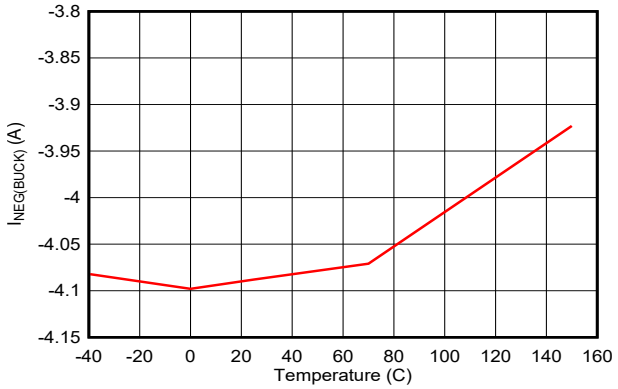


Figure 7-21. Buck Negative Current Limit vs Temperature

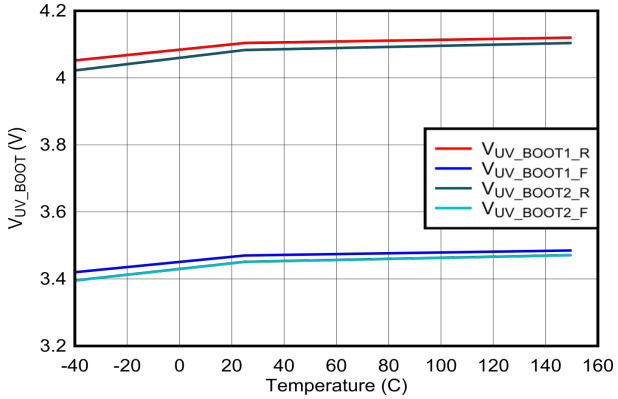


Figure 7-22. BOOTx UVLO vs Temperature

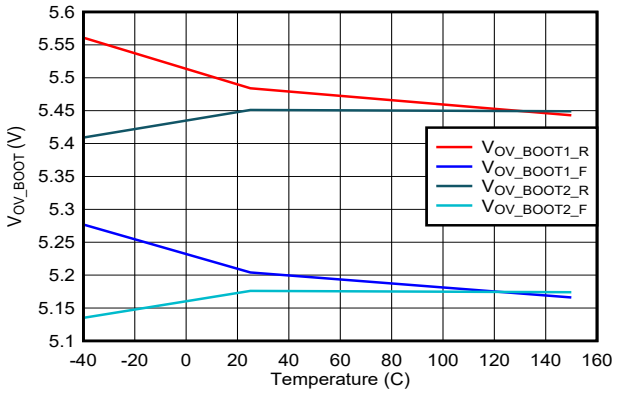


Figure 7-23. BOOTx OVP vs Temperature

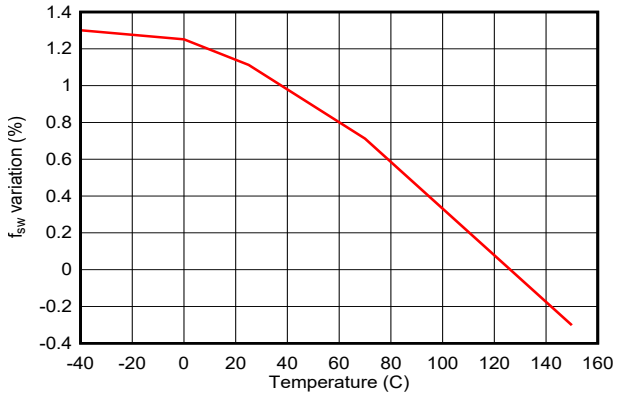


Figure 7-24. Buck-Boost Switching Frequency Variation vs Temperature

7.17 Typical Characteristics (continued)

At V_{IN} = 12 V, f_{sw} = 400 kHz, unless otherwise stated.

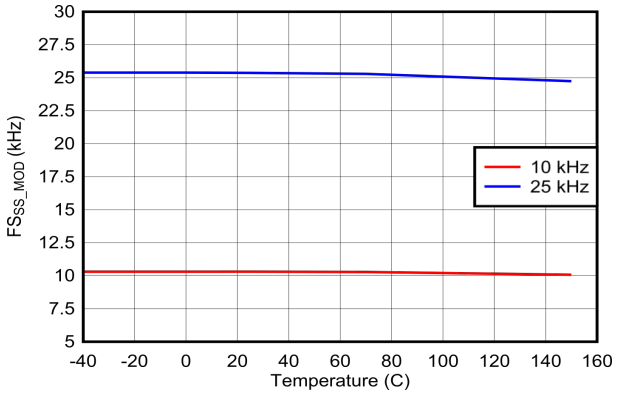
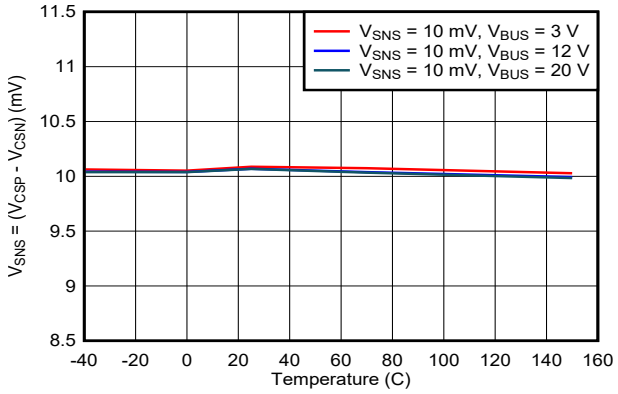
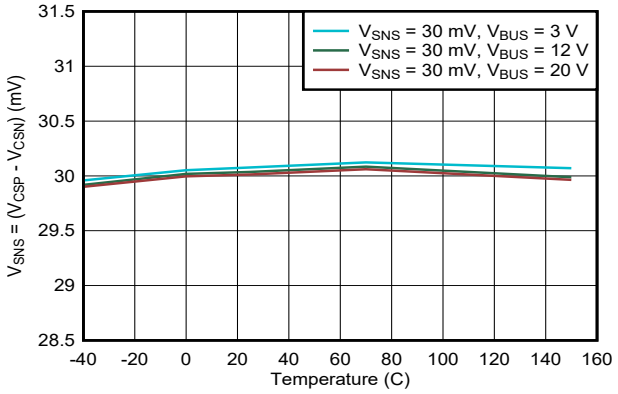


Figure 7-25. f_{SW} Dither Modulation Frequency vs Temperature



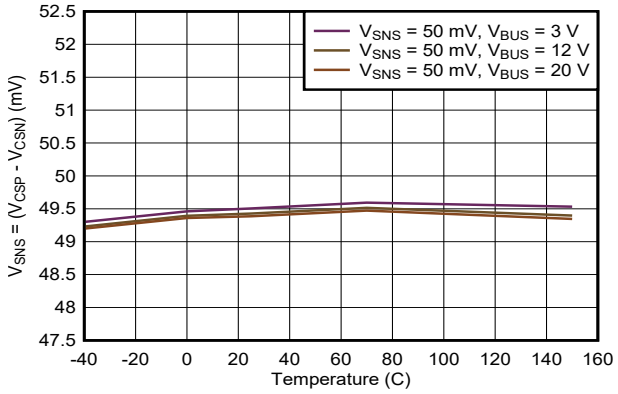
Target V_{SNS} for Current Limit = 10 mV
Current Limiting Engaged

Figure 7-26. Current Loop Regulation Voltage vs V_{BUS} and Temperature



Target V_{SNS} for Current Limit = 30 mV
Current Limiting Engaged

Figure 7-27. Current Loop Regulation Voltage vs V_{BUS} and Temperature



Target V_{SNS} for Current Limit = 50 mV
Current Limiting Engaged

Figure 7-28. Current Loop Regulation Voltage vs V_{BUS} and Temperature

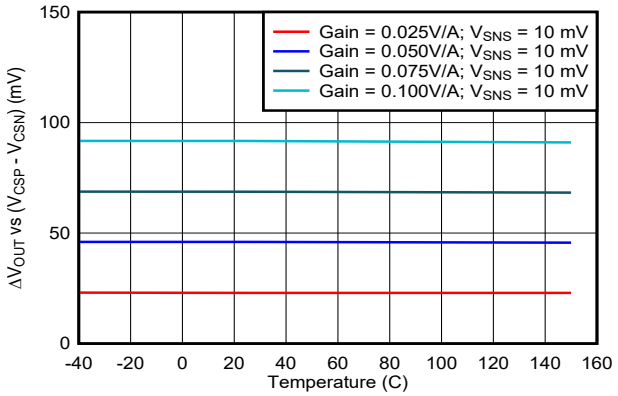


Figure 7-29. Cable Voltage Droop Compensation vs Temperature

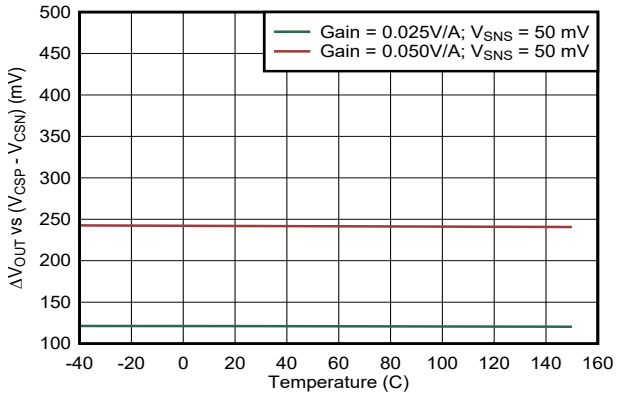


Figure 7-30. Cable Voltage Droop Compensation vs Temperature

7.17 Typical Characteristics (continued)

At V_{IN} = 12 V, f_{sw} = 400 kHz, unless otherwise stated.

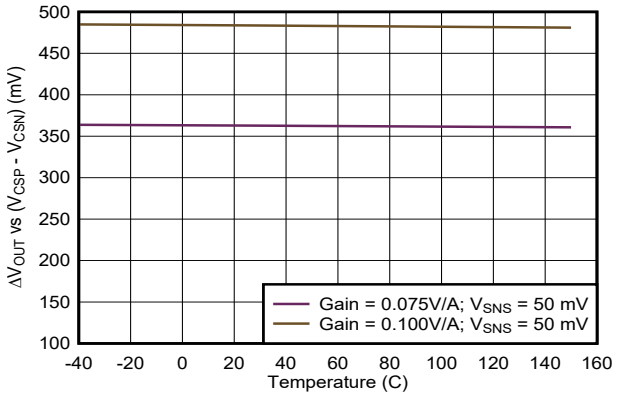
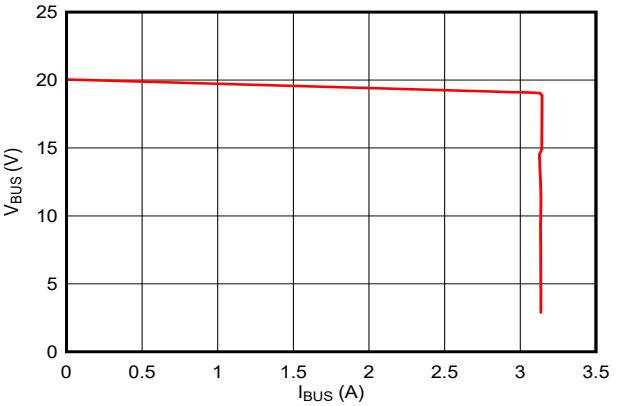
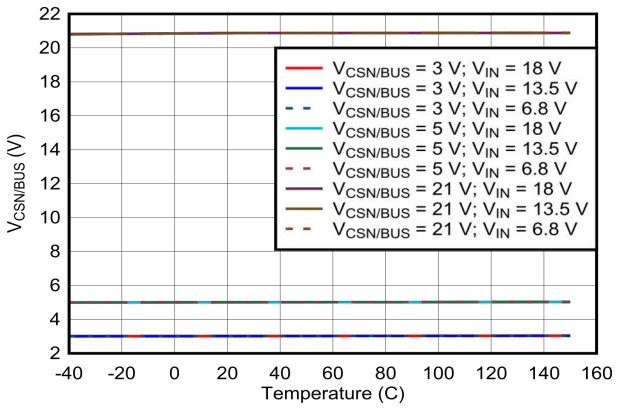


Figure 7-31. Cable Voltage Droop Compensation vs Temperature



V_{IN} = 13.5 V V_{BUS} = 20 V (CV) I_{LIMIT} = 3.15 A (CC)

Figure 7-32. Constant Voltage to Constant Current Transition



I_{BUS} = 0 A

Figure 7-33. Buck-boost Output Voltage Regulation vs Temperature

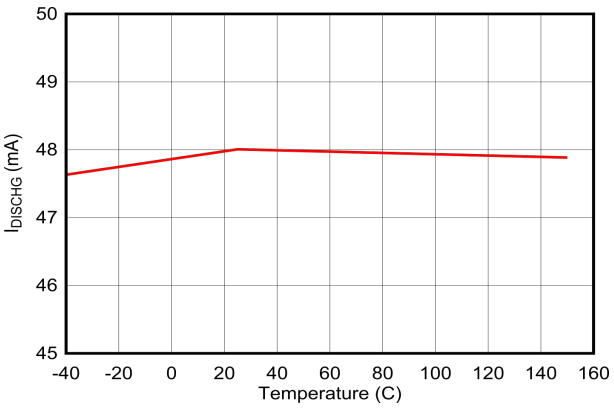


Figure 7-34. V_{BUS} Discharge Current vs Temperature

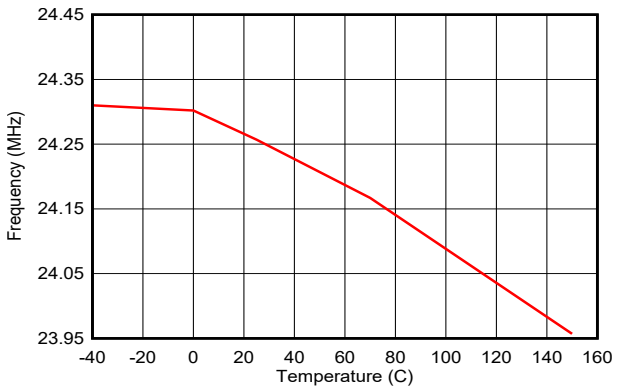


Figure 7-35. (M0) 24 MHz Oscillator vs Temperature

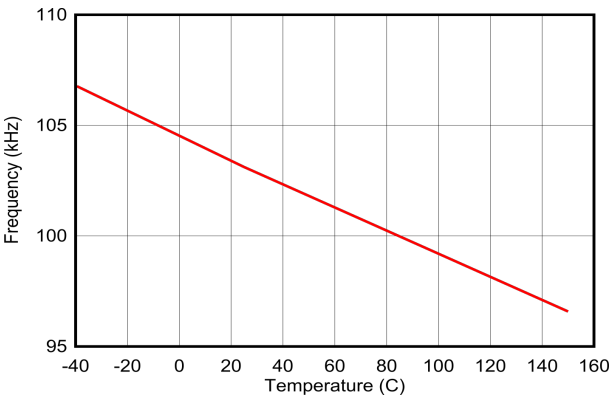


Figure 7-36. (M0) 100 kHz Oscillator vs Temperature

7.17 Typical Characteristics (continued)

At V_{IN} = 12 V, f_{sw} = 400 kHz, unless otherwise stated.

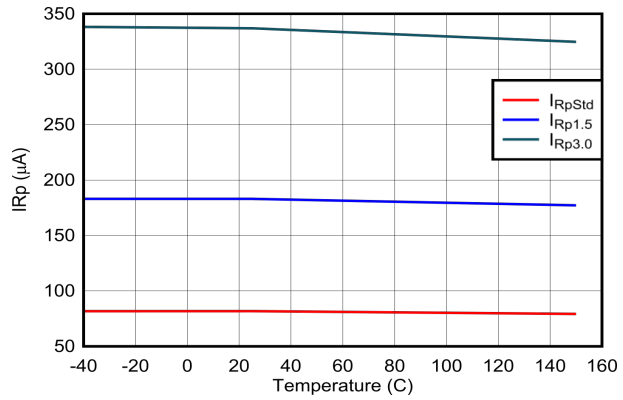


Figure 7-37. Type-C Cable Detect: I_{Rp} vs Temperature

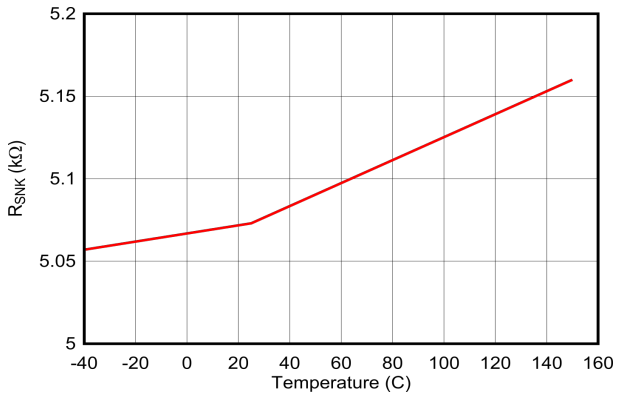


Figure 7-38. Type-C Cable Detect: R_{SNK} vs Temperature

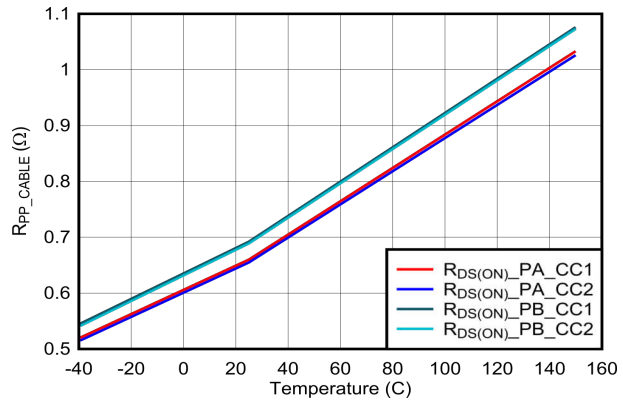


Figure 7-39. V_{CONN} Power Path: $R_{DS(ON)}$ vs Temperature

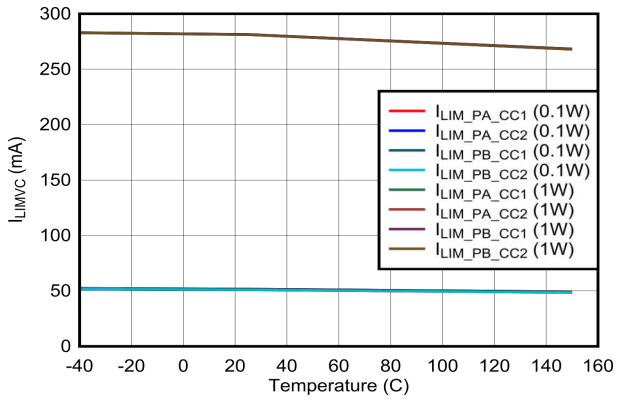


Figure 7-40. V_{CONN} Power Path: Current Limit vs Temperature

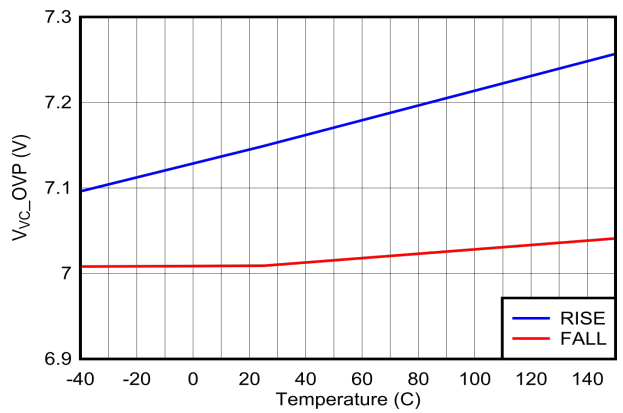


Figure 7-41. Type-C Cable Detect & V_{CONN}: Over-voltage Protection Thresholds vs Temperature

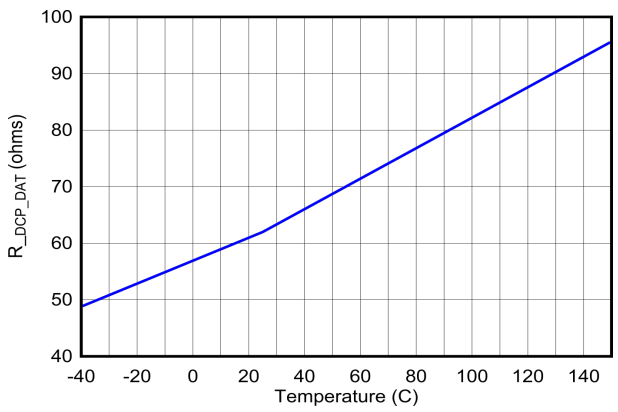


Figure 7-42. USB BC1.2: DP to DM Shorting Resistance, R_{DCP_DAT}

7.17 Typical Characteristics (continued)

At V_{IN} = 12 V, f_{sw} = 400 kHz, unless otherwise stated.

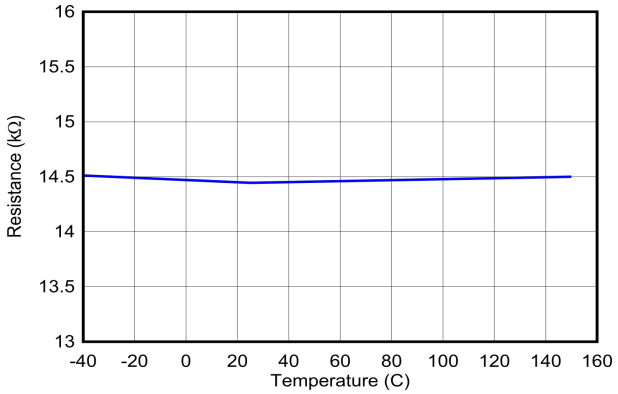


Figure 7-43. USB BC1.2: DM to AGND 15 kΩ Resistance, $R_{DM\_DWN\_15k}$

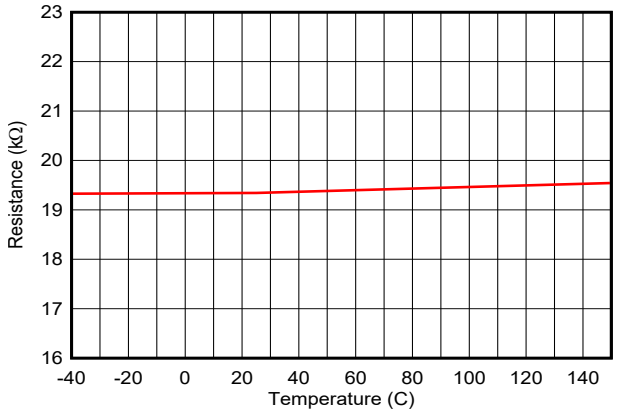


Figure 7-44. USB BC1.2: DM to AGND 20 kΩ Resistance, $R_{DM\_DWN\_20k}$

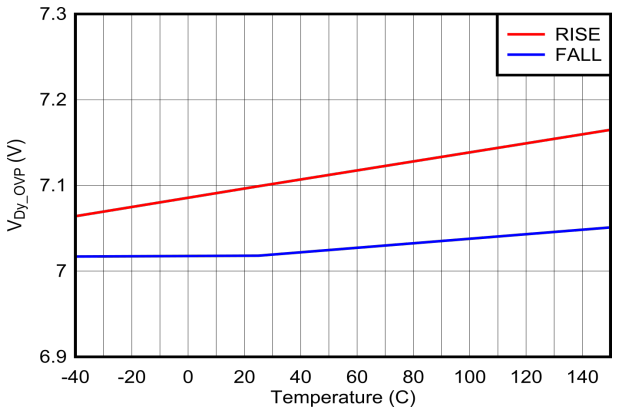
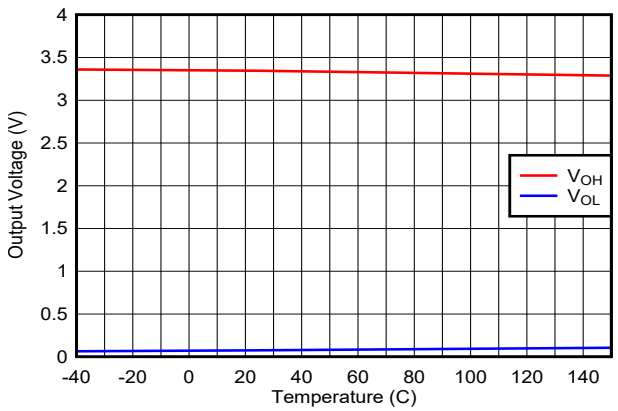
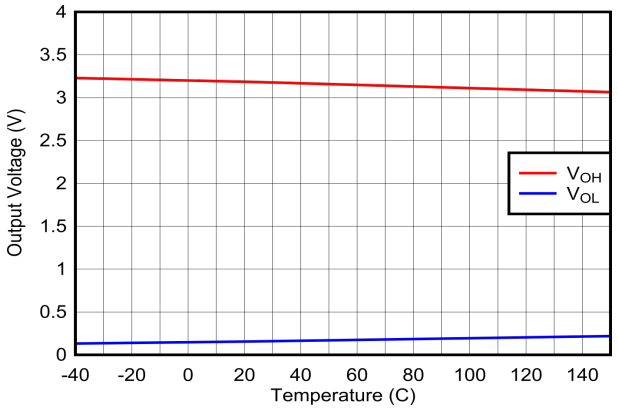


Figure 7-45. USB BC1.2: DP and DM Pin Over-voltage Protection Thresholds vs Temperature



GPIO 0, 1, 4, 7, 8, 9
IO = ±2 mA

Figure 7-46. GPIO: Output Voltage vs Output Current and Temperature



GPIO 2, 3, 5, 6
IO = ±5 mA

Figure 7-47. GPIO: Output Voltage vs Output Current and Temperature

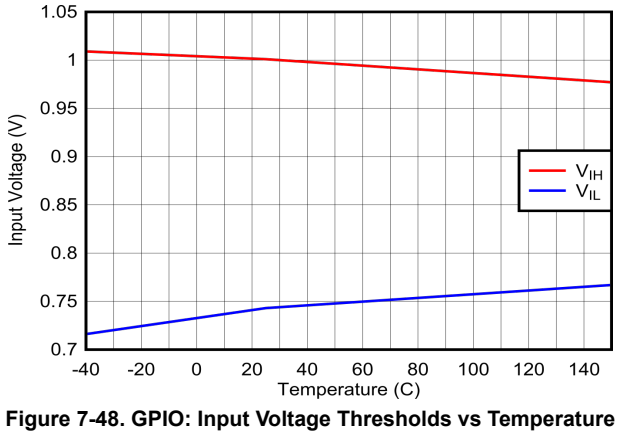


Figure 7-48. GPIO: Input Voltage Thresholds vs Temperature

8 Parameter Measurement Information

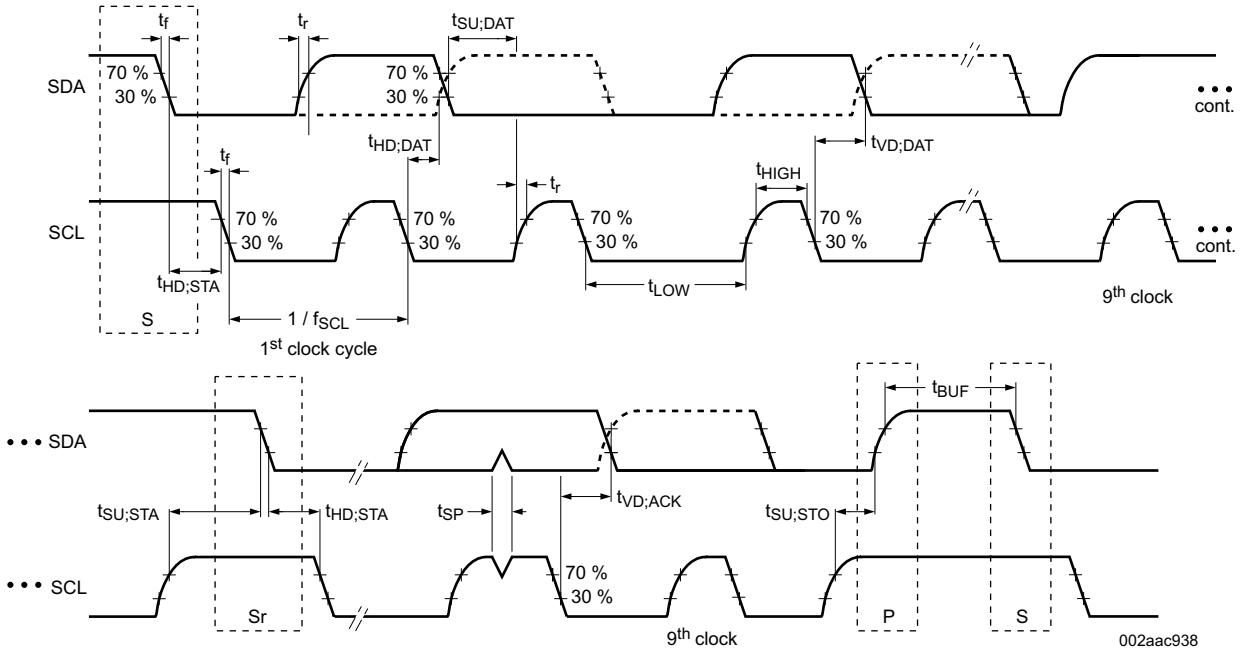


Figure 8-1. I²C Slave Interface Timing

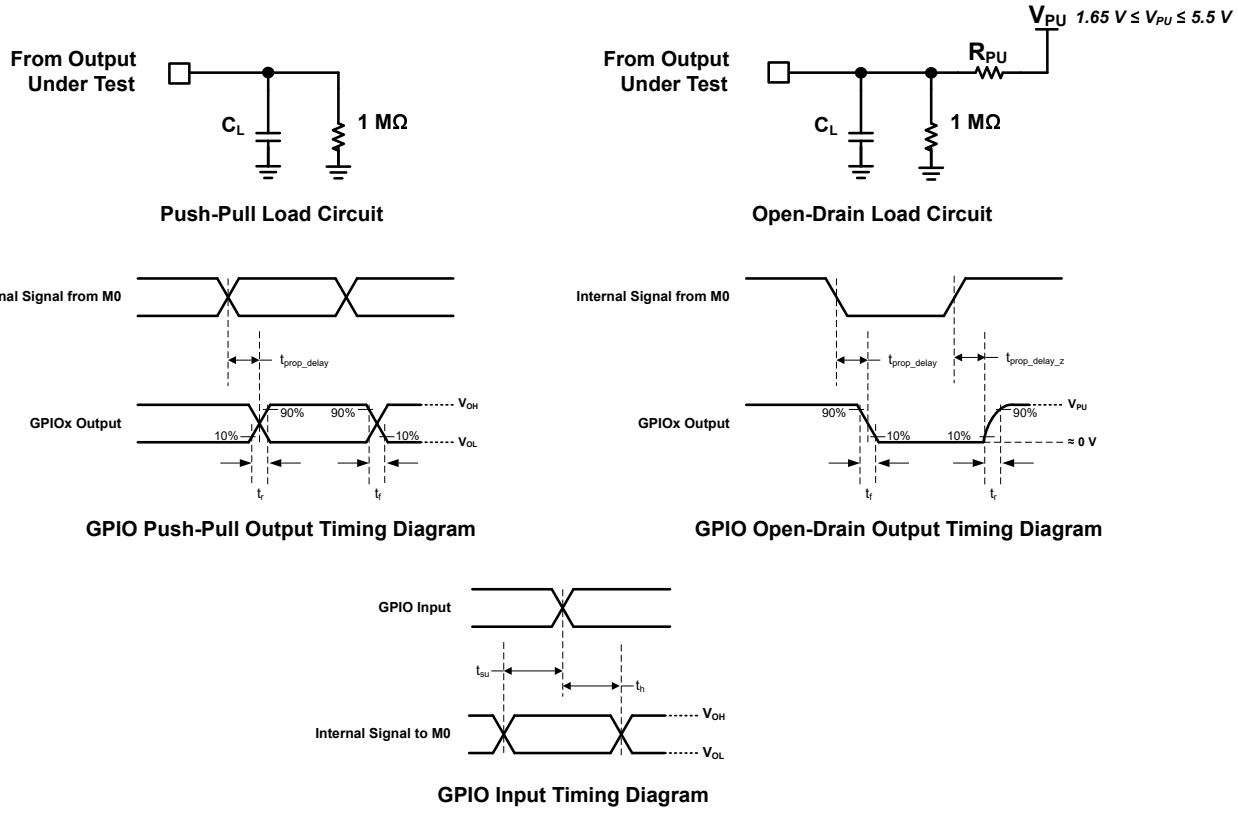


Figure 8-2. GPIO Output Timing Diagram (rise/fall vs capacitive load)

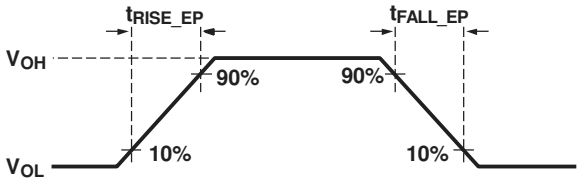


Figure 8-3. USB Endpoint Transmitter Rise and Fall Time

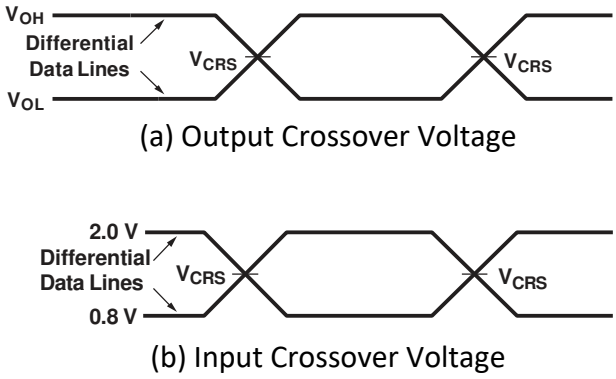


Figure 8-4. USB Endpoint Crossover Voltages

9 Detailed Description

9.1 Overview

The TPS25772-Q1 is a fully-integrated AEC-Q100 USB Power Delivery (USB-PD) source intended for use in 12-V automotive battery systems. Input supply pin, V_{IN}, must be connected to a load dump clamped battery supply, V_{BAT}, and never exceed 40 V (ABS MAX).

The device consists of seven sub-blocks: USB-PD controller; Type-C cable plug and orientation detection circuitry; USB Endpoint; USB Battery Charging Specification Version 1.2 (BC1.2) detection circuitry; digital core; device power management and supervisory circuitry; and a buck-boost converter integrated with 4 power switches.

The USB-PD controller provides the physical layer (PHY) functionality of the USB-PD protocol. The USB-PD data is output through either the Px_CC1 pin or the Px_CC2 pin, depending on the orientation of the reversible USB Type-C cable. For a high-level block diagram of the USB-PD physical layer, a description of its features and more detailed circuitry, see *USB-PD Physical Layer*.

The cable plug and orientation detection analog circuitry automatically detects a USB Type-C cable plug insertion and also automatically detects the cable orientation. For a high-level block diagram of cable plug and orientation detection, a description of its features and more detailed circuitry, see *Cable Plug and Orientation Detection*.

A USB Endpoint is included for downloading configuration information and firmware updates. When enabled by firmware, the USB Endpoint connects to the Port A DP and DM pins.

The USB BC1.2 sub-block contains circuitry to support legacy USB charging methods which signal on the USB DP and DM data lines including: DCP, Divider-3, 1.2 V mode, and HVDCP. See BC 1.2, legacy and fast charging modes (Px_DP, Px_DM).

The power management and supervisory circuitry generates the LDO_5V, LDO_3V3, and LDO_1V5 voltage rails used by the device. LDO_5V supplies the LDO_3V3 and LDO_1V5 rails. For a high-level block diagram of the power management circuitry, a description of its features and more detailed operation, see *Internal LDO Regulators* section.

The digital core contains an ARM Cortex-M0 with 160-kB ROM and 27-kB RAM memory. The ROM contains firmware code to execute device functionality. RAM stores application configuration code created using the Graphical User Interface (GUI) and post-manufacturing firmware updates. The digital core is the engine for autonomously managing the system including: USB port connection status and communication; system power budget and allocation; system thermal monitoring and load shedding; and fault detection and reporting. All devices contain one controller I^2C port (I^2C1) for controlling external peripherals such as external EEPROM memory; DC/DC converters; USB data multiplexers/redrivers; GPIO expanders; and additional temperature sensors. Some devices include an I^2C target port (I^2C2) for connection to an external processor, HUB or embedded controller. An integrated 8-bit analog-to-digital converter ADC (see the *ADC* section), monitors USB port telemetry information. USB port connection status, voltage, current and fault information can be read from I^2C2 target port. For a high-level block diagram of the digital core and a description of its features, see the *Digital Core* section.

The integrated buck-boost converter is the PA_VBUS power source. It operates in buck mode when V_{IN} is greater than V_{OUT} and boost mode when V_{IN} is less than V_{OUT}. When V_{IN} and V_{OUT} are nearly the same, it operates in transition mode.

Dual Port Devices

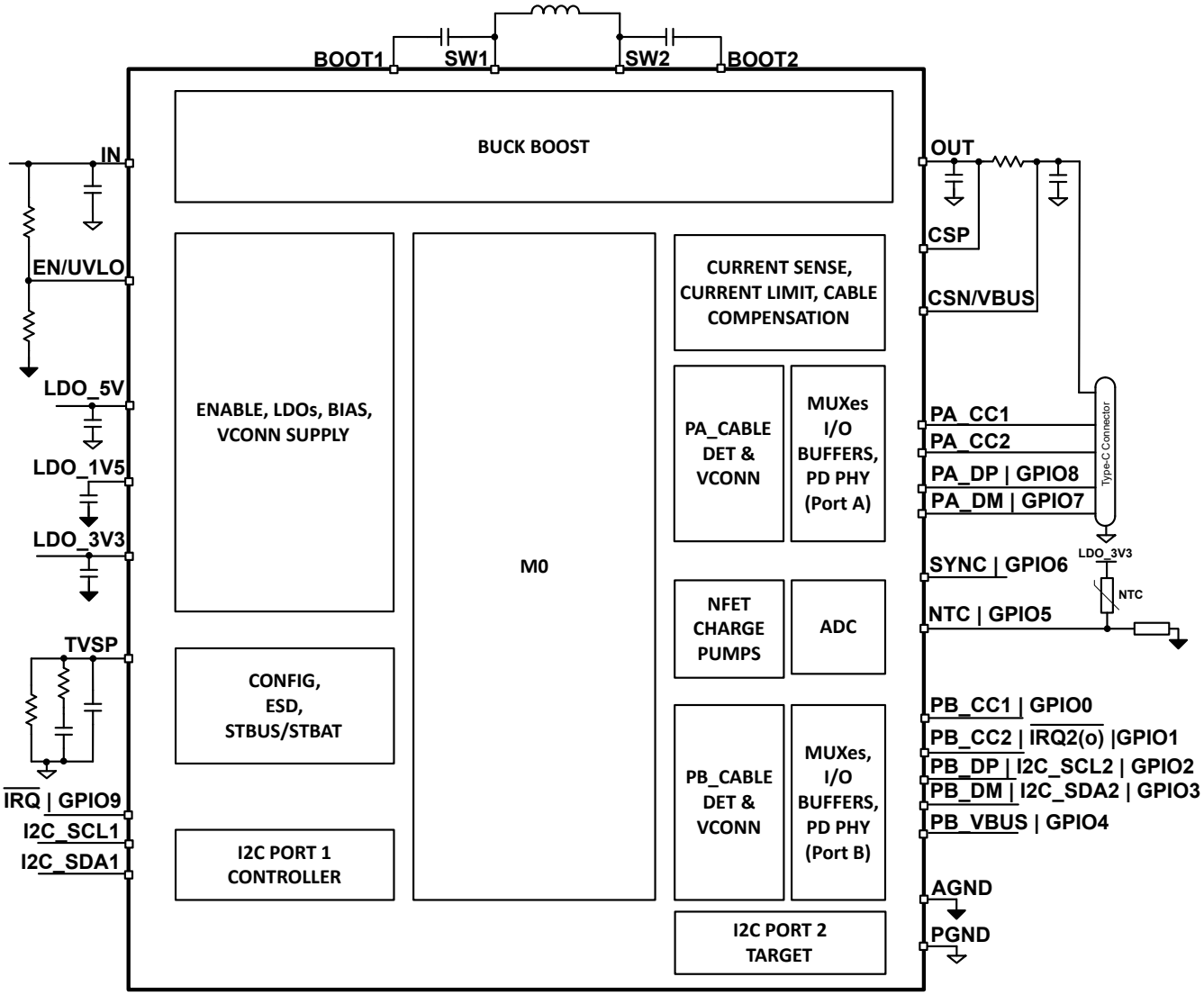
TPS25772-Q1 is a dual USB port device. Refer to *Device Comparison Table* for functional differences. The TPS25772-Q1 consists of a single 3 to 21 V output internal buck-boost converter, two USB-PD port controllers providing cable plug and orientation detection, two internal VCONN source paths, legacy USB Battery Charging Specification v1.2 Dedicated Charging Port (DCP) as well as legacy (non-USB compliant) charger detection including: Divider-3, 1.2 V, and HVDCP modes on each port.

PB_VBUS for TPS25772-Q1 must be supplied from an external power source. The implementation of this power is shown in Table 9-1.

Table 9-1. Supported Dual USB Port Implementations

Port A (PA)	Port B (PB)	Port B (PB) Suggested Power Devices
USB Power Delivery (including PPS)	Type-C with USB Power Delivery (including PPS)	TPS55288-Q1

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Device Power Management and Supervisory Circuitry

9.3.1.1 VIN UVLO and Enable/UVLO

The TPS25772-Q1 has one internally fixed V_{IN} UVLO and one user programmable UVLO using the EN/UVLO pin. Both thresholds must be cleared for the device to start up.

- The fixed $V_{IN(UVLO)}$ has a rising threshold between 5 and 5.5 V to ensure internal circuits have sufficient headroom for proper operation.
- The EN/UVLO pin provides the user with a resistor programmable UVLO threshold and master enable / disable for the device.

The EN/UVLO pin has three distinct voltage ranges: shutdown, standby, and operating. When the EN/UVLO pin is below the standby threshold $V_{EN(STBY)}$, the device is disabled in a low power shutdown. When EN/UVLO voltage is greater than the standby threshold $V_{EN(STBY)}$ but less than the operating threshold $V_{EN(OPER)}$, the internal bias rails, LDO_5V, LDO_3V3, and LDO_1V5 regulators are enabled but remaining device functions are disabled. When EN/UVLO is greater than the operating threshold $V_{EN(OPER)}$ and LDO_5V, LDO_3V3 and LDO_1V5 regulators are above their respective undervoltage threshold UVLO thresholds, the device is fully functional. The EN/UVLO pin includes fixed hysteresis between the shutdown mode and the standby mode.

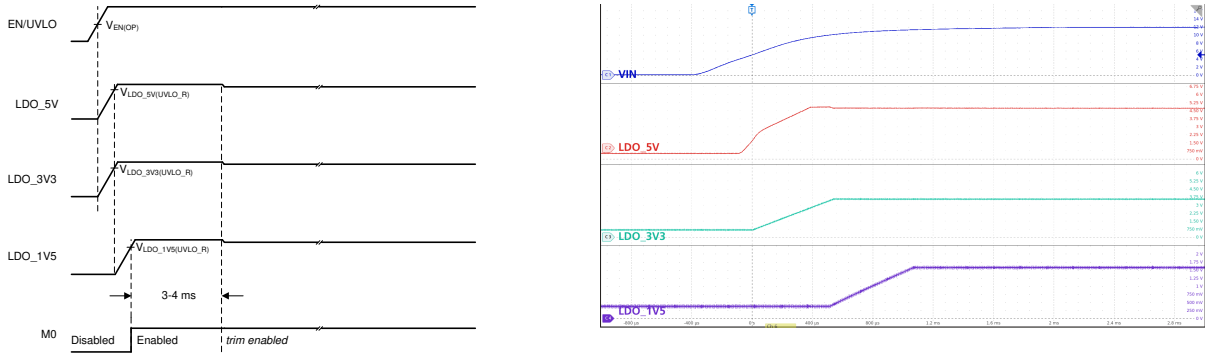


Figure 9-1. EN/UVLO and LDO Sequencing

Table 9-2. EN/UVLO and LDO_UVLO Operation

EN/UVLO (1)	LDOs	DEVICE OPERATION
$V_{EN/UVLO} < V_{EN(LDO\_V5V\_F)}$	—	Shutdown: LDO_5V, LDO_3V3 and LDO_1V5 OFF. M0 (MCU) is OFF.
$V_{EN(LDO\_V5V\_R)} < V_{EN/UVLO} < V_{EN(STBY)}$	—	Standby: LDO_5V, LDO_3V3 and LDO_1V5 ON. M0 (MCU) is OFF.
$V_{EN/UVLO} > V_{EN(OPER)}$	LDO_5V < $V_{LDO\_5V(UVLO\_R)}$, or LDO_3V3 < $V_{LDO\_3V3(UVLO\_R)}$; or LDO_1V5 < $V_{LDO\_1V5(UVLO\_R)}$	LDO_5V, LDO_3V3 and LDO_1V5 ON, M0 (MCU) is OFF.
$V_{EN/UVLO} > V_{EN(OPER)}$	LDO_5V > $V_{LDO\_5V(UVLO\_R)}$, and LDO_3V3 > $V_{LDO\_3V3(UVLO\_R)}$, and LDO_1V5 > $V_{LDO\_1V5(UVLO\_R)}$	Operating: M0 (MCU) is ON.

(1) Valid when $V_{IN} > V_{IN(UVLO\_R)}$.

In some cases an input UVLO level different than that provided by the internal $V_{IN(UVLO)}$ is needed. This can be accomplished by using the circuit shown in *UVLO Threshold Programming*. The input voltage at which the device turns on is designated V_{ON}; while the turnoff voltage is V_{OFF}. First a value for R_{ENB} is chosen in the range of 13 kΩ to 22 kΩ. Use Equation 1 and Equation 2 to calculate R_{ENT} and V_{OFF}.

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN(OPER)}} - 1\right) \times R_{ENB} \quad (1)$$

The hysteresis between the UVLO turn-on threshold and turn-off threshold is set by the upper resistor in the EN/UVLO resistor divider and is given by:

$$V_{OFF} = \left(1 - \frac{V_{EN(HYS)}}{V_{EN(OPER)}}\right) \times V_{ON} \quad (2)$$

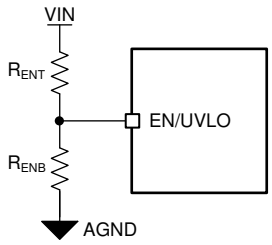


Figure 9-2. UVLO Threshold Programming

Where

- V_{ON} = V_{IN} turn-on voltage
- V_{OFF} = V_{IN} turn-off voltage

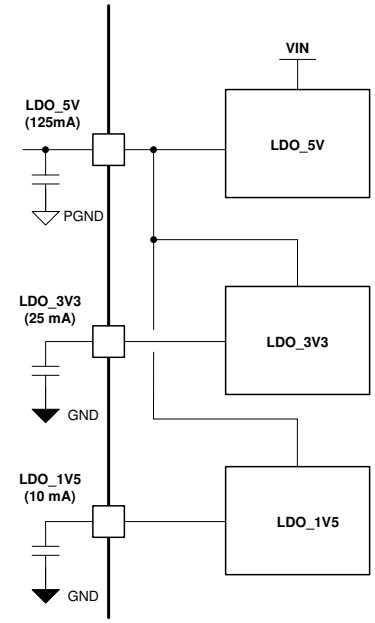
Note: Ensure R_{ENT} ≥ 47 kΩ

If the programmable UVLO is not required, the EN/UVLO pin can be connected to the IN pin with a 47 kΩ, or larger, resistor.

9.3.1.2 Internal LDO Regulators

Three internal LDOs provide regulated supplies for operation of internal circuitry.

- LDO_5V: Supplies buck-boost gate drive circuitry, LDO_3V3, LDO_1V5, and PA and PB VCONN power paths. External bypass capacitance, C_{LDO_5V} is required for proper operation. It is highly recommended to include an additional high frequency 0.1 µF capacitor in parallel with C_{LDO_5V}. C_{LDO_5V} and the parallel high frequency should be placed as close to the LDO_5V pin as possible. This capacitance: 1) provides energy storage for the buck-boost internal FET gate drivers, and 2) is required to stabilize the internal 5-V LDO in applications where an external 5-V supply is not connected. The TPS25772-Q1 will not operate (release reset) until $V_{LDO\_5V(UVLO\_R)}$ threshold is met. Hard reset occurs when V_{LDO_5V} < $V_{LDO\_5V(UVLO\_F)}$ threshold. Current from LDO_5V returns to PGND pin. The LDO_5V output may be used to supply a small external loads such as indicator LEDs. When supplying external components, it is recommended that the total external load current not exceed 25 mA (MAX).
  - 0.1W VCONN: when enabled in the application configuration GUI, LDO_5V is capable of sourcing 20 mA each to PA_VCONN and PB_VCONN.
  - 1W VCONN: when enabled in the application configuration GUI, this mode of operation *requires* an external 4.75 - 5.5 V, 500-mA capable supply connected to LDO_5V. Back-feeding of LDO_5V is allowed.
- LDO_3V3: Supplies internal analog circuits, GPIO buffers, USB PD and the USB Endpoint PHYs. External bypass capacitance of C_{LDO_3V3} is required for proper operation. An additional 0.1 µF capacitor in parallel with C_{LDO_3V3} is highly recommended to filter high frequency noise from the I/O buffers and PHYs. The LDO_3V3 can supply external circuits at up to 25 mA. Expected loads include: EEPROM (5mA), NTC resistor divider network (< 1 mA). Current may be drawn up to $I_{LDO\_3V3(ILIMIT)}$. Note: the USB PD and Endpoint PHYs draw current from LDO_3V3. If a CCx or Dx pin is shorted to GND during a transmission the current drawn may reach the current limit threshold. Similarly, if any GPIO pins are configured as push-pull outputs and a GPIO short to GND event occurs, the LDO_3V3 current limit may be reached. Current returns to AGND pin.
- LDO_1V5: Supplies digital core. External bypass capacitance of C_{LDO_1V5} is required for proper operation. An additional 0.1 µF capacitor in parallel with C_{LDO_1V5} is highly recommended to filter noise generated by the digital core. The M0 is held in reset until all three UVLO_R (rising) thresholds are met. Current returns to AGND pin.



Note: LDO_5V max regulation current includes LDO_3V3 (25 mA) and LDO_1V5 (10 mA)

Figure 9-3. Internal LDO Connection Diagram

9.3.2 TVSP Device Configuration and ESD Protection

The **T**ransient **V**oltage protection and firmware **S**etting **P**in (**TVSP**) has three functions: 1) Boot configuration settings; 2) USB connector pin short to V_{BUS} or V_{BAT} protection; and 3) USB connector pin enhanced ESD protection.

- **R_{TVSP}:** At power on, the resistance between the TVSP pin and PGND determines the boot method, USB PD port I^2C addresses and I^2C logic thresholds. Refer to *Table 9-4 and Table 9-5*. The most common configuration is shown in Figure 9-4 with R_{TVSP} open, corresponding to TVSP Index 0. During device initialization and boot, typically within 4 seconds after power on, V_{IN} must be above 7.6 V to ensure proper bias of the TVSP pin to 5.5 V. Once boot is complete the device can operate over the full V_{IN} range.
- **C_{TVSP}:** A 0.1-µF capacitor (C_{TVSP}) *must* be connected to PGND. Place C_{TVSP} as close to the TVSP pin as possible to minimize parasitic inductance. C_{TVSP} is part of the centralized protection circuitry fortifying connector pins Px_CCy, Px_DP and Px_DM from damage during short to V_{BUS}, V_{BAT} and ESD events. A 40-V 0.1-µF capacitor is recommended for proper operation of the internal TVSP regulator circuit.
- **TVSP Damper Network:** Capacitance, C_{DAMP}, and resistance, R_{DAMP}, form an RC network preventing excessive current from flowing inside the device durging connector pin over-voltage and ESD events.
  - **C_{DAMP}:** A 0.47-µF capacitor *must* be connected in series with R_{DAMP} to PGND. A 40-V 0.47-µF capacitor is recommended.
  - **R_{DAMP}:** A 10-Ω resistor *must* be connected in series with C_{DAMP} to PGND. A 0.25-W rating is recommended.

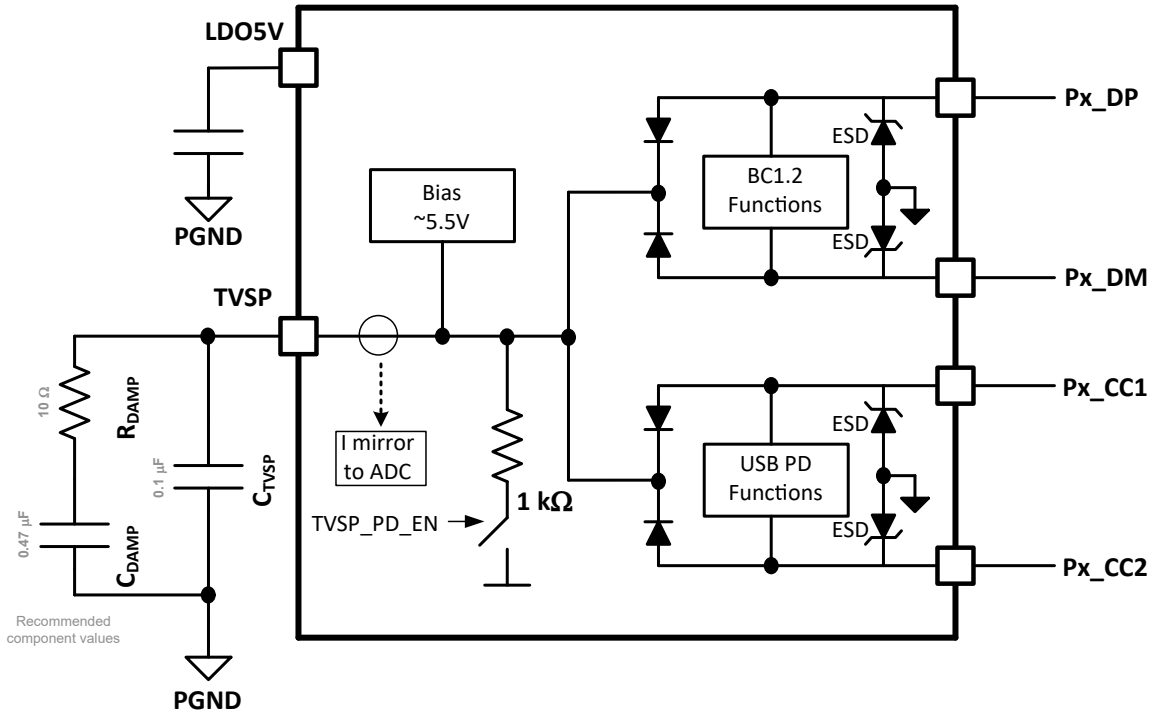


Figure 9-4. Basic TVSP Pin Connection

Table 9-3. Recommended TVSP Components

C_{TVSP}	R_{DAMP}	C_{DAMP}
0.1 µF	10 Ω	0.47 µF

Table 9-4. R_{TVSP} Configuration Settings (TPS25762CQRQLRQ1 and TPS25772CQRQLRQ1)

$R_{TVSP\ (kΩ)}$ (1)	TVSP Index	ADC Value	I2C Target Port Addresses (A | B)(2)	I2C Logic (V_{DD})	Boot Mode
Open	0	≤ 10 (0x0A)	0x22 | 0x26	3.3 V	EEPROM
93.1	1	≤ 24 (0x18)	0x23 | 0x27	3.3 V	External HUB/MCU
47.5	2	≤ 42 (0x2A)	0x22 | 0x26	1.8 V	EEPROM
29.4	3	≤ 63 (0x3F)	0x23 | 0x27	1.8 V	External HUB/MCU
20.0	4	≤ 89 (0x59)	0x23 | 0x27	3.3 V	EEPROM
14.7	5	≤ 119 (0x77)	0x22 | 0x26	3.3 V	External HUB/MCU
11.0	6	≤ 156 (0x9C)	0x23 | 0x27	1.8 V	EEPROM
8.45	7	≤ 201 (0xC9)	0x22 | 0x26	1.8 V	External HUB/MCU
6.65	8	≤ 255 (0xFF)	0x22 | 0x26	3.3 V	Firmware Update

Table 9-5. RTVSP Configuration Settings (TPS25762CAQRQLRQ1 and TPS25762CAQRQLRQ1)

$R_{TVSP\ (kΩ)}$ (1)	TVSP Index	ADC Value	I2C Target Port Addresses (A | B)(2)	I2C Logic (V_{DD})	Boot Mode
Open	0	≤ 201 (0x0A)	0x22 | 0x26	3.3 V	EEPROM
5.6	8	≤ 255 (0xFF)	0x22 | 0x26	3.3 V	Firmware Update

(1) 1% resistor required.
(2) 0x22h = 0100010; 0x26h = 0100110; 0x23h = 0100011; 0x27 = 0100111

Applications requiring a configuration other than standard, TVSP Index 0 (R_{TVSP} open), as shown in Table 9-4 must implement a circuit similar to the one shown in Figure 9-5. The base of the bipolar transistor is connected to LDO_5V to provide proper power up sequencing of the TVSP resistor - OFF when TPS25772-Q1 is disabled

and ON when TPS25772-Q1 is enabled. A 2N2222 is recommended for its large collector-emitter breakdown voltage, low-cost and wide availability.

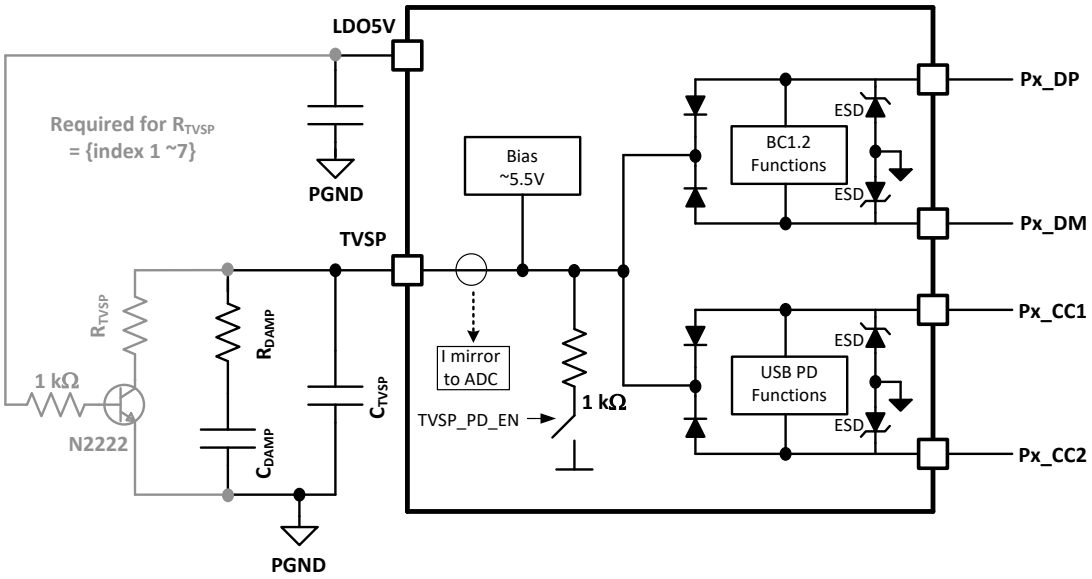


Figure 9-5. R_{TVSP} Circuit Configuration

Device firmware can be updated using the USB Endpoint on the PA_DP and PA_DM pins. To enable firmware update mode, boot the device with a resistance corresponding to Index 8 between TVPS and PGND. A boot cycle can be performed by power cycling the device or by pulling the EN/UVLO pin momentarily below $V_{EN(OPER)}$ threshold. An example circuit to enable USB Endpoint firmware update mode is shown in Figure 9-6

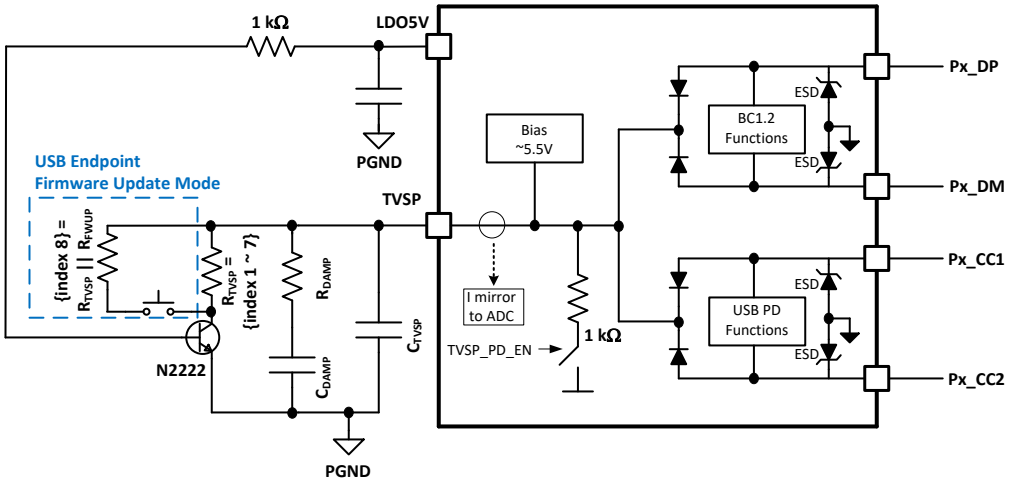


Figure 9-6. Example Circuit to Enable USB Endpoint Firmware Update Mode

9.3.3 Buck-Boost Regulator

9.3.3.1 Buck-Boost Regulator Operation

The TPS25772-Q1 devices utilize a fixed frequency, current mode control buck-boost converter. This converter operates in forced continuous conduction mode (CCM) and therefore allows inductor current to flow in either direction at light loads. The power train consists of five N-Channel power MOSFETs. See Figure 9-7. Transistors M1 and M2 are the high-side and low-side buck FETs. Transistors M3 and M4 are the high-side and low-side boost FETs. Transistor M5 blocks reverse conduction from OUT to SW2 during input overvoltage transients as explained in *VIN Supply and VIN Over-Voltage Protection*.

- **IN:** Receives power from the battery. The input bulk capacitor must be connected between IN and PGND.

- **OUT:** Delivers power from the switching converter. The output bulk capacitor connects between OUT to PGND.
- **PGND:** Ground return for the switching converter power train.
- **AGND:** Ground return for everything except the power train. The voltage feedback divider returns to AGND. PGND and AGND must connect together on the circuit board.
- **LDO_5V:** Provides gate drive for M2 and M4 and current for the bootstrap circuits feeding BOOT1 and BOOT2. A bypass capacitor must connect from LDO_5V to PGND. See *Internal LDO Regulators* for more information on LDO_5V.
- **LDO_3V3:** Analog circuitry power supply. A bypass capacitor must connect from LDO_3V3 to AGND. See *Internal LDO Regulators* for more information on LDO_3V3.
- **BOOT1:** Provides gate drive for M1. A bootstrap capacitor must connect from BOOT1 to SW1.
- **BOOT2:** Provides gate drive for M3. A bootstrap capacitor must connect from BOOT2 to SW2.
- **SW1:** Connects M1 and M2 to external inductor.
- **SW2:** Connects M3 and M4 to external inductor.
- **CSP:** Positive terminal of average current sense amplifier. Connects to positive terminal of output bulk capacitor.
- **CSN/BUS:** Negative terminal of average current sense amplifier. A 10-mΩ current sense resistor is externally connected from CSP to CSN/BUS.

Depending upon the input voltage V_{IN} and the output voltage V_{OUT}, the converter can operate in one of four different states, each of which is described in following sections.

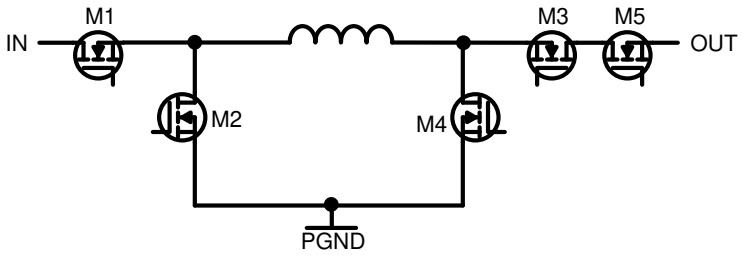


Figure 9-7. Buck-Boost Internal Power FETs

Buck State

When the input voltage V_{IN} significantly exceeds the output voltage V_{OUT}, the converter enters the buck region of operation in which it performs an endless series of buck switching cycles Buck State. M3 and M5 are constantly on and M4 is constantly off. When the clock signals that a switching cycle has begun, the controller turns on M2 and turns off M1. This switch configuration corresponds to the off-time interval of a traditional buck converter. The voltage difference $V_{SW1} – V_{SW2}$ across the inductor equals $–V_{OUT}$. The inductor current IL ramps down until it reaches a threshold I_{VALLEY} set by the error amplifiers. The controller then turns off M2 and turns on M1. This switch configuration corresponds to the on-time interval of a traditional buck converter. The voltage difference $V_{SW1} – V_{SW2}$ now equals $V_{IN} – V_{OUT}$. The inductor current now ramps up until the converter clock signals that the end of the switching cycle has been reached.

The on-time t_{on} equals the time interval during which M1 conducts. The off-time t_{off} equals the time interval during which M2 conducts. Because the converter operates in FCCM, the period τ equals the sum of t_{on} and t_{off}. During the buck state, the controller regulates power flow by adjusting the buck duty cycle D, which equals the ratio $t_{on}/τ$.

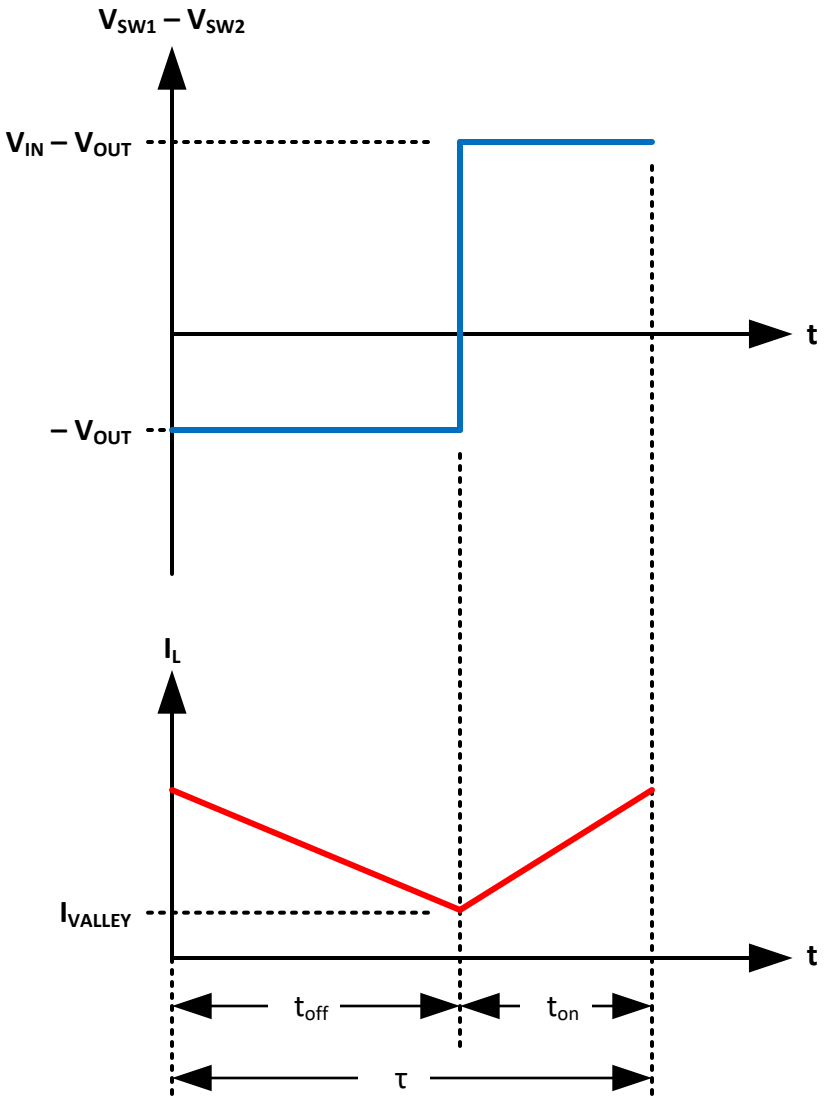


Figure 9-8. Buck State

Buck Transition State

When the input voltage V_{IN} is only slightly larger than the output voltage V_{OUT}, the converter enters the buck transition region of operation in which it alternately performs buck and boost switching cycles Buck Transition. M5 is always on. When the clock signals that a buck switching cycle has begun, the controller turns on M2 and M3, and it turns off M1 and M4. This switch configuration corresponds to the off-time of a traditional buck converter. The inductor current I_L ramps down until it reaches a threshold I_{VALLEY} set by the error amplifiers. The controller then turns off M2 and turns on M1. This switch configuration corresponds to the on-time of a traditional buck converter. The inductor current now ramps up slowly until the clock signals the end of the buck switching cycle. The next switching cycle is a boost switching cycle. When this cycle begins, the controller turns M3 off and turns M4 on. M2 remains off, and both M1 and M5 remain on. This switch configuration corresponds to the on-time of a traditional boost converter. The inductor current I_L now ramps up rapidly until the fixed on-time expires. The controller then turns off M4 and turns on M3. The inductor current now ramps down until the clock signals the end of the boost switching cycle. The next switching cycle will be another buck cycle.

During the buck transition state, the controller regulates power flow by adjusting the buck duty cycle. The boost duty cycle remains fixed. If the converter had remained in the buck state rather than move to the buck transition

state, the buck on-time would have become so short that it would have become impossible to regulate power flow without pulse skipping.

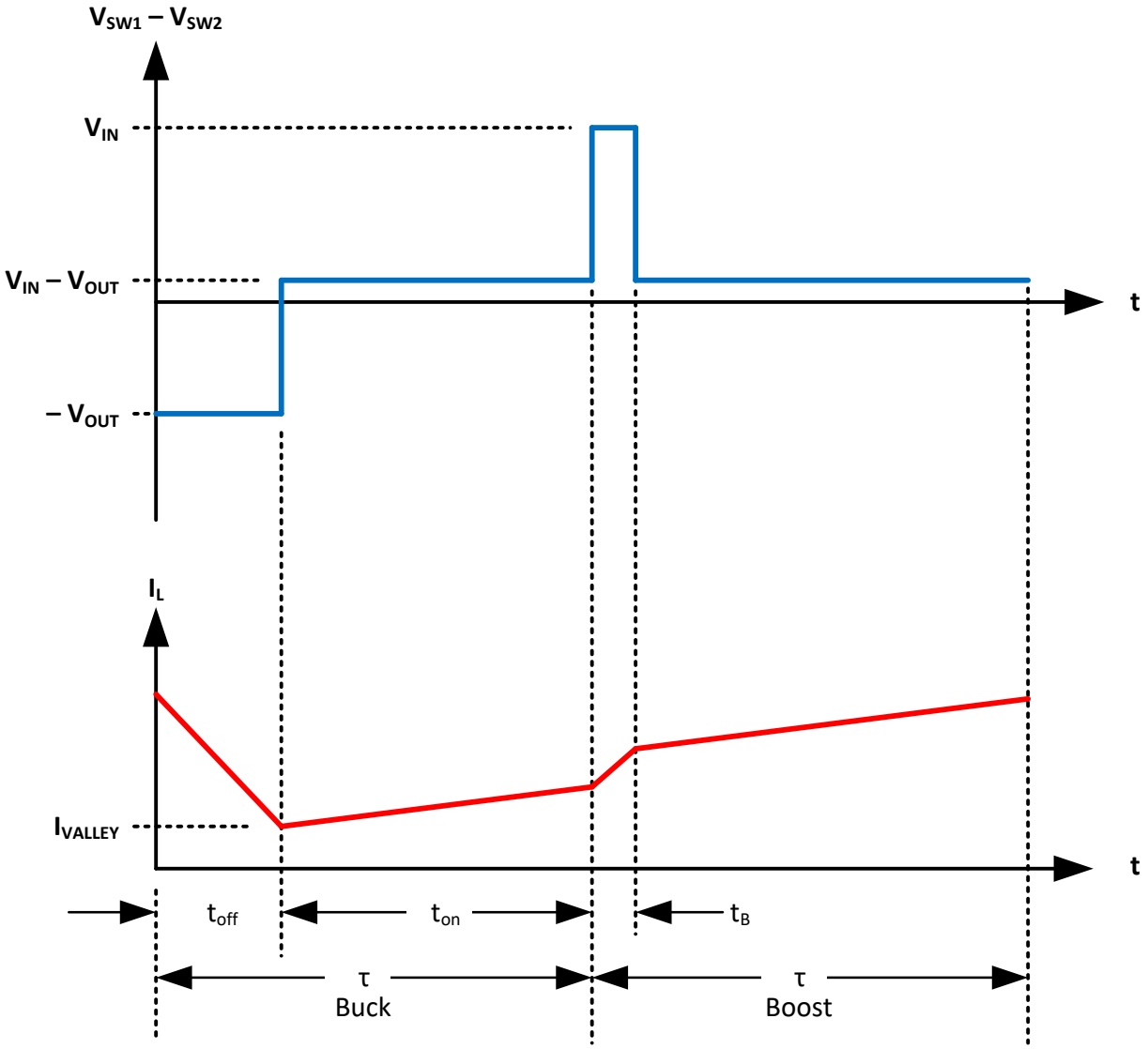


Figure 9-9. Buck Transition

Boost Transition State

When the input voltage V_{IN} is only slightly smaller than the output voltage V_{OUT}, the converter enters the boost transition region of operation in which it alternately performs boost and buck switching cycles Boost Transition. M5 is always on. When the clock signals that a boost switching cycle has begun, the controller turns on M1 and M4, and it turns off M2 and M3. This switch configuration corresponds to the on-time of a traditional boost converter. The inductor current I_L ramps up until it reaches a threshold I_{PEAK} set by the error amplifiers. The controller then turns off M4 and turns on M3. This switch configuration corresponds to the off-time of a traditional boost converter. The inductor current now ramps down slowly until the clock signals the end of the boost switching cycle. The next switching cycle is a buck switching cycle. When this cycle begins, the controller turns M1 off and turns M2 on. M4 remains off, and both M3 and M5 remain on. This switch configuration corresponds to the off-time of a traditional buck converter. The inductor current I_L now ramps down rapidly until the fixed off-time expires. The controller then turns off M2 and turns on M1. The inductor current now ramps up until the clock signals the end of the buck switching cycle. The next switching cycle will be another boost cycle.

During the boost transition state, the controller regulates power flow by adjusting the boost duty cycle. The buck duty cycle remains fixed. If the converter had remained in the boost state rather than move to the boost transition state, the boost on-time would have become so short that it would have become impossible to regulate power flow without pulse skipping.

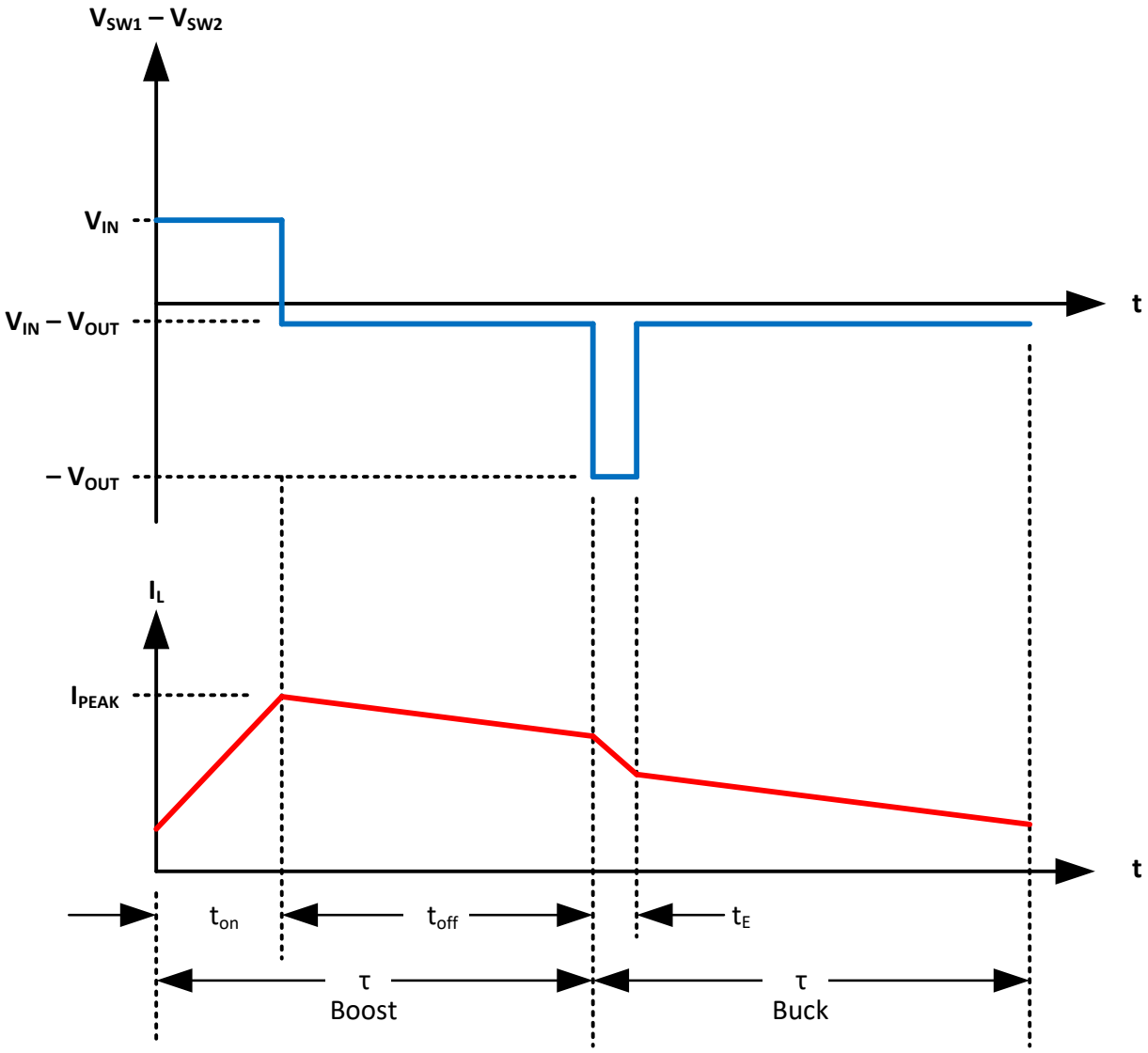


Figure 9-10. Boost Transition

Boost State

When the input voltage V_{IN} is significantly less than the output voltage V_{OUT}, the converter enters the boost region of operation in which it performs an endless series of boost switching cycles Boost State. M1 and M5 are constantly on and M2 is constantly off. When the clock signals that a switching cycle has begun, the controller turns on M4 and turns off M3. This switch configuration corresponds to the on-time interval of a traditional boost converter. The voltage difference $V_{SW1} – V_{SW2}$ across the inductor equals V_{IN}. The inductor current I_L ramps up until it reaches a threshold I_{PEAK} set by the error amplifiers. The controller then turns off M4 and turns on M3. This switch configuration corresponds to the off-time interval of a traditional boost converter. The voltage difference $V_{SW1} – V_{SW2}$ now equals $V_{IN} – V_{OUT}$, which is negative. The inductor current now ramps down until the converter clock signals that the end of the switching cycle has been reached.

The on-time t_{on} equals the time interval during which M4 conducts. The off-time t_{off} equals the time interval during which M3 conducts. Because the converter operates in FCCM, the period τ equals the sum of t_{on} and t_{off}.

During the boost state, the controller regulates power flow by adjusting the boost duty cycle D, which equals the ratio t_{on}/τ.

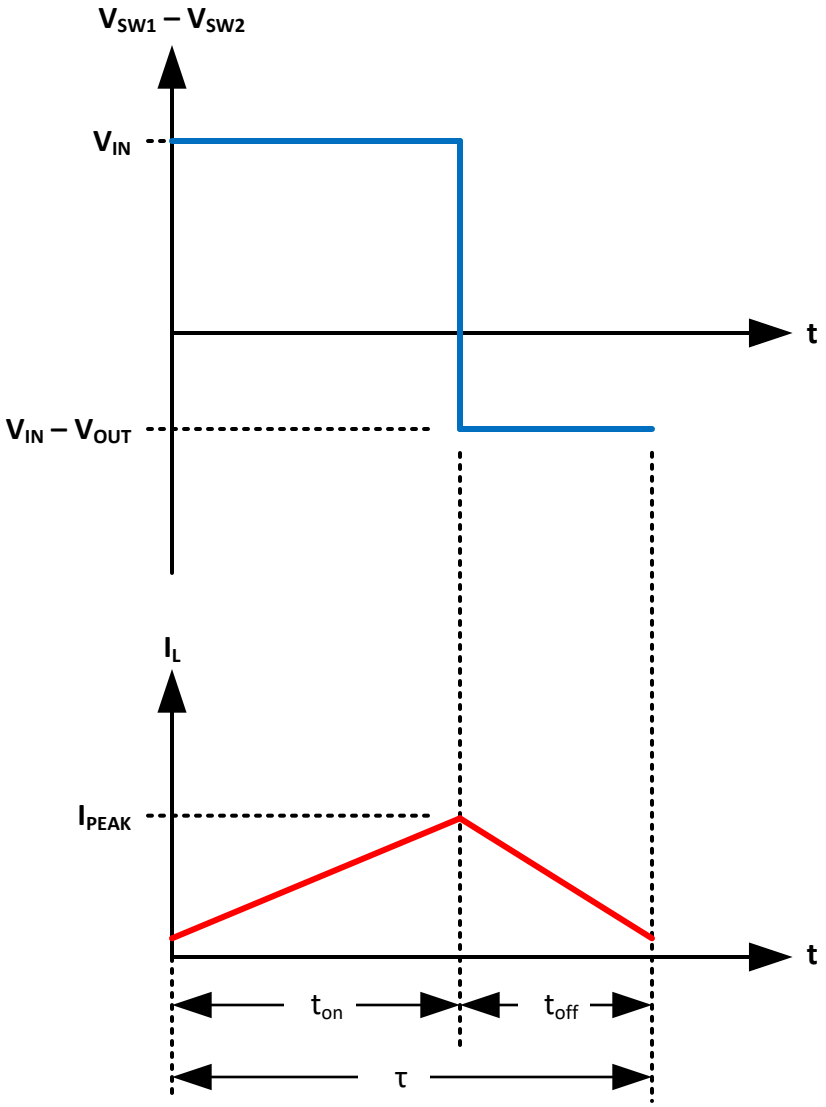


Figure 9-11. Boost State

Boundaries of the Regions of Operation

Regions of Operation graphically depicts the four regions of operation and the boundaries between them. When $V_{BUS} > kV_{IN}$, the converter remains in the boost region of operation. The value k is 1.2. When $V_{IN} < V_{BUS} < kV_{IN}$, the converter enters the boost transition region of operation. When $V_{IN}/k < V_{BUS} < V_{IN}$, the converter enters the buck transition region of operation. When $V_{BUS} < V_{IN}/k$, the converter enters the buck region of operation. The converter will cease operating if V_{IN} exceeds the OVP threshold, which lies between 18 and 20 V. Similarly, the converter will also cease operating if V_{IN} drops below either the internal UVLO threshold, which lies between 5 and 5.5 V, or the user programmed EN/UVLO threshold (see *VIN UVLO and ENABLE/UVLO*, whichever is greater).

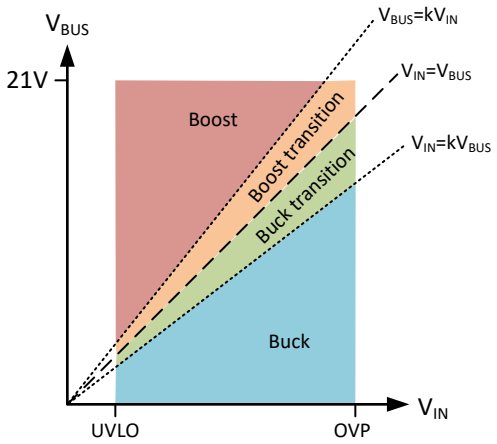


Figure 9-12. Regions of Operation

9.3.3.2 Switching Frequency, Frequency Dither, Phase-Shift and Synchronization

The PWM oscillator frequency (f_{sw}) is programmed by firmware using the application configuration GUI. The switching converter is intended for operation below the AM radio band (520 kHz - 1730 kHz). Three nominal f_{sw} settings below are available: 300 kHz, 400 kHz and 450 kHz.

Frequency dithering can be enabled by firmware via the application GUI. When enabled, the nominal oscillator frequency is dithered by $\pm FS_{SS}$ (approximately ±10%) using triangular waveform modulation (see Dithering using triangular waveform modulation). The dither period τ_M is the reciprocal of the dither modulation frequency FS_{SS_MOD}. Two firmware selectable dither modulation frequencies FS_{SS_M} are available: 10 and 25 kHz. Dithering spreads the spectral peaks generated by switching, thereby reducing the peak harmonic levels and easing EMI filter design.

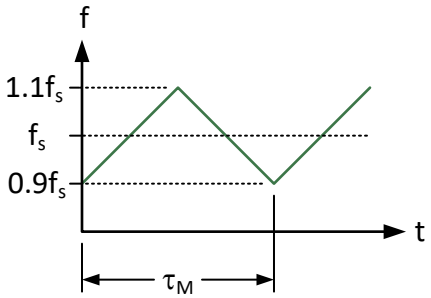


Figure 9-13. Dithering Using Triangular Waveform Modulation

Multiple converters can be synchronized using the SYNC pin. This pin can be firmware-configured as either an output SYNC(o) or an input SYNC(i).

- **SYNC(o):** The switching clock is placed on the SYNC(o) pin. This waveform will have a duty cycle of approximately 50%. If frequency dithering is configured by firmware, this signal will also exhibit dithering. Four phase settings are available by firmware configuration to shift the SYNC(o) output relative to the internal switching clock by 0°, 90°, 120°, or 180°. SYNC(o) is used to slave other DC/DC converter clocks to the switching converter clock inside the TPS25772-Q1. When two dc/dc converters operate out of phase, peak input current from the battery is reduced and total input bulk capacitance requirements decrease.

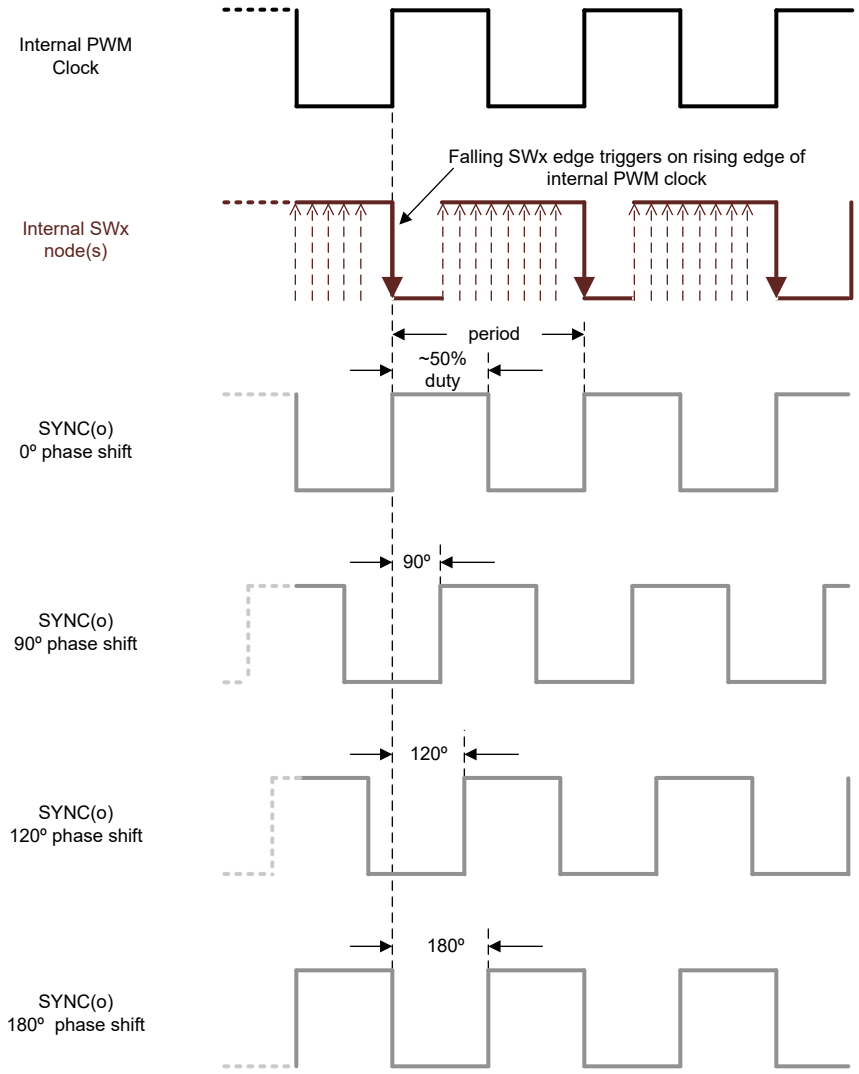


Figure 9-14. SYNC(o) Phase Shift

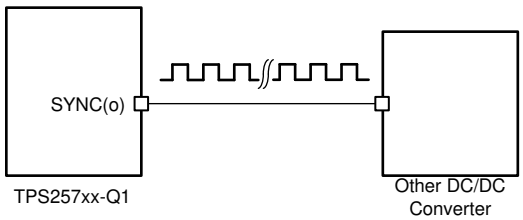


Figure 9-15. Using SYNC(o) to slave DC/DC Converter

- **SYNC(i):** The internal clock is synchronized to the pulse train on the SYNC(i) pin. This feature is used to slave the TPS25772-Q1 to an external clock. The period of this clock must meet synchronization requirements in SYNC(i) frequency ranges or the TPS25772-Q1 will instead use its internal switching clock. If an external clock deviates outside of the acceptable frequency range and then returns to within the acceptable frequency range, the TPS25772-Q1 will resume operation from the external clock after counting 8 consecutive clocks meeting the criteria of Table 9-6. When SYNC(i) is configured, frequency dithering is disabled when operating from the internal clock following a failure of the external clock.

Table 9-6. SYNC(i) Frequency Ranges

f_{SW} Firmware Setting	Allowed SYNC(i) Frequency Range	
	MIN	MAX

Table 9-6. SYNC(i) Frequency Ranges (continued)

f_{SW} Firmware Setting	Allowed SYNC(i) Frequency Range	
300 kHz	250 kHz	353 kHz
400 kHz	334 kHz	470 kHz
450 kHz	376 kHz	530 kHz

9.3.3.3 VIN Supply and VIN Over-Voltage Protection

V_{IN} Supply

The voltage V_{IN} at the input supply pin IN, measured with respect to AGND, must meet the following requirements:

- **Overvoltage:** The voltage V_{IN} must never exceed an absolute maximum of 40 V, and should not exceed 36 V under anticipated operating conditions. Automotive applications will typically require an external transient suppressor to meet this requirement.
- **Load dump:** When the converter is running and V_{IN} exceeds 18 V, the positive slew rate dV_{IN}/dt must not exceed 200 V/ms.
- **Double battery:** When the converter is not running, the positive slew rate dV_{IN}/dt must not exceed 10 V/µs. The input EMI filter can help mitigate input voltage slew rates.
- **Reverse battery:** The voltage V_{IN} must never go below –0.3 V. Automotive applications will typically require external reverse voltage blocking circuitry.

The buck-boost switching converter is capable of delivering its full rated output power of 65 W over an input supply range 6.8 V < V_{IN} < 18 V . The input voltage can dip down to the UVLO threshold providing that the output power level is appropriately derated.

V_{IN} Overvoltage Protection Circuitry

The TPS25772-Q1 contains circuitry that protects the power train against load dump and double battery conditions. When VIN exceeds about 19 V, a comparator determines that an input overvoltage condition has occurred. This comparator sends a signal that shuts the switching converter down. Transistors M1, M2, and M3 in Buck-Boost Internal Power FETs are turned off, and transistor M4 is turned on. However, current is still flowing through the inductor. Two cases may exist: the current may flow forward (from SW1 to SW2) or in reverse (from SW2 to SW1). Reverse current flow will forward-bias the body diode of M1. The voltage across the inductor will then equal the sum of the forward voltage of this diode plus the input voltage, which is sufficient to cause the inductor voltage to rapidly ramp down to zero. Forward current flow will forward-bias the body diode of M2. After the inductor current is released, a small linear regulator biases SW1 to about 15 V. When the overvoltage condition is removed, the switching regulator may resume operation.

9.3.3.4 Feedback Paths and Error Amplifiers

The TPS25772-Q1 includes not only a programmable voltage feedback path, but also a programmable average current feedback path that can be used to limit the average current provided by the switching converter to the USB cable. The voltage feedback path also includes provision for cable droop compensation. Figure 9-16 shows a simplified block diagram of the relevant portions of the integrated circuit.

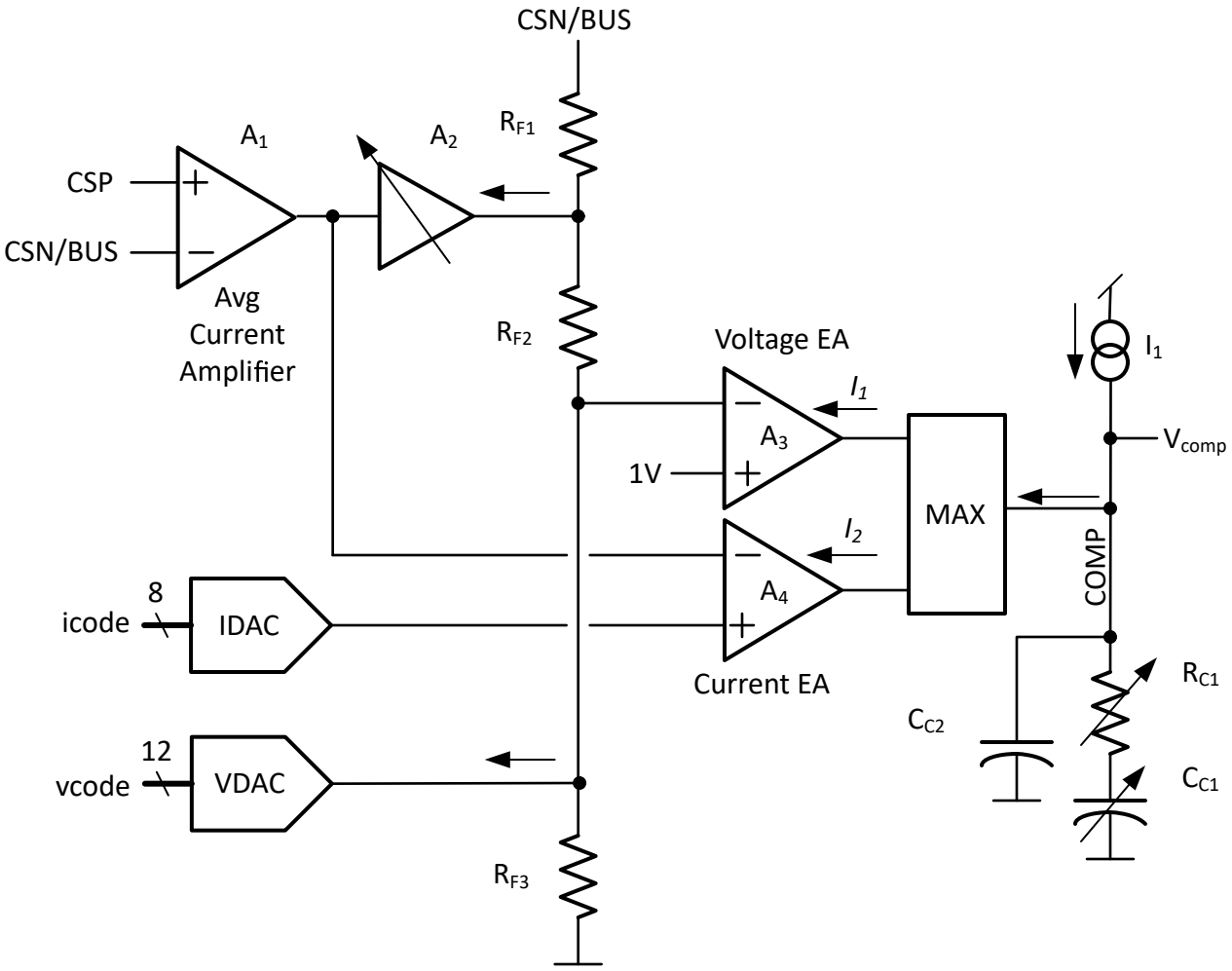


Figure 9-16. Simplified block diagram of feedback paths and error amplifiers.

9.3.3.5 Transconductors and Compensation

The TPS25772-Q1 is internally compensated. The overall slope compensation and loop compensation is internally fixed based on inductor and capacitance values shown in Table 10-1.

9.3.3.6 Output Voltage DAC, Soft-Start and Cable Droop Compensation

The buck-boost output voltage is regulated at the CSN/VBUS pin. A 12-bit digital-to-analog converter, VDAC, provides ±20-mV step voltage adjustments of $V_{CSP/BUS}$ as commanded by device firmware.

After a successful cable detect event, firmware sets the VDAC to output 5 V as measured on the $V_{CSN/BUS}$ output. An internal clock steps up the VDAC codes from an initial 0 V to final 5-V setting producing a monotonic ramp of $V_{CSN/BUS}$ to 5 V at t_{SS}.

In some applications, the USB-PD controller may be located 1 m, or more, from the USB receptacle. When configured and enabled by firmware, cable droop compensation will increase the $V_{CSP/BUS}$ linearly with increasing load current independent of the VDAC setting. Four selectable V_{OUT_CDC} ranges are available. 500 mV is the maximum supported cable droop voltage and it is disabled by default during USB-PD PPS contracts.

9.3.3.7 V_{BUS} Overvoltage Protection

A fixed threshold overvoltage comparator monitors the CSN/BUS pin for overvoltage conditions. When the V_{CSN/BUS_OVP_R} threshold is exceeded, output OV protection circuitry turns off the internal MOSFETs. Switching resumes when $V_{CSN/BUS}$ decreases below V_{CSN/BUS_OVP_F}.

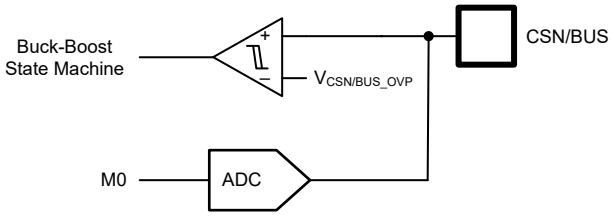


Figure 9-17. V_{BUS} OVP and UVP

9.3.3.8 V_{BUS} Undervoltage Protection

PA_VBUS and PB_VBUS undervoltage conditions are monitored by the internal ADC. In accordance with USB Power Delivery specifications, the TPS25772-Q1 firmware configures the threshold based on USB PD contract with the attached sink device.

9.3.3.9 Current Sense Resistor (R_{SNS}) and Current Limit Operation

The CSP and CSN/BUS pins are the positive and negative inputs to the average current sense amplifier (CSA). The TPS25772-Q1 devices sense port A load current across sense resistor, R_{SNS}, located between the CSP and CSN/BUS pins. A 10-mΩ, 1%, power resistor provides a 0 - 50-mV sense voltage over the range $0 \le I_{OUT} \le 5$ A.

A seven bit digital-to-analog converter, IDAC, provides ±50-mA step current limit adjustments and is automatically programmed by device firmware.

9.3.3.10 Buck-Boost Peak Current Limits

The buck and boost peak current limits are adjustable by firmware using the application configuration GUI. Refer to the BUCK-BOOST PEAK CURRENT LIMITS in Section 7.6 of the *Electrical Characteristics* tables for selectable values.

In most applications it is desirable to limit input current to the automotive USB module to protect module components, connectors and wiring from over-current conditions. The worst case input current condition occurs when V_{IN} is minimum and $V_{CSN/BUS}$ is maximum (21 V) while supplying maximum 3.25 A output current. When $V_{IN} < V_{BUS}$, the internal DC/DC converter is operating in boost mode. Refer to the Table 10-6 tables in the *Inductor Currents* section to estimate the peak current versus recommended inductor value for the application.

The buck peak current limit setting selection should be just lower than the boost peak current limit. Set as close to the boost peak current limit as selections allow to prevent the possibility of limit cycling between the two peak current limits under extreme transients. $I_{PEAK(BUCK)} \cong I_{PEAK(BOOST)}$.

When selecting an inductor, it is important select one with an appropriate saturation current rating, $I_{L(SAT)}$. The inductor $I_{L(SAT)}$ rating should larger than the maximum (MAX) $I_{PEAK(BOOST)}$ limit from the *Electrical Characteristics* tables to avoid excessive current flow in the TPS25772-Q1 or the inductor.

9.3.4 USB-PD Physical Layer

Figure 9-18 shows the USB PD physical layer block surrounded by a simplified version of the analog plug and orientation detection block. This block applies to Port A and Port B.

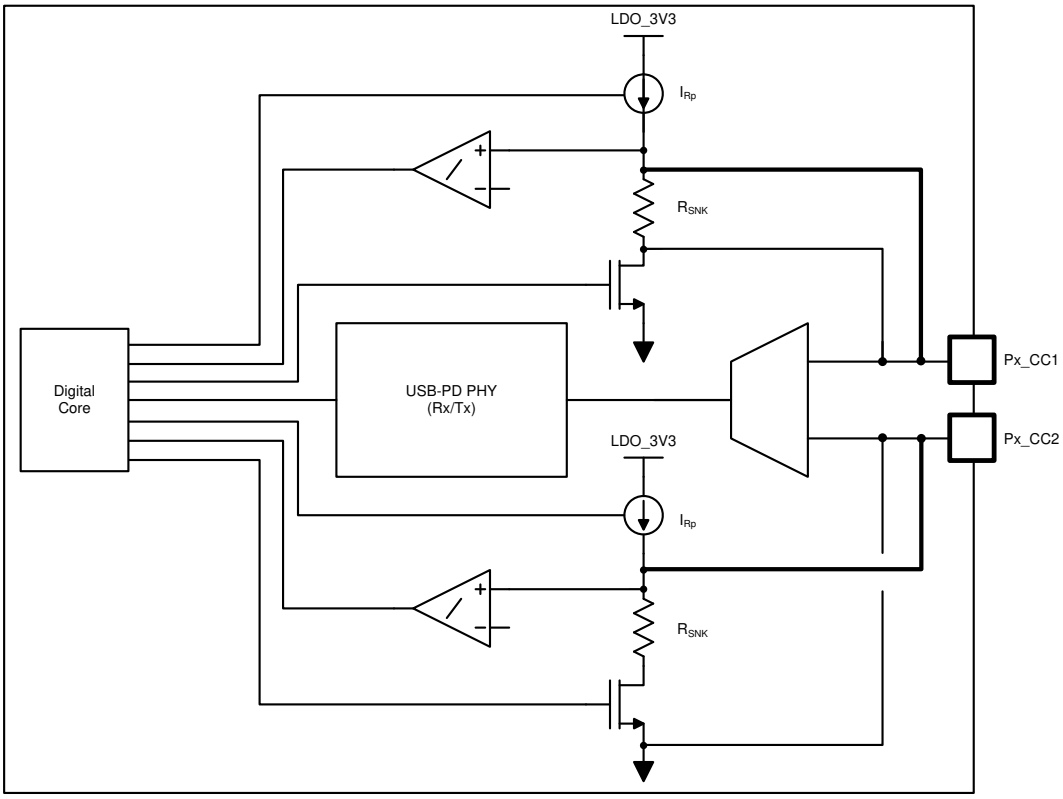


Figure 9-18. USB-PD Physical Layer and Simplified Plug and Orientation Detection Circuitry

USB-PD messages are transmitted in a USB Type-C system using a BMC (Biphase Mark Coding) signaling. The BMC signal is output on the same pin (Px_CC1 or Px_CC2) that is DC biased due to the Rp (or Rd) cable attach mechanism discussed in the *USB-PD BMC Transmitter* section.

9.3.4.1 USB-PD Encoding and Signaling

Figure 9-19 illustrates the high-level block diagram of the baseband USB-PD transmitter. Figure 9-20 illustrates the high-level block diagram of the baseband USB-PD receiver.

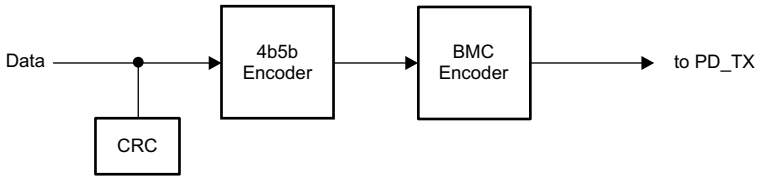


Figure 9-19. USB-PD Baseband Transmitter Block Diagram

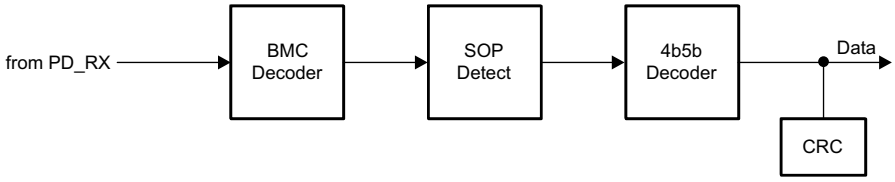


Figure 9-20. USB-PD Baseband Receiver Block Diagram

9.3.4.2 USB-PD Bi-Phase Marked Coding

The USB-PD physical layer implemented in the TPS25772-Q1 is compliant to the *USB-PD Specifications*. The encoding scheme used for the baseband PD signal is a version of Manchester coding called Biphase Mark Coding (BMC). In this code, there is a transition at the start of every bit time and there is a second transition in the middle of the bit cell when a 1 is transmitted. This coding scheme is nearly DC balanced with limited disparity (limited to 1/2 bit over an arbitrary packet, so a very low DC level). Figure 9-21 illustrates Biphase Mark Coding.

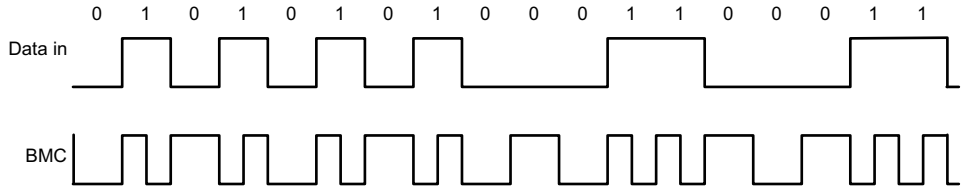


Figure 9-21. Biphase Mark Coding Example

The USB PD baseband signal is driven onto the Px_CC1 or Px_CC2 pin with a tri-state driver. The tri-state driver controls slew rate to limit coupling to D+/D– and to other signal lines in the Type-C fully featured cables. When sending the USB-PD preamble, the transmitter starts by transmitting a low level. The receiver at the other end tolerates the loss of the first edge. The transmitter terminates the final bit by an edge to ensure the receiver clocks the final bit of EOP.

9.3.4.3 USB-PD Transmit (TX) and Receive (Rx) Masks

The USB-PD driver meets the defined USB-PD BMC TX masks. Since a BMC coded “1” contains a signal edge at the beginning and middle of the UI, and the BMC coded “0” contains only an edge at the beginning, the masks are different for each. The USB-PD receiver meets the defined USB-PD BMC Rx masks. The boundaries of the Rx outer mask are specified to accommodate a change in signal amplitude due to the ground offset through the cable. The Rx masks are therefore larger than the boundaries of the TX outer mask. Similarly, the boundaries of the Rx inner mask are smaller than the boundaries of the TX inner mask. Triangular time masks are superimposed on the TX outer masks and defined at the signal transitions to require a minimum edge rate that has minimal impact on adjacent higher speed lanes. The TX inner mask enforces the maximum limits on the rise and fall times. Refer to the *USB-PD Specifications* for more details.

9.3.4.4 USB-PD BMC Transmitter

The TPS25772-Q1 transmits and receives USB-PD data over one of the Px_CCy pins for a given CC pin pair (one pair per USB Type-C port). The Px_CCy pins are also used to determine the cable orientation (see the *Cable Plug and Orientation Detection* section) and maintain cable/device attach detection. Thus, a DC bias exists on the Px_CCy pins. The transmitter driver overdrives the Px_CCy DC bias while transmitting, but returns to a Hi-Z state allowing the DC voltage to return to the Px_CCy pin when not transmitting. While either Px_CC1 or Px_CC2 may be used for transmitting and receiving, during a given connection only the one that mates with the CC pin of the plug is used; so there is no dynamic switching between Px_CC1 and Px_CC2. Figure 9-22 shows the USB-PD BMC TX and RX driver block diagram.

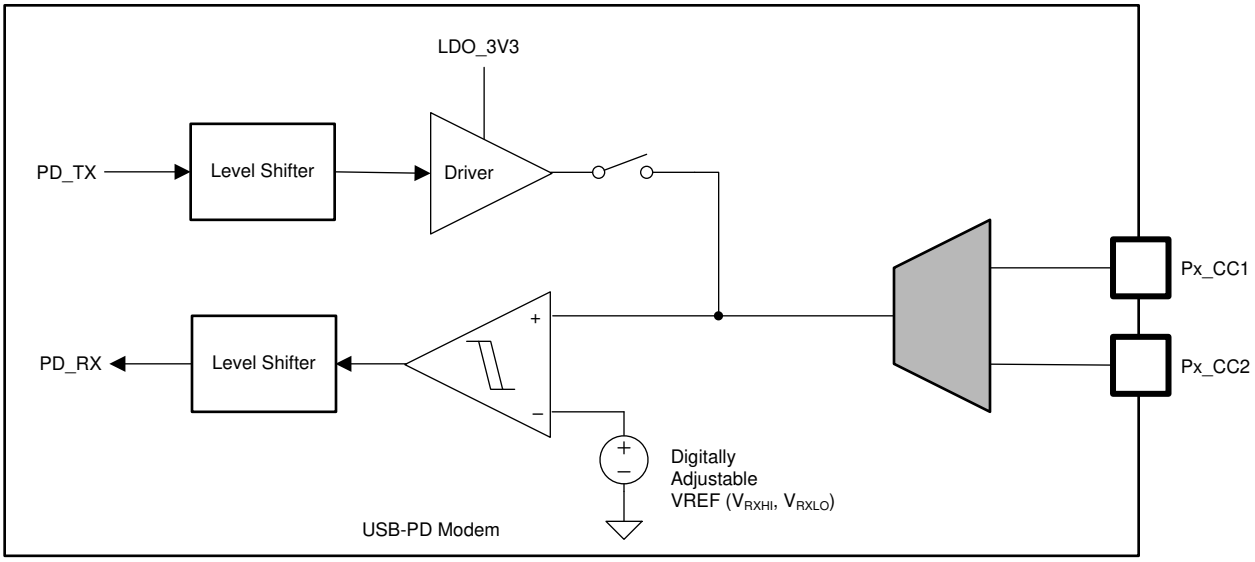


Figure 9-22. USB-PD BMC TX/Rx Block Diagram

Figure 9-23 shows the transmission of the BMC data on top of the DC bias. Note, The DC bias can be anywhere between the minimum threshold for detecting a UFP attach and the maximum threshold for detecting a Sink attach to a Source. This means that the DC bias can be above or below the V_{OH} of the transmitter driver.

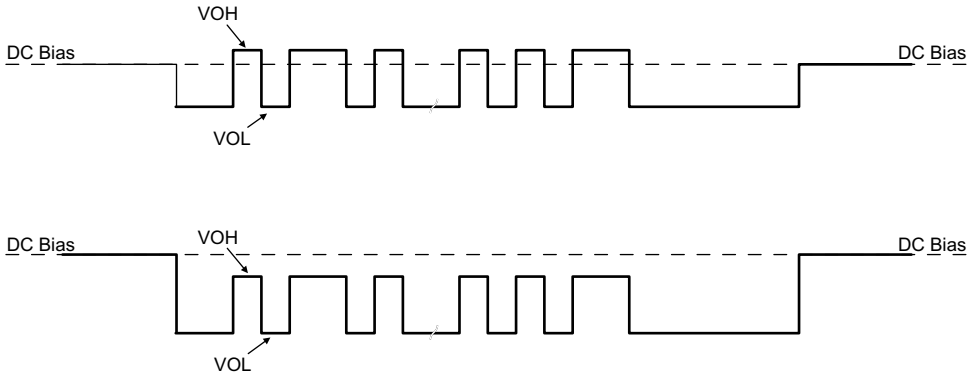


Figure 9-23. TX Driver Transmission with DC Bias

The transmitter drives a digital signal onto the Px_CCy lines. The signal peak, V_{TXHI}, is set to meet the TX masks defined in the *USB-PD Specifications*. Note that the TX mask is measured at the far-end of the cable.

When driving the line, the transmitter driver has an output impedance of Z_{DRIVER}. Z_{DRIVER} is determined by the driver resistance and the shunt capacitance of the source and is frequency dependent. Z_{DRIVER} impacts the noise ingression in the cable.

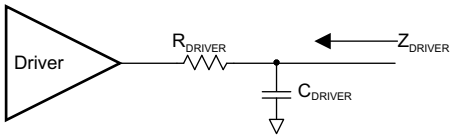


Figure 9-24. ZDRIVER Circuit

9.3.4.5 USB-PD BMC Receiver

The receiver block of the TPS25772-Q1 receives a signal that falls within the allowed Rx masks defined in the USB PD specification. The receive thresholds and hysteresis come from this mask.

Figure 9-25 shows an example of a multi-drop USB-PD connection (only the CC wire). This connection has the typical Sink (device) to Source (host) connection, but also includes cable USB-PD Tx/Rx blocks. Only one system can be transmitting at a time. All other systems are Hi-Z (Z_{BMCRX}). The *USB-PD Specification* also specifies the capacitance that can exist on the wire as well as a typical DC bias setting circuit for attach detection.

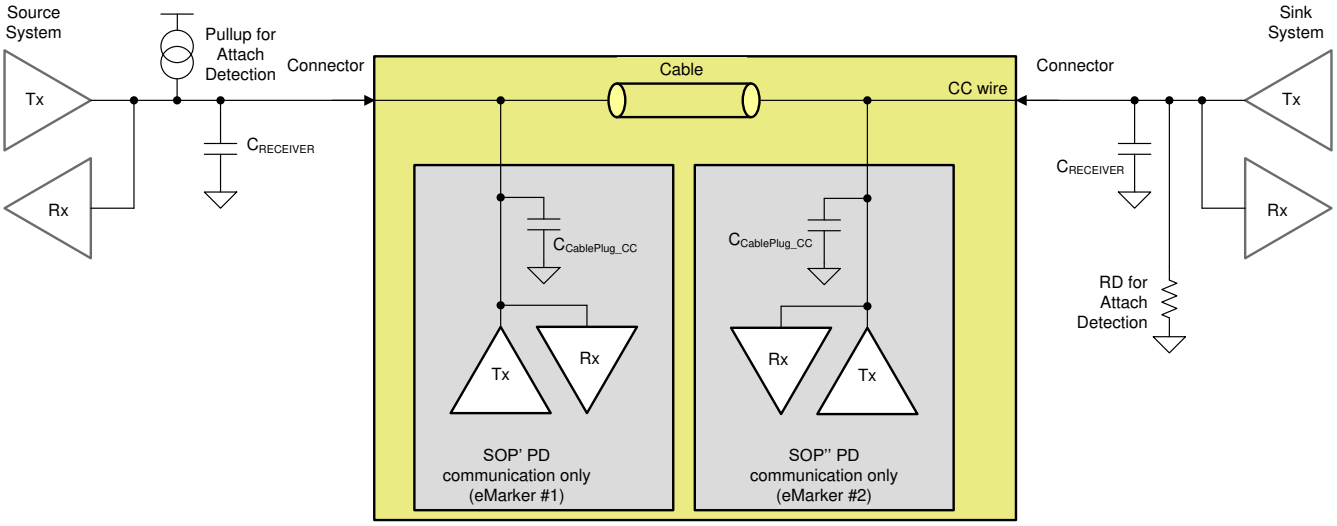


Figure 9-25. Example USB-PD Multi-Drop Configuration

9.3.4.6 Squelch Receiver

The TPS25772-Q1 has a squelch receiver to monitor for the bus idle condition as defined by the USB PD specification. The squelch receiver output reflects the state of the CC pin regardless of the source of the transmission.

9.3.5 VCONN

Internal VCONN sourcing power paths are firmware configurable. Using only the internal LDO_5V supply, both Port A and Port B are able to draw 20 mA continuously. If an external 5-V regulator is connected to the LDO_5V pin and the application GUI settings are enabled, both Port A and Port B are able to draw 200 mA continuously. When disabled, blocking FETs in the both Port A and Port B VCONN paths protect the LDO_5V rail from high-voltage and reverse current.

When VCONN power is enabled and provided, the internal VCONN power switches have a current limit of I_{LIMVC}. If the VCONN load current exceeds I_{LIMVC}, the current clamping circuit activates within $t_{iOS\_PP\_CABLE}$ and the switch behaves as a constant current source. Reverse current blocking is disabled when current is flowing to Px_CC1 or Px_CC2.

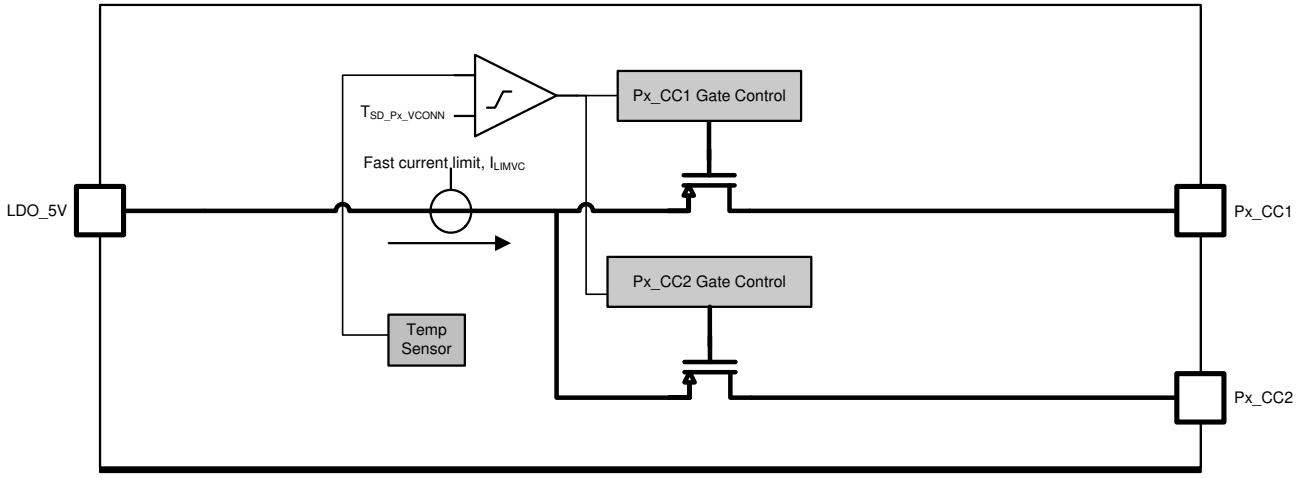


Figure 9-26. VCONN Power Switches

When operating in current limit, the VCONN FET temperature rises. Local temperature sensors disable the Px_VCONN path in current limit when T_{sensor} > $T_{SD\_Px\_VCONN}$ within $t_{PP\_CABLE\_off}$. The application firmware enters USB Type-C Error Recovery on the affected port.

LDO_5V must remain above its under voltage lock out threshold ($V_{LDO\_5V(UVLO\_F)}$) for Px_VCONN operation. If the $V_{LDO\_5V(UVLO\_F)}$ threshold is reached, Px_VCONN paths are automatically disabled within $t_{PP\_CABLE\_off}$.

9.3.6 Cable Plug and Orientation Detection

Figure 9-27 shows the plug and orientation detection block at each Px_CCy pin (PA_CC1, PA_CC2, PB_CC1, PB_CC2). Each CC pin has identical detection circuitry.

When the port is operating as a Type-C source, the V_{REFx} nodes are multiplexed to the V_{SRC} thresholds corresponding to the advertised Type-C source capability current, $I_{Rp\_}$.

When the port is operating as a Type-C sink, the V_{REFx} nodes are multiplexed to the V_{SNK} thresholds corresponding to sink detection.

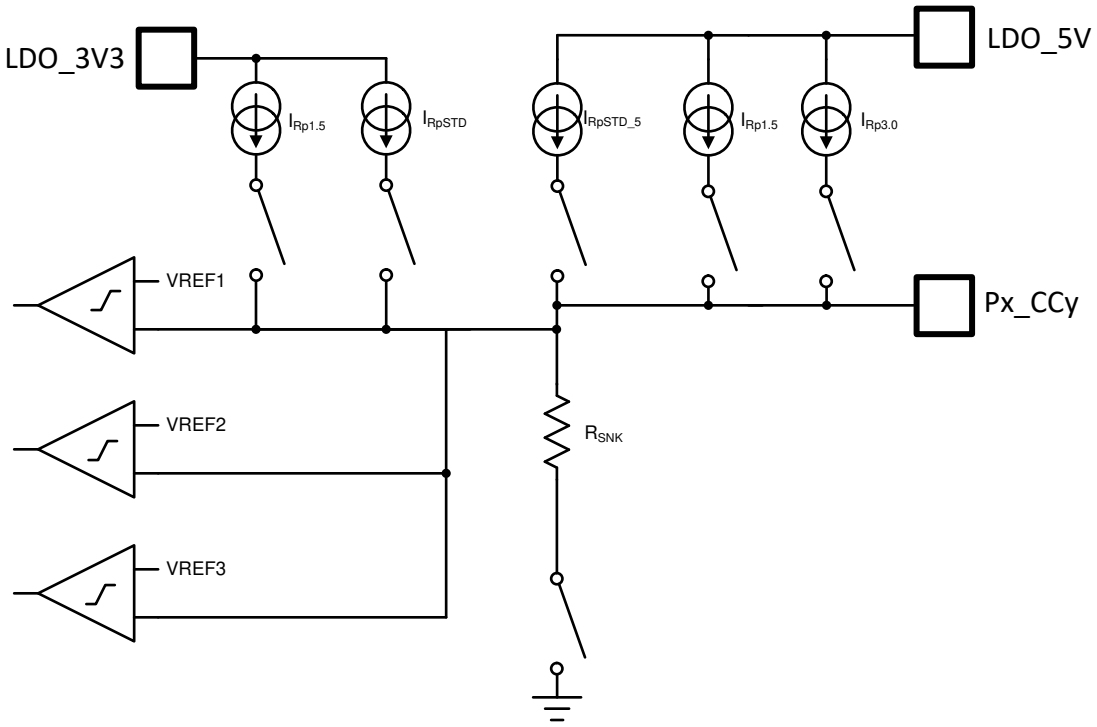


Figure 9-27. Plug and Orientation Detection Block

9.3.6.1 Configured as a Source

When either of the PA or PB ports is configured as a Source, the device detects when a cable or a Sink is attached using the Px_CC1 and Px_CC2 pins. When in a disconnected state, the device monitors the voltages on these pins to determine what, if anything, is connected. See *USB Type-C Specification* for more information.

Table 9-7 shows the Cable Detect States for a Source.

Table 9-7. Cable Detect States for a Source

Px_CC1	Px_CC2	CONNECTION STATE	RESULTING ACTION
Open	Open	Nothing attached	Continue monitoring both Px_CCy pins for attach. Power is not applied to Px_VBUS or VCONN.
Rd	Open	Sink attached	Monitor Px_CC1 for detach. Power is applied to Px_VBUS but not to VCONN (Px_CC2).
Open	Rd	Sink attached	Monitor Px_CC2 for detach. Power is applied to Px_VBUS but not to VCONN (Px_CC1).
Ra	Open	Powered Cable-No UFP attached	Monitor Px_CC2 for a Sink attach and Px_CC1 for cable detach. Power is not applied to Px_VBUS or VCONN (Px_CC1).
Open	Ra	Powered Cable-No UFP attached	Monitor Px_CC1 for a Sink attach and Px_CC2 for cable detach. Power is not applied to Px_VBUS or VCONN (Px_CC2).
Ra	Rd	Powered Cable-UFP Attached	Provide power on Px_VBUS and VCONN (Px_CC1) then monitor Px_CC2 for a Sink detach. Px_CC1 is not monitored for a detach.
Rd	Ra	Powered Cable-UFP attached	Provide power on Px_VBUS and VCONN (Px_CC2) then monitor Px_CC1 for a Sink detach. Px_CC2 is not monitored for a detach.

When a port is configured as a Source, a current $I_{Rp1.5A}$, is driven out of each Px_CCy pin and each pin is monitored for different states. When a Sink is attached to the pin a pull-down resistance of Rd to GND exists. The current $I_{Rp1.5A}$ is then forced across the resistance Rd generating a voltage at the Px_CCy pin. The device applies the configured $I_{Rp1.5A}$ until the buck-boost regulator is enabled and operating at 5 V, at which time application firmware may remain at $I_{Rp1.5A}$ or change to $I_{Rp3.0A}$.

When the Px_CCy pin is connected to an electronically marked cable VCONN input, the pull-down resistance is different (Ra). In this case the voltage on the Px_CCy pin will pull below V_{RDstd} and the system recognizes the electronically marked cable.

The $V_{Dstd1.5}$ or $V_{D3.0}$ threshold is monitored to detect a disconnection depending upon which Rp current source is active. When a connection has been recognized and the voltage on Px_CCy subsequently rises above the disconnect threshold for t_{CC}, the system registers a disconnection.

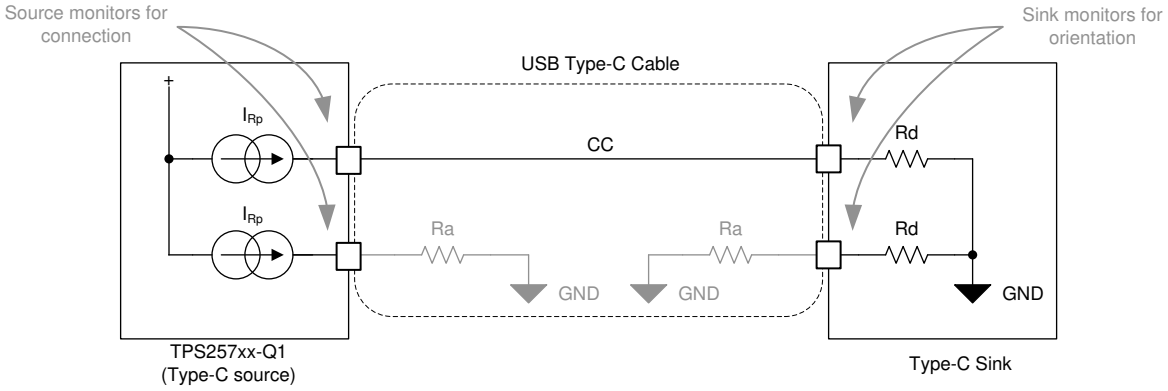


Figure 9-28. Type-C Cable

9.3.6.2 Configured as a Sink

When the TPS25772-Q1 port is configured as a Sink, such as in Firmware Update Mode with TVSP Index 8, the device presents a pull-down resistance R_{SNK} on each PA_CCy pin and waits for a Source to attach and pull-up the voltage on the pin. The Source pulls-up the PA_CCy pin by applying either a resistance or a current. The Sink detects an attachment by the presence of VBUS. The Sink determines the advertised current from the Source by the pull-up applied to the PA_CCy pin.

9.3.6.3 Overvoltage Protection (Px_CC1, Px_CC2)

Comparators on the Px_CCy pins detect when the voltage on CC1 or CC2 is too high, or there is reverse current into the LDO_5V output. During an overvoltage event, VCONN is disabled within tPP_CABLE_FSD and the associated USB PD transmitter is disabled.

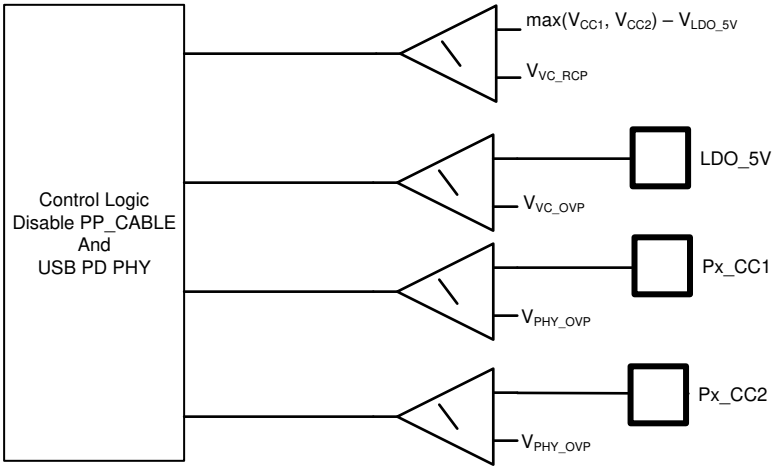


Figure 9-29. Over-voltage and Reverse Current Protection

9.3.7 ADC

The ADC is shown in Figure 9-30. The ADC is an 8-bit successive approximation ADC. The input to the ADC is an analog input mux that supports multiple inputs from various voltages and currents in the device. The output from the ADC is available to be read and used by application firmware.

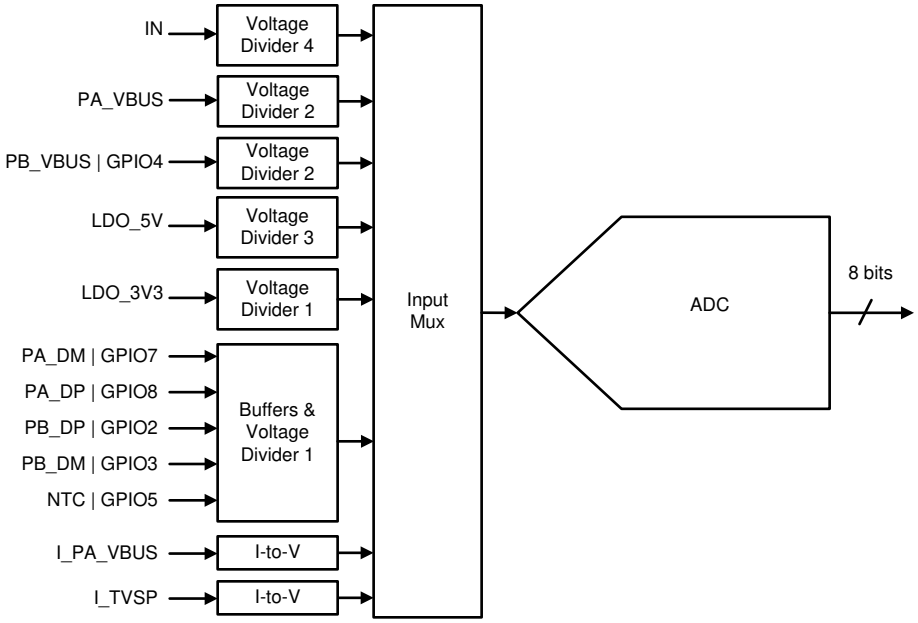


Figure 9-30. SAR ADC

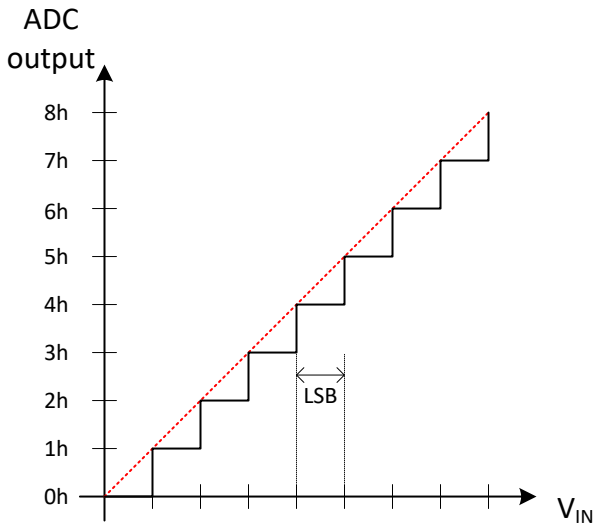


Figure 9-31. ADC Conversion

9.3.7.1 ADC Divider Ratios

The ADC voltage inputs are each divided down to the full-scale input of 1.2 V. The ADC current sensing elements are not divided.

Table 9-8 shows the divider ratios for each ADC input. The application firmware may select any group of channels to be auto-sequenced in the round robin automatic readout mode.

Table 9-8. ADC Inputs

CHANNEL	SIGNAL	TYPE	DIVIDER RATIO	BUFFERED
0	I_TVSP	Current	n/a	No
1	IN	Voltage	17	No
2	LDO_3V3	Voltage	3	No
3	PA_VBUS	Voltage	21	No

Table 9-8. ADC Inputs (continued)

CHANNEL	SIGNAL	TYPE	DIVIDER RATIO	BUFFERED
4	GPIO4 | PB_VBUS	Voltage	21	No
5	I_{PA_VBUS}	Current	n/a	No
6	GPIO2 | PB_DP	Voltage	3	Yes
7	GPIO3 | PB_DM	Voltage	3	Yes
8	GPIO5 | NTC	Voltage	3	Yes
9	GPIO7 | PA_DM	Voltage	3	Yes
10	GPIO8 | PA_DP	Voltage	3	Yes
11	LDO_5V	Voltage	5	No

9.3.8 BC 1.2, Legacy and Fast Charging Modes (Px_DP, Px_DM)

BC 1.2 downstream port charger emulation is application GUI configurable. The following charging modes can be enabled or disabled:

- DCP (Dedicated Charging Port) Shorted Mode
- Divider-3 Mode
- 1.2-V Mode
- HVDCP (High Voltage Dedicated Charging Port) Mode

The following table shows voltage sources, resistors and comparator hardware used in each mode. Symbol "X" represents that the corresponding module is implemented.

Application	2.7-V SRC	1.2-V SRC	R_{DCP_DAT}	R_{DM_DWN} (20 kΩ)	V_{DAT_REF}	V_{SEL_REF}
DCP			X			
Divider-3	X					
1.2 V		X	X			
HVDCP				X	X	X

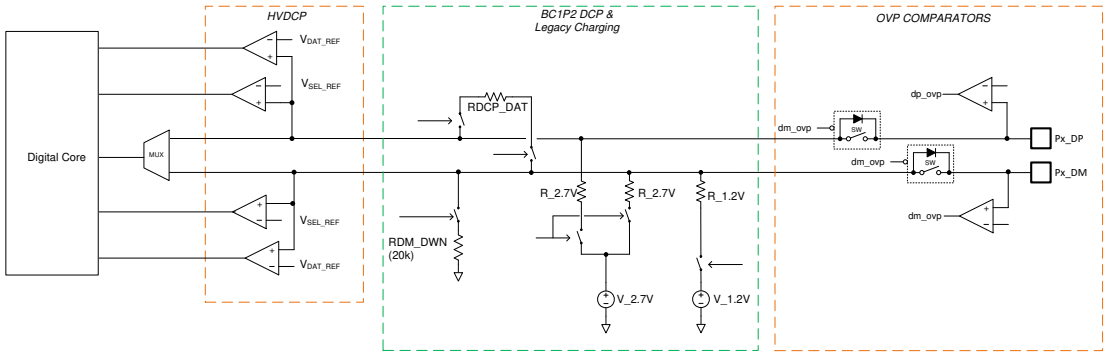


Figure 9-32. BC1P2 Functional Diagram

9.3.9 USB2.0 Low-Speed Endpoint

The USB low-speed Endpoint is a USB 2.0 low-speed (1.5 Mbps) interface used to support HID class based accesses. The TPS25772-Q1 supports control of endpoint EP0. This endpoint enumerates to a USB 2.0 host during firmware update mode. Firmware update mode is entered with when the device is powered on with an R_{TVSP} corresponding to TVSP Index 8.

Figure 9-33 shows the USB Endpoint physical layer. The physical layer consists of the analog transceiver, the Serial Interface Engine, and the Endpoint FIFOs and supports low-speed USB operation.

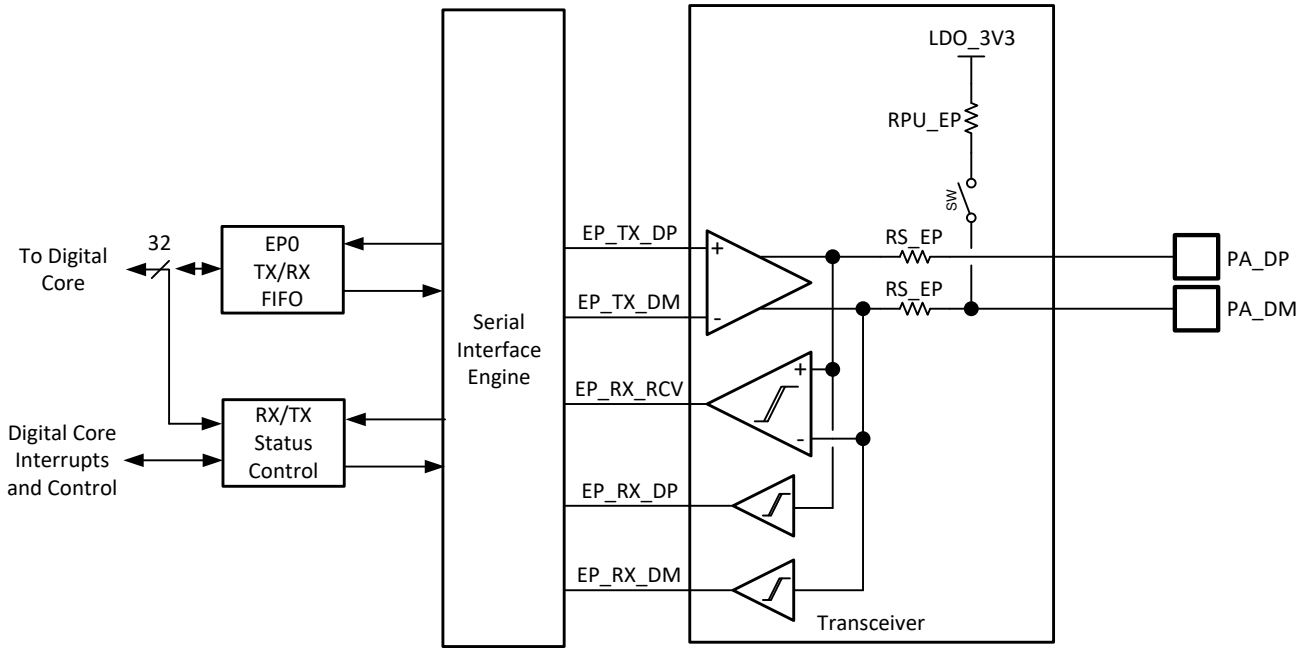


Figure 9-33. USB Endpoint PHY

The transceiver is made up of a fully differential output driver, a differential to single-ended receive buffer and two single-ended receive buffers on the D+/D– independently. The output driver drives the D+/D– through a source resistance RS_EP. RPU_EP is disconnected during transmit mode of the transceiver.

When the endpoint is in receive mode, the resistance RPU_EP is connected to the PA_DM pin. The RPU_EP resistance advertises low speed mode only.

9.3.10 Digital Interfaces

The TPS25772-Q1 contains one I^2C controller which used for communicating with I^2C target devices. Depending upon application GUI firmware configuration, an I^2C target and GPIOs may be available.

9.3.10.1 General GPIO

An application configuration GUI manages the multi-function pins which contain General Purpose Input/Output functionality. Each buffer is configurable to be a push-pull output or open drain output. When configured as an input, the signal can be a de-glitched digital input or an analog input to the ADC (only designated pins). The push-pull output is a simple CMOS totem-pole structure. Independent pull-up and pull-down enables can be configured using the application GUI. When interfacing with non 3.3-V I/O devices the output buffer should be configured as an open drain output and an external pull-up resistor attached to the GPIO pin.

9.3.10.2 I^2C Buffer

The TPS25772-Q1 features two I^2C interfaces that each use an I^2C I/O driver like the one shown in Figure 9-34. This I/O consists of an open-drain output and an input comparator with de-glitching.

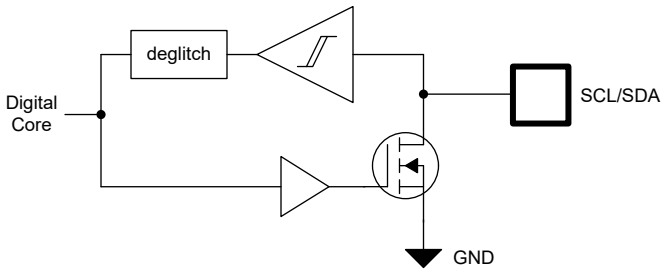


Figure 9-34. I^2C Driver

9.3.11 I²C Interface

The TPS25772-Q1 has two I²C ports. I²C1 is a controller interface. I²C2 is a target interface.

I²C1 is used to read from or write to external target devices. During boot I²C1 is configured to read firmware patch and application configuration data from an external EEPROM with target address 0x50.

Depending upon application configuration, the TPS25772-Q1 may expose target port, I²C2, using multi-function pins: GPIO2 (I²C_SCL2), GPIO3 (I²C_SDA2). When the TPS257xx-Q1 is used in systems with a HUB or MCU, the I²C2 port can provide connection status and telemetry information as well as transfer firmware updates from the HUB or MCU to an EEPROM connected on I²C1.

$\overline{\text{IRQ}}$ functionality depends upon firmware application configuration. $\overline{\text{IRQ}}$ is not always available on both I²C1 and I²C2 simultaneously. the IRQ is available as follows:

- Multi-function pin GPIO9: $\overline{\text{IRQ1(i)}}$, $\overline{\text{IRQ1(o)}}$, $\overline{\text{IRQ2(o)}}$
- Multi-function pin GPIO1: $\overline{\text{IRQ2(o)}}$

Where (i) = operates as an input, and (o) = operates as output.

In HUB applications where I²C control is not used, GPIO9 can be configured as a simple $\overline{\text{FAULT}}$ pin reporting port over-current conditions as required by the USB 2.0 specifications.

Table 9-9. I²C Summary

I2C Bus	Type	Typical Usage	Max Bus Frequency
I2C1c	Controller	Connect to I²C EEPROM, USB Type-C mux, I2C temperature sensor, I2C GPIO expander, or other I2C target. Use LDO_5V or LDO_3V3 pin as the pull-up voltage. Multi-controller configuration is not supported.	1 MHz (Fast Mode Plus)
I2C2t	Target	Connect to I²C capable USB HUB, MCU or automotive processor.	1 MHz (Fast Mode Plus)

9.3.11.1 I²C Interface Description

The I²C1 and I²C2 ports support Standard, Fast Mode, and Fast Mode Plus I²C interfaces. The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a supply through a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

A controller sending a Start condition, a high-to-low transition on the SDA input/output, while the SCL input is high initiates I²C communication. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period as changes in the data line at this time are interpreted as control commands (Start or Stop). The controller sends a Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high.

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a target receiver is addressed, it must generate an ACK after each byte is received. Similarly, the controller must generate an ACK after each byte that it receives from the target transmitter. Setup and hold times must be met to ensure proper operation.

A controller receiver signals an end of data to the target transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the target. The controller receiver holding the SDA line high does this. In this event, the target transmitter must release the data line to enable the controller to generate a Stop condition.

Figure 9-35 shows the start and stop conditions of the transfer. Figure 9-36 shows the SDA and SCL signals for transferring a bit. Figure 9-37 shows a data transfer sequence with the ACK or NACK at the last clock pulse.

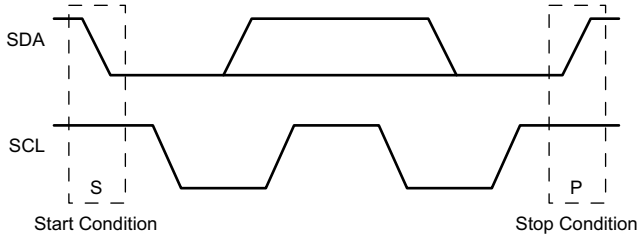


Figure 9-35. I²C Definition of Start and Stop Conditions

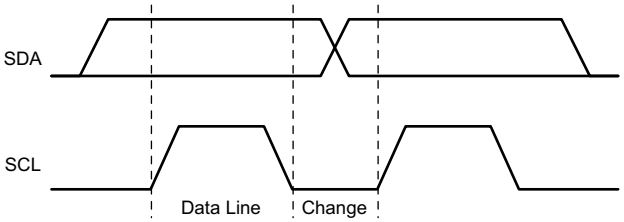


Figure 9-36. I²C Bit Transfer

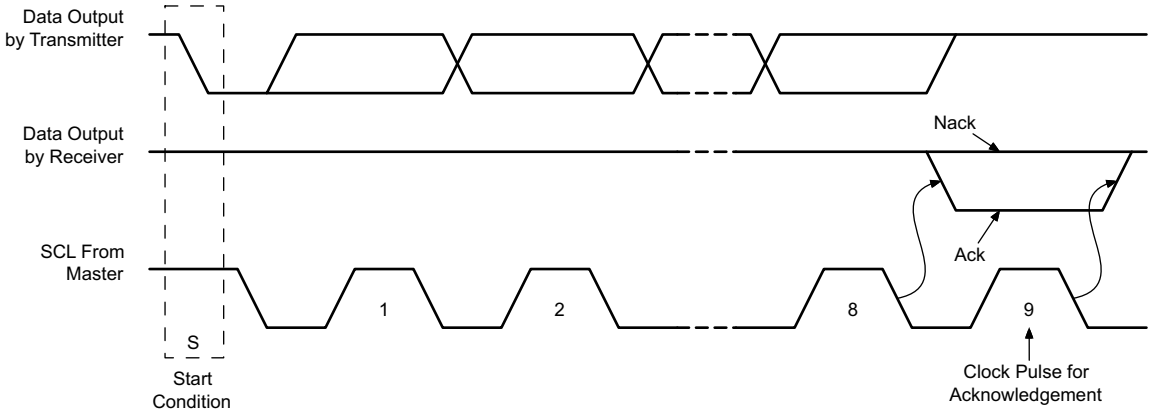


Figure 9-37. I²C Acknowledgment

9.3.11.2 I²C Clock Stretching

Clock stretching for I²C2. The target I²C port may hold the clock line (SCL) low after receiving (or sending) a byte, indicating that it is not yet ready to process more data. The controller communicating with the target must not finish the transmission of the current bit and must wait until the clock line actually goes high. When the target is clock stretching, the clock line remains low.

The controller must wait until it observes the clock line transitioning high plus an additional minimum time (4 µs for standard 100-kbps I²C) before pulling the clock low again.

Any clock pulse may be stretched but typically it is the interval before or after the acknowledgment bit.

9.3.11.3 I²C Address Setting

A HUB, MCU, or automotive processor host should only use I²C_SCL2 and I²C_SDA2 for loading a firmware patches or general status communication. Once the boot process is complete, each I²C port is assigned a unique target address as determined by the TVSP pin. The target address used by each port on the I2C2s bus are determined from the application configuration.

9.3.11.4 Unique Address Interface

The Unique Address Interface allows for complex interaction between an I²C controller and a single TPS25772-Q1. The I²C target sub-address is used to receive or respond to Host Interface protocol commands. Figure 9-38 and Figure 9-39 show the write and read protocol for the I²C target interface, and a key is included in Figure

9-40 to explain the terminology used. The TPS25772-Q1 host interface utilizes a different unique address to identify each of the two USB Type-C ports controlled by the TPS25772-Q1. The key to the protocol diagrams is in the SMBus Specification and is repeated here in part.

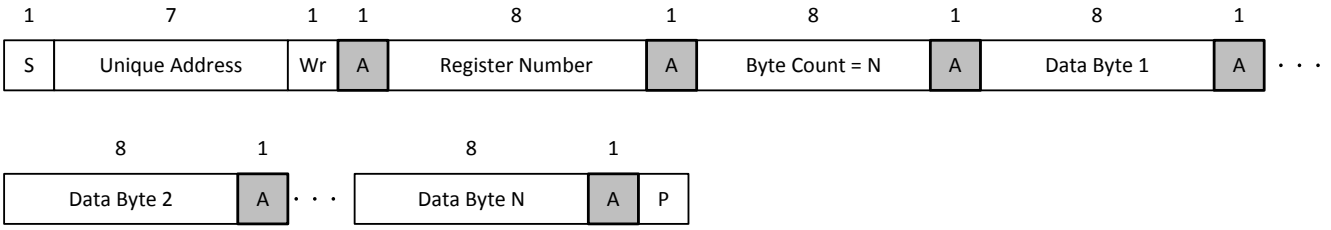


Figure 9-38. I²C Unique Address Write Register Protocol

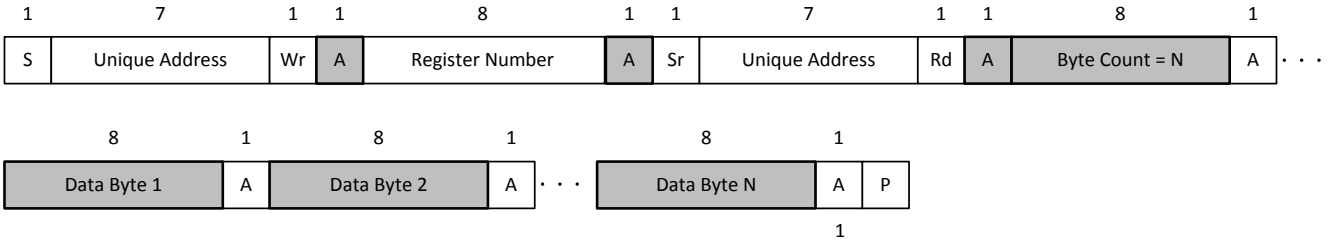


Figure 9-39. I²C Unique Address Read Register Protocol

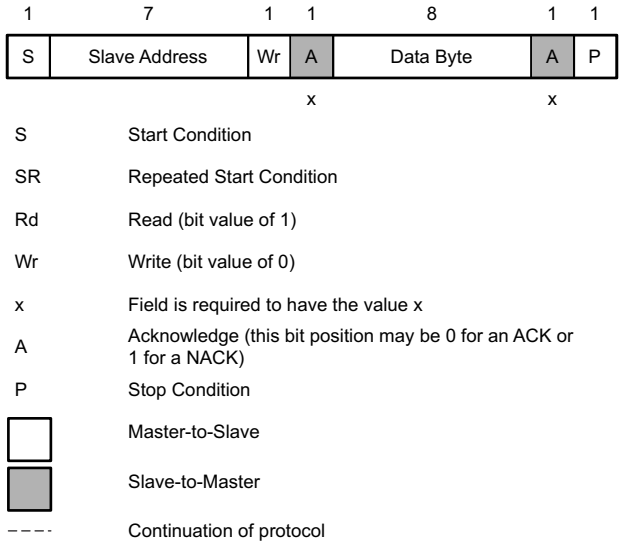


Figure 9-40. I²C Read/Write Protocol Key

9.3.11.5 I²C Pullup Resistor Calculation

Typical value for R_P, the I²C pullup resistor is given by:

$R_P = t_r / (0.8473 \times C_b)$

Refer to Table 9-10 for values of t_r, C_b and V_{OL}.

Table 9-10. Parametrics from I2C Specifications

Parameter		Standard Mode (Max)	Fast Mode (Max)	Fast Mode Plus (Max)	Unit
f_{SCL}	SCL clock frequency	100	400	1000	kHz
t_r	Rise time of both SDA and SCL signals	1000	300	120	ns
C_b	Capacitive load for each bus line	400	400	550	pF

Table 9-10. Parametrics from I2C Specifications (continued)

Parameter		Standard Mode (Max)	Fast Mode (Max)	Fast Mode Plus (Max)	Unit
V_{OL}	Low-level output voltage (at 3-mA current sink, V_{DD} > 2 V)	0.4	0.4	0.4	V
	Low-level output voltage (at 2-mA current sink, V_{DD} ≤ 2 V)	–	0.2 × V_{DD}	0.2 × V_{DD}	V

For additional background regarding I2C pullup resistor calculations, please refer to application report, *I^2C Bus Pullup Resistor Calculation*.

9.3.12 Digital Core

Figure 9-41 shows a simplified block diagram of the digital core.

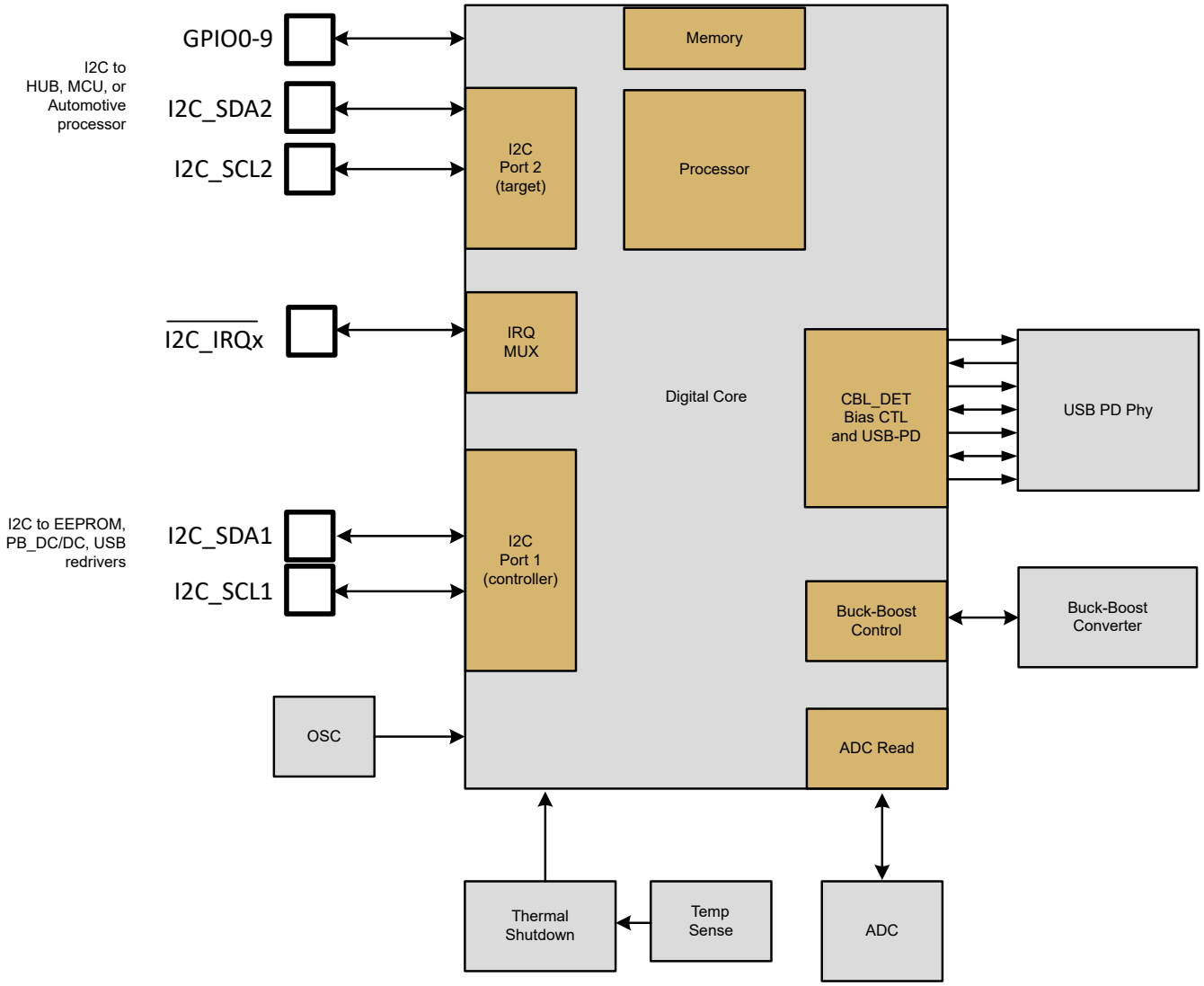


Figure 9-41. Digital Core Simplified Block Diagram

9.3.12.1 Device Memory

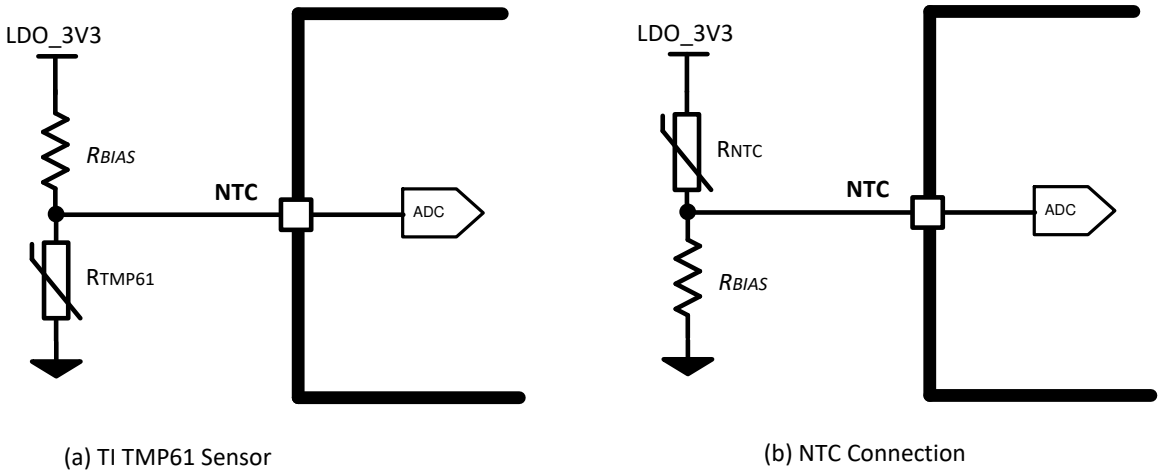
The digital core contains a combination of ROM, SRAM, and OTP. ROM and SRAM function as the storage and operational space for application firmware. OTP contains boot configuration settings. There are 27 kBytes of SRAM, 160 kBytes of ROM, and 512 bytes of OTP.

9.3.12.2 Core Microprocessor

The digital core is an ARM M0+ clocked at 24MHz with zero wait states.

9.3.13 NTC Input

The NTC pin is used by the device firmware to monitor system temperature. Rising or falling voltages on the NTC pin indicate increasing or decreasing system temperatures, respectively. To achieve a positive temperature slope on the TPS25772-Q1 NTC pin, thermistors should be connected to LDO_3V3 as shown in Figure 9-42.



(a) TI TMP61 Sensor

(b) NTC Connection

Figure 9-42. Thermistor Connections (a) PTC, (b) NTC

See Figure 9-43 and Figure 9-44. Using the application configuration GUI, the user can configure system power policy management responses for up to three V_{NTC} voltages.

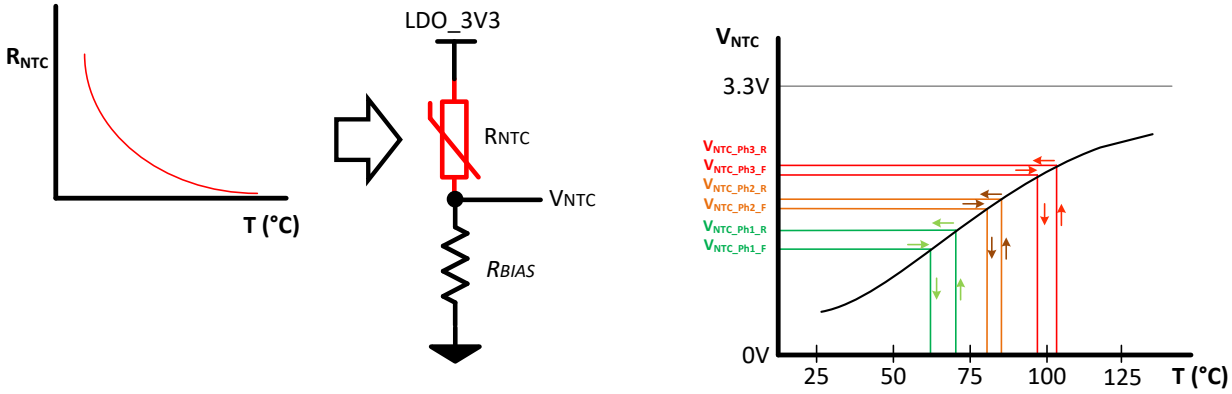


Figure 9-43. NTC Response Curve

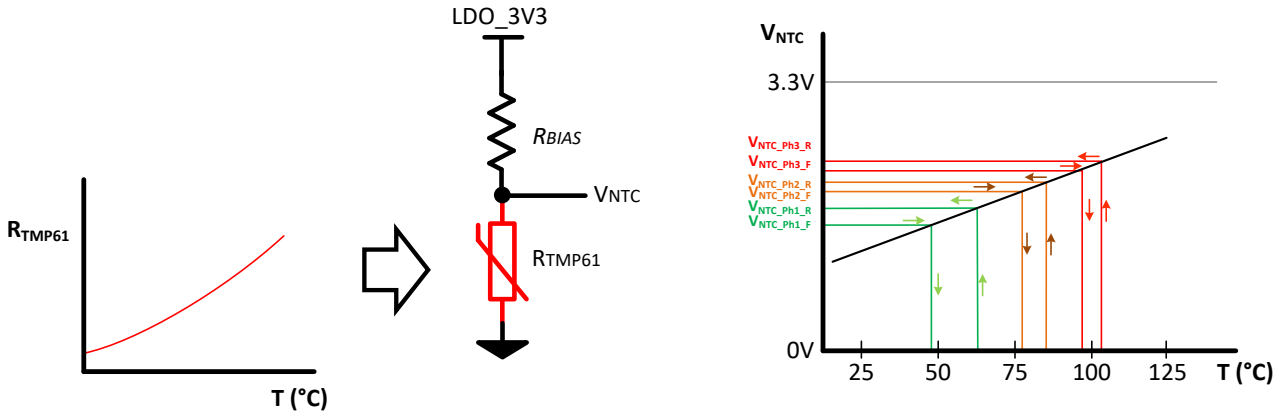


Figure 9-44. TMP61 PTC Response Curve

Note

For optimum accuracy, use the V_{LDO_3V3} specifications in *Electrical Characteristics* tables when performing resistor divider calculations.

9.3.14 Thermal Sensors and Thermal Shutdown

There are five internal thermal sensors in the TPS25772-Q1 devices:

- T_{SD_BB}. Two diode OR'ed thermal sensors to monitor buck-boost power FETs. Disables buck-boost regulator when asserted. USB-PD engine enters error recovery.
- $T_{SD\_PA\_VCONN}$. One thermal sensor located in the PA_VCONN path. Opens PA_VCONN FET during over-temperature event. USB-PD engine enters error recovery.
- $T_{SD\_PB\_VCONN}$. Applicable to dual port devices. One thermal sensor located in the PB_VCONN path. Opens PB_VCONN FET during over-temperature event. USB-PD engine enters error recovery.
- $T_{SD\_PA\_VBUS\_DISCH}$. One thermal sensor located in the PA_VBUS discharge path. Opens PA_VBUS discharge FET during over-temperature. Closes PA_VBUS discharge FET when temperature decreases below falling hysteresis. (T_{SD_HYS}) if PA_VBUS is above discharge threshold set by firmware during decreasing VBUS transition.
- T_{SD_LDO5V}. One thermal sensor located in the LDO_5V regulator. Operates as master thermal shutdown. Disables device completely during over-temperature events causing M0 to hard reset. Allows device operation when temperature decreases below falling hysteresis (T_{SD_HYS}).

9.4 Device Functional Modes

Shutdown Mode

The EN/UVLO pin provides electrical ON and OFF control for the TPS25772-Q1. When $V_{EN/UVLO}$ is below 1.15 V (typ), the device is in shutdown mode in which the Cortex M0 is disabled and only minimal analog functions are operating. Refer to VIN UVLO and Enable/UVLO section for the detailed description of the EN/UVLO pin functionality.

Active Mode

The TPS25772-Q1 enters active mode when $V_{EN/UVLO}$ is above its rising threshold, $V_{EN(OPER)}$, and the supply voltage on the IN pin is above the V_{IN} undervoltage lockout threshold, $V_{IN(UVLO\_R)}$. In active mode, the internal analog circuits are fully operational with the M0 enabled and executing firmware from ROM.

At the onset of active mode, firmware boot code will attempt to measure the resistance on the TVSP pin and decode a TVSP Index value. Upon successful configuration and firmware patch load, the device is ready to begin operation per configuration settings stored on the external EEPROM. If the configuration and patch data do not load successfully due to communications error the device will continue to operate with only Port A

enabled with standard Type-C functionality. Index value 8 is reserved for use when updating device configuration and firmware patch information through the TPS25772-Q1 GUI and Port A connection. Once device boot is complete, device firmware will control and manage USB connections in accordance with loaded application configuration settings.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The TPS25772-Q1 application GUI provides default settings suitable for most applications.

The most common implementations are dual port USB PD charger and dual port USB PD with USB HUB. Consult the TPS2576x, TPS2577x Configuration GUI User's Guide and application GUI for additional configurations.

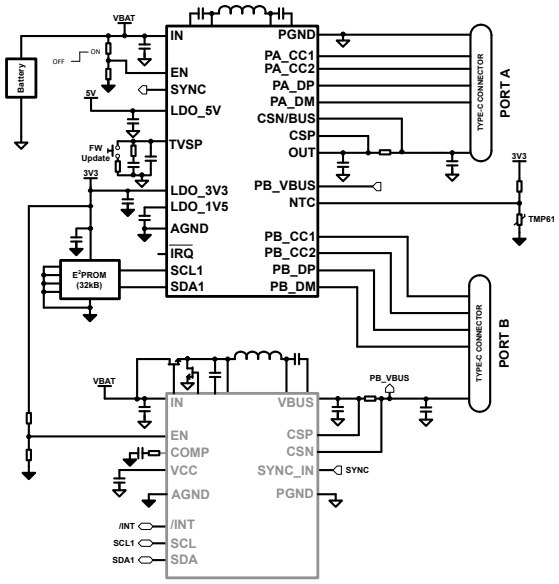


Figure 10-1. Simplified Dual USB PD Charger

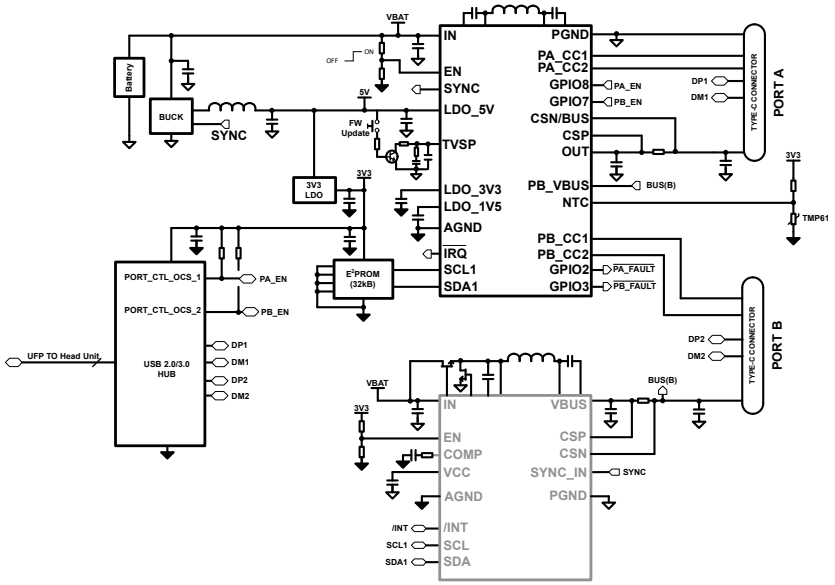


Figure 10-2. Simplified Dual USB PD with HUB

Typical Application describes a detailed step-by-step design procedure for a typical charger application circuit.

10.2 Typical Application

Figure 10-3 Shows a typical example of a 65 W output automotive USB Type-C Power Delivery port. The device is internally compensated and optimized for components shown in Table 10-1.

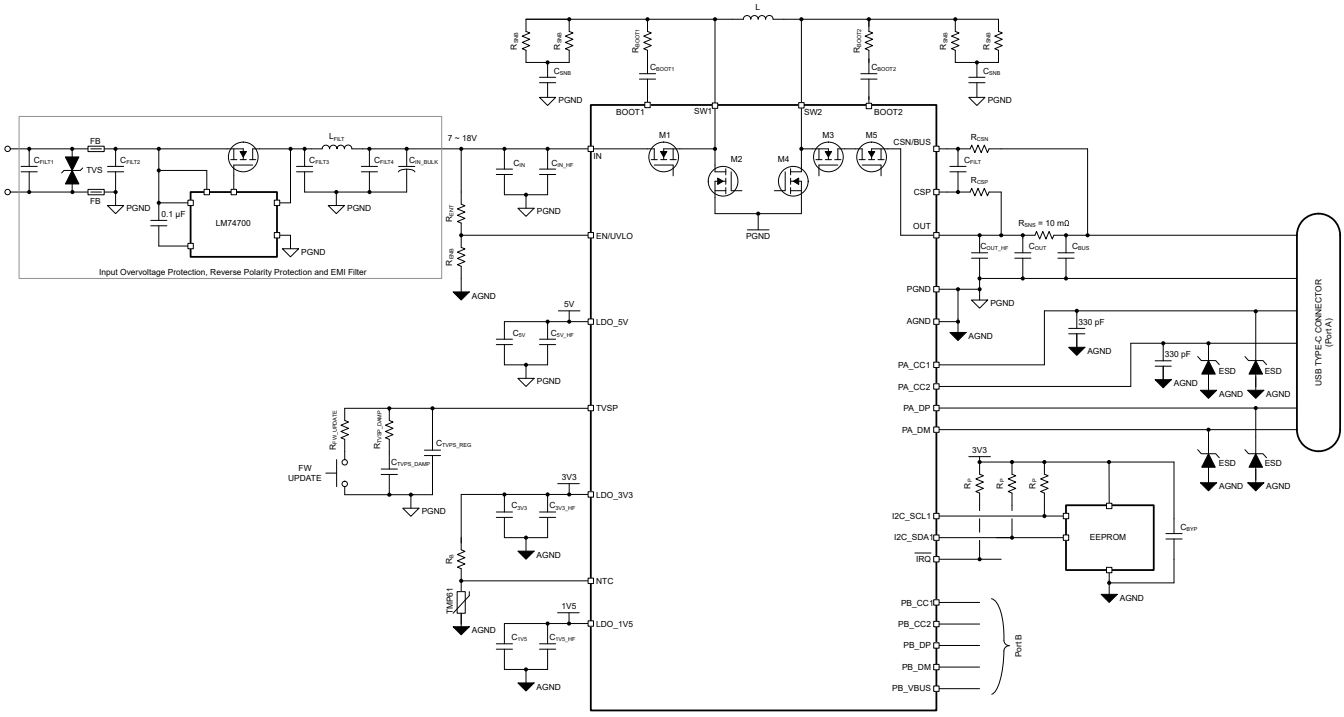


Figure 10-3. TPS25772-Q1 Application Schematic

Table 10-1. Recommended Inductors, Input and Output Capacitance

f_{SW}	C_{IN} + C_{HF}	L	MIN of C_{OUT} + C_{BUS}	C_{OUT} + C_{HF}	C_{BUS}
300	22 µF + 2 × 0.1 µF	4.7 µH	160 µF	30 µF + 2 × 0.1 µF	130 µF + 2 × 0.1 µF
400	22 µF + 2 ×0.1 µF	4.7 µH	120 µF	30 µF + 2 × 0.1 µF	90 µF + 2 × 0.1 µF

Table 10-1. Recommended Inductors, Input and Output Capacitance (continued)

f_{SW}	C_{IN} + C_{HF}	L	MIN of C_{OUT} + C_{BUS}	C_{OUT} + C_{HF}	C_{BUS}
400	22 µF + 2 × 0.1 µF	3.3 µH	140 µF	30 µF + 2 × 0.1 µF	110 µF + 2 × 0.1 µF
450	22 µF + 2 × 0.1 µF	3.3 µH	140 µF	30 µF + 2 × 0.1 µF	110 µF + 2 × 0.1 µF

- 50 V rated capacitors recommended.

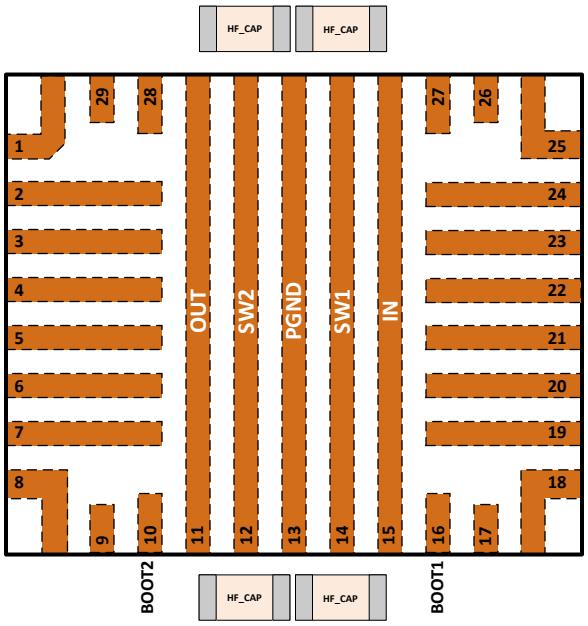


Figure 10-4. Input and Output C_{HF} Capacitor Placement

To ensure adequate decoupling of V_{IN} and V_{OUT} and robust device operation, use two 0.1 µF, C_{HF} capacitors per node, placed on opposite sides of the IC package, as close to the pins as possible. Typically, the inductor is placed on the same PCB layer (top or bottom) as the IC package. The C_{HF} capacitors on the inductor end of the IC package may be placed on the opposite side of the PCB (bottom or top) using vias to minimize trace length from the inductor side IN and OUT pins to the physical location of these capacitors.

Table 10-2. Recommended SWx Snubber and Current Sense Filter Components

SW1 (1)		SW2 (2)		CSP & CSN Filter (3)		
R_{SNB} (0.25 W)	C_{SNB} (50 V)	R_{SNB} (0.25 W)	C_{SNB} (50 V)	R_{CSP} (0.1 W)	R_{CSN} (0.1 W)	C_{FLT} (50 V)
2.2 Ω || 2.2 Ω	1 nf	2.2 Ω || 2.2 Ω	3.3 nF	10 Ω	0 Ω	0.22 µF

1. As needed for EMI mitigation - user optional. (Use of this snubber can also aid in supporting devices with high initial inrush load current that exceeds the power delivery specification.)
2. **Required** for robust device operation.
3. **Required** to meet USB-IF current regulation requirements.

10.2.1 Design Requirements

For this example, Table 10-3 are used as the target parameters.

Table 10-3. Design Inputs

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	6.8 V to 18 V (transients to 36 V)
UVLO Turn on Voltage	6.5 V
USB PD Power	65 W

Table 10-3. Design Inputs (continued)

DESIGN PARAMETER	EXAMPLE VALUE
USB PD V_{BUS} Voltages	5 V, 9 V, 15 V, 20 V and 3.3 to 21 V (PPS)
Output	3.3 - 21 V
Load Current	PDO: 5 V, 3 A; 9 V, 3 A; 15 V, 3 A, 20 V, 3.25 A APDO: 3.3 - 21 V, 3 A
Switching Frequency	400 kHz
V_{CONN}	0.1 W
Automotive Module Maximum Current	15 A

10.2.2 Detailed Design Procedure

10.2.2.1 Application GUI Selections

Use the application GUI to select the desired operating conditions. Once complete, save the settings to the programming PC, flash the firmware to EEPROM, and power cycle device. Once complete the TPS25772-Q1 will be ready for operation.

Table 10-4. Application GUI Selections

PARAMETER	GUI SELECTION
BUCK-BOOST AND USB INPUTS	
Port A V_{BUS} Power	65 W
Port A PDOs and APDOs	PDO: 5 V, 3 A; 9 V, 3 A; 15 V, 3 A; 20 V, 3.25 A APDO: 3.3 - 21 V, 3A
Port A V_{CONN} Power	0.1 W
f_{SW} Switching Frequency	400 kHz
L Inductor	4.7 µH
Automotive Module Maximum Current	15 A
LOW BATTERY INPUTS	
Engine ON voltage	12.5 V
Engine OFF voltage	11 V
Run timer after engine off	600 seconds
THERMAL MANAGEMENT INPUTS	
V_{NTC_PHASE1}	1.65 V
NTC_PHASE1 Power as Percentage of MAX	50 %
V_{NTC_PHASE2}	2.1 V
NTC_PHASE2 Power as Percentage of MAX	30 %
V_{NTC_PHASE3}	2.4 V
NTC_PHASE3 Power as Percentage of MAX	0 % (disable PA_VBUS)

10.2.2.2 EEPROM Selection

An EEPROM is required to store user application configuration data as any firmware patch updates released by Texas Instruments during the life of the product.

Basic requirements:

- 32kB (256kb)
- 7 Bit I2C address (0x50)
- Organization: 32kb x 8 (totals 256kb)
- Active firmware image is stored in one 16kb x 8 partition. The previous firmware image is retained in the other 16kb x 8 partition for reliability.
- Page size/buffer should be 64b

Table 10-5. Suggested EEPROMs

Manufacturer	Part Number
On Semi	CAV24C256
Microchip	24LC256
ST Micro	M24256
Rohm	BRA24T512=3AM

10.2.2.3 EN/UVLO

The TPS25772-Q1 has a fixed $V_{IN(UVLO)}$ with rising and falling thresholds between 5 and 5.5 V, refer to Section 7.6 for exact values. The falling threshold, $V_{IN(UVLO\_F)}$, disables the device when the battery voltage is too low for continued operation. To establish a turn on voltage higher than $V_{IN(UVLO\_R)}$, connect a resistor divider from the IN supply voltage to the EN/UVLO pin. When $V_{EN/UVLO} > V_{EN(OPER)}$, nominally 1.25 V, the device exits low power shutdown and begins to startup.

In this example a V_{IN} turn on voltage of approximately 6.5 V is required. Use the equations and examples below to determine the required resistor values.

- Choose standard value R_{ENB} = 22 kΩ.
- Calculate R_{ENT}

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN(OPER)}} - 1\right) \times R_{ENB} \quad (3)$$

$$R_{ENT} = \left(\frac{6.5\ V}{1.25\ V} - 1\right) \times 22\ k\Omega = 92.4\ k\Omega \quad (4)$$

- Select a standard value of 91 kΩ.
- Using 22 kΩ and 91 kΩ. Rearranging Equation 3 results in

$$V_{ON} = \left(\frac{R_{ENT}}{R_{ENB}} + 1\right) \times V_{EN(OPER)} \quad (5)$$

$$V_{ON} = \left(\frac{91\ k\Omega}{22\ k\Omega} + 1\right) \times 1.25\ V = 6.42\ V \quad (6)$$

- Calculate V_{OFF}

$$V_{OFF} = \left(1 - \frac{V_{EN(HYS)}}{V_{EN(OPER)}}\right) \times V_{ON} \quad (7)$$

$$V_{OFF} = \left(1 - \frac{0.1\ V}{1.25\ V}\right) \times 6.42\ V = 5.91\ V \quad (8)$$

- Lastly, confirm the selected resistors do not trigger the EN/UVLO pin MAX clamp voltage. Assuming 36 V as a maximum V_{IN} transient.

$$V_{EN/UVLO(MAX)} = \left(\frac{V_{IN(MAX)} \times R_{ENB}}{R_{ENT} + R_{ENB}}\right) \quad (9)$$

$$V_{EN/UVLO(MAX)} = \left(\frac{36\ V \times 22\ k\Omega}{22\ k\Omega + 91\ k\Omega}\right) = 7\ V \quad (10)$$

- The result, 7 V, is less than the EN/UVLO pin maximum clamp voltage.

10.2.2.4 Sense Resistor, R_{SNS}, R_{CSP}, R_{CSN} and C_{FILT}

The TPS25772-Q1 requires a 10-mΩ resistance between the CSP and CSN/BUS pins. For accurate current limit regulation, ±1% precision or better is required. For a DC output current of 3.25 A, the power dissipation in the resistor is

I^2R, or $(3.25\ A)^2 \times 0.01\ \Omega = 0.106\ W$.

A power resistor with 0.33-W rating, ± 1% tolerance and 2010 case is chosen. *Check the manufacturers power derating curves when selecting the component. Most derate maximum power above 70°C.*

An RC filter network is required on the CSP and CSN/BUS pins for proper USB PD PPS current limit accuracy. A filter network with R_{CSP} = 10 Ω, R_{CSN} = 0 Ω, and filter capacitor, C_{FILT} = 0.22 µF is recommended. Suggested RC filter component ratings are shown in Table 10-2. R_{CSN} must be zero ohm to avoid interfering with the V_{BUS} discharge functionality.

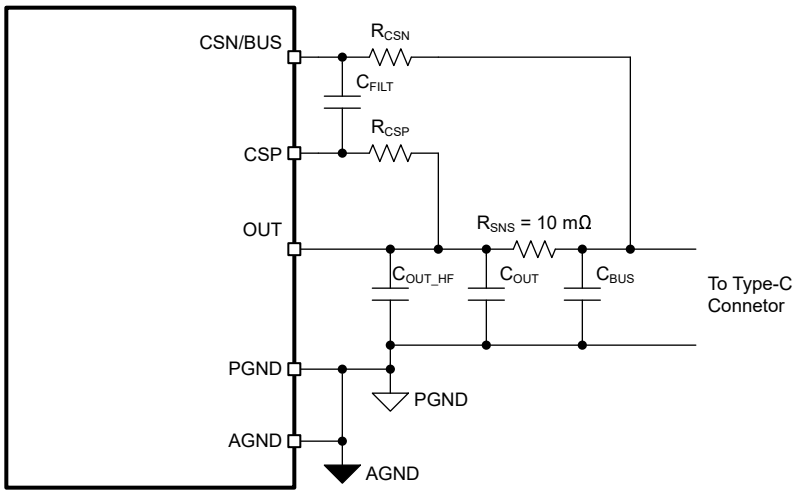


Figure 10-5. Current Sense Amplifier: RC Filter Components

10.2.2.5 Inductor Currents

Table 10-1 lists recommended inductor values based on desired switching frequency, f_{SW}. The following equations were used to derive the values in the *Buck Calculation* and *Boost Calculation* results tables below.

$$D_{BUCK} = \frac{V_{OUT}}{V_{IN(MAX)} \times \eta} \tag{11}$$

$$D_{BOOST} = 1 - \frac{V_{IN(MIN)} \times \eta}{V_{OUT}} \tag{12}$$

where

- $V_{IN(MAX)}$ = maximum input voltage
- $V_{IN(MIN)}$ = minimum input voltage
- V_{OUT} = output voltage
- D_{BUCK} = minimum duty cycle for buck mode
- D_{BOOST} = maximum duty cycle for boost mode
- η = estimated efficiency calculated at V_{IN}, V_{OUT}, and I_{OUT}

Buck Mode

$$I_{SW\_BUCK(MAX)} = \frac{\Delta I_{L\_BUCK(MAX)}}{2} + I_{OUT} \tag{13}$$

$$\Delta I_{L\_BUCK(MAX)} = \frac{(V_{IN(MAX)} - V_{OUT(MIN)}) \times D_{BUCK}}{f_{SW} \times L} \quad (14)$$

where

- $V_{IN(MAX)}$ = maximum input voltage
- $V_{OUT(MIN)}$ = minimum output voltage
- I_{OUT} = maximum DC output current
- $\Delta I_{L\text{-}BUCK(MAX)}$ = maximum ripple current through the inductor when in buck operation
- $I_{SW\_BUCK(MAX)}$ = maximum switch current when in buck operation
- D_{BUCK} = minimum duty cycle for buck operation
- f_{SW} = switching frequency of the converter
- L = selected inductor value

$$I_{MAXOUT(BUCK)} = I_{PEAK(BUCK)} - \frac{\Delta I_{L\_BUCK(MAX)}}{2} \quad (15)$$

where

- $I_{MAXOUT(BUCK)}$ = maximum deliverable current through inductor by the converter
- $I_{PEAK(BUCK)}$ = buck switch peak current limit from *Electrical Characteristics* table
- $\Delta I_{L\_BUCK(MAX)}$ = Ripple current through the inductor calculated in Equation 14.

Boost Mode

$$I_{SW\_BOOST(MAX)} = \frac{\Delta I_{L\_BOOST(MAX)}}{2} + \frac{I_{OUT}}{1 - D_{BOOST}} \quad (16)$$

$$\Delta I_{L\_BOOST(MAX)} = \frac{V_{IN(MIN)} \times D_{BOOST}}{f_{SW} \times L} \quad (17)$$

where

- $V_{IN(MIN)}$ = minimum input voltage
- $V_{OUT(MAX)}$ = desired output voltage
- I_{OUT} = desired output current
- $\Delta I_{L\_BOOST(MAX)}$ = maximum ripple current through the inductor in boost operation
- $I_{SW\_BOOST(MAX)}$ = maximum switch current in boost operation
- D_{BOOST} = maximum duty cycle for boost operation
- f_{SW}= switching frequency of the converter
- L = selected inductor value

$$I_{MAXOUT(BOOST)} = \left(I_{PEAK(BOOST)} - \frac{\Delta I_{L\_BOOST(MAX)}}{2}\right) \times (1 - D_{BOOST}) \quad (18)$$

where

- $I_{MAXOUT(BOOST)}$ = maximum deliverable current through inductor by the converter
- D_{BOOST} = maximum duty cycle for boost mode
- $I_{PEAK(BOOST)}$ = boost switch peak current limit from *Electrical Characteristics* table
- $\Delta I_{L\_MAX(BOOST)}$ = Ripple current through the inductor calculated in Equation 17.

Buck Operation

Table 10-6 provides the tabulated $\Delta I_{L\_BUCK(MAX)}$ and $I_{SW\_BUCK(MAX)}$ for the conditions below.

- η = 0.95
- $V_{IN(MAX)}$ = 18 V
- $V_{OUT(MIN)}$ = 3.3 V
- $D_{BUCK(MIN)}$ = 0.193

Table 10-6. Buck Calculation Results (L = 4.7 µH), I_{BUS} = 3 A

f_{SW} (kHz)	I_{OUT} (A)	$\Delta I_{L\_BUCK(MAX)}$ (A)	$I_{SW\_BUCK(MAX)}$ (A)
300	3.00	2.87	4.44
400	3.00	2.15	4.08
450	3.00	1.91	3.96
300	3.00	2.01	4.01
400	3.00	1.51	3.76
450	3.00	1.34	3.67

Boost Operation

Table 10-7 provides the tabulated $\Delta I_{L\_BOOST(MAX)}$, $I_{SW\_BOOST(MAX)}$, suggested GUI $I_{PEAK(BOOST)}$ (MIN) settings for the maximum output power conditions shown below.

If $I_{SW\_BOOST(MAX)} > I_{PEAK(BOOST)}$ (MIN) → V_{BUS} dropout likely.

If $I_{SW\_BOOST(MAX)} < I_{PEAK(BOOST)}$ (MIN) → V_{BUS} regulates normally.

- η = 0.95
- $V_{IN(MIN)}$ = 5.5 V to 9 V
- $V_{OUT(MAX)}$ = 21 V
- I_{OUT} = 3 A

To be noted, the calculation here uses 21V 3 A instead of 20 V 3.25A because 21 V 3A has bigger inductor peak current.

Table 10-7. Boost Calculation Results (L = 4.7 µH), I_{BUS} = 3 A

f_{SW} (kHz)	$V_{IN(MIN)}$ (V)	$D_{BOOST(MAX)}$	$\Delta I_{L\_BOOST(MAX)}$ (A)	$I_{SW\_BOOST(MAX)}$ (A)	GUI [1] $I_{PEAK(BOOST)}$ (A)
300	5.5	0.751	2.93	13.51	12.3
	6	0.729	3.10	12.62	12.3
	6.5	0.706	3.25	11.83	12.3
	7	0.683	3.39	11.16	12.3
	7.5	0.661	3.52	10.61	10.8
	8	0.638	3.62	10.10	10.8
	8.5	0.615	3.71	9.65	10.8
	9	0.593	3.79	9.27	9.3

Table 10-7. Boost Calculation Results (L = 4.7 µH), I_{BUS} = 3 A (continued)

f_{SW} (kHz)	$V_{IN(MIN)}$ (V)	$D_{BOOST(MAX)}$	$\Delta I_{L\_BOOST(MAX)}$ (A)	$I_{SW\_BOOST(MAX)}$ (A)	GUI [1] $I_{PEAK(BOOST)}$ (A)
400	5.5	0.751	2.20	13.15	12.3
	6	0.729	2.33	12.24	12.3
	6.5	0.706	2.44	11.42	12.3
	7	0.683	2.54	10.73	10.8
	7.5	0.661	2.64	10.17	10.8
	8	0.638	2.71	9.64	10.8
	8.5	0.615	2.78	9.18	9.3
	9	0.593	2.84	8.79	9.3
450	5.5	0.751	1.95	13.02	12.3
	6	0.729	2.07	12.11	12.3
	6.5	0.706	2.17	11.29	12.3
	7	0.683	2.26	10.59	10.8
	7.5	0.661	2.34	10.02	10.8
	8	0.638	2.41	9.49	9.3
	8.5	0.615	2.47	9.03	9.3
	9	0.593	2.51	8.63	9.3

(1) MIN value of boost peak ILIM shown. See electrical characteristics table for MIN, TYP, MAX values.

10.2.2.6 Output Capacitor

In the boost mode, the output capacitor conducts high ripple current. The output capacitor RMS ripple current is given by Equation 19 where the minimum V_{IN} corresponds to the maximum capacitor current.

$$I_{COUT(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} - 1} \tag{19}$$

In this example the maximum output ripple RMS current is $I_{COUT(RMS)}$ = 3.18 A. A 5-mΩ output capacitor ESR causes an output ripple voltage of 34 mV as given by:

$$\Delta V_{RIPPLE(ESR)} = \frac{I_{OUT} \times V_{OUT}}{V_{IN(MIN)}} \times ESR \tag{20}$$

A 140 µF output capacitor (C_{OUT} + C_{BUS}) causes a capacitive ripple voltage of 26 mV as given by:

$$\Delta V_{RIPPLE(COUT)} = \frac{I_{OUT} \times \left(1 - \frac{V_{IN(MIN)}}{V_{OUT}}\right)}{C_{OUT} \times F_{sw}} \tag{21}$$

Typically a combination of ceramic and bulk capacitors is needed to provide low ESR and high ripple current capacity. The complete schematic in *Typical Application* section provides C_{OUT} and C_{BUS} recommendations suitable for most applications.

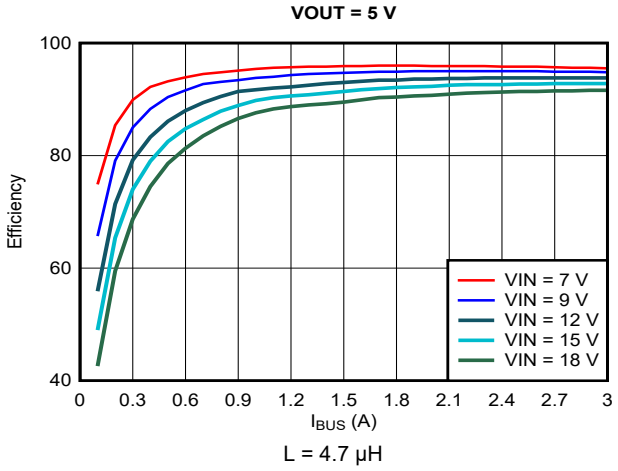
10.2.2.7 Input Capacitor

In the buck mode, the input capacitor supplies high ripple current. The RMS current in the input capacitor is given by:

$$I_{CIN(RMS)} = I_{OUT}\sqrt{D \times (1-D)} \quad (22)$$

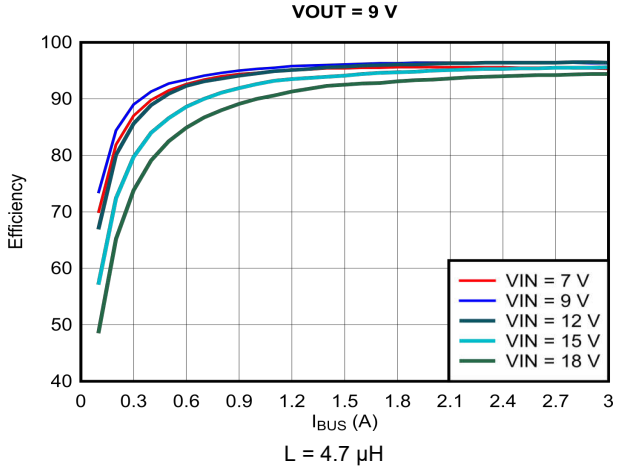
The maximum RMS current occurs at D = 0.5, which gives $I_{CIN(RMS)} = I_{OUT}/2 = 1.5$ A. A combination of ceramic and bulk capacitors should be used to provide short path for high di/dt current and to reduce the output voltage ripple. Table 10-1 in the *Typical Application* section is a good starting point for C_{IN} selection.

10.2.3 Application Curves



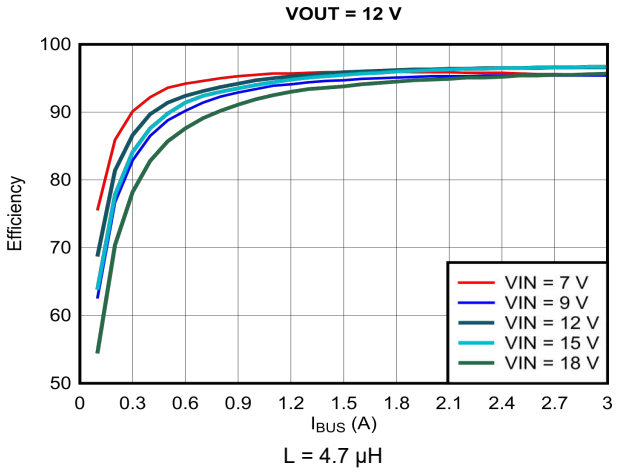
L = 4.7 µH

Figure 10-6. Efficiency vs Output Current (I_{OUT}), V_{OUT} = 5 V



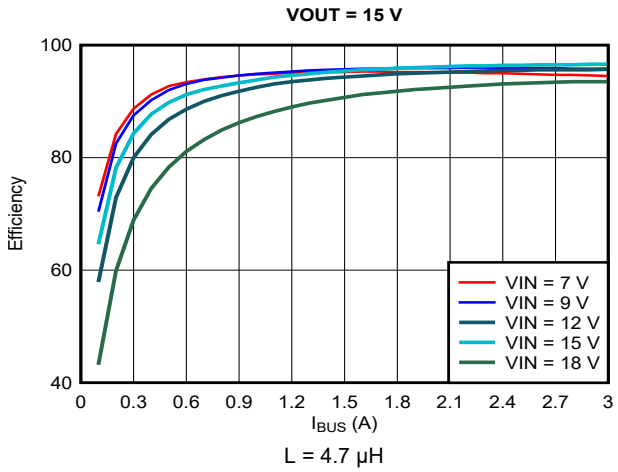
L = 4.7 µH

Figure 10-7. Efficiency vs Output Current (I_{OUT}), V_{OUT} = 9 V



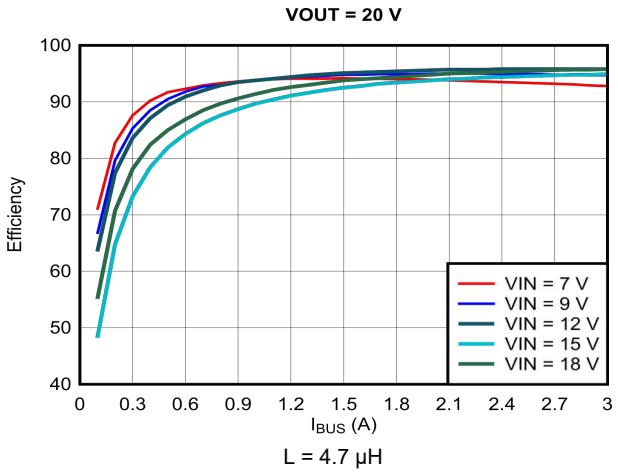
L = 4.7 µH

Figure 10-8. Efficiency vs Output Current (I_{OUT}), V_{OUT} = 12 V



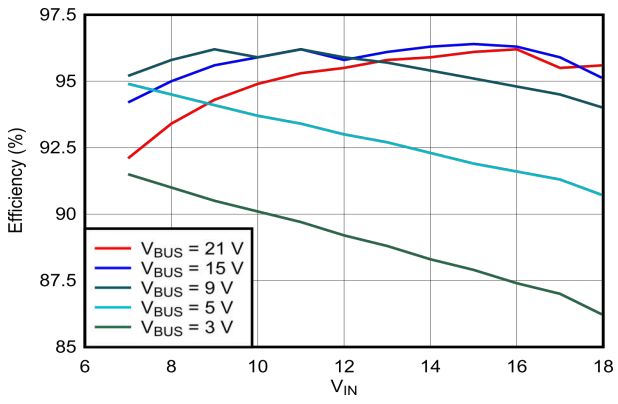
L = 4.7 µH

Figure 10-9. Efficiency vs Output Current (I_{OUT}), V_{OUT} = 15 V



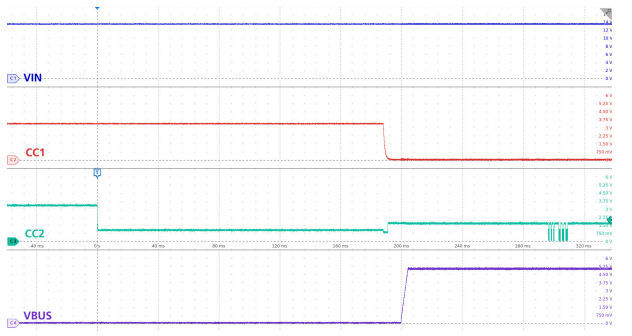
L = 4.7 µH

Figure 10-10. Efficiency vs Output Current (I_{OUT}), V_{OUT} = 20 V



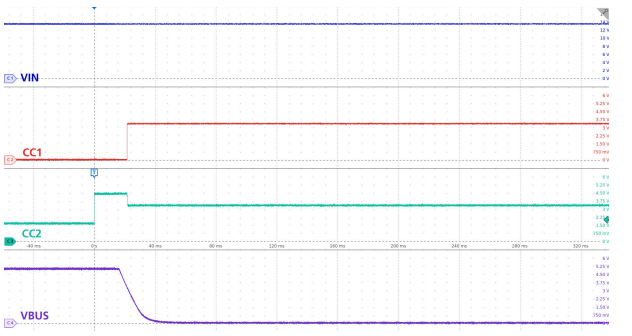
IBUS = 3 A
L = 4.7 µH

Figure 10-11. Efficiency vs Input Voltage



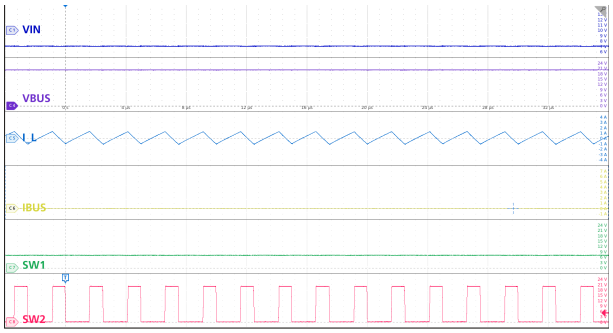
V_{IN} = 13.5 V V_{BUS} = 0 V to 5 V I_{BUS} = 0 A

Figure 10-12. Type-C Attach



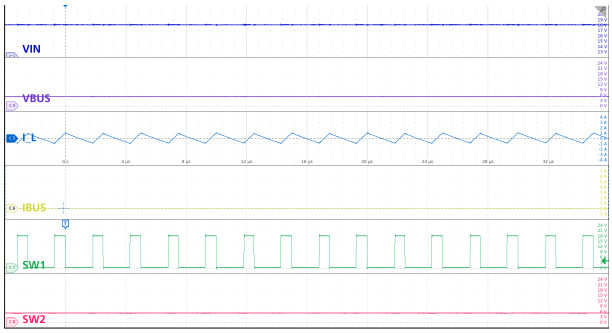
V_{IN} = 13.5 V V_{BUS} = 5 V to 0 V I_{BUS} = 0 A

Figure 10-13. Type-C Detach



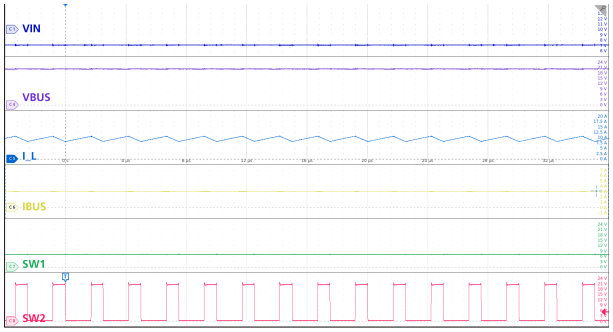
V_{IN} = 7 V V_{BUS} = 20 V I_{BUS} = 0 A

Figure 10-14. Boost Mode: Low V_{IN}, No Load



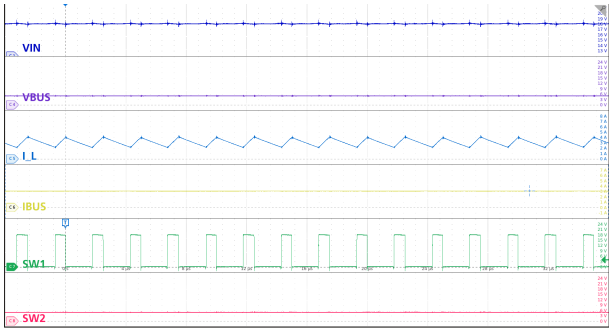
V_{IN} = 18 V V_{BUS} = 5 V I_{BUS} = 0 A

Figure 10-15. Buck Mode: High V_{IN}, No Load



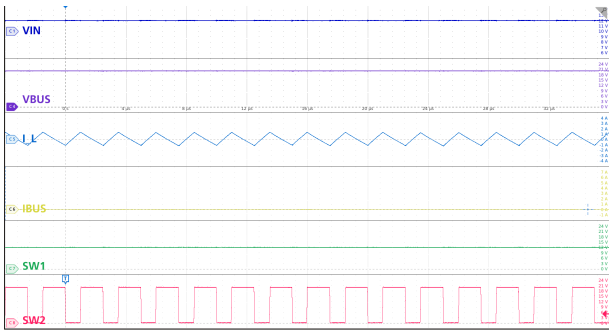
V_{IN} = 7 V V_{BUS} = 20 V I_{BUS} = 3 A

Figure 10-16. Boost Mode: Low V_{IN}, 3 A Load



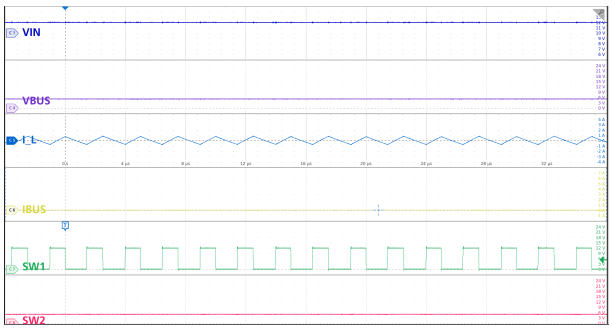
V_{IN} = 18 V V_{BUS} = 5 V I_{BUS} = 3 A

Figure 10-17. Buck Mode: High V_{IN}, 3 A load



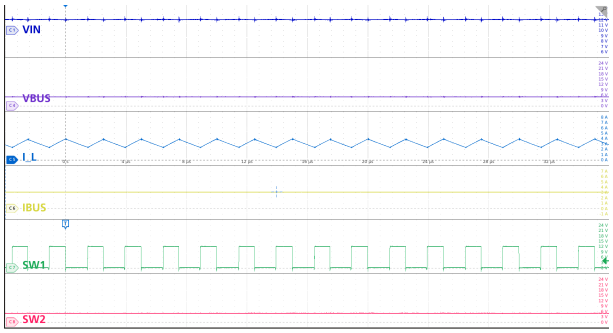
V_{IN} = 12 V V_{BUS} = 20 V I_{BUS} = 0 A

Figure 10-18. Boost Mode: Nominal V_{IN}, No Load



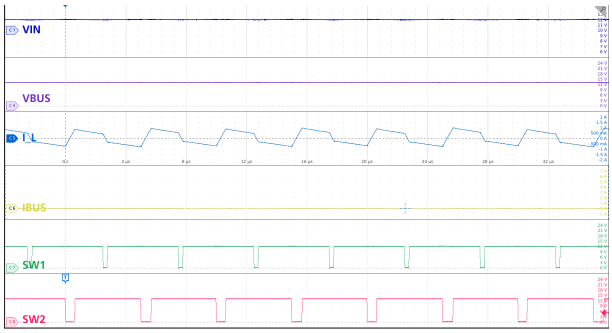
V_{IN} = 12 V V_{BUS} = 5 V I_{BUS} = 0 A

Figure 10-19. Buck Mode: Nominal V_{IN}, No Load



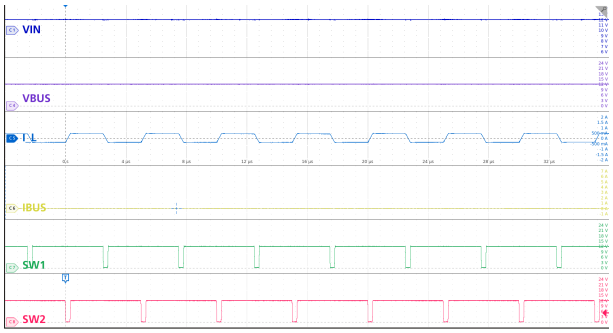
V_{IN} = 12 V V_{BUS} = 5 V I_{BUS} = 3 A

Figure 10-20. Buck Mode: nominal V_{IN}, 3 A Load



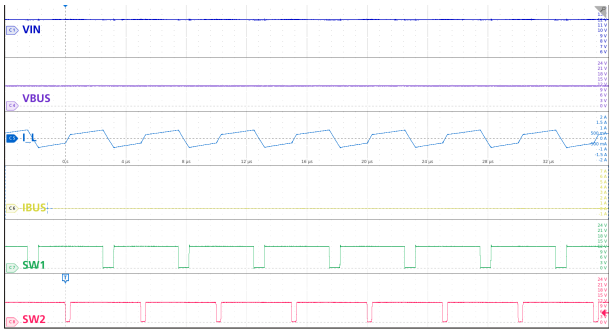
V_{IN} = 12 V V_{BUS} = 13 V I_{BUS} = 0 A

Figure 10-21. Buck-Boost Mode: $V_{IN} \lessgtr V_{BUS}$, No Load



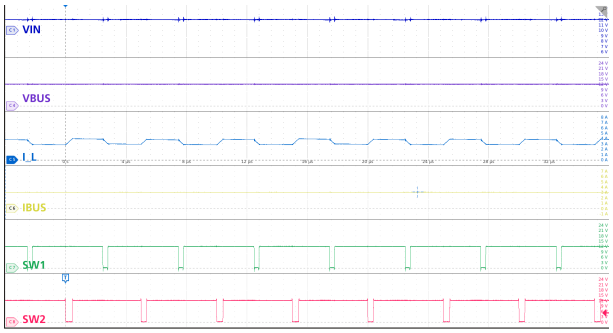
V_{IN} = 12 V V_{BUS} = 12 V I_{BUS} = 0 A

Figure 10-22. Buck-Boost Mode: V_{IN} = V_{BUS}, No Load



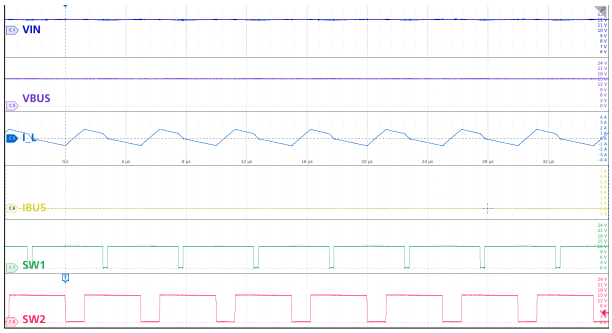
V_{IN} = 12 V V_{BUS} = 11 V I_{BUS} = 0 A

Figure 10-23. Buck-Boost Mode: VIN ≱ VBUS, No Load



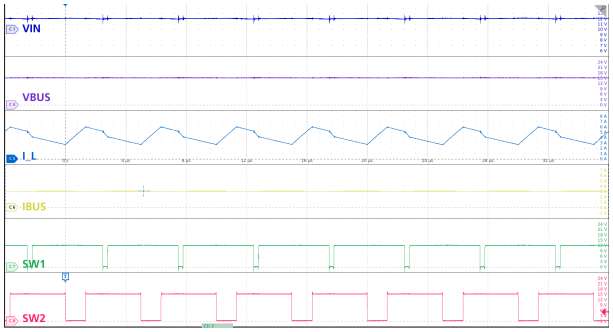
V_{IN} = 12 V V_{BUS} = 12 V I_{BUS} = 3 A

Figure 10-24. Buck-Boost Mode: V_{IN} = V_{BUS}, 3 A Load



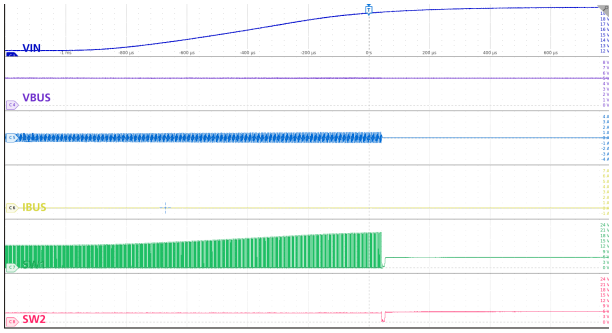
V_{IN} = 12 V V_{BUS} = 15 V I_{BUS} = 0 A

Figure 10-25. Buck-Boost Mode: Nominal V_{IN}, No Load



V_{IN} = 12 V V_{BUS} = 15 V I_{BUS} = 3 A

Figure 10-26. Buck-Boost Mode: Nominal V_{IN}, 3 A Load

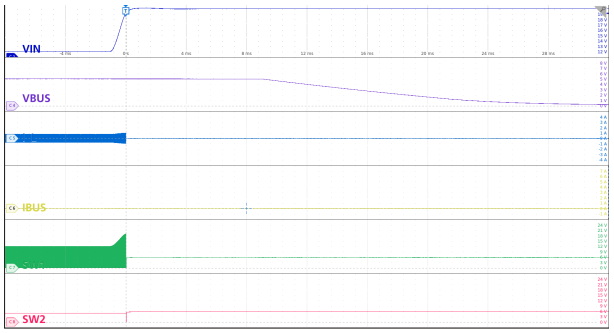


V_{IN} 12 V ➔ 20 V

Figure 10-27. $V_{IN(OVP)}$ Entry

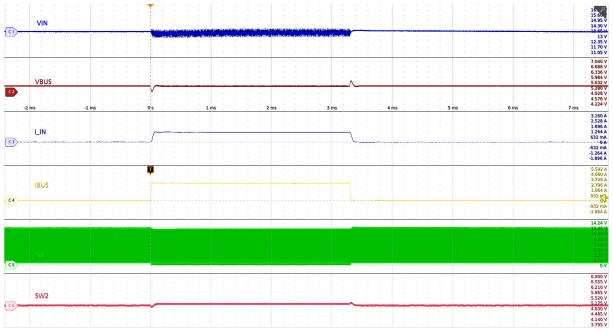
V_{IN} 20 V ➔ 12 V

Figure 10-28. $V_{IN(OVP)}$ Recovery



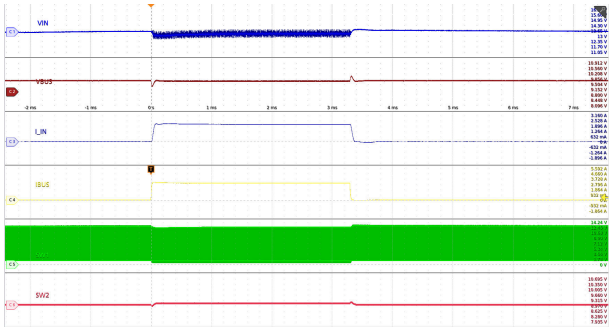
V_{IN} 12 V ➔ 20 V V_{BUS} = 0 V I_{BUS} = 0 A

Figure 10-29. $V_{IN(OVP)}$ Showing V_{BUS} Discharge



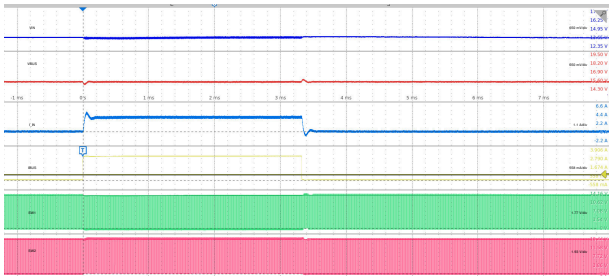
V_{IN} = 13.5V V_{BUS} = 5 V I_{BUS} 0 A ➔ 3 A

Figure 10-30. Load Transient (Buck): V_{BUS} = 5 V



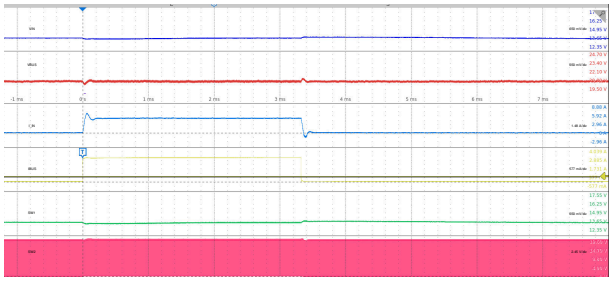
V_{IN} = 13.5V V_{BUS} = 9 V I_{BUS} 0 A ➔ 3 A

Figure 10-31. Load Transient (Buck): V_{BUS} = 9 V



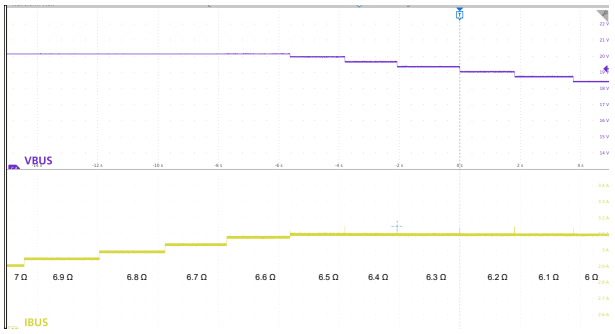
V_{IN} = 13.5V V_{BUS} = 15 V I_{BUS} 0 A ➔ 3 A

Figure 10-32. Load Transient (Buck-Boost): V_{BUS} = 15 V



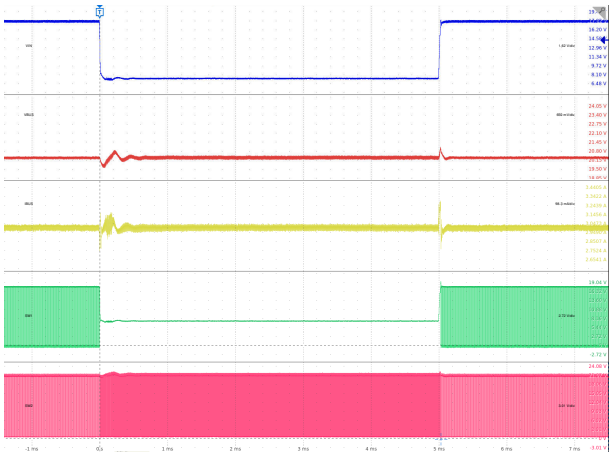
V_{IN} = 13.5V V_{BUS} = 20 V I_{BUS} 0 A ➔ 3 A

Figure 10-33. Load Transient (Boost): V_{BUS} = 20 V



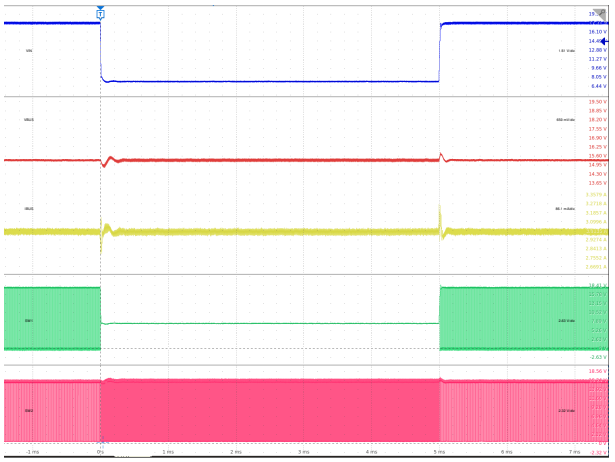
V_{IN} 12 V V_{BUS} = 20 V I_{LIMIT} = 3.1 A

Figure 10-34. Current Limit: Stepped Resistive Load



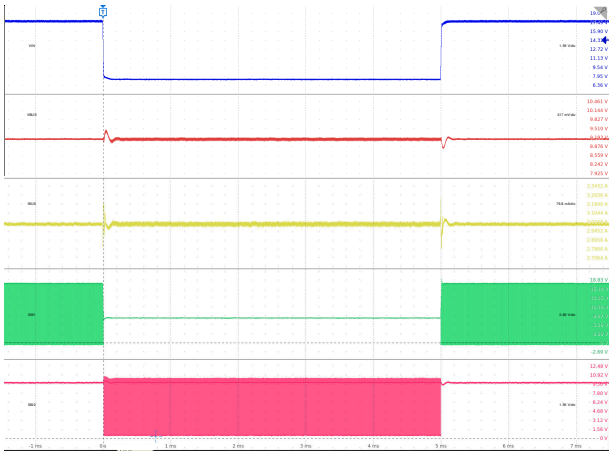
V_{IN} 7 V ➔ 18 V V_{BUS} = 20 V I_{BUS} = 3 A

Figure 10-35. Line Transient: V_{BUS} = 20 V



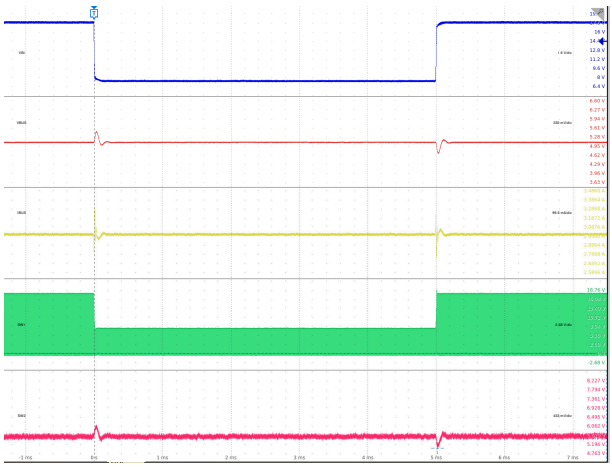
V_{IN} 7 V ➔ 18 V V_{BUS} = 15 V I_{BUS} = 3 A

Figure 10-36. Line Transient: V_{BUS} = 15 V



V_{IN} 7 V ➔ 18 V V_{BUS} = 9 V I_{BUS} = 3 A

Figure 10-37. Line Transient: V_{BUS} = 9 V



V_{IN} 7 V ➔ 18 V V_{BUS} = 5 V I_{BUS} = 3 A

Figure 10-38. Line Transient: V_{BUS} = 5 V

10.3 Power Supply Recommendations

The TPS25772-Q1 is a power management device typically operated from an automotive battery, though the power supply for the device can be any dc voltage source within the specified V_{IN} input range. The supply should be capable of supplying sufficient current based on the maximum inductor current in boost mode operation. The input supply should be bypassed with bulk capacitors at the input of the application board to avoid ringing due to parasitic impedance of the connecting cables. A typical choice is an aluminum electrolytic capacitor of 47 to 100 µF.

10.4 Layout

10.4.1 Layout Guidelines

The basic PCB board layout requires separation of sensitive signal and power paths. This checklist must be followed to get good performance for a well designed board.

- Use a combination of bulk capacitors and smaller ceramic capacitors with low series impedance for the IN, OUT, and V_{BUS} capacitors. Place the smaller capacitors closer to the IC to provide a low impedance path for high di/dt switching currents.
- Refer to Table 10-1 for suggested C_{IN} values. Place the input bypass capacitors, C_{IN} and C_{IN_HF}, as close to the IN and PGND pins as possible to minimize the loop area for input switching current in buck operation. The C_{IN_HF} capacitors should be as close as possible - see Figure 10-4. The IN and PGND pins transverse the package and it is highly recommended to split C_{IN} and C_{IN_HF} such that capacitors can be placed on either side.
- Place the output filter capacitors, C_{OUT} and C_{OUT_HF}, as close to the OUT and PGND pins as possible to minimize the loop area for output switching current in boost operation. Refer to Table 10-1 for suggested C_{OUT} and C_{OUT_HF} values.
- Place the current sense resistor and filter components. R_{SNS}, R_{CSP}, R_{CSN}, and C_{FLT}. Place the filter capacitor for the current sense signal as close to the IC CSP and CSN/BUS as possible. Use Kelvin connections between R_{SNS} through the CSP and CSN resistors and to the CSP and CSN/BUS pins to avoid creating offsets in the current sense amplifier. Avoid crossing noisy areas such as SW1 and SW2 nodes. The recommended values in Table 10-2 provide a good starting point but may require some fine adjustment to meet PPS current limit accuracy requirements. When deviating from recommended values, R_{CSP} must not be larger than 10 ohms. R_{CSN} must be 0 ohms. CFLT should not be larger than 0.33 µF.
- Place C_{BUS} between the R_{SNS} and the USB Type-C connector. See Table 10-1 for suggested C_{BUS} values. .
- Place the C_{IN}, C_{OUT}, and C_{BUS} ground connections as close as possible to the IC with thick ground trace and/or planes on multiple layers.
- Minimize the SW1 and SW2 loop areas as these are high dv/dt nodes.
- Place the LDO_5V bypass capacitors, C_{5V} and C_{5V_HF} close to the IC pin, between the LDO_5V and PGND pins. A 4.7 µF and 0.1 µF ceramic capacitors are typically used. LDO_5V supplies LDO_3V3 and LDO_1V5 as well as the low side buck and boost MOSFETs.
- Place the LDO_3V3 bypass capacitors, C_{3V3} and C_{3V3_HF} close to the IC pin, between the LDO_3V3 and AGND pins. A 4.7 µF and 0.1 µF ceramic capacitors are typically used. LDO_3V3 supplies the analog IO circuits.
- Place the LDO_1V5 bypass capacitors, C_{1V5} and C_{1V5_HF} close to the IC pin, between the LDO_1V5 and AGND pins. A 4.7 µF and 0.1 µF ceramic capacitors are typically used. LDO_3V3 supplies the Cortex M0 and digital circuits.
- Place the BOOT1 bootstrap capacitor close to the IC and connect directly to the BOOT1 to SW1 pins. For EMI mitigation, a series resistor R_{BOOT1} may be added.
- Place the BOOT2 bootstrap capacitor close to the IC and connect directly to the BOOT2 to SW2 pins. For EMI mitigation, a series resistor R_{BOOT2} may be added.
- Bypass the TVSP pin to PGND with a low ESR ceramic capacitor, C_{TVSP} located close to the IC. A 0.1 µF ceramic capacitor is typically used. R_{TVSP_DAMP} and C_{TVSP_DAMP} should be added in parallel close to C_{TVSP}. 10 Ω and 0.47 µF are recommended values.
- Use care to separate the power and signal paths so that no power or switching current flows through the AGND connections which can either corrupt the USB PD modem or GPIO signals. The PGND and AGND traces can be connected near the AGND pin.

- USB data lines, DP and DM should be differentially routed between the IC pins and USB connector. Impedance control is based on the PCB stack-up. 90 Ω differential is recommended. Route the DP and DM USB signals using a minimum of vias and corners which will reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities. Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mm.
- CC lines should be routed with a 10-mil trace to ensure the needed current for supporting powered Type-C cables through VCONN. For more information on VCONN refer to the Type-C specifications. For the 330 pF CC capacitor GND pins use a 16-mil trace if possible.
- GPIO signals can be fanned out on the top or bottom layer using either a 8-mil or 10-mil trace.

10.4.2 Layout Example

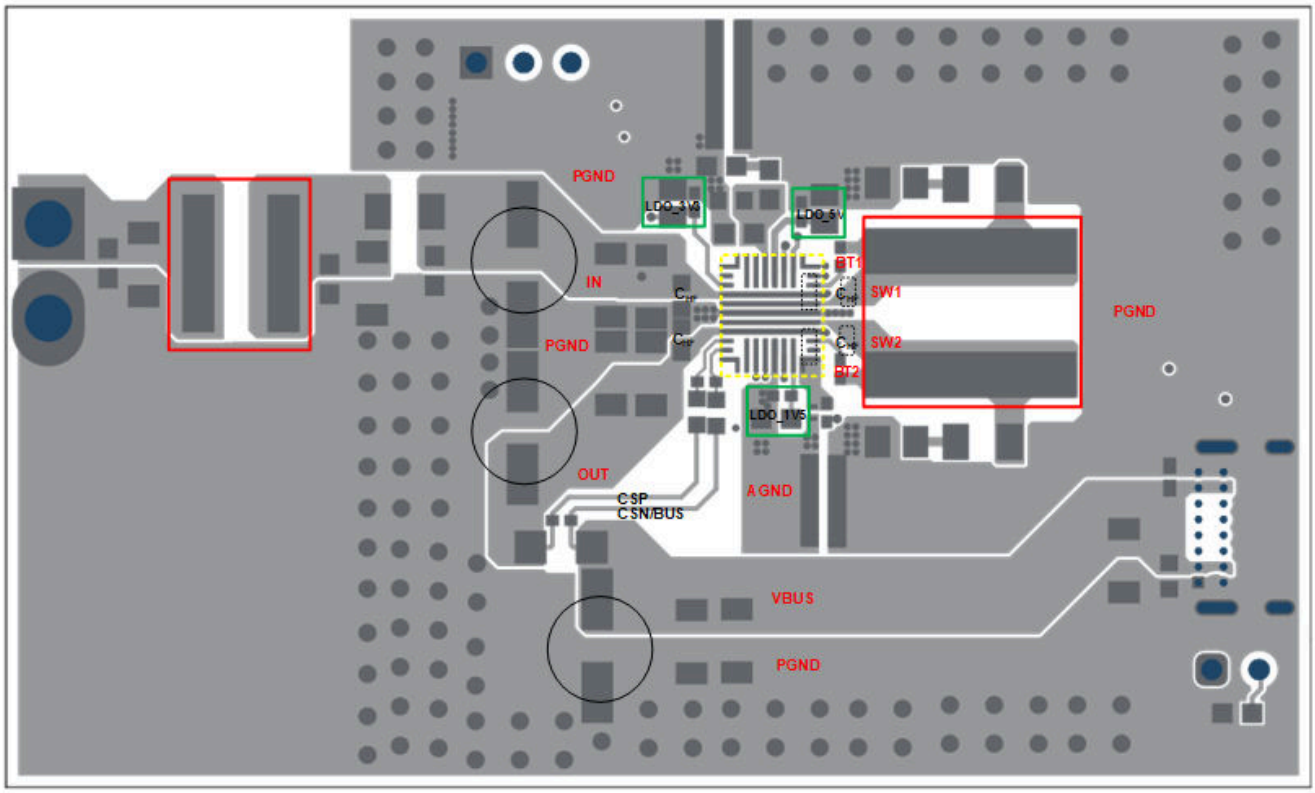


Figure 10-39. TPS25772-Q1 Power Stage Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

Please visit TI homepage for latest technical document including application notes, user guides, and reference designs.

IC Package Thermal Metrics application report, *Semiconductor and IC Package Thermal Metrics*.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS25772CAQRQLRQ1	ACTIVE	VQFN-HR	RQL	29	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS25772 CA	Samples
TPS25772CQRQLRQ1	ACTIVE	VQFN-HR	RQL	29	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS25772 C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

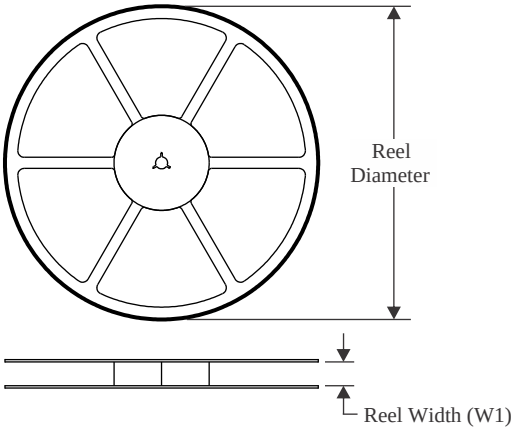
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

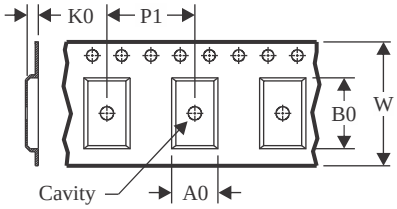
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

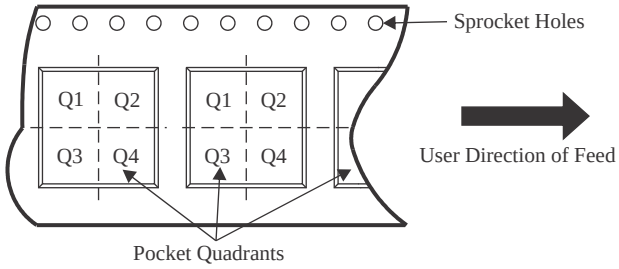


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

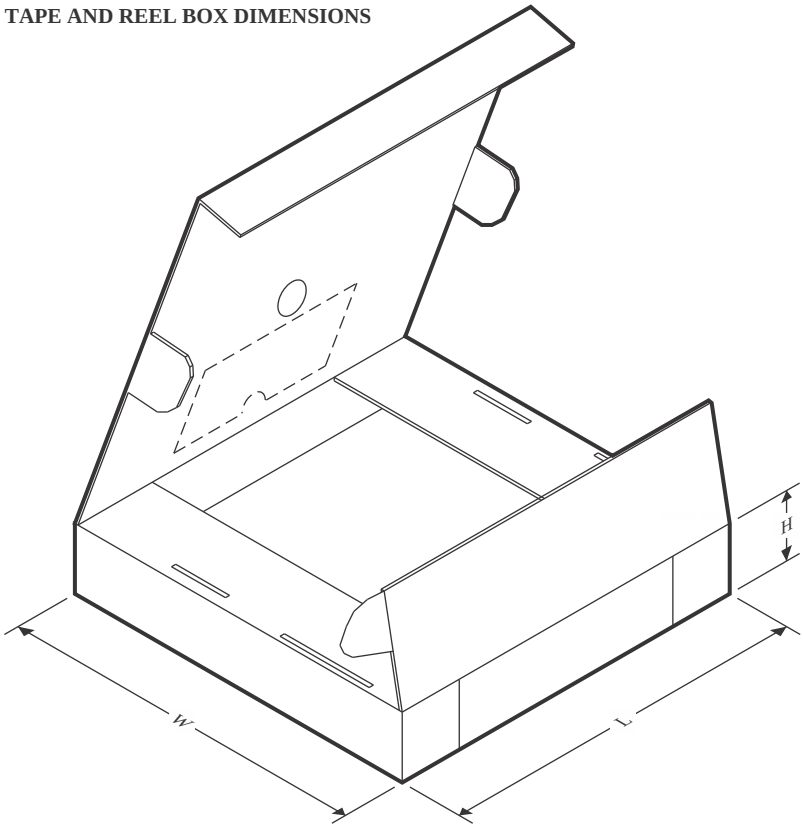
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25772CAQRQLRQ1	VQFN-HR	RQL	29	3000	330.0	12.4	5.3	6.3	1.15	8.0	12.0	Q2
TPS25772CQRQLRQ1	VQFN-HR	RQL	29	3000	330.0	12.4	5.3	6.3	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25772CAQRQLRQ1	VQFN-HR	RQL	29	3000	367.0	367.0	35.0
TPS25772CQRQLRQ1	VQFN-HR	RQL	29	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

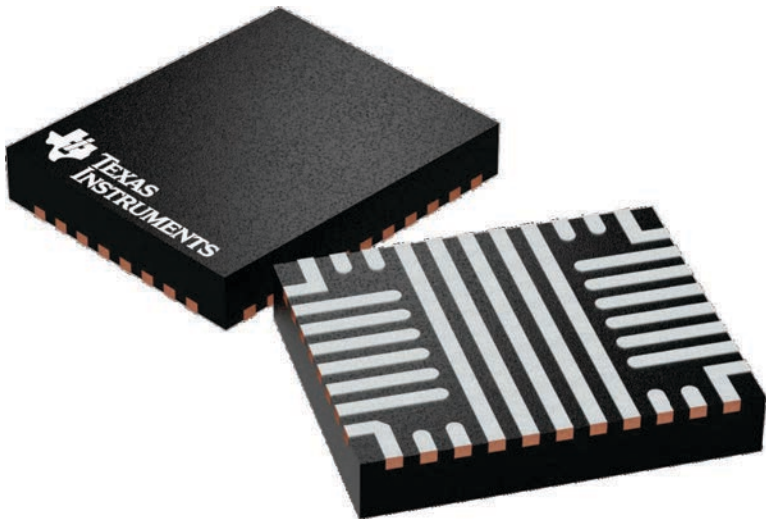
RQL 29

VQFN-HR - 1 mm max height

5 x 6, 0.5 mm pitch

VERY THIN QUAD FLATPACK-HotRod

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

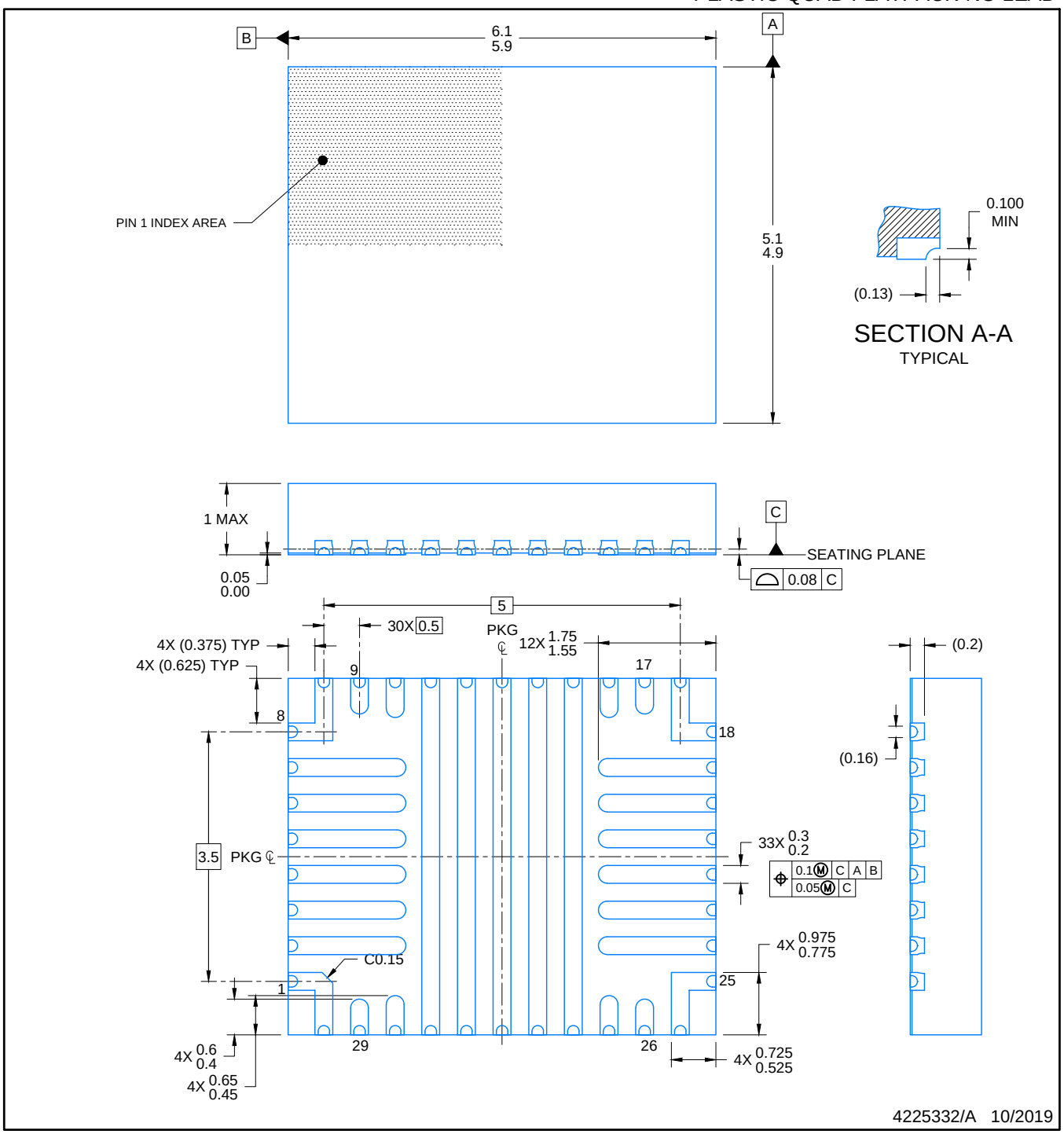


PACKAGE OUTLINE

RQL0029A

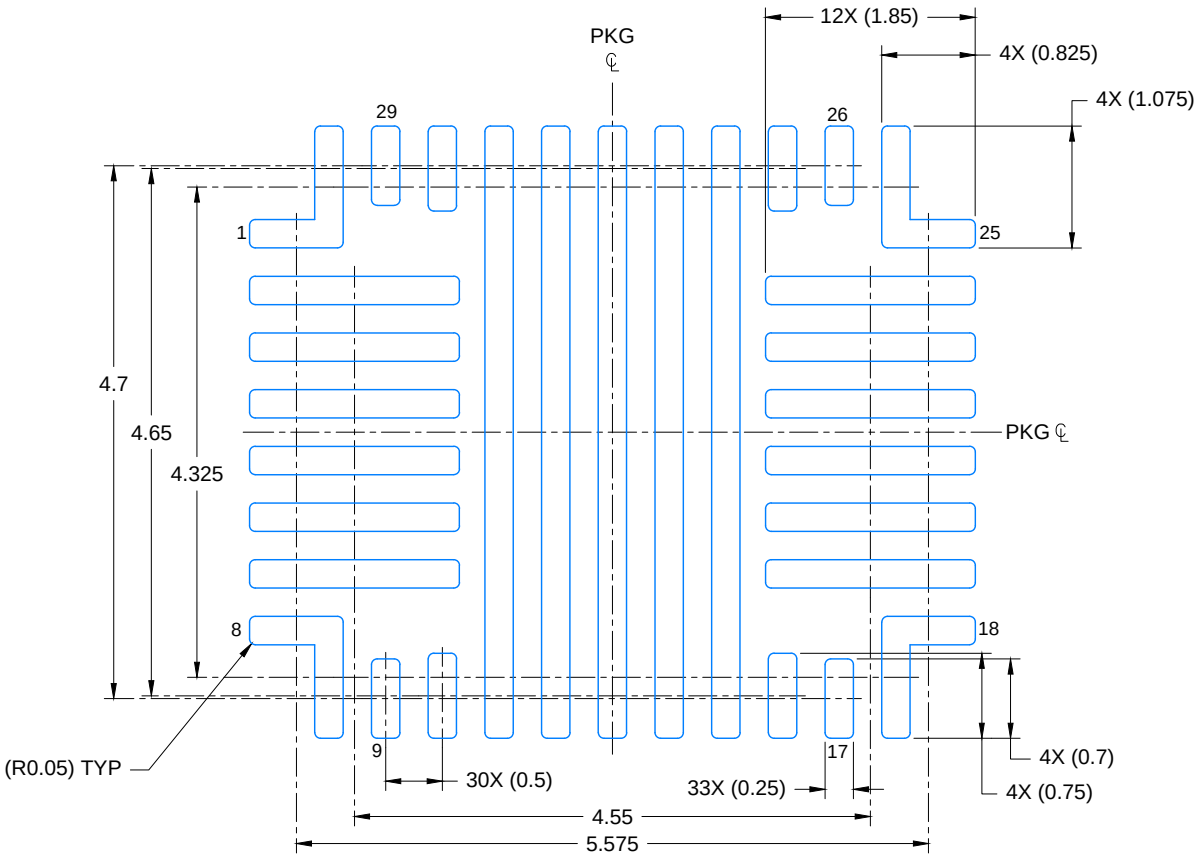
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

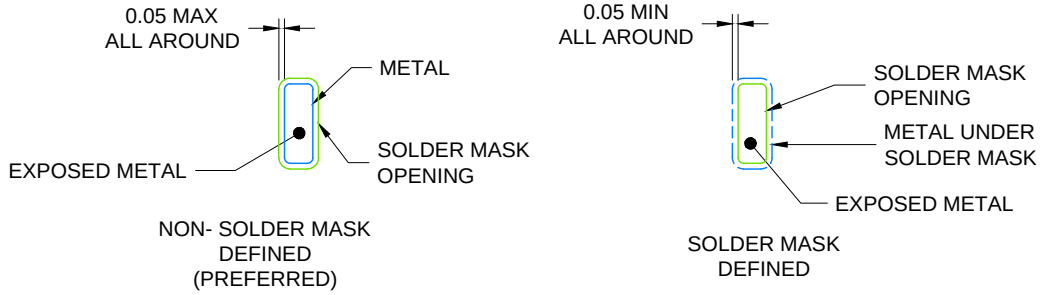
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 15X



SOLDER MASK DETAILS

NOT TO SCALE

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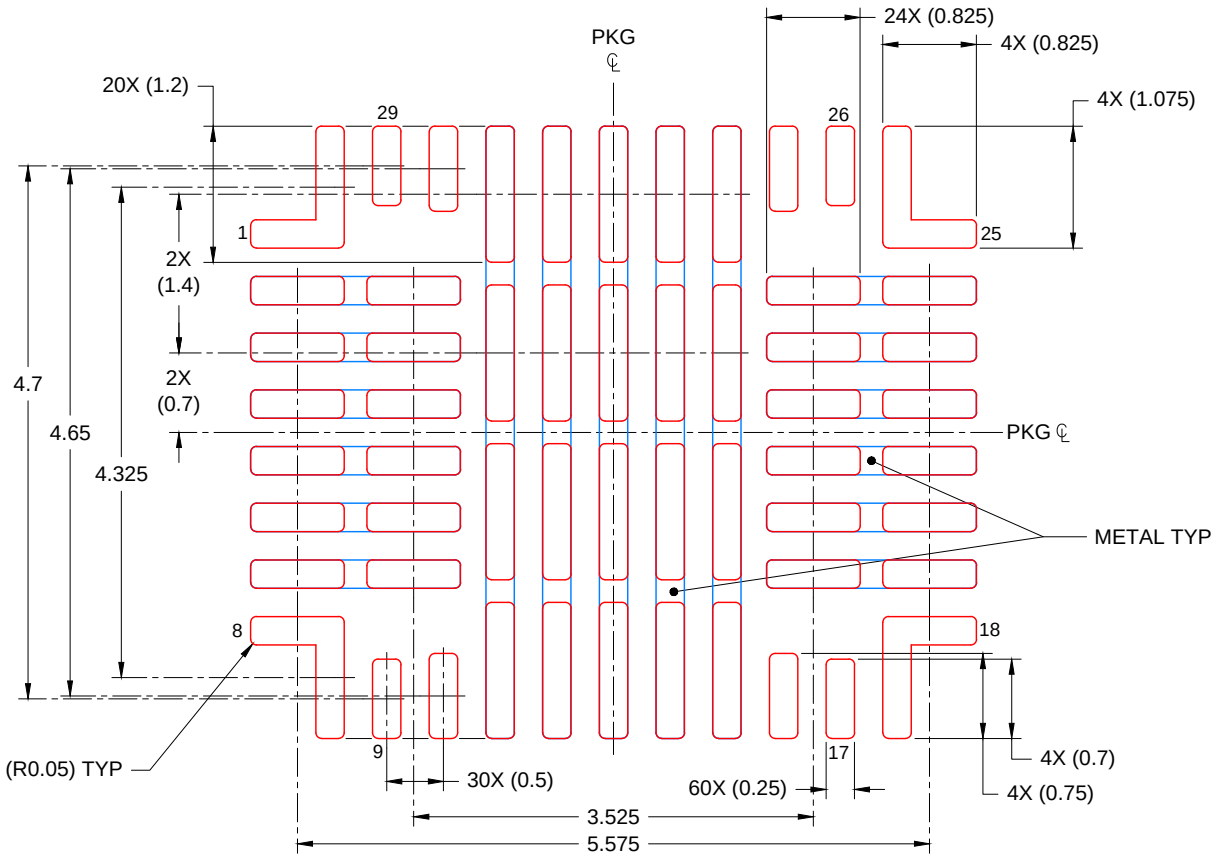
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PADS 2-7 & 19-24: 89%
PADS 11-15: 88%
SCALE: 15X

4225332/A 10/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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