1 Features
- Wide input voltage range: 2.7-V to 19-V
  - 21-V Absolute maximum
- Low On-Resistance: Ron = 89-mΩ (typical)
- Active high enable input with adjustable undervoltage lockout (UVLO)
- Overvoltage protection options available:
  - Fast overvoltage clamp (3.8-V, 5.7-V and 13.8-V pin-selectable thresholds) with a response time of 5-μs (typical)
  - Adjustable overvoltage lockout (OVLO) with a response time of 1.3-μs (typical)
- Adjustable current limit with load current monitor output (ILM)
  - Current range: 0.125-A to 2-A
  - Current limit accuracy:
    - ±10.4 % (maximum) across current range
    - ±5.5 % (maximum) at 1-A current limit
- Immune to Electrical Fast Transients (IEC 61000-4-4)
- Adjustable output slew rate control (dVdt)
- Overtemperature protection (OTP)
- Fault indication pin (FLT)
- UL 2367 recognition (pending)
- IEC 62368 CB certification (pending)
- Small footprint: 4.91 mm x 3.9 mm SOIC package

2 Applications
- Energy meters
- UL 60335-1 15-W LPC in Appliances
  - Refrigerators
  - Dishwashers
  - Washing machine and dryers
- Set-top boxes
- IP Network cameras

3 Description
The TPS2596xx family of eFuses (integrated FET hot-swap devices) is a highly integrated circuit protection and power management solution in a small package. The devices provide multiple protection modes using very few external components and are a robust defense against overloads, short circuits, voltage surges, and excessive inrush current. Output current limit level can be set with a single external resistor. It is also possible to get an accurate sense of the output load current by measuring the voltage drop across the current limit resistor. Applications with particular inrush current requirements can set the output slew rate with a single external capacitor. For the TPS25962x variants, in case of an input overvoltage condition, internal clamping circuits limit the output to a safe fixed maximum voltage (pin selectable), with no external components. The TPS25963x variants provide an option to set a user-defined overvoltage cutoff threshold.

The devices are characterized for operation over a junction temperature range of –40 °C to +125 °C.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS259620DDA</td>
<td>SOIC</td>
<td>4.91 mm x 3.9 mm</td>
</tr>
<tr>
<td>TPS259621DDA</td>
<td>SOIC</td>
<td>4.91 mm x 3.9 mm</td>
</tr>
<tr>
<td>TPS259630DDA</td>
<td>SOIC</td>
<td>4.91 mm x 3.9 mm</td>
</tr>
<tr>
<td>TPS259631DDA</td>
<td>SOIC</td>
<td>4.91 mm x 3.9 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
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4 Revision History

Changes from Original (May 2019) to Revision A

• Change from Advance Information to Production Data ................................................................. 1
## 5 Device Comparison Table

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Overvoltage Response</th>
<th>Response to Thermal Shutdown (TSD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS259620</td>
<td>OVC - 3.8 V, 5.7 V, 13.8 V (Pin Selectable)</td>
<td>Latch-off</td>
</tr>
<tr>
<td>TPS259621</td>
<td>OVC - 3.8 V, 5.7 V, 13.8 V (Pin Selectable)</td>
<td>Auto-retry</td>
</tr>
<tr>
<td>TPS259630</td>
<td>Adjustable OVLO</td>
<td>Latch-off</td>
</tr>
<tr>
<td>TPS259631</td>
<td>Adjustable OVLO</td>
<td>Auto-retry</td>
</tr>
</tbody>
</table>
6 Pin Configuration and Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>1</td>
<td>Ground</td>
</tr>
<tr>
<td>dVdt</td>
<td>2</td>
<td>Analog Output A capacitor from this pin to GND sets the output turn on slew rate. Leave this pin floating for the fastest turn on slew rate.</td>
</tr>
<tr>
<td>EN/UVLO</td>
<td>3</td>
<td>Analog Input Active High Enable for the Device. A resistor divider can be used to adjust the Undervoltage Lockout threshold. Do not leave floating.</td>
</tr>
<tr>
<td>IN</td>
<td>4</td>
<td>Power</td>
</tr>
<tr>
<td>OUT</td>
<td>5</td>
<td>Power</td>
</tr>
<tr>
<td>FLT</td>
<td>6</td>
<td>Digital Output Active Low indicator which will be pulled low when a fault is detected. It is an open-drain output that requires an external pull-up resistance.</td>
</tr>
<tr>
<td>ILM</td>
<td>7</td>
<td>Analog Output This is a dual function pin used to limit and monitor the output current. An external resistor from this pin to GND sets the output current limit. The pin voltage can also be used to monitor the output load current.</td>
</tr>
<tr>
<td>OVLO</td>
<td>8</td>
<td>Analog Input TPS25963x: A resistor divider can be used to adjust the Overvoltage Lockout threshold. Do not leave floating.</td>
</tr>
<tr>
<td>OVCSEL</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

TPS25962x: Overvoltage Clamp level select pin. Refer to Overvoltage Clamp for more details.

Thermal pad | Ground The Exposed Pad is used primarily for heat dissipation and must be connected to system ground plane for best thermal performance.
7 Specifications

7.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>PIN</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{IN}})</td>
<td>(\text{IN})</td>
<td>(-0.3)</td>
<td>21</td>
<td>V</td>
</tr>
<tr>
<td>Maximum Input Voltage Range</td>
<td>(\text{IN})</td>
<td>(-0.3)</td>
<td>22</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{OUT}})</td>
<td>(\text{OUT})</td>
<td>(-0.3)</td>
<td>(\min (21, V_{\text{IN}} + 0.3))</td>
<td>V</td>
</tr>
<tr>
<td>Maximum Output Voltage Range</td>
<td>(\text{OUT})</td>
<td>(-0.3)</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{EN/UVLO}})</td>
<td>(\text{EN/UVLO})</td>
<td>(-0.3)</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Maximum Enable Pin Voltage Range</td>
<td>(\text{EN/UVLO})</td>
<td>(-0.3)</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{OV}})</td>
<td>(\text{OVCSEL/OVLO})</td>
<td>(-0.3)</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Maximum OVCSEL/OVLO Voltage Range</td>
<td>(\text{OVCSEL/OVLO})</td>
<td>(-0.3)</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{dVdT}})</td>
<td>(\text{DVDT})</td>
<td>2.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Maximum (dV/dt) Pin Voltage Range</td>
<td>(\text{DVDT})</td>
<td>(-0.3)</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>(I_{\text{FLTB}})</td>
<td>(\text{FLT})</td>
<td>10</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Maximum FLTB Pin Voltage Range</td>
<td>(\text{FLT})</td>
<td>(-0.3)</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>(I_{\text{ILM}})</td>
<td>(\text{ILM})</td>
<td>453</td>
<td>7869</td>
<td>(\Omega)</td>
</tr>
<tr>
<td>ILM Pin Resistance</td>
<td>(\text{ILM})</td>
<td>453</td>
<td>7869</td>
<td>(\Omega)</td>
</tr>
<tr>
<td>(I_{\text{MAX}})</td>
<td>(\text{IN to OUT})</td>
<td>Internally Limited</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Maximum Continuous Switch Current</td>
<td>(\text{IN to OUT})</td>
<td>Internally Limited</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>(T_{\text{J}})</td>
<td></td>
<td>(-65)</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

<table>
<thead>
<tr>
<th>(V_{\text{ESD}})</th>
<th>Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human body model (HBM), per</td>
<td></td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>ANSI/ESDA/JEDEC JS-001, all pins(^{(1)})</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Charged device model (CDM), per JEDEC specification/JESD22-C101, all pins(^{(2)})</td>
<td></td>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>PIN</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{IN}})</td>
<td>(\text{IN})</td>
<td>2.7</td>
<td>19(^{(1)})</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>(\text{IN})</td>
<td>2.7</td>
<td>19(^{(1)})</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{OUT}})</td>
<td>(\text{OUT})</td>
<td>(V_{\text{IN}} + 0.3)</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output Voltage Range</td>
<td>(\text{OUT})</td>
<td>(V_{\text{IN}} + 0.3)</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{\text{EN/UVLO}})</td>
<td>(\text{EN/UVLO})</td>
<td>(V_{\text{IN}} + 0.3)</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Enable Pin Voltage Range</td>
<td>(\text{EN/UVLO})</td>
<td>(V_{\text{IN}} + 0.3)</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{\text{OV}})</td>
<td>(\text{OVLO})</td>
<td>0.5</td>
<td>2</td>
<td>V</td>
</tr>
<tr>
<td>OVLO Pin Voltage Range (TPS25963x Only)</td>
<td>(\text{OVLO})</td>
<td>0.5</td>
<td>2</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{dVdT}})</td>
<td>(\text{DVDT})</td>
<td>4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>dV/dt Pin Capacitor Voltage Rating</td>
<td>(\text{DVDT})</td>
<td>4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{\text{FLTB}})</td>
<td>(\text{FLT})</td>
<td>6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>FLTB Pin Voltage Range</td>
<td>(\text{FLT})</td>
<td>6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(R_{\text{ILM}})</td>
<td>(\text{ILM})</td>
<td>453</td>
<td>7869</td>
<td>(\Omega)</td>
</tr>
<tr>
<td>ILM Pin Resistance</td>
<td>(\text{ILM})</td>
<td>453</td>
<td>7869</td>
<td>(\Omega)</td>
</tr>
<tr>
<td>(I_{\text{MAX}})</td>
<td>(\text{IN to OUT})</td>
<td>Internally Limited</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Continuous Switch Current</td>
<td>(\text{IN to OUT})</td>
<td>Internally Limited</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>(T_{\text{J}})</td>
<td></td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) For TPS25962x, the input voltage should be limited to the selected Output Voltage Clamp Option as listed in the Electrical Characteristics section
(2) For supply voltages below 6V, it is okay to pull up the EN pin to IN through a resistor of 100 KΩ or higher. For supply voltages greater than 6V, it is recommended to use an appropriate resistor divider between IN, EN and GND to ensure the voltage at the EN pin is within the specified limits.
### 7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TPS2596X DDA (SOIC-EP)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>R&lt;sub&gt;θJA&lt;/sub&gt;</td>
<td>Junction-to-ambient thermal resistance</td>
<td>52.7&lt;sup&gt;(2)&lt;/sup&gt;</td>
</tr>
<tr>
<td>R&lt;sub&gt;θJA&lt;/sub&gt;</td>
<td>Junction-to-ambient thermal resistance</td>
<td>119.8&lt;sup&gt;(3)&lt;/sup&gt;</td>
</tr>
<tr>
<td>Ψ&lt;sub&gt;JT&lt;/sub&gt;</td>
<td>Junction-to-top characterization parameter</td>
<td>8.9&lt;sup&gt;(2)&lt;/sup&gt;</td>
</tr>
<tr>
<td>Ψ&lt;sub&gt;JT&lt;/sub&gt;</td>
<td>Junction-to-top characterization parameter</td>
<td>17.5&lt;sup&gt;(3)&lt;/sup&gt;</td>
</tr>
<tr>
<td>Ψ&lt;sub&gt;JB&lt;/sub&gt;</td>
<td>Junction-to-board characterization parameter</td>
<td>27.1&lt;sup&gt;(2)&lt;/sup&gt;</td>
</tr>
<tr>
<td>Ψ&lt;sub&gt;JB&lt;/sub&gt;</td>
<td>Junction-to-board characterization parameter</td>
<td>68.1&lt;sup&gt;(3)&lt;/sup&gt;</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) With exposed pad soldered to PCB
(3) Without exposed pad soldered to PCB

### 7.5 Electrical Characteristics

(Test conditions unless otherwise noted) –40°C ≤ T<sub>J</sub> ≤ 125°C, V<sub>IN</sub> = 12 V , R<sub>ILM</sub> = 453 Ω , C<sub>UV</sub> = Open, OUT = Open. All voltages referenced to GND.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT SUPPLY (IN)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;Q&lt;/sub&gt;</td>
<td>IN quiescent current</td>
<td>TPS25963x</td>
<td>193</td>
<td>259</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>TPS25962x</td>
<td>206</td>
<td>266</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;SD&lt;/sub&gt;</td>
<td>IN Shutdown Current</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; &lt; 4 V, V&lt;sub&gt;EN/UVLO&lt;/sub&gt; &lt; V&lt;sub&gt;SD&lt;/sub&gt;</td>
<td>0.1</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; ≥ 4 V, V&lt;sub&gt;EN/UVLO&lt;/sub&gt; &lt; V&lt;sub&gt;SD&lt;/sub&gt;</td>
<td>0.4</td>
<td>1.132</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;UVP(R)&lt;/sub&gt;</td>
<td>IN Undervoltage Protection threshold</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; Rising</td>
<td>2.46</td>
<td>2.53</td>
<td>2.58</td>
</tr>
<tr>
<td>V&lt;sub&gt;UVP(F)&lt;/sub&gt;</td>
<td>IN Undervoltage Protection</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; Falling</td>
<td>2.36</td>
<td>2.42</td>
<td>2.46</td>
</tr>
<tr>
<td></td>
<td>Hysteresis</td>
<td>110</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>OUTPUT VOLTAGE CLAMP (OUT) - TPS25962X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;OVC&lt;/sub&gt;</td>
<td>Overvoltage Clamp Threshold</td>
<td>R&lt;sub&gt;OVCSEL&lt;/sub&gt; = Short to GND, R&lt;sub&gt;OUT&lt;/sub&gt; = 10 KΩ</td>
<td>3.75</td>
<td>3.83</td>
<td>3.92</td>
</tr>
<tr>
<td></td>
<td>R&lt;sub&gt;OVCSEL&lt;/sub&gt; = 400 KΩ to GND, R&lt;sub&gt;OUT&lt;/sub&gt; = 10 KΩ</td>
<td>5.54</td>
<td>5.69</td>
<td>5.83</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>R&lt;sub&gt;OVCSEL&lt;/sub&gt; = OPEN, R&lt;sub&gt;OUT&lt;/sub&gt; = 10 KΩ</td>
<td>12.97</td>
<td>13.77</td>
<td>14.52</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;CLAMP&lt;/sub&gt;</td>
<td>Output Voltage During Clamping</td>
<td>R&lt;sub&gt;OVCSEL&lt;/sub&gt; = Short to GND, I&lt;sub&gt;OUT&lt;/sub&gt; = 10 mA</td>
<td>3.47</td>
<td>3.59</td>
<td>3.7</td>
</tr>
<tr>
<td></td>
<td>R&lt;sub&gt;OVCSEL&lt;/sub&gt; = 400 KΩ to GND, I&lt;sub&gt;OUT&lt;/sub&gt; = 10 mA</td>
<td>5.28</td>
<td>5.45</td>
<td>5.61</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>R&lt;sub&gt;OVCSEL&lt;/sub&gt; = OPEN, I&lt;sub&gt;OUT&lt;/sub&gt; = 10 mA</td>
<td>13.13</td>
<td>13.58</td>
<td>13.97</td>
<td>V</td>
</tr>
<tr>
<td>OUTPUT CURRENT LIMIT AND MONITOR (ILM)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G&lt;sub&gt;MON&lt;/sub&gt;</td>
<td>Current monitor gain as measured on ILM pin (I&lt;sub&gt;ILM&lt;/sub&gt; / I&lt;sub&gt;OUT&lt;/sub&gt;)</td>
<td>I&lt;sub&gt;OUT&lt;/sub&gt; = 0.13 A</td>
<td>531.22</td>
<td>653.21</td>
<td>800.00</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I&lt;sub&gt;OUT&lt;/sub&gt; = 2 A</td>
<td>635.77</td>
<td>657.15</td>
<td>684.05</td>
</tr>
<tr>
<td>I&lt;sub&gt;ILM&lt;/sub&gt;</td>
<td>I&lt;sub&gt;OUT&lt;/sub&gt; Current Limit</td>
<td>R&lt;sub&gt;ILM&lt;/sub&gt; = 7.87 KΩ, V&lt;sub&gt;DS&lt;/sub&gt; = 0.5 V, –40°C ≤ T&lt;sub&gt;A&lt;/sub&gt; ≤ 80°C</td>
<td>0.113</td>
<td>0.125</td>
<td>0.139</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R&lt;sub&gt;ILM&lt;/sub&gt; = 3.83 KΩ, V&lt;sub&gt;DS&lt;/sub&gt; = 0.5 V</td>
<td>0.224</td>
<td>0.247</td>
<td>0.269</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R&lt;sub&gt;ILM&lt;/sub&gt; = 909 Ω, V&lt;sub&gt;DS&lt;/sub&gt; = 0.5 V</td>
<td>0.949</td>
<td>1.005</td>
<td>1.051</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R&lt;sub&gt;ILM&lt;/sub&gt; = 453 Ω, V&lt;sub&gt;DS&lt;/sub&gt; = 0.5 V</td>
<td>1.83</td>
<td>2.004</td>
<td>2.147</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R&lt;sub&gt;ILM&lt;/sub&gt; = OPEN</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;CB&lt;/sub&gt;</td>
<td>I&lt;sub&gt;OUT&lt;/sub&gt; Circuit Breaker Threshold during R&lt;sub&gt;ILM&lt;/sub&gt; Short condition</td>
<td>R&lt;sub&gt;ILM&lt;/sub&gt; = Short to GND (Single Point Failure Test IEC 62368-1)</td>
<td>1.5</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Electrical Characteristics (continued)

(Test conditions unless otherwise noted) \(-40^\circ C \leq T_J \leq 125^\circ C, V_{IN} = 12 \, V, R_{ILM} = 453 \, \Omega, C_{dVT} = \) Open, \(OUT = \) Open. All voltages referenced to GND.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{ON})</td>
<td>ON State Resistance</td>
<td>(V_{IN} &lt; 4 , V, I_{OUT} = 0.2 , A, T_J = 25 , ^\circ C)</td>
<td>97</td>
<td>99.8</td>
<td>(\mu\Omega)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{IN} &lt; 4 , V, I_{OUT} = 0.2 , A, T_J = -40 \text{ to } 85 , ^\circ C)</td>
<td>125.4</td>
<td>(\mu\Omega)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{IN} &lt; 4 , V, I_{OUT} = 0.2 , A, T_J = -40 \text{ to } 125 , ^\circ C)</td>
<td>143.4</td>
<td>(\mu\Omega)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{IN} &gt; 4 , V, I_{OUT} = 0.2 , A, T_J = 25 , ^\circ C)</td>
<td>89</td>
<td>92.6</td>
<td>(\mu\Omega)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{IN} &gt; 4 , V, I_{OUT} = 0.2 , A, T_J = -40 \text{ to } 85 , ^\circ C)</td>
<td>115.3</td>
<td>(\mu\Omega)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{IN} &gt; 4 , V, I_{OUT} = 0.2 , A, T_J = -40 \text{ to } 125 , ^\circ C)</td>
<td>131</td>
<td>(\mu\Omega)</td>
<td></td>
</tr>
</tbody>
</table>

**ENABLE/UNDEVROLTAGE LOCK OUT (EN/UVLO)**

- \(V_{UVLO(R)}\) UVLO Threshold
  - \(V_{EN}\) Rising
    - \(V_{EN}\) Failing
  - UVLO Hysteresis
    - 95 \(\mu\V\)

- \(V_{SD}\) \(V_{EN}\) threshold for lowest shutdown current
  - \(V_{EN}\) Failing
    - 0.53 \(V\)
    - 1.05 \(V\)

- \(I_{ENLKG}\) EN leakage current
  - –0.1 \(\mu\A\)
    - 0.1 \(\mu\A\)

**OVERVOLTAGE LOCKOUT (OVLO) - TPS25963X**

- \(V_{OVLO(R)}\) OVLO Threshold
  - \(V_{OVLO}\) Rising
    - \(V_{OVLO}\) Failing
  - OVLO Hysteresis
    - 95 \(\mu\V\)

- \(I_{OVLKG}\) OVLO pin leakage current
  - \(0.5 \leq V_{OVLO} \leq 1.5\, V\)
    - –0.1 \(\mu\A\)
    - 0.1 \(\mu\A\)

**FAULT INDICATION (FLT)**

- \(R_{FLT}\) FLT Internal Pull-down resistance
  - FLT asserted
    - 11.52 \(\Omega\)

- \(I_{FLTlKG}\) FLT pin leakage current
  - FLT de-asserted, pull-up voltage 6 \(V\)
    - –1 \(\mu\A\)
    - 1 \(\mu\A\)

**OVERTEMPERATURE PROTECTION (OTP)**

- \(T_{SD}\) Thermal Shutdown Rising Threshold
  - \(T_J\) Rising
    - 157 \(^\circ\C\)

- \(T_{SDHYS}\) Thermal Shutdown Hysteresis
  - \(T_J\) Falling
    - 11.5 \(^\circ\C\)

**DVDT**

- \(I_{DVDT}\) dVdt Pin Charging Current
  - 1.89 \(\mu\A\)
  - 2.11 \(\mu\A\)
  - 2.33 \(\mu\A\)

- \(Q_{DVDT}\) DVDT gain
  - 20.31 \(V\)
  - 20.93 \(V\)
  - 21.5 \(V\)
7.6 Timing Requirements

Typical Values are taken at $T_J = 25^\circ C$ unless specifically noted otherwise.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_LIM$</td>
<td>Current limit response time</td>
<td>87</td>
<td></td>
<td></td>
<td>$\mu s$</td>
</tr>
<tr>
<td>$t_{SC}$</td>
<td>Short circuit response time</td>
<td>5</td>
<td></td>
<td></td>
<td>$\mu s$</td>
</tr>
<tr>
<td>$t_{OVLO}$</td>
<td>Overvoltage lockout response time</td>
<td>1.3</td>
<td></td>
<td></td>
<td>$\mu s$</td>
</tr>
<tr>
<td>$t_{OVC}$</td>
<td>Output clamp response time</td>
<td>5</td>
<td></td>
<td></td>
<td>$\mu s$</td>
</tr>
<tr>
<td>$t_{TSD,RST}$</td>
<td>Thermal Shutdown Auto-Retry Interval</td>
<td>95</td>
<td></td>
<td></td>
<td>$ms$</td>
</tr>
</tbody>
</table>

7.7 Switching Characteristics

The output rising slew rate is internally controlled and constant across the entire operating voltage range to ensure the turn-on timing is not affected by the load conditions. The rising slew rate can be adjusted by adding capacitance from the dVdt pin to ground. As $C_{dVdt}$ is increased, it will slow the rising slew rate (SR). See Slew Rate and Inrush Current Control (dVdt) section for more details. The fall time, however, is dependent on the RC time constant of the load capacitance ($C_{OUT}$) and Load Resistance ($R_L$). The Switching Characteristics are only valid for the power-up sequence where the supply is available in steady state condition and the load voltage is completely discharged before the device is enabled. Typical Values are taken at $T_J = 25^\circ C$ unless specifically noted otherwise. $R_{OUT} = 100 \Omega$, $C_{OUT} = 1 \mu F$.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>$V_{IN}$</th>
<th>$C_{dVdt} = $ Open</th>
<th>$C_{dVdt} = $ 3300pF</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>SR$_{ON}$</td>
<td>2.7 V</td>
<td>28.9</td>
<td>12.1</td>
<td>V/\mu s</td>
</tr>
<tr>
<td></td>
<td>5 V</td>
<td>42.7</td>
<td>13.1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>12 V</td>
<td>75.1</td>
<td>13.6</td>
<td></td>
</tr>
<tr>
<td>$t_{ON}$</td>
<td>2.7 V</td>
<td>77.5</td>
<td>216.5</td>
<td>$\mu s$</td>
</tr>
<tr>
<td></td>
<td>5 V</td>
<td>78.9</td>
<td>247.3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>12 V</td>
<td>82.9</td>
<td>314.9</td>
<td></td>
</tr>
<tr>
<td>tr</td>
<td>2.7 V</td>
<td>74.7</td>
<td>182.4</td>
<td>$\mu s$</td>
</tr>
<tr>
<td></td>
<td>5 V</td>
<td>94.1</td>
<td>311.0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>12 V</td>
<td>128.4</td>
<td>707.8</td>
<td></td>
</tr>
<tr>
<td>$t_{ON}$</td>
<td>2.7 V</td>
<td>152.2</td>
<td>398.9</td>
<td>$\mu s$</td>
</tr>
<tr>
<td></td>
<td>5 V</td>
<td>173</td>
<td>558.4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>12 V</td>
<td>211.3</td>
<td>1022.7</td>
<td></td>
</tr>
<tr>
<td>$t_{OFF}$</td>
<td>2.7 V</td>
<td>12.2</td>
<td>12.3</td>
<td>$\mu s$</td>
</tr>
<tr>
<td></td>
<td>5 V</td>
<td>11.6</td>
<td>11.9</td>
<td></td>
</tr>
<tr>
<td></td>
<td>12 V</td>
<td>10.3</td>
<td>10.4</td>
<td></td>
</tr>
</tbody>
</table>
Figure 1. TPS2596xx Switching Times
7.8 Typical Characteristics

Figure 2. TPS25963x Quiescent Current

Figure 3. TPS25962x Quiescent Current

Figure 4. TPS25962x Quiescent Current During Overvoltage Clamping

Figure 5. Disabled State Current

Figure 6. Shutdown Current

Figure 7. ON Resistance
Typical Characteristics (continued)

Figure 8. IN Supply Undervoltage Threshold

Figure 9. EN/UVLO Disable Threshold

Figure 10. EN/UVLO Shutdown Threshold for Lowest Current Consumption

Figure 11. EN/UVLO Pin Leakage Current

Figure 12. TPS2596x Overvoltage Lockout Threshold

Figure 13. TPS2596x OVLO Pin Leakage Current
Typical Characteristics (continued)

Figure 14. TPS25962x Overvoltage Clamp Threshold

Figure 15. TPS25962x Overvoltage Clamping Voltage

Figure 16. TPS25962x Overvoltage Clamping Voltage

Figure 17. TPS25962x Overvoltage Clamping Voltage

Figure 18. DVDT Charging Current

Figure 19. DVDT Gain
Typical Characteristics (continued)

Figure 20. Current Limit vs RILM

Figure 21. Current Limit Accuracy

Figure 22. Current Limit Foldback

Figure 23. Current Limit Foldback

Figure 24. Current Monitor Gain

Figure 25. Current Monitor Accuracy
Typical Characteristics (continued)

1- Layer PCB: 2 oz Cu with GND Plane area: 4.43 cm² (Top)

Figure 26. Thermal Shutdown Plot

2- Layer PCB: 2 oz Cu with GND Plane area: 4.93 cm² (Top) and 1.07 cm² (Bottom)

Figure 27. Thermal Shutdown Plot

Figure 28. Input Hotplug Response

VIN = 12 V, COUT = 220 μF, RILM = 453 Ω

Figure 29. Output Voltage Ramp and Inrush Current at Start
Up, Cdvdt = 2200 pF

VIN = 12 V, COUT = 10 μF, RILM = 453 Ω, Cdvdt = 2200 pF

Figure 30. Output Voltage Ramp and Inrush Current at Start
Up, Cdvdt = OPEN

VIN = 12 V, COUT = 10 μF, RILM = 453 Ω, Cdvdt = OPEN

Figure 31. Turn ON with EN

VIN = 12 V, VEN = 3.3 V
Typical Characteristics (continued)

**Figure 32. Turn ON with VIN**

$V_{IN} = 12 \, \text{V}, \, V_{EN} = 3.3 \, \text{V}$

**Figure 33. Overcurrent Response**

$V_{IN} = 12 \, \text{V}, \, R_{ILM} = 453 \, \Omega, \, R_{OUT} \text{ Varied From } 8.33 \, \Omega \text{ to } 4.54 \, \Omega$

**Figure 34. Thermal Shutdown Latch-off Response - TPS2596x0**

$V_{IN} = 12 \, \text{V}, \, R_{ILM} = 453 \, \Omega, \, R_{OUT} = 5 \, \Omega$

**Figure 35. Thermal Shutdown Auto-Retry Response - TPS2596x1**

$V_{IN} = 12 \, \text{V}, \, R_{ILM} = 453 \, \Omega, \, R_{OUT} = 5 \, \Omega$

**Figure 36. Short-Circuit While ON Response**

$V_{IN} = 12 \, \text{V}, \, R_{ILM} = 453 \, \Omega$

**Figure 37. Short-Circuit While ON Response (Zoomed In)**

$V_{IN} = 12 \, \text{V}, \, R_{ILM} = 453 \, \Omega$
Typical Characteristics (continued)

**Figure 38. Power Up Into Short-Circuit**

- $V_{IN} = 12\,\text{V}$, $R_{ILM} = 453\,\Omega$

**Figure 39. Power Up Into Short-Circuit (Zoomed In)**

- $V_{IN} = 12\,\text{V}$, $R_{ILM} = 453\,\Omega$

**Figure 40. TPS25963x Overvoltage Lockout Response**

- $V_{IN}$ increased from 12 V to 15 V

**Figure 41. TPS25962x Overvoltage Clamp Response**

- OVCSEL = Shorted to GND, $V_{IN}$ increased from 3 V to 5 V

**Figure 42. TPS25962x Overvoltage Clamp Response**

- OVCSEL = 400 K$\Omega$ to GND, $V_{IN}$ increased from 5 V to 7 V

**Figure 43. TPS25962x Overvoltage Clamp Response**

- OVCSEL = OPEN, $V_{IN}$ increased from 12 V to 14 V
8 Detailed Description

8.1 Overview

The TPS2596xx is an integrated eFuse device that is used to manage load voltage and load current. The device provides various factory programmed settings and user manageable settings, which allow device configuration for handling different transient and steady state supply and load fault conditions, thereby protecting the input supply and the downstream circuits connected to the device. The device also uses an in-built thermal shutdown mechanism to protect itself during these fault events.

8.2 Functional Block Diagram

* Only for Auto-Retry Variant (TPS259621)
8.3 Feature Description

8.3.1 Undervoltage Protection (UVP) and Undervoltage Lockout (UVLO)

TPS2596xx constantly monitors the input supply to ensure that the load is powered up only when the voltage is at a sufficient level. During the start-up condition, the device waits for the input supply to rise above an internal fixed threshold $V_{UVP(R)}$ before it proceeds to turn ON the FET. Similarly, during the ON condition, if the input supply falls below the UVP threshold $V_{UVP(F)}$, the FET is turned OFF. The UVP rising and falling thresholds are slightly different, thereby providing some hysteresis and ensuring stable operation around the threshold voltage.

The TPS2596xx devices also provide an user adjustable UVLO mechanism to ensure that the load is powered up only when the voltage is at a sufficient level. This can be achieved by dividing the input supply and feeding it to the EN/UVLO pin. Whenever the voltage at the EN/UVLO pin falls below a threshold $V_{UVLO(F)}$, the device turns OFF the FET. The FET is turned ON again when the voltage rises above the threshold $V_{UVLO(R)}$. The rising and falling thresholds on this pin are slightly different, thereby providing some hysteresis and ensuring stable operation around the threshold voltage.

The user must choose the resistor divider values appropriately to map the desired input undervoltage level to the UVLO threshold of the part.
Feature Description (continued)

Figure 44. Adjustable Undervoltage Lockout

\[
V_{IN(UV)} = V_{UVLO(F)} \times \frac{(R1 + R2)}{R2}
\]

(1)

8.3.2 Overvoltage Protection

The TPS2596xx devices provide 2 ways to handle an input overvoltage condition.

8.3.2.1 Overvoltage Lockout

The TPS25963x variants provide an user adjustable OVLO mechanism to ensure that the supply to the load is cut off if the input supply voltage exceeds a certain level. This can be achieved by dividing the input supply and feeding it to the OVLO pin. Whenever the voltage at the OVLO pin rises above a threshold \( V_{OVLO(R)} \), the device turns OFF the FET. When the voltage at the OVLO pin falls below the threshold \( V_{OVLO(F)} \), the FET is turned ON again. The rising and falling thresholds on this pin are slightly different, thereby providing some hysteresis and ensuring stable operation around the threshold voltage.

Figure 45. TPS25963x Overvoltage Lockout Response
**Feature Description (continued)**

The user should choose the resistor divider values appropriately to map the desired input overvoltage level to the OVLO threshold of the part.

![Resistor Divider Diagram]

\[
V_{IN(OV)} = V_{OVLO(R)} \times \frac{(R_1 + R_2)}{R_2}
\]  

(2)

### 8.3.2.2 Overvoltage Clamp

The TPS25962x variants provide a mechanism to clamp the output voltage to a user-selectable level quickly if the input voltage crosses a certain threshold. This ensures the load is not exposed to high voltages during any input overvoltage events and lowers the dependence on external protection devices (such as TVS/Zener diodes) in this condition. Once the input supply voltage rises above the OVC threshold voltage \( V_{OVC} \), the device responds by clamping the voltage to \( V_{CLAMP} \) within a very short response time \( t_{OVC} \). As long as an overvoltage condition is present on the input, the output voltage will be clamped to \( V_{CLAMP} \). When the input drops below the output clamp threshold \( V_{OVC} \), the clamp releases the output voltage as shown in Figure 47.
Feature Description (continued)

The OVC threshold can be configured to one of 3 pre-defined levels by connecting the OVCSEL pin as shown in Table 1.

Table 1. TPS25962x Overvoltage Clamp Threshold Selection

<table>
<thead>
<tr>
<th>OVCSEL Pin Connection</th>
<th>OVC Threshold (typ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shorted to GND</td>
<td>3.8 V</td>
</tr>
<tr>
<td>Connected to GND through 400 KΩ resistor</td>
<td>5.7 V</td>
</tr>
<tr>
<td>Open</td>
<td>13.7 V</td>
</tr>
</tbody>
</table>

During the overvoltage clamp condition, there could be significant heat dissipation in the internal FET depending on the $V_{IN} - V_{OUT}$ voltage drop and the current ($I_{OUT}$) through the FET leading to thermal shutdown if the condition persists for an extended period of time. In this case, the device would either stay latched-off or start an auto-retry cycle as explained in the Overtemperature Protection (OTP) section.

8.3.3 Inrush Current, Overcurrent and Short Circuit Protection

The TPS2596xx devices incorporate three levels of protection against overcurrent:
- Adjustable slew rate for inrush current control ($dV/dt$)
- Active current limiting with adjustable limit ($I_{LIM}$) for overcurrent protection
- Fast short-circuit response to protect against hard short-circuits

8.3.3.1 Slew Rate and Inrush Current Control ($dV/dt$)

The inrush current during turn on is directly proportional to the load capacitance and rising slew rate. Equation 3 can be used to find the slew rate $SR_{ON}$ required to limit the inrush current $I_{INRUSH}$ for a given load capacitance $C_{OUT}$. 
\[ SR (\text{mV} / \mu\text{s}) = \frac{I_{\text{INRUSH}}(\text{mA})}{C_L (\mu\text{F})} \]  

(3)

For loads requiring a slower rising slew rate, a capacitor can be connected to the dVdt pin to adjust the rising slew rate and lower the inrush current during turn on. The required \( C_{dVdt} \) capacitance value to produce a given slew rate can be calculated using Equation 4.

\[ C_{dVdt} (\text{pF}) = \frac{42000}{SR (\text{mV} / \mu\text{s})} \]  

(4)

8.3.3.2 Active Current Limiting

The load current is monitored during start-up and normal operation. When the load current exceeds the current limit \( I_{\text{LIM}} \) programmed by \( R_{\text{ILM}} \) resistor, the device regulates the current to the set limit \( I_{\text{LIM}} \) within \( t_{\text{LIM}} \). The device exits current limiting when the load current falls below \( I_{\text{LIM}} \). Equation 5 can be used to find the \( R_{\text{ILM}} \) value for a desired current limit.

\[ R_{\text{ILM}}(\Omega) = \frac{903}{I_{\text{LIM}}(A) - 0.0112} \]  

(5)

In the current limiting state, the output voltage drops resulting in increased power dissipation in the internal FET leading to thermal shutdown if the condition persists for an extended period of time. In this case, the device either stays latched-off or starts an auto-retry cycle as explained in the Overtemperature Protection (OTP) section.

![Figure 48. TPS2596x1 Overcurrent Response (Auto-retry)](image-url)
8.3.3.3 Short-Circuit Protection

The current through the device increases very rapidly during a short-circuit event. If the current exceeds 1.5 \( I_{\text{LIM}} \), the device engages a fast current clamping circuit to regulate down the current faster than the nominal overcurrent response time \( t_{\text{LIM}} \). The device does not completely turn off the power FET to ensure uninterrupted power in the event of transient overcurrents or supply transients. The device stops limiting the current once the load current falls below the programmed \( I_{\text{LIM}} \) threshold.

The output voltage drops in the current limiting state, resulting in increased power dissipation in the internal FET and might lead to thermal shutdown if the condition persists for an extended period of time. In this case, the device either stays latched-off or starts an auto retry cycle as explained in the Overtemperature Protection (OTP) section.
8.3.4 Analog Load Current Monitor (IMON)

The device allows the system to monitor the output load current accurately by providing an analog current on the ILM pin which is proportional to the current ($I_{OUT}$) through the FET. The user can sense the voltage ($V_{ILM}$) across the $R_{ILM}$ to get a measure of the output load current.

$$I_{OUT}(A) = \frac{V_{ILM}(V)}{G_{IMON}(\mu A / A) \times R_{ILM}(\Omega)}$$

(6)

8.3.5 Overtemperature Protection (OTP)

Thermal Shutdown will occur when the junction temperature ($T_J$) exceeds the thermal shutdown threshold (TSD). When the TPS2596x0 variant detects thermal overload, it will be shut down and remain latched off until the device is power cycled or re-enabled by toggling the EN/UVLO pin. When the TPS2596x1 variant detects thermal overload, it will remain off until it has cooled down sufficiently. Once the TPS2596x1 junction has cooled down below $TSD - TSD_{HYS}$, it will remain off for an additional delay of $t_{TSD,RST}$ after which it will automatically retry to turn on if it is still enabled.

<table>
<thead>
<tr>
<th>Device</th>
<th>Enter TSD</th>
<th>Exit TSD</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS2596x0 (Latch-Off)</td>
<td>$T_J \geq TSD$</td>
<td>$T_J &lt; TSD - TSD_{HYS}$ and Power Cycle ($V_{IN} &lt; V_{UVP(F)}$) / Enable Cycle ($V_{EN} &lt; V_{SD}$)</td>
</tr>
<tr>
<td>TPS2596x1 (Auto-Retry)</td>
<td>$T_J \geq TSD$</td>
<td>$T_J &lt; TSD - TSD_{HYS}$ and $t_{TSD,RST}$ timer expired</td>
</tr>
</tbody>
</table>
8.3.6 Fault Indication

Table 3 summarizes the protection response to various fault conditions.

<table>
<thead>
<tr>
<th>Event / Fault</th>
<th>Protection Response</th>
<th>FLT Asserted</th>
<th>FLT Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overtemperature</td>
<td>Shutdown</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>Undervoltage</td>
<td>Cut-off</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>Overvoltage</td>
<td>Clamp (OVC - TPS25962x only)</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Cut-off (OVLO - TPS25963x only)</td>
<td>Yes</td>
<td>tOVLO</td>
</tr>
<tr>
<td>Overcurrent</td>
<td>Current Limit</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>Short-Circuit</td>
<td>Current Limit</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>ILM Pin Short to GND</td>
<td>Shut down</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>ILM Pin Open</td>
<td>Shut down</td>
<td>No</td>
<td></td>
</tr>
</tbody>
</table>

When the device turns off due to one of these fault conditions, the FLT pin is pulled low.

Power cycling the part or pulling the EN/UVLO pin voltage below $V_{SD}$ clears the fault and the FLT pin is de-asserted. It also clears the $t_{TSD,RST}$ timer (Auto-retry variants only). Pulling the EN/UVLO just below the UVLO threshold ($V_{UVLO(F)}$) has no impact on the device in this condition. This is true for both Latch-off (TPS2596x0) and Auto-retry (TPS2596x1) variants.

For Auto-retry (TPS2596x1) variants, at the end of the $t_{TSD,RST}$ timer after a fault, the device restarts automatically and the FLT pin is de-asserted.

8.4 Device Functional Modes

The features of the device depend on the operating mode.

8.4.1 Enable and Fault Pin Functional Mode 1: Single Device, Self-Controlled

In this mode of operation, the device is enabled by the VIN voltage without the need of an external processor to drive the ENABLE pin. The FLT pin is optionally monitored by an external host as shown in Figure 51.

![Figure 51. Single Device, Self-Controlled](image-url)

8.4.2 Enable and Fault Pin Functional Mode 2: Single Device, Host-Controlled

In this mode of operation, the device is enabled by the VIN voltage without the need of an external processor to drive the ENABLE pin. The FLT pin is optionally monitored by an external host as shown in Figure 53.
Device Functional Modes (continued)

8.4.3 Enable and Fault Pin Functional Mode 3: Multiple Devices, Self-Controlled

In this mode of operation, the devices are self-controlled (no host present). The EN and FLT pins of multiple devices are shorted together as shown in Figure 52. In this configuration, when any one of the TPS2596xx devices detects a fault, it automatically disables the other TPS2596xx devices in the system.

Figure 52. Single Device, Self-Controlled

Figure 53. Multiple Devices, Self-Controlled
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information
The TPS2596xx device is an integrated eFuse that is typically used for hot-swap and power rail protection applications. The device operates from 2.7 V to 19 V with adjustable current limit and undervoltage protection. The device aids in controlling the in-rush current and provides precise current limiting during overload conditions for systems such as energy meters, white goods, building automation and adapter input protection. The device also provides robust protection for multiple faults on the sub-system rail.

The following design procedure can be used to select the supporting component values based on the application requirement.

9.2 Typical Application

9.2.1 Precision Current Limiting and Protection for White Goods

![Typical Application Schematic: Simple eFuse for White Goods](image)

(1) $C_{IN}$ is optional and 0.1 µF is recommended to suppress transients due to the inductance of PCB routing or from input wiring. If system needs to pass IEC 61000-4-4 EFT test, minimum $C_{IN}$ of 1 µF should be used to prevent eFuse from turning off during EFT bursts.

Figure 54. Typical Application Schematic: Simple eFuse for White Goods

9.2.2 Design Requirements

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage, $V_{IN}$</td>
<td>12 V</td>
</tr>
<tr>
<td>Undervoltage lockout set point, $V_{UV}$</td>
<td>8 V</td>
</tr>
<tr>
<td>Overvoltage protection set point, $V_{OV}$</td>
<td>13.7 V</td>
</tr>
<tr>
<td>Overvoltage protection type</td>
<td>Lock-out</td>
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<tr>
<td>Load at start-up, $R_{L(SU)}$</td>
<td>24 Ω</td>
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</table>

Table 4. Design Parameters
Typical Application (continued)

Table 4. Design Parameters (continued)

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current limit, (I_{\text{LM}})</td>
<td>1 A</td>
</tr>
<tr>
<td>Load capacitance, (C_{\text{OUT}})</td>
<td>100 µF</td>
</tr>
<tr>
<td>Maximum ambient temperatures, (T_A)</td>
<td>85°C</td>
</tr>
</tbody>
</table>

9.2.3 Detailed Design Procedure

The designer must know the following:
- Normal input operation voltage
- Maximum output capacitance
- Maximum current limit
- Load during start-up
- Maximum ambient temperature of operation

This design procedure seeks to control the junction temperature of device under both static and transient conditions by proper selection of output ramp-up time and associated support components. The designer can adjust this procedure to fit the application and design criteria. A spreadsheet design tool TPS2596 Design Calculator is also available for simplified calculations.

9.2.3.1 Programming the Current-Limit Threshold: \(R_{\text{ILM}}\) Selection

The \(R_{\text{ILM}}\) resistor at the ILM pin sets the over load current limit, this can be set using Equation 7.

\[
R_{\text{ILM}}(\Omega) = \frac{V_{\text{ILM}}(A)}{I_{\text{ILM}}(A) - 0.0112} = \frac{903}{1 - 0.0112} = 913.2 \Omega
\]

Choose closest standard value resistor: 909 Ω with 1% tolerance.

9.2.3.2 Undervoltage and Overvoltage Lockout Set Point

The undervoltage lockout (UVLO) and overvoltage lockout (OVLO) trip point is adjusted using the external voltage divider network of \(R_1\), \(R_2\) and \(R_3\) as connected between IN, EN/UVLO, OVLO and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated solving Equation 8 and Equation 9.

\[
V_{\text{UVLO}} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{\text{IN(UV)}}
\]

\[
V_{\text{OVLO}} = \frac{R_3}{R_1 + R_2 + R_3} \times V_{\text{IN(OV)}}
\]

Where \(V_{\text{UVLO}}\) is UVLO rising threshold (1.2 V). Because \(R_1\), \(R_2\) and \(R_3\) leak the current from input supply \(V_{\text{IN}}\), these resistors must be selected based on the acceptable leakage current from input power supply \(V_{\text{IN}}\).

The current drawn by \(R_1\), \(R_2\) and \(R_3\) from the power supply is \(I_{R123} = V_{\text{IN}} / (R_1 + R_2 + R_3)\).

However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, \(I_{R123}\) must be chosen to be 20 times greater than the leakage current expected.

From the device electrical specifications, \(V_{\text{OVLO}} = 1.2 \text{ V}\) and \(V_{\text{UVLO}} = 1.2 \text{ V}\). For design requirements, \(V_{\text{OV}} = 13.7 \text{ V}\) and \(V_{\text{UV}} = 8 \text{ V}\). To solve the equation, first choose the value of \(R_3 = 47 \text{ kΩ}\) and use Equation 9 to solve for \((R_1 + R_2) = 489.58 \text{ kΩ}\). Use Equation 8 and value of \((R_1 + R_2)\) to solve for \(R_2 = 33.48 \text{ kΩ}\) and finally \(R_1 = 456.1 \text{ kΩ}\).

Using the closest standard 1% resistor values gives \(R_1 = 464 \text{ kΩ}\), \(R_2 = 33.2 \text{ kΩ}\), and \(R_3 = 47.5 \text{ kΩ}\).
9.2.3.3 Setting Output Voltage Ramp Time (T_{dVdT})

For a successful design, the junction temperature of device must be kept below the absolute maximum rating during both dynamic (start-up) and steady state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and in-rush current limit required with system capacitance to avoid thermal shutdown during start-up with and without load.

The required ramp-up capacitor \( C_{dVdT} \) is calculated considering the two possible cases (see Case 1: Start-Up Without Load. Only Output Capacitance \( C_{OUT} \) Draws Current and Case 2: Start-Up With Load. Output Capacitance \( C_{OUT} \) and Load Draw Current ).

9.2.3.3.1 Case 1: Start-Up Without Load. Only Output Capacitance \( C_{OUT} \) Draws Current

During start-up, as the output capacitor charges, the voltage drop as well as the power dissipated across the internal FET decreases. The average power dissipated in the device during start-up is calculated using Equation 11.

For TPS2596xx device, the inrush current is determined as shown in Equation 10.

\[
I_{INRUSH} = C_{OUT} \times \frac{V_{IN}}{T_{dVdT}}
\]  

(10)

Power dissipation during start-up is shown in Equation 11.

\[
P_{D(INRUSH)} = 0.5 \times V_{IN} \times I_{INRUSH}
\]  

(11)

Equation 11 assumes that load does not draw any current until the output voltage has reached its final value.

9.2.3.3.2 Case 2: Start-Up With Load. Output Capacitance \( C_{OUT} \) and Load Draw Current

When the load draws current during the turnon sequence, there is additional power dissipated. Considering a resistive load during start-up \( R_{L(SU)} \), load current ramps up proportionally with increase in output voltage during \( T_{dVdT} \) time. Equations 12 to 15 show the average power dissipation in the internal FET during charging time due to resistive load.

\[
P_{D(LOAD)} = \left( \frac{1}{6} \right) \times \frac{V_{IN}^2}{R_{L(SU)}}
\]  

(12)

Total power dissipated in the device during start-up is Equation 13.

\[
P_{D(STARTUP)} = P_{D(INRUSH)} + P_{D(LOAD)}
\]  

(13)

Total current during start-up is given by Equation 14.

\[
I_{STARTUP} = I_{INRUSH} + I_L(t)
\]  

(14)

If \( I_{STARTUP} > I_{LIMIT} \), the device limits the current to \( I_{LIMIT} \) and the current-limited charging time is determined by Equation 15.

\[
T_{dVdT(Current-Limited)} = C_{OUT} \times R_{L(SU)} \times \left[ \frac{I_{LIMIT}}{I_{INRUSH}} - 1 + \ln \left( \frac{I_{INRUSH}}{I_{LIMIT}} - \frac{V_{IN}}{R_{L(SU)}} \right) \right]
\]  

(15)

The power dissipation, with and without load, for selected start-up time must not exceed the shutdown limits as shown in Figure 55.
For the design example under discussion, select ramp-up capacitor $C_{\text{dvdt}} = 22000$ pF. The default slew rate for $C_{\text{dvdt}} = 22000$ pF is 1.9 mV/µs. With slew rate of 1.9 mV/µs, the ramp-up time $T_{\text{dvdt}}$ for 12 V input is 6.3 ms.

The inrush current drawn by the load capacitance $C_{\text{OUT}}$ during ramp-up using Equation 16.

$$I_{\text{INRUSH}} = \frac{100 \, \mu\text{F} \times 1.9 \, \text{mV}}{\mu\text{s}} = 190 \, \text{mA}$$ (16)

The inrush power dissipation is calculated using Equation 17.

$$P_{\text{D(INRUSH)}} = 0.5 \times 12 \times 190 \, \text{m} = 1.14 \, \text{W}$$ (17)

For 1.14 W of power loss, the thermal shutdown time of the device must not be less than the ramp-up time $T_{\text{dvdt}}$ to avoid the false trip at the maximum operating temperature. Figure 55 shows the thermal shutdown limit at $T_A = 85 \, ^\circ\text{C}$, for 1.14 W of power, the shutdown time is infinite. Therefore, it is safe to use 6.3 ms as the start-up time without any load on the output.

The additional power dissipation when a 10-Ω load is present during start-up is calculated using Equation 18.

$$P_{\text{D(LOAD)}} = \left( \frac{1}{6} \right) \times \frac{12 \times 12}{24} = 1\,\text{W}$$ (18)

The total device power dissipation during start-up is given in Equation 19.

$$P_{\text{D(STARTUP)}} = 1 + 1.14 = 2.24 \, \text{W}$$ (19)

Figure 55 shows $T_A = 85 \, ^\circ\text{C}$ and the thermal shutdown time for 2.24 W is approximately 2000 ms, which increases the margins further for shutdown time and ensures successful operation during start up and steady state conditions.

When $C_{\text{OUT}}$ is large, there is a need to decrease the power dissipation during start-up. This can be done by increasing the value of the $C_{\text{dvdt}}$ capacitor.

### 9.2.4 Support Component Selection: $R_{\text{FLT}}$ and $C_{\text{IN}}$

Referring to application schematics, $R_{\text{FLT}}$ is required only if FLT is used; The resistor serves as pull-up for the open-drain output driver. The current sunk by this pin should not exceed 10 mA. $C_{\text{IN}}$ is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise. Where acceptable, a value in the range from 0.001 µF to 0.1 µF is recommended for $C_{\text{IN}}$. 
9.2.5 Application Curves

![Application Curves Diagrams](image)

9.3 System Examples

The TPS2596xx provides a simple solution for current limiting, inrush current control and supervision of power rails for wide range of applications operating at 2.7 V to 19 V and delivering up to 2 A.

9.3.1 Current Limiting and Overvoltage Protection and for Energy Meter Power Rails

Energy meters generally use a single AC/DC power supply (for example: flyback converter) with multiple DC outputs for powering blocks like Metrology (analog front-end, microcontroller, memory), Real Time Clock (RTC), Relay (for remote load connect/disconnect) and Communications module. Metrology is the most critical subsystem and is required to operate uninterrupted under all conditions, even if a fault occurs in any of the supplementary blocks. One solution would be to oversize the power supply design so that it can handle the excess current demands during a fault condition, which increases the cost of the meter. A more elegant and cost-optimized solution would be to add an eFuse like TPS2596xx on the supplementary power rails, which provides accurate current limiting and fast short-circuit protection, thereby ensuring reliable operation of the metrology block without increasing the size or cost of the power supply. Apart from that, the TPS2596xx provides additional benefits such as:

- Overvoltage Protection (Lock-out and Clamp) to shield down-stream low voltage circuits from harmful overvoltages arising from poor cross-regulation between windings or AC input voltage surges.
System Examples (continued)

- Disconnect supply to rarely used loads to minimize power consumption

Figure 60 shows a typical energy meter power supply implementation using TPS2596xx.

**Figure 60. Energy Meter Power Rail Protection Example**

TIDA-010037 demonstrates energy meter design using eFuse for protecting auxiliary rails.

### 9.3.2 Precision Current Limiting and Protection in Appliances

Household and similar electrical appliances are subjected to various tests (for example: needle flame, glow wire) as part of the certification for electrical and fire safety compliance as per the regulations. Special precautions need to be taken in the design to pass these tests, which include the use of higher grade flame retardant plastic material for the housing enclosures. There are certain provisions in the standard which can be leveraged to make the certification easier, faster and also reduce the cost of plastic materials. For example, any node which has less than 15 W of power available to it is classified as a LPC (Low Power Circuit as per the definition in IEC 60335-1) and deemed to be safe. All circuits or sub-systems further downstream from a LPC node are exempt from the aforementioned tests.

eFuses like TPS2596xx are a simple and cost effective way to limit the power delivered to the downstream load. The key parameter to be considered is the current limit tolerance and accuracy, which determines how high one can set the nominal current limit without exceeding the 15-W power limit on the upper end. On the lower end, it determines the maximum power the load can draw in normal conditions without hitting the current limit. TPS2596xx provides a current limit accuracy of ±5 % (at room temperature), which allows the load to use nearly 90% out of the 15-W limit under normal operating conditions.

In contrast, an alternative current limiting solution with wider current limit tolerance, say ±25 % would leave only 50 % out of 15 W for the load circuit to operate under normal conditions. This places severe constraints on the load circuit design and/or capabilities.

Figure 61 shows a sub-system example of a refrigerator and freezer system where TPS2596xx is used for precision current limiting and protection of 15-W rails to ease the qualification as low-power circuit as per IEC 60335-1.
System Examples (continued)

**Figure 61. Appliances 15-W LPC Implementation Example**

*TIDA-010004* demonstrates a multi-load drive using single driver chip with eFuse for protection and 15-W LPC implementation.

Refer to this *Designing Low-Power Circuits (LPCs) using TPS2596 for Household and similar Appliances* application note for a detailed insight into implementing power limited circuits using eFuses.
10 Power Supply Recommendations

The TPS2596xx devices are designed for a supply voltage range of \(2.7 \leq V_{IN} \leq 19\) V. An input ceramic bypass capacitor higher than 0.1 \(\mu F\) is recommended if the input supply is located more than a few inches from the device. The power supply must be rated higher than the set current limit to avoid voltage droops during overcurrent and short-circuit conditions.

10.1 Transient Protection

In the case of a short circuit and overload current limit when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Use a Schottky diode across the output to absorb negative spikes.
- Use a low-value ceramic capacitor \(C_{IN} = 0.001\ \mu F\) to 0.1 \(\mu F\) to absorb the energy and dampen the transients.

The approximate value of input capacitance can be estimated with Equation 20:

\[
V_{SPIKE(Absolute)} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}}
\]

(20)

where:
- \(V_{IN}\) is the nominal supply voltage
- \(I_{LOAD}\) is the load current
- \(L_{IN}\) equals the effective inductance seen looking into the source
- \(C_{IN}\) is the capacitance present at the input

NOTE: Systems which need to pass IEC 61000-4-4 tests for immunity to Electrical Fast Transients (EFT) should use a minimum \(C_{IN}\) of 1 \(\mu F\) to ensure the TPS2596xx does not turn OFF during the EFT burst.

Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device. The circuit implementation with optional protection components (a ceramic capacitor, TVS and Schottky diode) is shown in Figure 62.

![Figure 62. Circuit Implementation with Optional Protection Components](image-url)
10.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. The following contribute to variation in results:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.
11 Layout

11.1 Layout Guidelines

- For all applications, a ceramic decoupling capacitor of 0.01 \( \mu \text{F} \) or greater is recommended between the IN terminal and GND terminal. For hot-plug applications, where input power-path inductance is negligible, this capacitor can be eliminated or minimized.

- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See Figure 63 for a PCB layout example.

- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.

- The GND terminal must be tied to the PCB ground plane at the terminal of the IC. The PCB ground must be a copper plane or island on the board.

- Locate the following support components close to their connection pins:
  - \( R_{ILM} \)
  - \( C_{dVdT} \)
  - Resistor network for the EN/UVLO pin
  - Resistor network for the OVLO pin for TPS25693x variants
  - Pull-down resistor on the OVCSEL pin for TPS25962x variants

Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing from the \( R_{ILM}, C_{dVdT} \) and \( R_{OVCSEL} \) (for TPS25962x variants) components to the device pins must be as short as possible to reduce parasitic effects on the current limit, soft-start timing and overvoltage clamp response. These traces must not have any coupling to switching signals on the board.

- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it must be physically close to the OUT pins.

- Obtaining acceptable performance with alternate layout schemes is possible. The Layout Example shown in Figure 63 has been shown to produce good results and is intended as a guideline.
### 11.2 Layout Example

* Optional: Needed only to suppress the transients caused by inductive load switching

**Figure 63. TPS2596xx Layout Example**
12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation
For related documentation see the following:

- Basics of eFuses
- TPS2596EVM: Evaluation Module for TPS2596xx
- TPS2596 Design Calculator
- Designing Low-Power Circuits (LPCs) using TPS2596 for Household and similar Appliances
- TIDA-010037 High Accuracy Split-Phase CT Electricity Meter
- TIDA-010004 12 V, Highly Protected, Single Driver-Based Stepper, Brushed DC and Actuator Drive

12.2 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community  Ti's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support  Ti's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks
E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
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<tbody>
<tr>
<td>TPS259620DDAR</td>
<td>ACTIVE</td>
<td>SO PowerPAD</td>
<td>DDA</td>
<td>8</td>
<td>2500</td>
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<td>SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>259620</td>
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<td>Samples</td>
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</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a “~” will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Description</th>
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<tbody>
<tr>
<td>A0</td>
<td>Dimension designed to accommodate the component width</td>
</tr>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
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</table>

### REEL DIMENSIONS

- Reel Diameter
- Reel Width (W1)

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- Sprocket Holes
- User Direction of Feed
- Pocket Quadrants

*All dimensions are nominal.*

### TAPE AND REEL INFORMATION TABLE

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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Pack Materials-Page 1
**PACKAGE MATERIALS INFORMATION**

www.ti.com 17-Apr-2020

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<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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**TAPE AND REEL BOX DIMENSIONS**

*All dimensions are nominal*

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<tr>
<th>Device</th>
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<th>Package Drawing</th>
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<td>366.0</td>
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<td>50.0</td>
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</table>
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

PowerPAD is a trademark of Texas Instruments.
THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments
LAND PATTERN DATA

DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

Example Board Layout
Via pattern and copper pad size may vary depending on layout constraints

Example Solder Mask Defined Pad
(See Note C, D)

Non Solder Mask Defined Pad

Example Solder Mask Opening
(Note F)

Center Power Pad Solder Stencil Opening

<table>
<thead>
<tr>
<th>Stencil Thickness</th>
<th>X</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1mm</td>
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<td>0.178mm</td>
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</table>

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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