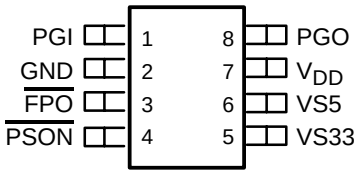
- **Overvoltage Protection and Lockout for 12 V, 5 V, 3.3 V**
- **Undervoltage Protection and Lockout for 5 V and 3.3 V**
- **Fault Protection Output With Open-Drain Output Stage**
- **Open-Drain Power Good Output Signal for Power Good Input, 3.3 V and 5 V**
- **Power Good Delay; 300-ms TPS3510, 150-ms TPS3511**
- **75-ms Delay for 5-V and 3.3-V Power Supply Short-Circuit Turnon Protection**
- **2.3-ms $\overline{\text{PSON}}$ Control to $\overline{\text{FPO}}$ Turnoff Delay**
- **38-ms $\overline{\text{PSON}}$ Control Debounce**
- **73-μs Width Noise Deglitches**
- **Wide Supply Voltage Range From 4 V to 15 V**

D OR P PACKAGE
(TOP VIEW)



description

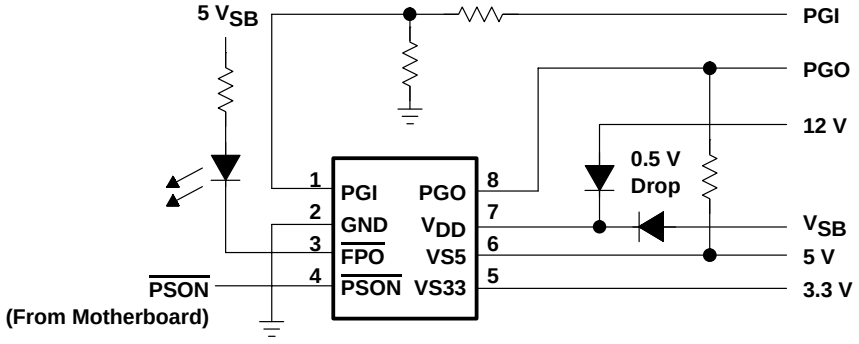
The TPS3510/1 is designed to minimize external components of personal-computer switching power supply systems. It provides protection circuits, power good indicator, fault protection output ($\overline{\text{FPO}}$) and $\overline{\text{PSON}}$ control.

Overvoltage protection (OVP) monitors 3.3 V, 5 V, and 12 V (12-V signal detects via V_{DD} pin). Undervoltage protection (UVP) monitors 3.3 V and 5 V. When an OV or UV condition is detected, the power good output (PGO) is set to low and $\overline{\text{FPO}}$ is latched high. $\overline{\text{PSON}}$ from low to high resets the protection latch. UVP function is enabled 75 ms after $\overline{\text{PSON}}$ is set low and debounced. Furthermore, there is a 2.3-ms delay (and an additional 38-ms debounce) at turnoff. There is no delay during turnon.

Power good feature monitors PGI, 3.3 V and 5 V and issues a power good signal when the output is ready.

The TPS3510/1 is characterized for operation from –40°C to 85°C.

typical application



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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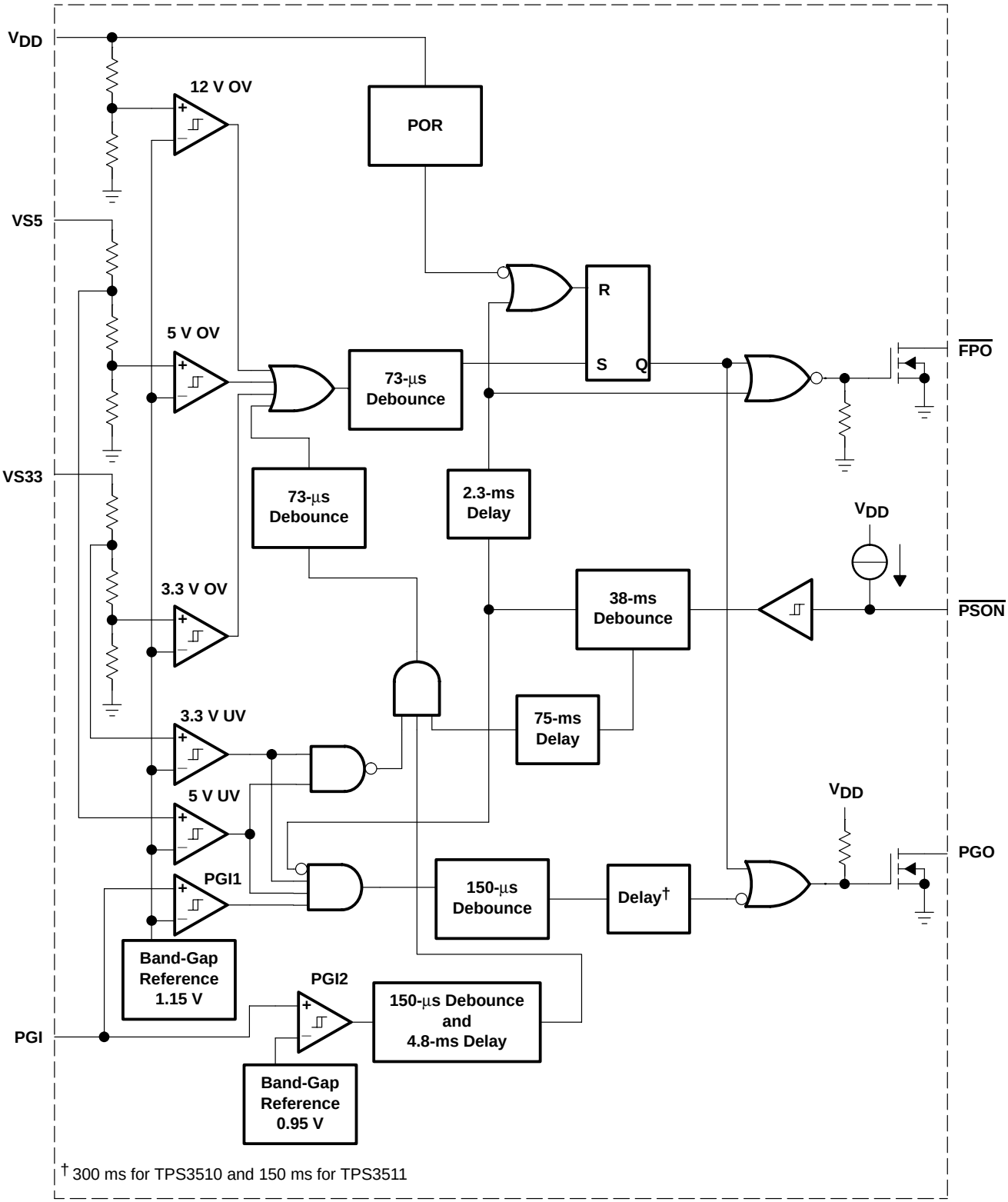
FUNCTION TABLE

PGI	$\overline{\text{PSON}}$	UV CONDITION (3.3 V OR 5 V)	OV CONDITION (3.3 V, 5 V, OR 12 V)	$\overline{\text{FPO}}$	PGO
<0.95 V	L	no	no	L	L
<0.95 V	L	no	yes	H	L
<0.95 V	L	yes	no	L	L
0.95 V<PGI<1.15 V	L	no	no	L	L
0.95 V<PGI<1.15 V	L	no	yes	H	L
0.95 V<PGI<1.15 V	L	yes	no	H	L
PGI > 1.15 V	L	no	no	L	H
PGI > 1.15 V	L	no	yes	H	L
PGI > 1.15 V	L	yes	no	H	L
x	H	x	x	H	L

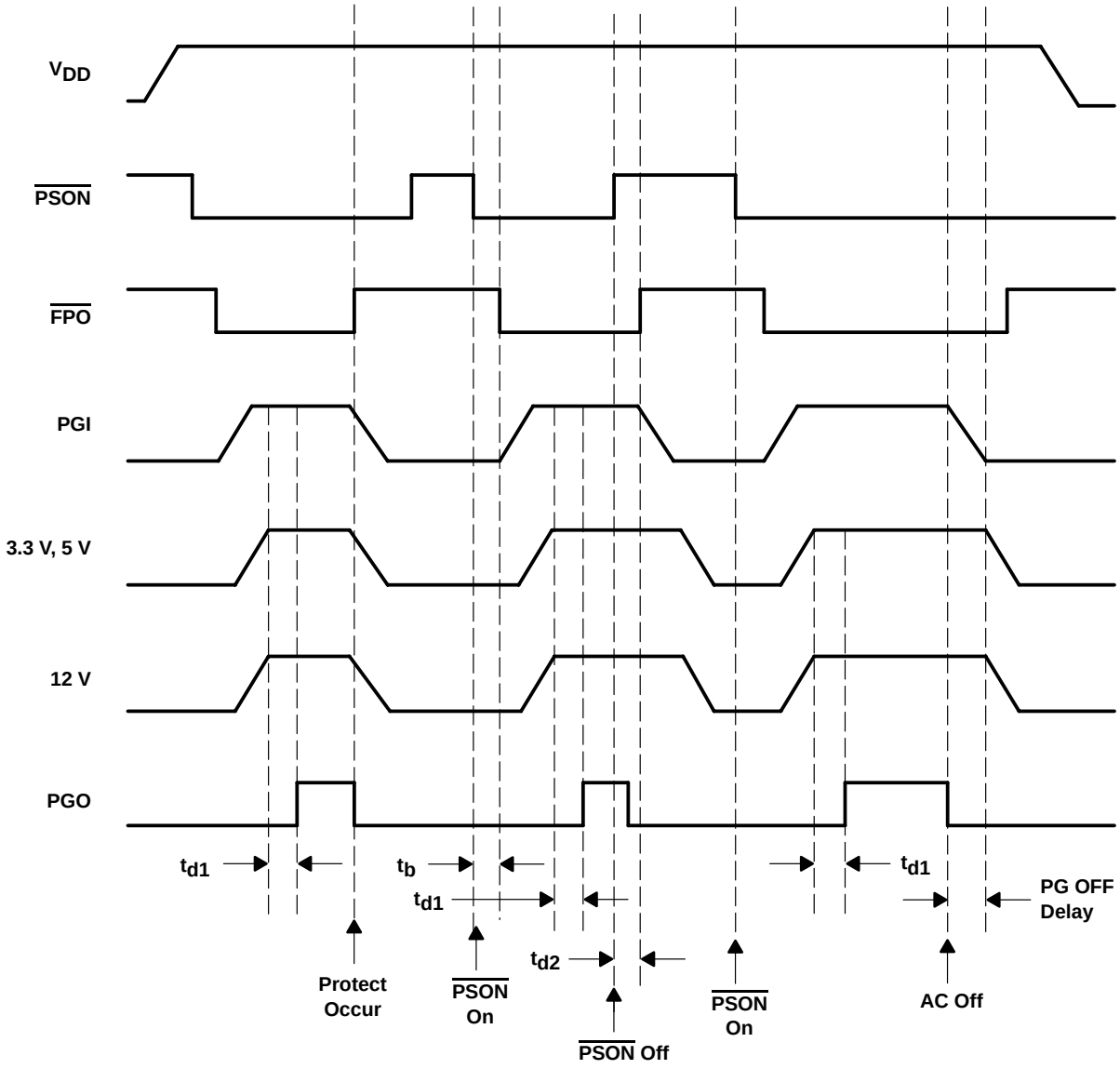
x = don't care
$\overline{\text{FPO}}$ = L means: fault IS NOT latched
$\overline{\text{FPO}}$ = H means: fault IS latched
PGO = L means: fault
PGO = H means: NO fault

functional block diagram



† 300 ms for TPS3510 and 150 ms for TPS3511

timing diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{FPO}}$	3	O	Inverted fault protection output, open drain output stage
GND	2		Ground
PGI	1	I	Power good input
PGO	8	O	Power good output, open drain output stage
$\overline{\text{PSON}}$	4	I	ON/OFF control
V_{DD}	7	I	Supply voltage/12 V overvoltage protection input pin
VS33	5	I	3.3 V over/undervoltage protection
VS5	6	I	5 V over/undervoltage protection

detailed description

power good and power good delay

A PC power supply is commonly designed to provide a power-good signal, which is defined by the computer manufacturers. PGO is a power-good signal and should be asserted high by the PC power supply to indicate that the 5-V and 3.3-V outputs are above the under-voltage threshold limit. At this time the converter should be able to provide enough power to ensure continuous operation within the specification. Conversely, when either the 5-V or the 3.3-V output voltages fall below the under-voltage threshold, or when ac power has been removed for a time sufficiently long so that power supply operation is no longer ensured, PGO should be de-asserted to a low state.

Figure 1 represents the timing characteristics of the power good (PGO), dc enable ($\overline{\text{PSON}}$), and the 5 V/3.3 V supply rails.

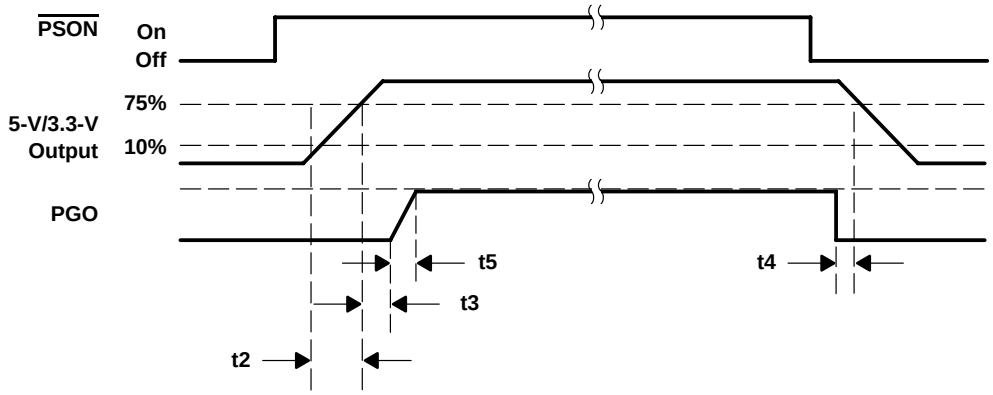


Figure 1. Timing of $\overline{\text{PSON}}$ and PGO

Although there is no requirement to meet specific timing parameters, the following signal timings are recommended:

2 ms ≤ t2 ≤ 20 ms, 100 ms < t3 < 2000 ms, t4 > 1 ms, t5 ≤ 10 ms

Furthermore motherboards should be designed to comply with the previously recommended timing. If timings other than these are implemented or required, this information should be clearly specified.

The TPS3510/1 family of power-supply supervisors provides a power-good output (PGO) for the 3.3-V and 5-V supply voltage rails and a separate power-good input (PGI). An internal timer is used to generate a power-good delay. If the voltage signals at PGI, VS33, and VS5 rise above the under-voltage threshold, the open-drain power-good output (PGO) goes high after a delay of 150 ms or 300 ms. When the PGI voltage or either the 3.3-V and 5-V power rails drops below the under-voltage threshold, PGO is disabled immediately (after 150-µs debounce).

power supply remote on/off ($\overline{\text{PSON}}$) and fault protect output ($\overline{\text{FPO}}$)

Since the latest personal computer generation focuses on easy turnon and power saving functions, the PC power supply requires two characteristics. One is a dc power supply remote on/off function, the other is standby voltage to achieve very low power consumption of the PC system. Thus the main power needs to be shut down.

The power supply remote on/off ($\overline{\text{PSON}}$) is an active low signal that turns on all of the main power rails including 3.3 V, 5 V, –5 V, 12 V, and –12 V power rails. When this signal is held high by the PC motherboard or left open circuited, the signal of the fault protect output ($\overline{\text{FPO}}$) also goes high. Thus, the main power rails should not deliver current and should be held at 0 V.

power supply remote on/off ($\overline{\text{PSON}}$) and fault protect output ($\overline{\text{FPO}}$)(continued)

When the $\overline{\text{FPO}}$ signal is held high due to an occurring fault condition, the fault status is latched and the outputs of the main power rails should not deliver current but are held at 0 V. Toggling the power supply remote on/off ($\overline{\text{PSON}}$) from low to high resets the fault-protection latch. During this fault condition only the standby power is not affected.

When $\overline{\text{PSON}}$ goes from high to low or low to high, the 38-ms debounce block is active to avoid a glitch on the input that disables/enables the $\overline{\text{FPO}}$ output. During this period the under-voltage function is disabled for 75 ms to prevent turnon failure. At turnoff, there is an additional delay of 2.3 ms from $\overline{\text{PSON}}$ to $\overline{\text{FPO}}$.

Power should be delivered to the rails only if the $\overline{\text{PSON}}$ signal is held at ground potential, thus $\overline{\text{FPO}}$ is active-low. The $\overline{\text{FPO}}$ pin can be connected to 5 V (or up to 15 V) through a pullup resistor.

undervoltage protection

The TPS3510/1 provides under-voltage protection (UVP) for the 3.3-V and 5-V rails. When an undervoltage condition appears at either one of the 3.3-V (VS33) or 5-V (VS5) input pins for more than 146 μs, the $\overline{\text{FPO}}$ output goes high and PGO goes low. Also, this fault condition is latched until $\overline{\text{PSON}}$ is toggled from low to high or V_{DD} is removed.

The need for undervoltage protection is often overlooked in off-line switching power supply system design. But it is very important in battery-powered or hand-held equipment since the TTL or CMOS logic often results in malfunction.

In flyback or forward-type off-line switching power supplies, usually designed for low power, the overload protection design is very simple. Most of these types of power supplies are only sensing the input current for an overload condition. The trigger point needs to be set much higher than the maximum load in order to prevent false turnon.

However, this causes one critical problem. If the connected load is larger than the maximum allowable load but smaller than the trigger point, the system always becomes overheated with failure and damage occurring.

overvoltage protection

The overvoltage protection (OVP) of TPS3510/1 monitors 3.3 V, 5 V, and 12 V (12 V is sensed via the V_{DD} pin). When an overvoltage condition appears at one of the 3.3-V, 5-V, or 12-V input pins for more than 73 μs, the $\overline{\text{FPO}}$ output goes high and PGO goes low. Also, this fault condition is latched until $\overline{\text{PSON}}$ is toggled from low to high or V_{DD} is removed. During fault conditions, most power supplies have the potential to deliver higher output voltages than those normally specified or required. In unprotected equipment, it is possible for output voltages to be high enough to cause internal or external damage of the system. To protect the system under these abnormal conditions, it is common practice to provide overvoltage protection within the power supply.

Because TTL and CMOS circuits are very vulnerable to overvoltages, it is becoming industry standard to provide overvoltage protection on all 3.3-V and 5-V outputs. However, not only the 3.3-V and 5-V rails for the logic circuits on the motherboard need to be protected, but also the 12-V peripheral devices such as the hard disk, floppy disk, and CD-ROM players etc., need to be protected.

short-circuit power supply turnon

During safety testing the power supply might have tied the output voltage direct to ground. If this happens during the normal operating, this is called a short-circuit or over-current condition. When it happens before the power supply turns on, this is called a short-circuit power supply turnon. It can happen during the design period, in the production line, at quality control inspection or at the end user. The TPS3510/1 provides an undervoltage protection function with a 75-ms delay after $\overline{\text{PSON}}$ is set low.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note1) . . . . . 16 V
Output voltage V_O: $\overline{FPO}$ . . . . . 16 V
PGO . . . . . 8 V
All other pins (see Note 1) . . . . . –0.3 V to 16 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Soldering temperature . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
P	1092 mW	8.74 mW/°C	699 mW	568 mW
D	730 mW	5.84 mW/°C	467 mW	379 mW

recommended operating conditions at specified temperature range

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4		15	V
Input voltage, V_I	$\overline{PSON}$, VS5, VS33			7	V
	PGI			V_{DD} + 0.3 V (max = 7 V)	
Output voltage, V_O	$\overline{FPO}$			15	V
	PGO			7	
Output sink current, $I_{O,sink}$	$\overline{FPO}$			20	mA
	PGO			10	
Supply voltage rising time, t_r	See Note 2	1			ms
Operating free-air temperature range, T_A		–40		85	°C

NOTE 2: V_{DD} rising and falling slew rate must be less than 14 V/ms.

electrical characteristics over recommended operating conditions (unless otherwise noted)

overvoltage protection

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Overvoltage threshold	VS33		3.7	3.9	4.1	V
		VS5		5.7	6.1	6.5	
		V_{DD}		13.2	13.8	14.4	
I_{LKG}	Leakage current ($\overline{FPO}$)		$V(\overline{FPO})$ = 5 V			5	µA
V_{OL}	Low-level output voltage ($\overline{FPO}$)		V_{DD} = 5 V, I_{sink} = 20 mA			0.7	V
	Noise deglitch time OVP		V_{DD} = 5 V	35	73	110	µs

PGI and PGO

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PGI}	Input threshold voltage (PGI)	PGI1		1.1	1.15	1.2	V
		PGI2		0.9	0.95	1	
V_{IT}	Undervoltage threshold	VS33		2	2.2	2.4	V
		VS5		3.3	3.5	3.7	
I_{LKG}	Leakage current (PGO)		PGO = 5 V			5	µA
V_{OL}	Low-level output voltage (PGO)		V_{DD} = 4 V, I_{sink} = 10 mA			0.4	V
	Short-circuit protection delay	3.3 V, 5 V		49	75	114	ms
t_{d1}	Delay time	TP3510	PGI to PGO	200	300	450	ms
		TP3511		100	150	225	
			PGI to $\overline{FPO}$	3.2	4.8	7.2	
	Noise deglitch time		PGI to PGO	88	150	225	µs
			PGI to $\overline{FPO}$	180	296	445	
			UVP to $\overline{FPO}$	82	146	220	

$\overline{PSON}$ control

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Input pullup current	$\overline{PSON}$ = 0 V		120		µA
V_{IH}	High-level input voltage		2.4			V
V_{IL}	Low-level input voltage				1.2	V
t_b	Debounce time ($\overline{PSON}$)	V_{DD} = 5 V	24	38	57	ms
t_{d2}	Delay time ($\overline{PSON}$ to $\overline{FPO}$)	V_{DD} = 5 V	t_b+1.1	t_b+2.3	t_b+4	ms

total device

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	$\overline{PSON}$ = 5 V			1	mA

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

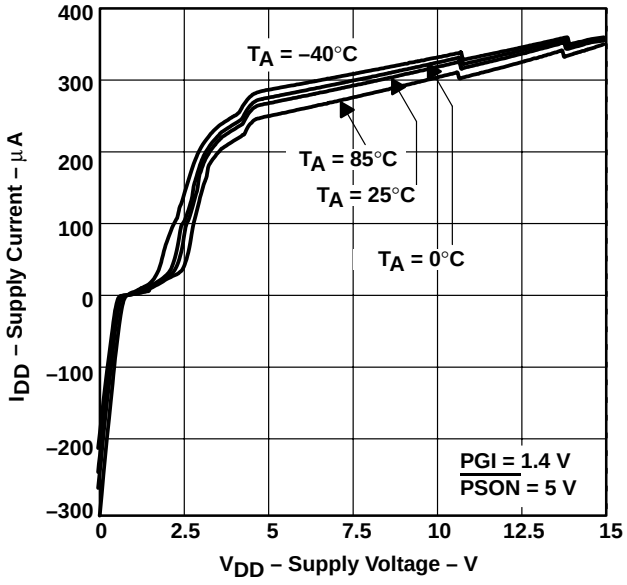


Figure 2

INPUT CURRENT (PSON) vs INPUT VOLTAGE (PSON)

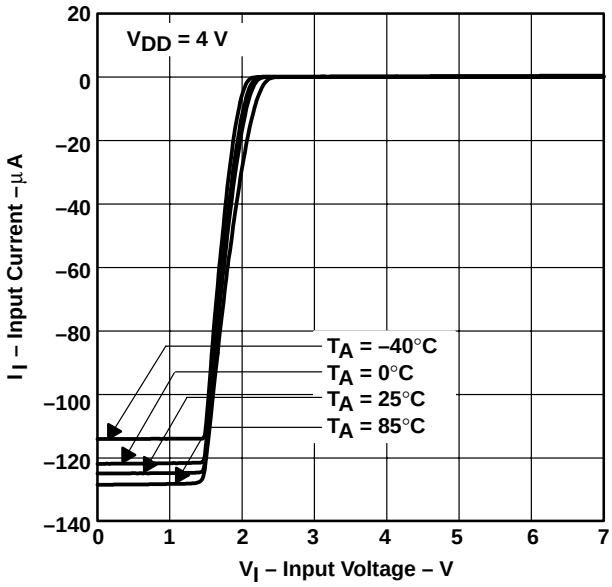


Figure 3

LOW-LEVEL OUTPUT VOLTAGE (FPO) vs LOW-LEVEL OUTPUT CURRENT (FPO)

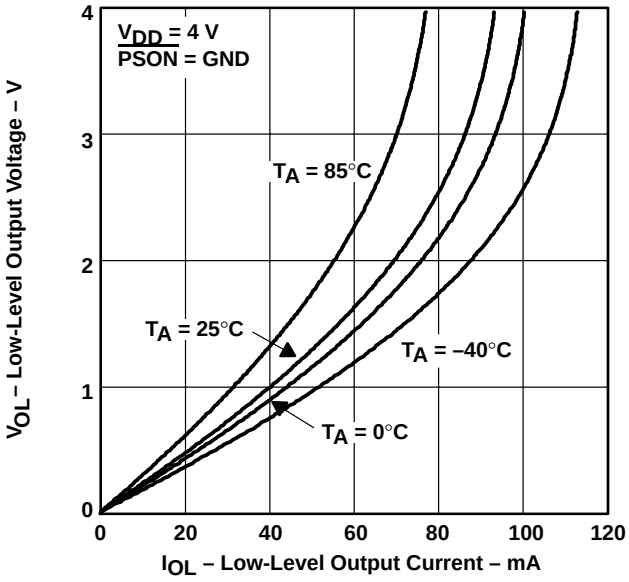


Figure 4

LOW-LEVEL OUTPUT VOLTAGE (FPO) vs LOW-LEVEL OUTPUT CURRENT (FPO)

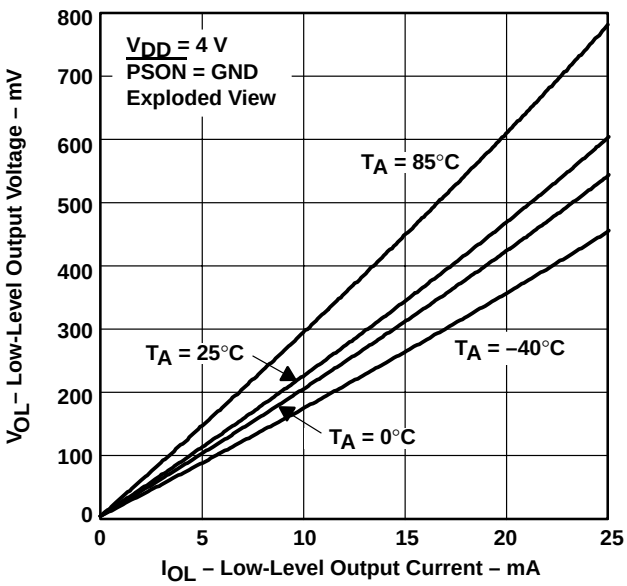


Figure 5

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE (PGO)
vs
LOW-LEVEL OUTPUT CURRENT (PGO)

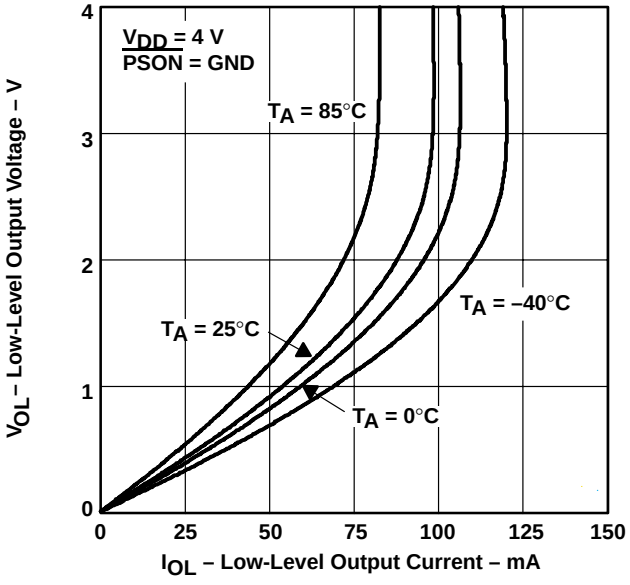


Figure 6

LOW-LEVEL OUTPUT VOLTAGE (PGO)
vs
LOW-LEVEL OUTPUT CURRENT (PGO)

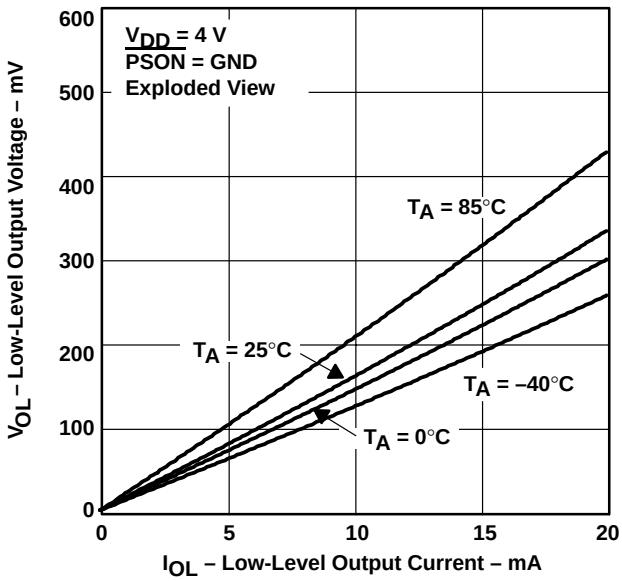


Figure 7

NORMALIZED SENSE THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE AT V_{DD}

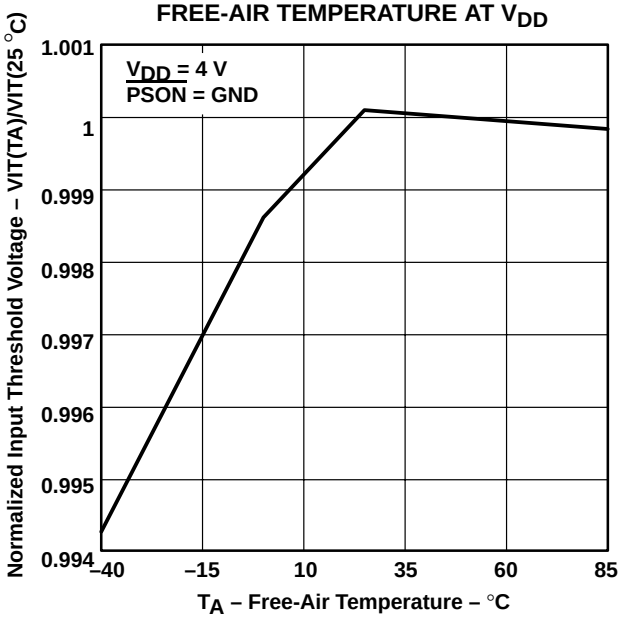


Figure 8

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3510D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS3510
TPS3510D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS3510
TPS3510DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS3510
TPS3510DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS3510
TPS3510P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TPS3510P
TPS3510P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TPS3510P
TPS3511D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	PS3511
TPS3511DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PS3511
TPS3511DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PS3511

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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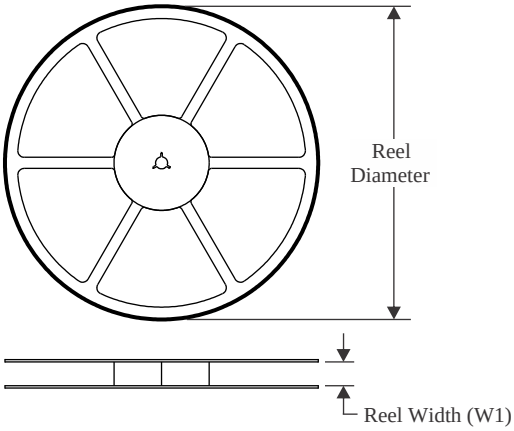
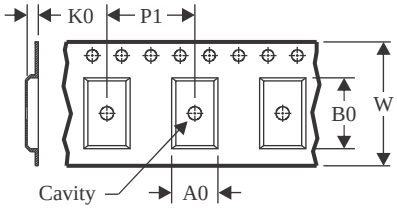
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

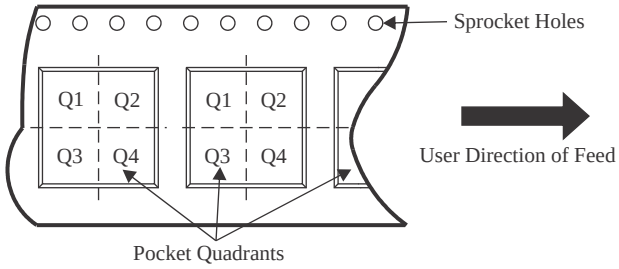


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

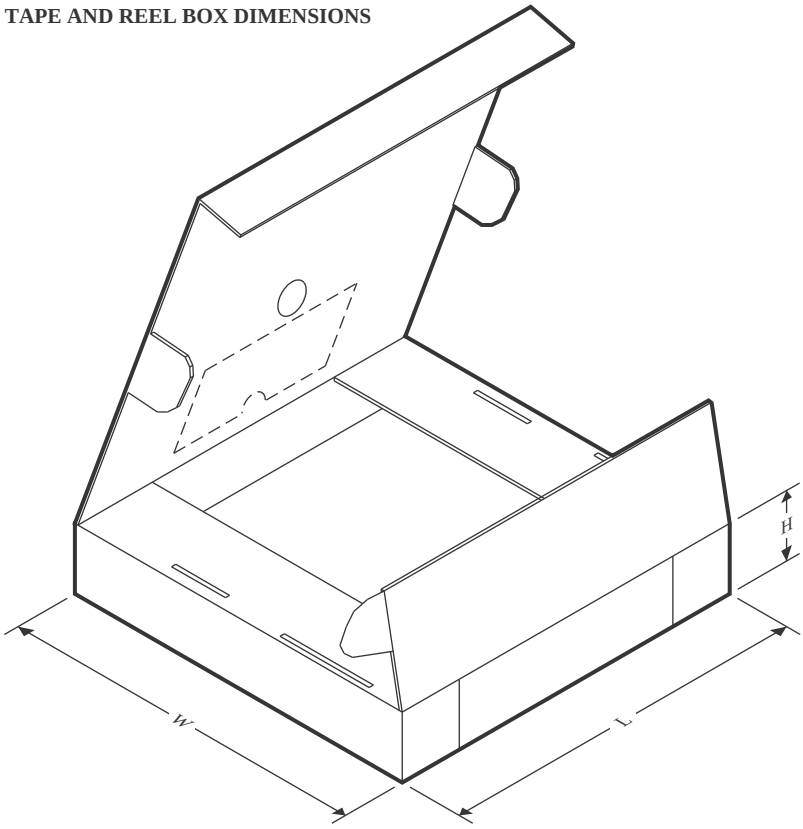
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3510DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3511DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

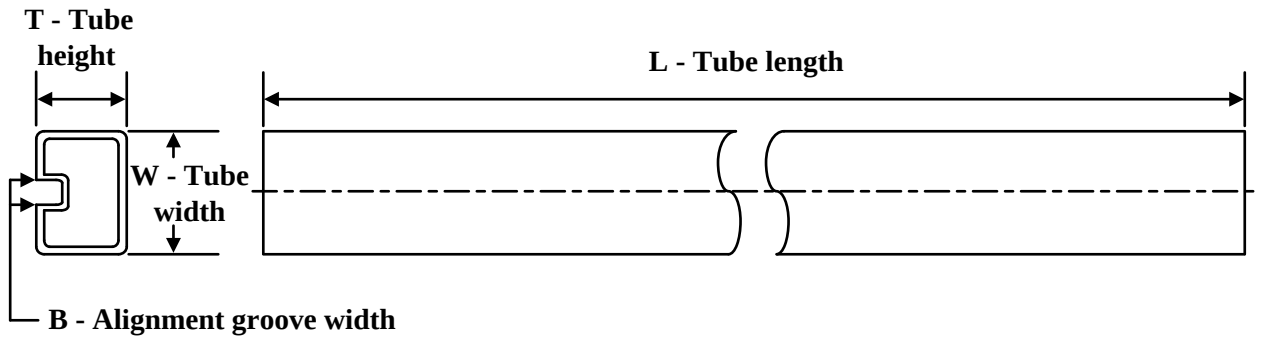
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

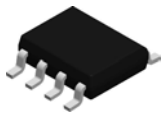
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3510DR	SOIC	D	8	2500	353.0	353.0	32.0
TPS3511DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS3510D	D	SOIC	8	75	507	8	3940	4.32
TPS3510D.A	D	SOIC	8	75	507	8	3940	4.32
TPS3510P	P	PDIP	8	50	506	13.97	11230	4.32
TPS3510P.A	P	PDIP	8	50	506	13.97	11230	4.32

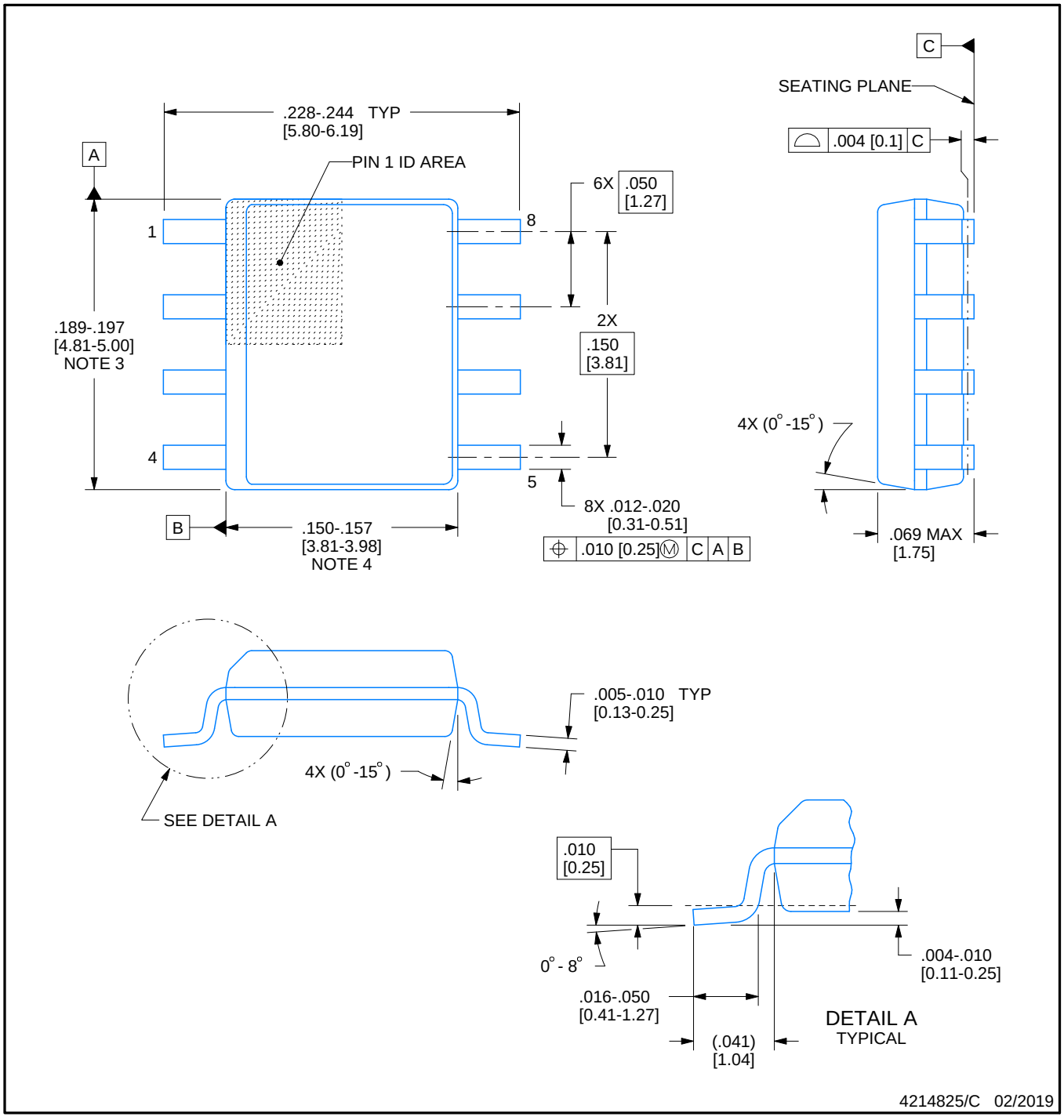


PACKAGE OUTLINE

D0008A

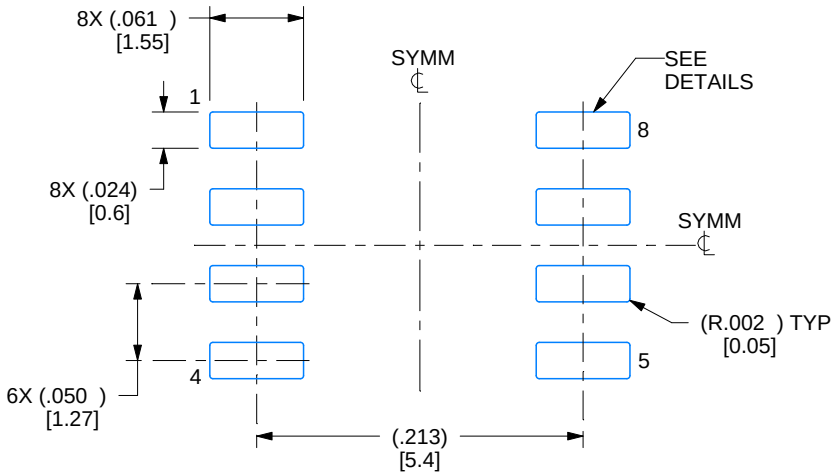
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

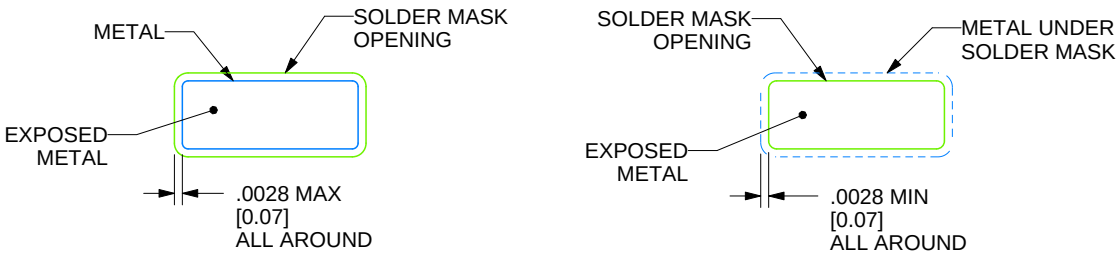


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

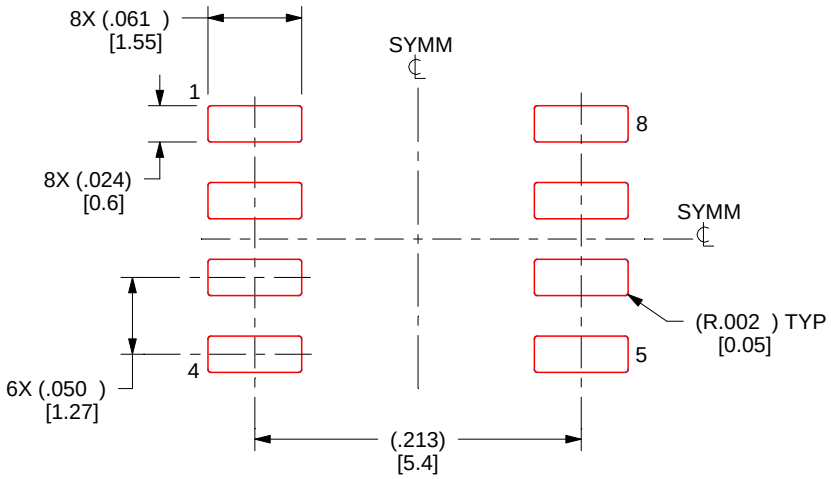
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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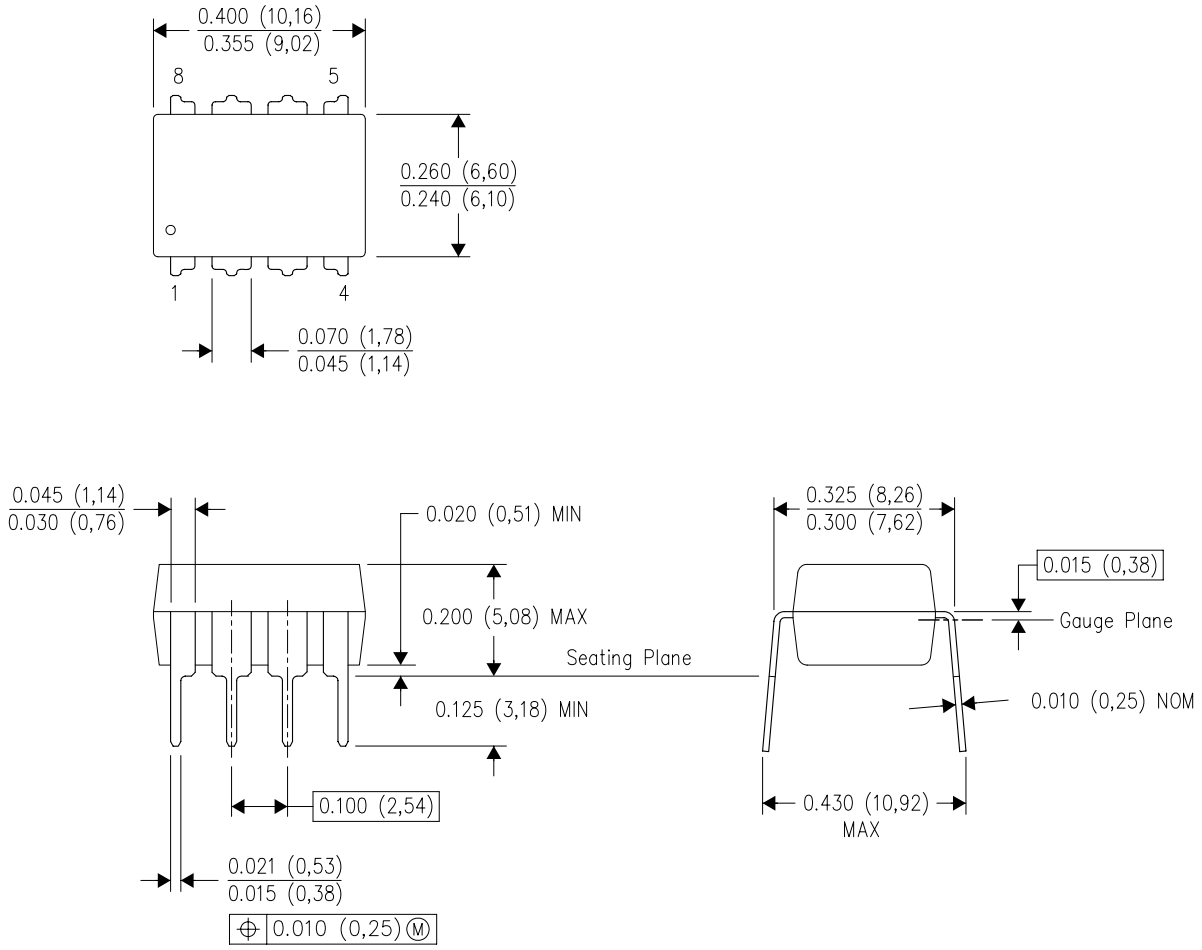
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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