TPS51100 3-A Sink / Source DDR Termination Regulator

1 Features

- Input Voltage Range: 4.75 V to 5.25 V
- VLDOIN Voltage Range: 1.2 V to 3.6 V
- 3-A Sink/Source Termination Regulator Includes Droop Compensation
- Requires Only 20-µF Ceramic Output Capacitance
- Supports Hi-Z in S3 and Soft-Off in S5
- 1.2-V Input (VLDOIN) Helps Reduce Total Power Dissipation
- Integrated Divider Tracks 0.5 VDDQSNS for VTT and VTTREF
- Remote Sensing (VTTSNS)
- ±20-mV Accuracy for VTT and VTTREF
- 10-mA Buffered Reference (VTTREF)
- Built-In Soft-Start, UVLO, and OCL
- Thermal Shutdown
- Supports JEDEC Specifications

2 Applications

- DDR, DDR2, DDR3 Memory Termination
- SSTL-2, SSTL-18, and HSTL Termination

3 Description

The TPS51100 is a 3-A, sink/source tracking termination regulator. The device is specifically designed for low-cost and low-external component count systems where space is a premium.

The TPS51100 maintains fast transient response, only requiring 20 µF (2 × 10 µF) of ceramic output capacitance. The TPS51100 supports remote sensing functions and all features required to power the DDR and DDR2 VTT bus termination according to the JEDEC specification. The part also supports DDR3 VTT termination with VDDQ at 1.5 V (typical). In addition, the TPS51100 includes integrated sleep-state controls, placing VTT in Hi-Z in S3 (suspend to RAM) and soft-off for VTT and VTTREF in S5 (suspend to disk). The TPS51100 is available in the thermally efficient 10-pin MSOP PowerPAD™ package and is specified from −40°C to 85°C.

Device Information (1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
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</thead>
<tbody>
<tr>
<td>TPS51100</td>
<td>HVSSOP (10)</td>
<td>3.00 mm x 3.00 mm</td>
</tr>
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</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

Capacitor | Manuf | Part Number |
----------|-------|-------------|
C1        | TDK   | C2012JB0J106K |
C2        | TDK   | C1608JB1H104K |

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<table>
<thead>
<tr>
<th>Changes from Revision D (May 2012) to Revision E</th>
<th>Page</th>
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<tbody>
<tr>
<td>• Added Pin Configuration and Functions section, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section</td>
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<tr>
<th>Changes from Revision C (June 2008) to Revision D</th>
<th>Page</th>
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<tr>
<td>• Added updated Thermal data</td>
<td>4</td>
</tr>
</tbody>
</table>
5 Pin Configuration and Functions

Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>NO</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>8</td>
<td>Signal ground. Connect to negative terminal of the output capacitor</td>
</tr>
<tr>
<td>PGND</td>
<td>4</td>
<td>Power ground output for the VTT LDO</td>
</tr>
<tr>
<td>S3</td>
<td>7</td>
<td>S3 signal input</td>
</tr>
<tr>
<td>S5</td>
<td>9</td>
<td>S5 signal input</td>
</tr>
<tr>
<td>VDDQSNS</td>
<td>1</td>
<td>VDDQ sense input</td>
</tr>
<tr>
<td>VIN</td>
<td>10</td>
<td>5-V power supply</td>
</tr>
<tr>
<td>VLDOIN</td>
<td>2</td>
<td>Power supply for the VTT LDO and VTTREF output stage</td>
</tr>
<tr>
<td>VTT</td>
<td>3</td>
<td>Power output for the VTT LDO</td>
</tr>
<tr>
<td>VTTREF</td>
<td>6</td>
<td>VTT reference output. Connect to GND through 0.1-μF ceramic capacitor.</td>
</tr>
<tr>
<td>VTTSNS</td>
<td>5</td>
<td>Voltage sense input for the VTT LDO. Connect to plus terminal of the output capacitor.</td>
</tr>
</tbody>
</table>

NOTE: For more information on the DGQ package, see the PowerPAD Thermally Enhanced Package application report (SLMA002).
6 Specifications

6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)(1)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage(2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIN, VLDOIN, VTTNS, VDDQSNS, S3, S5</td>
<td>–0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>PGND</td>
<td>–0.3</td>
<td>0.3</td>
<td></td>
</tr>
<tr>
<td>Output voltage(2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VTT, VTTSREF</td>
<td>–0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>TA</td>
<td>–40</td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td>Tstg</td>
<td>–55</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

6.2 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>4.75</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>Voltage range</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S3, S5</td>
<td>–0.1</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>VLDOIN, VDDQSNS, VTT, VTTSNS</td>
<td>–0.1</td>
<td>3.6</td>
<td></td>
</tr>
<tr>
<td>VTTREF</td>
<td>–0.1</td>
<td>1.8</td>
<td></td>
</tr>
<tr>
<td>PGND</td>
<td>–0.1</td>
<td>0.1</td>
<td></td>
</tr>
<tr>
<td>TA</td>
<td>–40</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

6.3 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TPS51100</th>
<th>UNIT</th>
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<tbody>
<tr>
<td>RJA</td>
<td>60.3</td>
<td></td>
</tr>
<tr>
<td>RJC(top)</td>
<td>63.5</td>
<td></td>
</tr>
<tr>
<td>RJB</td>
<td>51.6</td>
<td></td>
</tr>
<tr>
<td>ψJT</td>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td>ψJB</td>
<td>22.3</td>
<td></td>
</tr>
<tr>
<td>RJC(bot)</td>
<td>9.5</td>
<td></td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
### 6.4 Electrical Characteristics

$T_A = -40^\circ C$ to $85^\circ C$, $V_{VIN} = 5$ V, VLDOIN and VDDQSNS are connected to 2.5 V (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{VIN}$</td>
<td>Supply current, VIN</td>
<td>$T_A = 25^\circ C$, $V_{VIN} = 5$ V, no load, $V_{SS} = V_{SS} = 5$ V</td>
<td>0.25</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>$I_{VINSTB}$</td>
<td>Standby current, VIN</td>
<td>$T_A = 25^\circ C$, $V_{VIN} = 5$ V, no load, $V_{SS} = 0$ V, $V_{SS} = 5$ V</td>
<td>25</td>
<td>50</td>
<td>80</td>
</tr>
<tr>
<td>$I_{VNOTION}$</td>
<td>Shutdown current, VIN</td>
<td>$T_A = 25^\circ C$, $V_{VIN} = 5$ V, no load, $V_{SS} = V_{SS} = 0$ V, $V_{VLDOIN} = V_{VDDQSNS} = 0$ V</td>
<td>0.3</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>$I_{VLDOIN}$</td>
<td>Supply current, VLDOIN</td>
<td>$T_A = 25^\circ C$, $V_{VIN} = 5$ V, no load, $V_{SS} = V_{SS} = 5$ V</td>
<td>0.7</td>
<td>1.2</td>
<td>2</td>
</tr>
<tr>
<td>$I_{VLDOINSTB}$</td>
<td>Standby current, VLDOIN</td>
<td>$T_A = 25^\circ C$, $V_{VIN} = 5$ V, no load, $V_{SS} = 0$ V, $V_{SS} = 5$ V</td>
<td>6</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>$I_{VLDOINSDN}$</td>
<td>Shutdown current, VLDOIN</td>
<td>$T_A = 25^\circ C$, $V_{VIN} = 5$ V, no load, $V_{SS} = V_{SS} = 5$ V</td>
<td>0.3</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>$I_{VDDQSNS}$</td>
<td>Input current, VDDQSNS</td>
<td>$V_{VIN} = 5$ V, $V_{SS} = V_{SS} = 5$ V</td>
<td>1</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>$I_{VTTNS}$</td>
<td>Input current, VTNS</td>
<td>$V_{VIN} = 5$ V, $V_{SS} = V_{SS} = 5$ V</td>
<td>$-1$</td>
<td>$-0.25$</td>
<td>1</td>
</tr>
<tr>
<td><strong>VTT OUTPUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{VTTNS}$</td>
<td>Output voltage, VTT</td>
<td>$V_{VLDOIN} = V_{VDDQSNS} = 2.5$ V</td>
<td>1.25</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{VLDOIN} = V_{VDDQSNS} = 1.8$ V</td>
<td>0.9</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{VLDOIN} = V_{VDDQSNS} = 1.5$ V</td>
<td>0.75</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{VTTLTO}$</td>
<td>Output voltage tolerance to VTTREF, VTT</td>
<td>$V_{VLDOIN} = V_{VDDQSNS} = 2.5$ V, $</td>
<td>V_{VTT}</td>
<td>= 0$ A</td>
<td>$-20$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{VLDOIN} = V_{VDDQSNS} = 2.5$ V, $</td>
<td>V_{VTT}</td>
<td>= 1.5$ A</td>
<td>$-30$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{VLDOIN} = V_{VDDQSNS} = 2.5$ V, $</td>
<td>V_{VTT}</td>
<td>= 3$ A</td>
<td>$-40$</td>
</tr>
<tr>
<td>$V_{VTTLTOL}$</td>
<td>Output voltage tolerance to VTTREF, VTT</td>
<td>$V_{VLDOIN} = V_{VDDQSNS} = 1.8$ V, $</td>
<td>V_{VTT}</td>
<td>= 0$ A</td>
<td>$-20$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{VLDOIN} = V_{VDDQSNS} = 1.8$ V, $</td>
<td>V_{VTT}</td>
<td>= 1$ A</td>
<td>$-30$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{VLDOIN} = V_{VDDQSNS} = 1.8$ V, $</td>
<td>V_{VTT}</td>
<td>= 2$ A</td>
<td>$-40$</td>
</tr>
<tr>
<td>$V_{VTTLTOL}$</td>
<td>Output voltage tolerance to VTTREF, VTT</td>
<td>$V_{VLDOIN} = V_{VDDQSNS} = 1.5$ V, $</td>
<td>V_{VTT}</td>
<td>= 0$ A</td>
<td>$-20$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{VLDOIN} = V_{VDDQSNS} = 1.5$ V, $</td>
<td>V_{VTT}</td>
<td>= 1$ A</td>
<td>$-30$</td>
</tr>
<tr>
<td>$I_{VTTOCLRC}$</td>
<td>Source current limit, VTT</td>
<td>$V_{TT} = \left(\frac{V_{VDDQSNS}}{2}\right) \times 0.95$, PGOOD = High</td>
<td>3</td>
<td>3.8</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{VTT} = 0$ V</td>
<td>1.5</td>
<td>2.2</td>
<td>3</td>
</tr>
<tr>
<td>$I_{VTTOCLRN}$</td>
<td>Sink current limit, VTT</td>
<td>$V_{TT} = \left(\frac{V_{VDDQSNS}}{2}\right) \times 1.05$, PGOOD = High</td>
<td>3</td>
<td>3.6</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{VTT} = V_{VDOOD}$</td>
<td>1.5</td>
<td>2.2</td>
<td>3</td>
</tr>
<tr>
<td>$I_{VTTLK}$</td>
<td>Leakage current, VTT</td>
<td>$V_{TT} = \left(\frac{V_{VDDQSNS}}{2}\right) \times 1.25$ V, $T_A = 25^\circ C$</td>
<td>$-1$</td>
<td>0.5</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{SS} = 0$ V, $V_{SS} = 5$ V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{VTTSNSK}$</td>
<td>Leakage current, VTTSNS</td>
<td>$V_{TT} = \left(\frac{V_{VDDQSNS}}{2}\right) \times 1.25$ V, $T_A = 25^\circ C$</td>
<td>$-1$</td>
<td>0.01</td>
<td>1</td>
</tr>
<tr>
<td>$I_{ISCHG}$</td>
<td>Discharge current, VTT</td>
<td>$T_A = 25^\circ C$, $V_{VDDQSNS} = 0$ V, $V_{VTNS} = 0$ V, $V_{VTT} = 0.5$ V</td>
<td>10</td>
<td>17</td>
<td></td>
</tr>
<tr>
<td><strong>VTTREF OUTPUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{VTTREF}$</td>
<td>Output voltage, VTTREF</td>
<td>$V_{VDDQSNS} = 2.5$ V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{VTTREFTOL}$</td>
<td>Output voltage tolerance to VDDQSNS/2, VTTREF</td>
<td>$V_{VLDOIN} = V_{VDDQSNS} = 2.5$ V, $</td>
<td>V_{VTTREF}</td>
<td>&lt; 10$ mA</td>
<td>$-20$</td>
</tr>
<tr>
<td>$V_{VTTREFTOL}$</td>
<td>Output voltage tolerance to VDDQSNS/2, VTTREF</td>
<td>$V_{VLDOIN} = V_{VDDQSNS} = 1.8$ V, $</td>
<td>V_{VTTREF}</td>
<td>&lt; 10$ mA</td>
<td>$-17$</td>
</tr>
<tr>
<td>$V_{VTTREFTOL}$</td>
<td>Output voltage tolerance to VDDQSNS/2, VTTREF</td>
<td>$V_{VLDOIN} = V_{VDDQSNS} = 1.5$ V, $</td>
<td>V_{VTTREF}</td>
<td>&lt; 10$ mA</td>
<td>$-15$</td>
</tr>
<tr>
<td>$I_{VTTREFCL}$</td>
<td>Source current limit, VTTREF</td>
<td>$V_{VTTREF} = 0$ V</td>
<td>$-10$</td>
<td>20</td>
<td>30</td>
</tr>
</tbody>
</table>
### Electrical Characteristics (continued)

**T<sub>A</sub> = −40°C to 85°C, V<sub>VIN</sub> = 5 V, VLDOIN and VDDQSNS are connected to 2.5 V (unless otherwise noted)**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
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<tbody>
<tr>
<td><strong>UVLO/LOGIC THRESHOLD</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;VINUV&lt;/sub&gt;</td>
<td>Wake up</td>
<td>3.4</td>
<td>3.7</td>
<td>4.0</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Hysteresis</td>
<td>0.15</td>
<td>0.25</td>
<td>0.35</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;HI&lt;/sub&gt;</td>
<td>S3, S5</td>
<td>1.6</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>S3, S5</td>
<td>0.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;HYST&lt;/sub&gt;</td>
<td>S3, S5</td>
<td>0.2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>I&lt;sub&gt;LEAK&lt;/sub&gt;</td>
<td>S2, S5, T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td>−1</td>
<td></td>
<td>1</td>
<td>μA</td>
</tr>
<tr>
<td><strong>THERMAL SHUTDOWN</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T&lt;sub&gt;SDN&lt;/sub&gt;</td>
<td>Shutdown temperature</td>
<td>160</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>Hysteresis</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
6.5 Typical Characteristics

Figure 1. VIN Supply Current vs Temperature

Figure 2. VIN Shutdown Current vs Temperature

Figure 3. VIN Supply Current vs VTT Load Current

Figure 4. VLDOIN Supply Current vs Temperature

Figure 5. VLDOIN Shutdown Current vs Temperature

Figure 6. Discharge Current vs Temperature
Typical Characteristics (continued)

Figure 7. VTT Voltage Load Regulation vs VTT Load Current (DDR)

Figure 8. VTT Voltage Load Regulation vs VTT Load Current (DDR2)

Figure 9. VTT Voltage Load Regulation vs VTT Load Current (DDR3)

Figure 10. VTTREF Voltage Load Regulation vs VTTREF Load Current (DDR)

Figure 11. VTTREF Voltage Load Regulation vs VTTREF Load Current (DDR2)

Figure 12. VTTREF Voltage Load Regulation vs VTTREF Load Current (DDR3)
Typical Characteristics (continued)

Figure 13. VTT Voltage Load Transient Response

Figure 14. Startup Waveforms S5 Low-to-High

Figure 15. Startup Waveforms S3 Low-to-High

Figure 16. Shutdown Waveforms S3 High-to-Low

Figure 17. Shutdown Waveforms S3 and S5 High-to-Low

Figure 18. Bode Plot DDR Source
Typical Characteristics (continued)

**Figure 19. Bode Plot DDR Sink**

**Figure 20. Bode Plot DDR2 Source**

**Figure 21. Bode Plot DDR2 Sink**
7 Detailed Description

7.1 Overview
The TPS51100 is a sink / source double date rate (DDR) termination regulator with VTTREF buffered reference output.

7.2 Functional Block Diagram

![Simplified Block Diagram](image)

Figure 22. Simplified Block Diagram

7.3 Feature Description

7.3.1 VTT Sink/Source Regulator
The TPS51100 is a 3-A sink/source tracking termination regulator designed specially for low-cost, low-external-components systems where space is at premium, such as notebook PC applications. The TPS51100 integrates a high-performance, low-dropout linear regulator that is capable of sourcing and sinking current up to 3 A. This VTT linear regulator employs an ultimate fast-response feedback loop so that small ceramic capacitors are enough to keep tracking to the VTTREF within ±40 mV under all conditions, including fast load transient. To achieve tight regulation with minimum effect of trace resistance, a remote sensing terminal, VTTSNS, should be connected to the positive node of the VTT output capacitor(s) as a separate trace from the high-current line from VTT.

7.3.2 VTTREF Regulator
The VTTREF block consists of an on-chip 1/2 divider, low-pass filter (LPF), and buffer. This regulator can source current up to 10 mA. Bypass VTTREF to GND using a 0.1-μF ceramic capacitor to ensure stable operation.
Feature Description (continued)

7.3.3 Soft-Start

The soft-start function of the VTT is achieved via a current clamp, allowing the output capacitors to be charged with low and constant current that gives linear ramp-up of the output voltage. The current-limit threshold is changed in two stages using an internal powergood signal. When VTT is outside the powergood threshold, the current limit level is 2.2 A. When VTT rises above (VTTREF – 5%) or falls below (VTTREF + 5%), the current limit level switches to 3.8 A. The thresholds are typically VTTREF ±5% (from outside regulation to inside) and ±10% (when it falls outside). The soft-start function is completely symmetrical, and it works not only from GND to VTTREF voltage, but also from VDDQ to VTTREF voltage. Note that the VTT output is in a high-impedance state during the S3 state (S3 = low, S5 = high), and its voltage can be up to VDDQ voltage, depending on the external condition. Note that VTT does not start under a full-load condition.

7.3.4 VTT Current Protection

The LDO has a constant overcurrent limit (OCL) at 3.8 A. This trip point is reduced to 2.2 A before the output voltage comes within ±5% of the target voltage or goes outside of ±10% of the target voltage.

7.3.5 VIN UVLO Protection

For VIN undervoltage lockout (UVLO) protection, the TPS51100 monitors VIN voltage. When the VIN voltage is lower than UVLO threshold voltage, the VTT regulator is shut off. This is a non-latch protection.

7.3.6 Thermal Shutdown

TPS51100 monitors its temperature. If the temperature exceeds the threshold value, typically 160°C, the VTT and VTTREF regulators are shut off. This is also a non-latch protection.

7.4 Device Functional Modes

7.4.1 S5 Control and Soft-Off

The S3 and S5 terminals should be connected to SLP_S3 and SLP_S5 signals, respectively. Both VTTREF and VTT are turned on at the S0 state (S3 = high, S5 = high). VTTREF is kept alive while VTT is turned off and left high-impedance in the S3 state (S3 = low, S5 = high). Both VTT and VTTREF outputs are turned off and discharged to ground through internal MOSFETs during S4/S5 state (both S3 and S5 are low).

<table>
<thead>
<tr>
<th>STATE</th>
<th>S3</th>
<th>S5</th>
<th>VTTREF</th>
<th>VTT</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>H</td>
<td>H</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>S3(^{(1)})</td>
<td>L</td>
<td>H</td>
<td>1</td>
<td>0 (Hi-Z)</td>
</tr>
<tr>
<td>S4/S5(^{(1)})</td>
<td>L</td>
<td>L</td>
<td>0 (discharge)</td>
<td>0 (discharge)</td>
</tr>
</tbody>
</table>

\(^{(1)}\) In case S3 is forced to H and S5 to L, VTTREF is discharged and VTT is at Hi-Z state. This condition is not recommended.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The TPS51100 is typically used as a sink / source tracking termination regulator, which converts a voltage from VTT.

8.2 Typical Application

![Diagram of TPS51100 5-V Input / 1.8-V Output Reference Design]

Figure 23. TPS51100 5-V Input / 1.8-V Output Reference Design

8.2.1 Design Requirements

<table>
<thead>
<tr>
<th>DESIGN PARAMETERS</th>
<th>EXAMPLE VALUE</th>
</tr>
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<tbody>
<tr>
<td>VIN</td>
<td>4.75 V to 5.25 V</td>
</tr>
<tr>
<td>VDDQSNS, VLDOIN</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Output Current</td>
<td>±3 A</td>
</tr>
</tbody>
</table>

8.2.2 Detailed Design Procedure

<table>
<thead>
<tr>
<th>REFERENCE DESIGNATOR</th>
<th>SPECIFICATION</th>
<th>MANUFACTURER</th>
<th>PART NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>10-µF, 6.3-V, X5R, 2012 (0805)</td>
<td>TDK</td>
<td>C2012JB0J106K</td>
</tr>
<tr>
<td>C2</td>
<td>0.1-µF, 50-V, X5R, 1608 (0603)</td>
<td>TDK</td>
<td>C1608JB1H104K</td>
</tr>
</tbody>
</table>
8.2.2.1 Output Capacitor

For stable operation, total capacitance of the VTT output terminal can be equal to or greater than 20 μF. Attach two 10-μF ceramic capacitors in parallel to minimize the effect of ESR and ESL. If the ESR is greater than 2 mΩ, insert an R-C filter between the output and the VTTNS input to achieve loop stability. The R-C filter time constant should be almost the same or slightly lower than the time constant of the output capacitor and its ESR. Soft-start duration, \( t_{SS} \), is also a function of this output capacitance. Where \( I_{TTOCL} = 2.2 \) A (typ), \( t_{SS} \) can be calculated as,

\[
t_{SS} = \left( \frac{C_{OUT} \times V_{VTT}}{I_{VTTREF}} \right)
\]

(1)

8.2.2.2 Input Capacitor

Depending on the trace impedance between the VLDOIN bulk power supply to the part, transient increase of source current is supplied mostly by the charge from the VLDOIN input capacitor. Use a 10-μF (or more) ceramic capacitor to supply this transient charge. Provide more input capacitance as more output capacitance is used at VTT. In general, use 1/2 \( C_{OUT} \) for the input.

8.2.2.3 VIN Capacitor

Add a ceramic capacitor with a value between 1 μF and 4.7 μF placed close to the VIN pin, to stabilize 5 V from any parasitic impedance from the supply.

8.2.3 Application Curves

Figure 24. Start-Up Waveforms S5 Low-to-High

Figure 25. Start-Up Waveforms S3 Low-to-High
Figure 26. Shutdown Waveforms S3 High-to-Low
9 Power Supply Recommendations

TPS51100 is designed for a sink/source double data rate (DDR) termination regulator with VTTREF buffered reference output. Supply input voltage (VIN) support voltage from 4.75 V to 5.25 V; VLDOIN input voltage supports from 1.2 V to 3.6 V.

10 Layout

10.1 Layout Guidelines

Consider the following points before the layout of TPS51100 design begins.

- The input bypass capacitor for VLDOIN should be placed to the pin as close as possible with a short and wide connection.
- The output capacitor for VTT should be placed close to the pin with a short and wide connection in order to avoid additional ESR and/or ESL of the trace.
- VTTSNS should be connected to the positive node of VTT output capacitor(s) as a separate trace from the high current power line and is strongly recommended to avoid additional ESR and/or ESL. If it is needed to sense the voltage of the point of the load, it is recommended to attach the output capacitor(s) at that point. Also, it is recommended to minimize any additional ESR and/or ESL of the ground trace between the GND pin and the output capacitor(s).
- Consider adding an LPF at VTTSNS in case the ESR of the VTT output capacitor(s) is larger than 2 mΩ.
- VDDQSNS can be connected separately from VLDOIN. Remember that this sensing potential is the reference voltage of VTTREF. Avoid any noise generative lines.
- The negative node of the VTT output capacitor(s) and the VTTREF capacitor should be tied together, avoiding common impedance to the high-current path of the VTT source/sink current.
- The GND (signal GND) pin node represents the reference potential for the VTTREF and VTT outputs. Connect GND to the negative nodes of the VTT capacitor(s), VTTREF capacitor, and VDDQ capacitor(s) with care to avoid additional ESR and/or ESL. GND and PGND (Power GND) should be isolated, with a single point connection between them.
- In order to remove heat from the package effectively, prepare the thermal land and solder to the package thermal pad. The wide trace of the component-side copper, connected to this thermal land, helps heat spreading. Numerous vias 0.33 mm in diameter connected from the thermal land to the internal/solder-side ground plane(s) should be used to help dissipation.
10.2 Layout Example

NOTES: 1. The positive terminal of each output capacitor should be directly connected to VTT of the IC; do not use a VIA.
2. The negative terminal of each output capacitor should be directly connected to GND of the IC; do not use a VIA.
3. VIAs
   - VIA between 1st and 2nd layers
   - VIA between 1st and other layers under 2nd
4. Rs and Cs with dotted outlines are options.

Figure 27. TPS51100 PCB Layout Guideline

10.3 Thermal Considerations

As the TPS51100 is a linear regulator, the VTT current flow in both source and sink directions generates power dissipation from the device. In the source phase, the potential difference between $V_{VLDOIN}$ and $V_{VTT}$ times VTT current becomes the power dissipation, $W_{DSRC}$:

$$W_{DSRC} = (V_{VLDOIN} - V_{VTT}) \times I_{VTT}$$  \hspace{1cm} (2)$$

In this case, if VLDOIN is connected to an alternative power supply lower than $V_{DDQ}$ voltage, power loss can be decreased.

For the sink phase, VTT voltage is applied across the internal LDO regulator, and the power dissipation, and $W_{DSNK}$, is calculated by:

$$W_{DSNK} = V_{VTT} \times I_{VTT}$$  \hspace{1cm} (3)$$

Because the device does not sink and source the current at the same time and $I_{VTT}$ varies rapidly with time, the actual power dissipation that must be considered for thermal design is an average over the thermal relaxation duration of the system. Another power consumption is the current used for internal control circuitry from the VIN supply and VLDOIN supply. This can be estimated as 20 mW or less at normal operational conditions. This power must be effectively dissipated from the package. Maximum power dissipation allowed to the package is calculated by,

$$W_{PKG} = \frac{(T_{J(max)} - T_A(max))}{\theta_{JA}}$$  \hspace{1cm} (4)$$

where

$T_{J(max)}$ is 125°C
Thermal Considerations (continued)

$T_{A(max)}$ is the maximum ambient temperature in the system

$\theta_{JA}$ is the thermal resistance from the silicon junction to the ambient

This thermal resistance strongly depends on the board layout. TPS51100 is assembled in a thermally enhanced PowerPAD package that has an exposed die pad underneath the body. For improved thermal performance, this die pad must be attached to the ground trace via thermal land on the PCB. This ground trace acts as a heat sink/spread. The typical thermal resistance, 57.7°C/W, is achieved based on a 3 mm × 2 mm thermal land with two vias without air flow. It can be improved by using larger thermal land and/or increasing the number of vias. For example, assuming a 3 mm × 3 mm thermal land with four vias without air flow, it is 45.4°C/W. Further information about the PowerPAD package and its recommended board layout is described in the *PowerPAD Thermally Enhanced Package* application report (SLMA002). This document is available at [www.ti.com](http://www.ti.com).
11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer
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11.2 Trademarks
PowerPAD is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
# PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Lead finish/Ball material</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
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</thead>
<tbody>
<tr>
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<td>DGQ</td>
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<td>80</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAUAG</td>
<td>-40 to 85</td>
<td>51100</td>
<td>Samples</td>
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<td>DGQ</td>
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<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAUAG</td>
<td>-40 to 85</td>
<td>51100</td>
<td>Samples</td>
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<td>DGQ</td>
<td>10</td>
<td>2500</td>
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<td>NIPDAU</td>
<td>NIPDAUAG</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
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<td>HVSSOP</td>
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<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

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<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
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<th>SPQ</th>
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<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
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<td>1.4</td>
<td>8.0</td>
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<td>Q1</td>
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</table>

*All dimensions are nominal.

A0: Dimension designed to accommodate the component width
B0: Dimension designed to accommodate the component length
K0: Dimension designed to accommodate the component thickness
W: Overall width of the carrier tape
P1: Pitch between successive cavity centers
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
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<th>Device</th>
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<th>Width (mm)</th>
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<td>364.0</td>
<td>27.0</td>
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</table>
Notes:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.15.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.

E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

F. Falls within JEDEC MO-187 variation BA-1.

PowerPAD is a trademark of Texas Instruments.
THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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The exposed thermal pad dimensions for this package are shown in the following illustration.

Exposed Thermal Pad Dimensions

NOTE:  A.  All linear dimensions are in millimeters

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DGQ (S-PDSO-G10) PowerPAD™ PLASTIC SMALL OUTLINE

Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints

Stencil Openings based on a stencil
thickness of 0.127mm (0.005inch).
Reference table below for other
solder stencil thicknesses

(See Note E)

Increasing copper area will
enhance thermal performance
(See Note D)

8X(0.5)

SYMM

0.4

TYP

(0,8)

(0,4)

VIA

(2.2)

(1.83)

(1.89)

Example Solder Mask Defined Pad
(See Note C and D)

SYMM

0.8

TYP

(0,2)

1

Solder Mask
Over Copper

Example Non Soldermask Defined Pad

SYMM

0.05

TYP

(0,1)

10X(1.45)

10X(0.3)

(R0,05)

(0,05)

All Sides

Example Solder Mask Opening
(See Note F)

Pad Geometry

10X(1.45)

(R0,05)

(0,05)

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication
drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board.
Refer to Technical Brief, PowerPad
Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets
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metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

Center Power Pad Solder Stencil Opening

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<tr>
<th>Stencil Thickness</th>
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<th>Y</th>
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</thead>
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<td>2.06</td>
</tr>
<tr>
<td>0.127mm</td>
<td>1.89</td>
<td>1.83</td>
</tr>
<tr>
<td>0.152mm</td>
<td>1.73</td>
<td>1.67</td>
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<tr>
<td>0.178mm</td>
<td>1.60</td>
<td>1.55</td>
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</tbody>
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4207733-5/F 02/15

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