**TPS5516x-Q1 36-V, 1-A Output, 2-MHz, Single Inductor, Synchronous Step-Up and Step-Down Voltage Regulator**

### 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: \(-40^\circ\text{C to } +125^\circ\text{C}\) Ambient Operating Temperature
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- 2-V to 36-V Input Voltage Range for \(V_{OUT} = 5\text{ V}\)
- 5-V or 12-V Fixed Output Voltage (TPS55165-Q1)
- Adjustable Output Voltage Options from 5.7 V to 9 V (TPS55160-Q1 and TPS55162-Q1)
- Up to 85% Efficiency
- 1-A Output Current for \(V_{OUT} = 5\text{ V}\) and \(V_{IN} \geq 5.3\text{ V}\)
- 0.8-A Output Current for \(V_{OUT} = 5\text{ V}\) and \(V_{IN} \geq 3.8\text{ V}\)
- 0.4-A Output Current for \(V_{OUT} = 5\text{ V}\) and \(V_{IN} \geq 2.3\text{ V}\)
- Automatic Transition Between Step-Down and Step-Up Mode
- Low-Power Mode for Improved Efficiency at Light Load Conditions (TPS55160-Q1 and TPS55165-Q1)
- Device Quiescent Current Less than 15 \(\mu\text{A}\) in Low-Power Mode (TPS55160-Q1 and TPS55165-Q1)
- Device Shutdown Current Less than 3 \(\mu\text{A}\)
- Forced Fixed-Frequency Operation at 2 MHz
- Selectable Spread Spectrum (TPS55160-Q1 and TPS55165-Q1)
- Wake-up Through IGN With Power-Latch Function
- Smart Power-Good Output With Configurable Delay Time
- Overtemperature Protection and Output Overvoltage Protection
- Available in Easy-to-Use 20-Pin HTSSOP PowerPAD™ Package

### 2 Applications

- Start-Stop Sensitive Automotive Power Applications
  - Infotainment and Cluster
  - Body Electronics and Gateway Modules
- Industrial Applications With Fluctuating Input Voltage
  - Solar-to-Battery Charging
  - Li-Ion Battery Packs

### 3 Description

The TPS5516x-Q1 family of devices is a high-voltage synchronous buck-boost DC-DC converter. The device provides a stable power-supply output from a wide varying input-power supply such as an automotive car battery. The buck-boost overlap control ensures automatic transition between step-down and step-up mode with optimal efficiency. The TPS55165-Q1 output voltage can be set to a fixed level of 5 V or 12 V. The TPS55160-Q1 and TPS55162-Q1 devices have a configurable output voltage ranging from 5.7 V to 9 V that is set by an external resistive divider.

Output currents can be as high as 1 A for a normal car battery voltage, and can be maintained at 0.4 A for lower input voltages, such as those for common battery-cranking profiles. The buck-boost converter is based on a fixed-frequency, pulse-width-modulation (PWM) control circuit using synchronous rectification to obtain maximum efficiency. The switching frequency is set to 2 MHz (typical) which allows for the usage of a small inductor that uses less board space.

### Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS55160-Q1</td>
<td>HTSSOP (20)</td>
<td>6.50 mm × 4.40 mm</td>
</tr>
<tr>
<td>TPS55162-Q1</td>
<td>HTSSOP (20)</td>
<td>6.50 mm × 4.40 mm</td>
</tr>
<tr>
<td>TPS55165-Q1</td>
<td>HTSSOP (20)</td>
<td>6.50 mm × 4.40 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Available for preview.

### Simplified Schematic

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An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>November 2017</td>
<td>*</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>
5 Description (continued)
A selectable spread-spectrum option (TPS55160-Q1 and TPS55165-Q1) helps reduce radiated electromagnetic interference (EMI). Internal loop compensation eliminates the need for external compensation components. In low-power mode (TPS55160-Q1 and TPS55165-Q1), the device achieves a quiescent current of less than 15 µA which allows an automotive electronic control unit (ECU) to stay in standby mode (for example, listen-to-CAN mode) while achieving OEM quiescent-current requirements. The low-power mode can be disabled which forces the converter to operate in full continuous mode at a fixed switching frequency of 2 MHz (typical) for the entire load-current range. The maximum average current in the inductor is limited to a typical value of 2 A.

The converter can be disabled to minimize battery drain. Furthermore, the device offers a power-good (PG) pin to indicate when the output rail is less than the specified tolerance. The device also has a power-latch function to allow an external microcontroller unit (MCU) to keep the output voltage available for as long as needed.

The device is available in a 20-pin HTSSOP PowerPAD package.

6 Pin Configuration and Functions

![Pin Configuration Diagram](image)

### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O(1)</th>
<th>TYPE(2)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>PGND</td>
<td>I</td>
<td>G</td>
<td>Power-ground pin</td>
</tr>
<tr>
<td>L1</td>
<td>I</td>
<td>A</td>
<td>Buck power-stage switch node. Connect an inductor with a nominal value of 4.7 µH between the L1 and L2 pins.</td>
</tr>
<tr>
<td>BST1</td>
<td>I</td>
<td>A</td>
<td>Bootstrap node for the buck power stage. Connect a 100-nF capacitor between this pin and the L1 pin.</td>
</tr>
<tr>
<td>VINP</td>
<td>—</td>
<td>P</td>
<td>Supply-power input voltage. Connect this pin to the input supply line.</td>
</tr>
<tr>
<td>VINL</td>
<td>—</td>
<td>P</td>
<td>Supply-input voltage for internal biasing. Connect this pin to the input supply line.</td>
</tr>
<tr>
<td>IGN</td>
<td>I</td>
<td>D</td>
<td>Ignition-enable input signal. The ignition is enabled when this pin is high (1) and is disabled when this pin is low (0).</td>
</tr>
<tr>
<td>PS</td>
<td>I</td>
<td>D</td>
<td>Logic-level input signal to enable and disable low-power mode. The power mode is low-power mode when this pin is high (1) and is normal mode when this pin is low (1).</td>
</tr>
</tbody>
</table>

(1) I = Input Pin, O = Output Pin
(2) A = Analog Pin, D = Digital Pin, G = Ground Pin, P = Power Pin
## Pin Functions (continued)

<table>
<thead>
<tr>
<th>PIN</th>
<th>NO.</th>
<th>I/O(1)</th>
<th>TYPE(2)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>IGN_PWRL</td>
<td>8</td>
<td>I</td>
<td>D</td>
<td>Logic-level IGN power-latch signal. The IGN pin is latched when this pin is high (1) and is not latched when this pin is low (0).</td>
</tr>
<tr>
<td>SS_EN</td>
<td>9</td>
<td>I</td>
<td>D</td>
<td>Configuration pin to enable and disable the spread-Spectrum. The spread-spectrum feature is enabled when this pin is open and disabled when this pin is low.</td>
</tr>
<tr>
<td>PG_DLY</td>
<td>10</td>
<td>I</td>
<td>A</td>
<td>Configuration pin for power-good delay time. Connect this pin to a resistor with a value from 10kΩ to 100kΩ to configure the PG delay time from 0.5 ms to 40 ms. Connect this pin to ground for the default PG delay time which is 2 ms (typical).</td>
</tr>
<tr>
<td>VREG_Q(3)</td>
<td>11</td>
<td>I</td>
<td>A</td>
<td>Quiet feedback pin for the gate-drive supply of the buck-boost power stages. This pin must be connected close to the top side of the 4.7-µF (typical) decoupling capacitor at the VREG output pin.</td>
</tr>
<tr>
<td>VREG</td>
<td>12</td>
<td>O</td>
<td>A</td>
<td>Gate-drive supply for the buck-boost power stages. Apply a 4.7-µF (typical) decoupling capacitor at this pin to the power ground. The VREG pin cannot drive external loads in the application.</td>
</tr>
<tr>
<td>GND</td>
<td>13</td>
<td>—</td>
<td>G</td>
<td>Analog ground</td>
</tr>
<tr>
<td>VOS_FB</td>
<td>14</td>
<td>I</td>
<td>A</td>
<td>For the TPS55160-Q1 and TPS55162-Q1 devices, this pin is used to adjust the VOUT configuration. Connect this pin to a resistive feedback network with less than 1-MΩ total resistance between the VOUT pin, FB pin, and GND pin (analog ground). For the TPS55165-Q1 device, this pin is used to select the output voltage. The output voltage is set to 5 V when this pin is connected to the GND pin. The output voltage is 12 V when this pin is connected to the VREG pin.</td>
</tr>
<tr>
<td>PG</td>
<td>15</td>
<td>O</td>
<td>D</td>
<td>Output power good pin. This pin is an open-drain pin. The status of the power-good output is good when this pin is high (1) and has a failure when this pin is low (0).</td>
</tr>
<tr>
<td>VOUT_SENSE</td>
<td>16</td>
<td>I</td>
<td>A</td>
<td>Sense pin for the buck-boost converter output voltage. This pin must be connected to the VOUT pin.</td>
</tr>
<tr>
<td>VOUT</td>
<td>17</td>
<td>O</td>
<td>A</td>
<td>Buck-boost converter output voltage</td>
</tr>
<tr>
<td>GND</td>
<td>18</td>
<td>—</td>
<td>G</td>
<td>Analog ground</td>
</tr>
<tr>
<td>BST2</td>
<td>19</td>
<td>I</td>
<td>A</td>
<td>Bootstrap node for the boost power-stage. Connect a typical 100-nF capacitor between this pin and the L2 pin.</td>
</tr>
<tr>
<td>L2</td>
<td>20</td>
<td>I</td>
<td>A</td>
<td>Boost power-stage switch node. Connect an inductor with a nominal value of 4.7 µH between the L1 and L2 pins.</td>
</tr>
<tr>
<td>PowerPAD</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>The thermal pad must be soldered to the power ground to achieve the appropriate power dissipation through the analog ground plane.</td>
</tr>
</tbody>
</table>

(3) The VREG_Q pin must be connected to the VREG pin at all times while the device is in operation to prevent possible electrostatic over stress (EOS) damage to the device.
7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)\(^{(1)}\) \(^{(2)}\)

<table>
<thead>
<tr>
<th>POS</th>
<th>Description</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1.1</td>
<td>Protected battery voltage</td>
<td>VINP, VINL</td>
<td>–0.3</td>
<td>40</td>
</tr>
<tr>
<td>M1.2</td>
<td>Feedback voltage</td>
<td>VOS_FB</td>
<td>–0.3</td>
<td>5.5</td>
</tr>
<tr>
<td>M1.3</td>
<td>Low-power mode input</td>
<td>PS</td>
<td>–0.3</td>
<td>40</td>
</tr>
<tr>
<td>M1.4</td>
<td>Low-voltage inputs</td>
<td>IGN_PWRL, SS_EN, PG_DLY</td>
<td>–0.3</td>
<td>5.5</td>
</tr>
<tr>
<td>M1.5</td>
<td>Ignition enable input</td>
<td>IGN</td>
<td>–7</td>
<td>40</td>
</tr>
<tr>
<td>M1.6</td>
<td>Buck-boost output voltage</td>
<td>VOUT, VOUT_SENSE</td>
<td>–0.3</td>
<td>20</td>
</tr>
<tr>
<td>M1.7</td>
<td>Gate-driver supply</td>
<td>VREG, VREG_Q</td>
<td>–0.3</td>
<td>5.5</td>
</tr>
<tr>
<td>M1.8</td>
<td>Buck switching node voltage</td>
<td>L1</td>
<td>–0.3</td>
<td>40</td>
</tr>
<tr>
<td>M1.9</td>
<td>Boost switching node voltage</td>
<td>L2</td>
<td>–0.3</td>
<td>20</td>
</tr>
<tr>
<td>M1.10</td>
<td>Boot-strap overdrive voltage</td>
<td>BST1-L1, BST2-L2</td>
<td>–0.3</td>
<td>5.5</td>
</tr>
<tr>
<td>M1.11</td>
<td>Power-good output voltage</td>
<td>PG</td>
<td>–0.3</td>
<td>15</td>
</tr>
<tr>
<td>M1.12</td>
<td>Ground</td>
<td>PGND, GND</td>
<td>–0.3</td>
<td>0.3</td>
</tr>
<tr>
<td>M2</td>
<td>Junction temperature, (T_J)</td>
<td></td>
<td>–40</td>
<td>150</td>
</tr>
<tr>
<td>M3</td>
<td>Storage temperature, (T_{stg})</td>
<td></td>
<td>–65</td>
<td>175</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

7.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{(ESD)})</td>
<td>Human-body model (HBM), per AEC Q100-002(^{(1)})</td>
</tr>
<tr>
<td>All pins</td>
<td>±2000</td>
</tr>
<tr>
<td>Corner pins (1, 10, 11, and 20)</td>
<td>±500</td>
</tr>
</tbody>
</table>

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>POS</th>
<th>Description</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1.1a</td>
<td>Supply voltage at VINP and VINL pins (after wake-up)</td>
<td>TPS55165-Q1 with VOS_FB pin connected to GND</td>
<td>2</td>
<td>36</td>
</tr>
<tr>
<td>R1.1b</td>
<td>Supply voltage at VINP and VINL pins (after wake-up)</td>
<td>TPS55165-Q1 with VOS_FB pin connected to VREG</td>
<td>4</td>
<td>36</td>
</tr>
<tr>
<td>R1.1c</td>
<td>Supply voltage at VINP and VINL pins (after wake-up)</td>
<td>TPS55160-Q1 and TPS55162-Q1</td>
<td>3.6</td>
<td>36</td>
</tr>
<tr>
<td>R1.2a</td>
<td>Output voltage at VOUT and VOUT_SENSE pins</td>
<td>TPS55160-Q1 and TPS55162-Q1</td>
<td>0</td>
<td>12</td>
</tr>
<tr>
<td>R1.2b</td>
<td>Output voltage at PG pin</td>
<td>TPS55160-Q1 and TPS55162-Q1</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>R1.3</td>
<td>Input voltage on IGN pin</td>
<td>TPS55160-Q1 and TPS55162-Q1</td>
<td>0</td>
<td>36</td>
</tr>
<tr>
<td>R1.4</td>
<td>Input voltage on logic pins IGN_PWRL, PS and SS_EN</td>
<td>TPS55160-Q1 and TPS55162-Q1</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>R1.5a</td>
<td>Input voltage on VOS_FB pin</td>
<td>TPS55165-Q1</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>R1.5b</td>
<td>Input voltage on VOS_FB pin</td>
<td>TPS55160/2-Q1</td>
<td>0</td>
<td>0.8</td>
</tr>
<tr>
<td>R2.1</td>
<td>Operating free air temperature, (T_A)</td>
<td></td>
<td>–40</td>
<td>125</td>
</tr>
<tr>
<td>R2.2</td>
<td>Operating virtual junction temperature, (T_{J})</td>
<td></td>
<td>–40</td>
<td>150</td>
</tr>
</tbody>
</table>
7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TPS5516x-Q1</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{JA})</td>
<td>Junction-to-ambient thermal resistance</td>
<td>35.4</td>
</tr>
<tr>
<td>(R_{JC(top)})</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>19.8</td>
</tr>
<tr>
<td>(R_{JB})</td>
<td>Junction-to-board thermal resistance</td>
<td>16.8</td>
</tr>
<tr>
<td>(V_{JT})</td>
<td>Junction-to-top characterization parameter</td>
<td>0.5</td>
</tr>
<tr>
<td>(V_{JB})</td>
<td>Junction-to-board characterization parameter</td>
<td>16.5</td>
</tr>
<tr>
<td>(R_{JC(bot)})</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>0.9</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics — External Components

Over operating free air temperature range –40°C ≤ \(T_A\) ≤ 125°C and maximum junction temperature \(T_J = 150°C\) and recommended operating input supply range (unless otherwise noted)(1)

<table>
<thead>
<tr>
<th>POS</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>AN.1</td>
<td>(C_{OUT})</td>
<td>Value of output ceramic capacitor</td>
<td>Connect between VOUT and PGND</td>
<td>18</td>
<td>22</td>
<td>47</td>
</tr>
<tr>
<td>AN.1a</td>
<td>ESR (C_{OUT})</td>
<td>Value of ESR of output capacitor, (C_{OUT})</td>
<td>0</td>
<td>100</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>AN.2</td>
<td>(C_{BST})</td>
<td>Value of bootstrap ceramic capacitor</td>
<td>ESR &lt; 10 mΩ. Connect between BST1 and L1 with respect to BST2 and L2</td>
<td>100</td>
<td>nF</td>
<td></td>
</tr>
<tr>
<td>AN.2a</td>
<td>ESR (C_{BST})</td>
<td>Value of ESR of bootstrap ceramic capacitor, (C_{BST})</td>
<td>0</td>
<td>10</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>AN.3</td>
<td>(L)</td>
<td>Value of inductor</td>
<td>Saturation current &gt; 2.5 A, ESR &lt; 30 mΩ</td>
<td>3.3</td>
<td>4.7</td>
<td>6.2</td>
</tr>
<tr>
<td>AN.3a</td>
<td>DCR (L)</td>
<td>Value of DCR of inductor</td>
<td>0</td>
<td>40</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>AN.4</td>
<td>(C_{IN})</td>
<td>Value of supply input ceramic capacitor</td>
<td>40-V compliant. Connect between VIN and PGND</td>
<td>8.2</td>
<td>10</td>
<td>µF</td>
</tr>
<tr>
<td>AN.4a</td>
<td>ESR (C_{IN})</td>
<td>Value of ESR of input capacitor, (C_{IN})</td>
<td>0</td>
<td>100</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>AN.5</td>
<td>(C_{VREG})</td>
<td>Decoupling capacitor on VREG pin to ground</td>
<td>Connect between VREG and PGND</td>
<td>3.9</td>
<td>4.7</td>
<td>5.6</td>
</tr>
<tr>
<td>AN.5a</td>
<td>ESR (C_{VREG})</td>
<td>Value of ESR of input capacitor, (C_{VREG})</td>
<td>0</td>
<td>10</td>
<td>mΩ</td>
<td></td>
</tr>
</tbody>
</table>

(1) The term \(V_{IN}\) refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

7.6 Electrical Characteristics — Supply Voltage (VINP, VINL pins)

Over operating free air temperature range –40°C ≤ \(T_A\) ≤ 125°C and maximum junction temperature \(T_J = 150°C\) and recommended operating input supply range (unless otherwise noted)(1)

<table>
<thead>
<tr>
<th>POS</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1a</td>
<td>(V_{IN})</td>
<td>Operating supply input voltage</td>
<td>Applied at VINP and VINL pins, after device startup</td>
<td>2</td>
<td>14</td>
<td>36</td>
</tr>
<tr>
<td>1.1b</td>
<td>(V_{IN})</td>
<td>Minimum input voltage for startup</td>
<td>Applied at VIN and VINL pins; (T_J = 25°C). This minimum voltage is required until VOUT &gt; PG(\text{TH,UV}); (I_{\text{VOUT}} &lt; 400 \text{ mA}, C_{\text{VOUT}} = 22 \text{ µF})</td>
<td>4</td>
<td>14</td>
<td>36</td>
</tr>
<tr>
<td>1.1c</td>
<td>(V_{IN})</td>
<td>VIN Shutdown supply current</td>
<td>(V_{IN} = 12 \text{ V}, V_{\text{IGN}} = 0 \text{ V}, V_{\text{PG}} = 0 \text{ V}, V_{\text{IGN, PWRL}} = 0 \text{ V}, T_J = 25°C)</td>
<td>5.3</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

(1) The term \(V_{IN}\) refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).
### Electrical Characteristics — Supply Voltage (VINP, VINL pins) (continued)

Over operating free air temperature range $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ and maximum junction temperature $T_J = 150^\circ\text{C}$ and recommended operating input supply range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>POS</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.4</td>
<td>$I_Q$</td>
<td>VIN Quiescent supply current</td>
<td>TPS55165-Q1: $V_{IN} = V_{IGN} = 12\text{ V}$, $V_{OUT} = 5\text{ V}$, $I_{OUT} = 0\text{ mA}$, $T_J = 25^\circ\text{C}$ Device in low-power mode, Non-switching VOS_FB pin connected to GND</td>
<td>0</td>
<td>15</td>
<td>µA</td>
</tr>
</tbody>
</table>

### 7.7 Electrical Characteristics — Reference Voltage (VOS_FB Pin) and Output Voltage (VOUT Pin)

Over operating free air temperature range $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ and maximum junction temperature $T_J = 150^\circ\text{C}$ and recommended operating input supply range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>POS</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1a</td>
<td>$V_{FB_NM_adj}$</td>
<td>Feedback voltage in normal mode for adjustable $V_{OUT}$ setting(^{(2)})</td>
<td>TPS55160/2-Q1: Measured at VOS_FB pin Resistive divider with total resistance $&lt; 1\text{ M}\Omega$ connected between VOUT, VOS_FB, and GND pins</td>
<td>0.784</td>
<td>0.8</td>
<td>0.816</td>
</tr>
<tr>
<td>2.1b</td>
<td>$V_{FB_NM_5V}$</td>
<td>Feedback voltage in normal mode for $V_{OUT}$ in fixed 5-V setting(^{(2)})</td>
<td>TPS55165-Q1: Measured at VOUT_SENSE pin VOS_FB pin connected to GND; VOUT pin connected to VOUT_SENSE</td>
<td>4.9</td>
<td>5</td>
<td>5.1</td>
</tr>
<tr>
<td>2.1c</td>
<td>$V_{FB_NM_12V}$</td>
<td>Feedback voltage in normal mode for $V_{OUT}$ in fixed 12-V setting(^{(2)})</td>
<td>TPS55165-Q1: Measured at VOUT_SENSE pin VOS_FB pin connected to VREG; VOUT pin connected to VOUT_SENSE</td>
<td>11.76</td>
<td>12</td>
<td>12.24</td>
</tr>
<tr>
<td>2.2a</td>
<td>$V_{FB_PS_adj}$</td>
<td>Feedback voltage in low-power mode for adjustable $V_{OUT}$ setting(^{(3)})</td>
<td>TPS55160/2-Q1: Measured at VOS_FB pin Resistive divider with total resistance $&lt; 1\text{ M}\Omega$ connected between VOUT, VOS_FB, and GND pins</td>
<td>0.776</td>
<td>0.8</td>
<td>0.824</td>
</tr>
<tr>
<td>2.2b</td>
<td>$V_{FB_PS_5V}$</td>
<td>Feedback voltage in low-power mode for $V_{OUT}$ in 5-V setting(^{(3)})</td>
<td>TPS55165-Q1: Measured at VOUT_SENSE pin VOS_FB pin connected to GND; VOUT pin connected to VOUT_SENSE</td>
<td>4.85</td>
<td>5</td>
<td>5.15</td>
</tr>
<tr>
<td>2.2c</td>
<td>$V_{FB_PS_12V}$</td>
<td>Feedback voltage in low-power mode for $V_{OUT}$ in 12-V setting(^{(3)})</td>
<td>TPS55165-Q1: Measured at VOUT_SENSE pin VOS_FB pin connected to VREG; VOUT pin connected to VOUT_SENSE</td>
<td>11.64</td>
<td>12</td>
<td>12.36</td>
</tr>
<tr>
<td>2.3</td>
<td>$V_{OUT_OL}$</td>
<td>Adjustable output voltage range</td>
<td>TPS55160/2-Q1: Measured at VOUT_SENSE pin</td>
<td>5.7</td>
<td>9</td>
<td></td>
</tr>
<tr>
<td>2.6</td>
<td>$R_{PD_VOUT}$</td>
<td>Pulldown discharge resistance at VOUT</td>
<td>Device in OFF state, INIT state, or PRE_RAMP state; $V_{IGN} = 0\text{ V}$, $V_{PS} = 0\text{ V}$, $V_{IGN_PWRL} = 0\text{ V}$</td>
<td>250</td>
<td>365</td>
<td>850</td>
</tr>
</tbody>
</table>

\(^{(1)}\) The term $V_{IN}$ refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

\(^{(2)}\) $V_{PS} = 0\text{ V}$: Average DC value excluding ripple and load transients for $V_{IN}$ and load current ranges as specified in $I_{VOUT}$. Inclusive DC line and load regulation, temperature drift, and long term drift.

\(^{(3)}\) $V_{PS} = 5\text{ V}$: Average DC value excluding ripple and load transients for $V_{IN}$ and load current ranges as specified in $I_{VOUT}$. Inclusive DC line and load regulation, temperature drift, and long term drift.

### 7.8 Electrical Characteristics — Buck-Boost

Over operating free air temperature range $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ and maximum junction temperature $T_J = 150^\circ\text{C}$ and recommended operating input supply range (unless otherwise noted)\(^{(1)}\)

\(^{(1)}\) The term $V_{IN}$ refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).
Electrical Characteristics — Buck-Boost (continued)

Over operating free air temperature range –40°C ≤ TA ≤ 125°C and maximum junction temperature TJ = 150°C and recommended operating input supply range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOUT_5V</td>
<td>Max output current in normal operation for VOUT in 5-V setting</td>
<td>6 V ≤ VIN; DCR ≤ 40 mΩ</td>
<td>1</td>
<td>A</td>
<td>mA</td>
</tr>
<tr>
<td>IOUT_12V</td>
<td>Max output current in normal operation for VOUT in 12-V setting</td>
<td>9.2 V ≤ VIN ≤ 14 V; DCR ≤ 40 mΩ</td>
<td>14 V ≤ VIN; DCR ≤ 40 mΩ</td>
<td>800</td>
<td>mA</td>
</tr>
<tr>
<td>IOUT_adj_Vout</td>
<td>Max output current in normal operation for adjustable configuration, 8V &lt; VOUT &lt; 9V</td>
<td>0.76 * VOUT ≤ VIN ≤ (VOUT + 2V); DCR ≤ 40 mΩ</td>
<td>0.46 * VOUT ≤ VIN ≤ 0.76 * VOUT; DCR ≤ 40 mΩ</td>
<td>3.6 V ≤ VIN ≤ 0.46 * VOUT; DCR ≤ 40 mΩ</td>
<td>800</td>
</tr>
<tr>
<td>IOUT_adj_Vout</td>
<td>Max output current in normal operation for adjustable configuration, 5.7V ≤ VOUT ≤ 8V</td>
<td>0.76 * VOUT ≤ VIN ≤ (VOUT + 1V); DCR ≤ 40 mΩ</td>
<td>3.6 V ≤ VIN ≤ 0.76 * VOUT; DCR ≤ 40 mΩ</td>
<td>300</td>
<td>mA</td>
</tr>
<tr>
<td>OUT_PS</td>
<td>Max output current in low-power mode</td>
<td>500</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rson_Buck_HS</td>
<td>On-resistance buck-stage high-side (HS) FET</td>
<td>150</td>
<td>300</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>Rson_Buck_LS</td>
<td>On-resistance buck-stage low-side (LS) FET</td>
<td>150</td>
<td>300</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>Rson_Boost_HS</td>
<td>On-resistance boost-stage HS FET</td>
<td>150</td>
<td>300</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>Rson_Boost_LS</td>
<td>On-resistance boost-stage LS FET</td>
<td>150</td>
<td>300</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>ISW_limit</td>
<td>Peak current limit for HS buck, LS buck, and LS boost</td>
<td>Device in normal operating mode</td>
<td>2</td>
<td>3.5</td>
<td>4.5</td>
</tr>
<tr>
<td>IcoilAvglimit</td>
<td>Average coil current limit</td>
<td>Device in normal operating mode; L = 4.7 µH</td>
<td>2</td>
<td>2.8</td>
<td>A</td>
</tr>
<tr>
<td>TLDSR_5V_100</td>
<td>Transient load step response for VOUT in 5-V setting</td>
<td>TPS55165-Q1: Measured at VOUTSENSE pin; VIN = 12 V, IOUT = 0.1 A to 0.5 A, TR = TF = 1 µs, COUT = 47 µF</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TLDSR_5V_500</td>
<td>Transient load step response for VOUT in 5-V setting</td>
<td>TPS55165-Q1: Measured at VOUTSENSE pin; VIN = 12 V, IOUT = 0.5 A to 1 A, TR = TF = 1 µs, COUT = 47 µF</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vripple_5V</td>
<td>Output ripple for VOUT in 5-V setting</td>
<td>TPS55165-Q1: Measured at VOUTSENSE pin; VIN = 12 V, IOUT = 1 A, SS_EN = low</td>
<td>5.5</td>
<td>mVpp</td>
<td></td>
</tr>
<tr>
<td>Vripple_12V</td>
<td>Output ripple for VOUT in 12-V setting</td>
<td>TPS55165-Q1: Measured at VOUTSENSE pin; VIN = 14 V, IOUT = 0.8 A, SS_EN = low</td>
<td>5</td>
<td>mVpp</td>
<td></td>
</tr>
</tbody>
</table>
## 7.9 Electrical Characteristics — Undervoltage and Overvoltage Lockout

Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)

<table>
<thead>
<tr>
<th>POS</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.1a</td>
<td>UVLO</td>
<td>VIN Undervoltage (UV) lockout threshold</td>
<td>1.8</td>
<td>2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>4.1b</td>
<td>UVLO</td>
<td>VIN Undervoltage (UV) lockout threshold</td>
<td>3.6</td>
<td>4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>4.1c</td>
<td>UVLO</td>
<td>VIN Undervoltage (UV) lockout threshold</td>
<td>1.8</td>
<td>2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>4.2</td>
<td>OVLO</td>
<td>VIN Overvoltage (OV) lockout threshold</td>
<td>36</td>
<td>40</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>4.9</td>
<td>VOUT_PROT_OV</td>
<td>VOUT OV protection</td>
<td>110%</td>
<td>125%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) The term VIN refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

## 7.10 Electrical Characteristics — IGN Wakeup

Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)

<table>
<thead>
<tr>
<th>POS</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.1a</td>
<td>IGN_WAKE</td>
<td>IGN wake-up threshold</td>
<td>2.5</td>
<td>3</td>
<td>3.7</td>
<td>V</td>
</tr>
<tr>
<td>5.1b</td>
<td>IGN_BD</td>
<td>IGN power-down threshold</td>
<td>1.5</td>
<td>2.1</td>
<td>2.7</td>
<td>V</td>
</tr>
<tr>
<td>5.2</td>
<td>IGN_HYST</td>
<td>IGN wake-up hysteresis</td>
<td>0.76</td>
<td>1</td>
<td>1.35</td>
<td>V</td>
</tr>
<tr>
<td>5.3a</td>
<td>I_IGN 36V</td>
<td>IGN pin forward input current at 36 V</td>
<td>11</td>
<td>17</td>
<td>30</td>
<td>μA</td>
</tr>
<tr>
<td>5.3b</td>
<td>I_IGN 12V</td>
<td>IGN pin forward input current at 12 V</td>
<td>2.3</td>
<td>3.7</td>
<td>7.1</td>
<td>μA</td>
</tr>
<tr>
<td>5.5</td>
<td>I_IGNnev</td>
<td>IGN pin reverse current</td>
<td>370</td>
<td>650</td>
<td></td>
<td>μA</td>
</tr>
</tbody>
</table>

(1) The term VIN refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

## 7.11 Electrical Characteristics — Logic Pins PS, IGN_PWRL, SS_EN

Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)

<table>
<thead>
<tr>
<th>POS</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.1</td>
<td>VLOGIC_IN_HIGH</td>
<td>Logic input low-to-high threshold for pins IGN_PWRL PS, and SS_EN</td>
<td>2</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>6.2</td>
<td>VLOGIC_IN_LOW</td>
<td>Logic input high-to-low threshold for pins IGN_PWRL PS, and SS_EN</td>
<td>0.74</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>6.3</td>
<td>VLOGIC_IN_HYST</td>
<td>Logic input hysteresis for pins IGN_PWRL PS, and SS_EN</td>
<td>0.15</td>
<td>0.39</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>6.4</td>
<td>RLOGIC_IN_PD</td>
<td>Pulldown resistance on PS pin to GND</td>
<td>35</td>
<td>70</td>
<td>111</td>
<td>kΩ</td>
</tr>
<tr>
<td>6.5</td>
<td>pull-up_SS_EN</td>
<td>Pulldown current on SS_EN pin</td>
<td>85</td>
<td>266</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>6.6</td>
<td>pull-up_IGN_PWRL</td>
<td>Pulldown current on IGN_PWRL pin</td>
<td>1</td>
<td>8</td>
<td></td>
<td>μA</td>
</tr>
</tbody>
</table>

(1) The term VIN refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).
7.12 Electrical Characteristics – Overtemperature Protection

Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>POS</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.1</td>
<td>T_PROT</td>
<td>Overtemperature shutdown protection threshold</td>
<td>175</td>
<td>210</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>7.2</td>
<td>T_HYS</td>
<td>Overtemperature shutdown hysteresis</td>
<td></td>
<td></td>
<td>30</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) The term V_IN refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

7.13 Electrical Characteristics – Power Good

Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>POS</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>PGTH_UV</td>
<td>PG threshold undervoltage</td>
<td>Deviation from nominal V_OUT to assert PG low, in normal mode</td>
<td>−10%</td>
<td>−5%</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Deviation from nominal V_OUT to assert PG low, during low power mode to normal mode transition</td>
<td>−12%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Deviation from nominal V_OUT to assert PG low, in low power mode</td>
<td>−20%</td>
<td>−5%</td>
<td></td>
</tr>
<tr>
<td>8.2</td>
<td>V_PG_LOW</td>
<td>PG output-low voltage</td>
<td>IPGL ≤ 1mA</td>
<td></td>
<td>0.4</td>
<td>V</td>
</tr>
</tbody>
</table>

\(^{(1)}\) The term V_IN refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

7.14 Switching Characteristics — Reference Voltage (VOS_FB Pin) and Output Voltage (VOUT Pin)

Over operating free air temperature range –40°C ≤ T_A ≤ 125°C and maximum junction temperature T_J = 150°C and recommended operating input supply range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>POS</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5</td>
<td>I_START_VOUT</td>
<td>VOUT startup time</td>
<td>L = 4.7 µH, C_OUT = 22 µF; V_OUT rising from 10% to 90% of final value</td>
<td>1.5</td>
<td></td>
<td>ms</td>
</tr>
</tbody>
</table>

\(^{(1)}\) The term V_IN refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).
7.15 Switching Characteristics — Buck-Boost
Over operating free air temperature range \(-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}\) and maximum junction temperature \(T_J = 150^\circ\text{C}\) and recommended operating input supply range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>POS</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.8</td>
<td>(t_{\text{blank, Iswlim}})</td>
<td>Time until peak current limit is active</td>
<td>(V_{IN} = 14) V</td>
<td>40</td>
<td>70</td>
<td>ns</td>
</tr>
<tr>
<td>3.11</td>
<td>(f_{SW})</td>
<td>Switching frequency without Spread-Spectrum</td>
<td>(V_{IN_max} = 27) V</td>
<td>1860</td>
<td>2000</td>
<td>2140</td>
</tr>
<tr>
<td>3.12</td>
<td>(f_{SW_SS})</td>
<td>Switching frequency with Spread-Spectrum Enabled</td>
<td>(V_{IN_max} = 27) V; SS_EN pin not connected to GND; Device in buck operation</td>
<td>1800</td>
<td>2100</td>
<td>2400</td>
</tr>
<tr>
<td>3.14</td>
<td>(t_{\text{on, Min Buck}})</td>
<td>Minimum on time in buck operation</td>
<td>Device in normal operation mode</td>
<td>55</td>
<td>65</td>
<td>ns</td>
</tr>
<tr>
<td>3.15</td>
<td>(t_{\text{on, Max Boost}})</td>
<td>Maximum on time in boost operation</td>
<td>Device in normal operation mode</td>
<td>350</td>
<td>400</td>
<td>450</td>
</tr>
<tr>
<td>3.16</td>
<td>(t_{\text{on, Max Bst_L PM}})</td>
<td>Maximum boost on time in power save mode</td>
<td></td>
<td>4</td>
<td></td>
<td>(\mu)s</td>
</tr>
</tbody>
</table>

\(^{(1)}\) The term \(V_{IN}\) refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

7.16 Switching Characteristics — Undervoltage and Overvoltage Lockout
Over operating free air temperature range \(-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}\) and maximum junction temperature \(T_J = 150^\circ\text{C}\) and recommended operating input supply range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>POS</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.3</td>
<td>(t_{\text{deg, VINUVOV}})</td>
<td>(V_{IN}) UV and OV deglitch time</td>
<td></td>
<td>40</td>
<td>50</td>
<td>60</td>
</tr>
<tr>
<td>4.8</td>
<td>(t_{\text{deg, VREGUVOV}})</td>
<td>VREG UV and OV deglitch time</td>
<td></td>
<td>10</td>
<td></td>
<td>(\mu)s</td>
</tr>
</tbody>
</table>

\(^{(1)}\) The term \(V_{IN}\) refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

7.17 Switching Characteristics — IGN Wakeup
Over operating free air temperature range \(-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}\) and maximum junction temperature \(T_J = 150^\circ\text{C}\) and recommended operating input supply range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>POS</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.6</td>
<td>(\text{IGN_deg_Fifo_Filter_Time})</td>
<td>IGN deglitch filter time</td>
<td></td>
<td>7.5</td>
<td>22</td>
<td>ms</td>
</tr>
<tr>
<td>5.7</td>
<td>(\text{IGN_Startup_Time})</td>
<td>Time from IGN high till VOUT crossing 95% of the end-value</td>
<td></td>
<td>25</td>
<td></td>
<td>ms</td>
</tr>
</tbody>
</table>

\(^{(1)}\) The term \(V_{IN}\) refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

7.18 Switching Characteristics — Logic Pins PS, IGN_PWRL, SS_EN
Over operating free air temperature range \(-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}\) and maximum junction temperature \(T_J = 150^\circ\text{C}\) and recommended operating input supply range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>POS</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.7</td>
<td>(t_{\text{Delay_IGN_PWRL}})</td>
<td>Input Delay time for IGN_PWRL pin</td>
<td>Delay time between the toggling of the IGN_PWRL pin and the state change of the signal inside the device</td>
<td>213</td>
<td>256</td>
<td>272</td>
</tr>
<tr>
<td>6.8a</td>
<td>(t_{\text{Delay_PS_L2H}})</td>
<td>Input Delay time for PS pin pulling high</td>
<td>Delay time between pulling the PS high and the device enters low-power mode</td>
<td>59</td>
<td>136</td>
<td></td>
</tr>
<tr>
<td>6.8b</td>
<td>(t_{\text{Delay_PS_H2L}})</td>
<td>Input Delay time for PS pin going low</td>
<td>Delay time between releasing the PS pin and the device enters normal mode from low-power mode</td>
<td>262</td>
<td>510</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) The term \(V_{IN}\) refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).
7.19 Switching Characteristics – Power Good

Over operating free air temperature range \(-40°C \leq T_A \leq 125°C\) and maximum junction temperature \(T_J = 150°C\) and recommended operating input supply range (unless otherwise noted)(1):

<table>
<thead>
<tr>
<th>POS</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.3</td>
<td>PG_Deglitch</td>
<td>PG deglitch filter time</td>
<td>45</td>
<td>50</td>
<td>55</td>
<td>µs</td>
</tr>
<tr>
<td>8.4a</td>
<td>PG_exttime</td>
<td>PG extension time (rising edge only)</td>
<td>PG_DLY Shorted to VREG</td>
<td>40</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8.4b</td>
<td></td>
<td></td>
<td>100 kΩ between PG_DLY and GND</td>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8.4c</td>
<td></td>
<td></td>
<td>10 kΩ between PG_DLY and GND</td>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8.4d</td>
<td></td>
<td></td>
<td>PG_DLY grounded</td>
<td>0.7</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) The term \(V_{IN}\) refers to the voltage on all supply pins VINP and VINL (unless otherwise noted).

7.20 Typical Characteristics

![Figure 1. Shutdown I_Q vs Temperature](image1)

\(V_{IN} = 12\text{ V}\)

![Figure 2. Switching Frequency vs Temperature](image2)

![Figure 3. 5-V Output Regulation vs Load Current](image3)

![Figure 4. 5-V Output Regulation vs Input Voltage](image4)
Typical Characteristics (continued)

Figure 5. 12-V Output Regulation vs Load Current

Figure 6. 12-V Output Regulation vs Input Voltage

Figure 7. Power-Good Delay When PGDLY Is Grounded

Figure 8. Power-Good Delay When PGDLY Connects to 100-kΩ Resistor

Figure 9. Power-Good Delay When PGDLY Connects to VREG

Figure 10. Ignition Shutdown Sequence
Typical Characteristics (continued)

**Figure 11. Low-Power Mode Enabling**

\[ V_{IN} = 12 \text{ V} \quad V_{OUT} = 5 \text{ V} \quad I_{OUT} = 50 \text{ mA} \]

**Figure 12. Step-Up to Step-Down Mode Transition**

\[ 4 \text{ V} \leq V_{IN} \leq 12 \text{ V} \quad V_{OUT} = 5 \text{ V} \quad I_{OUT} = 0.5 \text{ A} \]

**Figure 13. Step-Down to Step-Up Mode Transition**

\[ 4 \text{ V} \leq V_{IN} \leq 8 \text{ V} \quad V_{OUT} = 5 \text{ V} \quad I_{OUT} = 0.5 \text{ A} \]

**Figure 14. Load Current Derating vs Input Voltage**

\[ \text{Load Current Derating (A)} \]

\[ 0 \text{ A} \quad 0.2 \text{ A} \quad 0.4 \text{ A} \quad 0.6 \text{ A} \quad 0.8 \text{ A} \quad 1 \text{ A} \quad 1.2 \text{ A} \]

\[ 0 \text{ V} \quad 5 \text{ V} \quad 10 \text{ V} \quad 15 \text{ V} \quad 20 \text{ V} \quad 25 \text{ V} \quad 30 \text{ V} \quad 35 \text{ V} \quad 40 \text{ V} \]
8 Detailed Description

8.1 Overview

The control circuit of the TPS5516x-Q1 buck-boost converter is based on an average current-mode topology. The control circuit also uses input and output voltage feedforward. Changes of input and output voltage are monitored and the duty cycle in the modulator is immediately adapted to achieve a fast response to those changes. The voltage error amplifier gets its feedback input from the VOS_FB pin. The feedback voltage is compared with the internal reference voltage to generate a stable and accurate output voltage.

The buck-boost converter uses four internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This feature enables the device to keep high efficiency over a wide input voltage and output power range. To avoid ground shift problems caused by the high currents in the switches, separate ground pins (GND and PGND) are used. The reference for all control functions are the GND pins. The power switches are connected to the PGND pins. Both grounds must be connected on the PCB at only one point which is ideally close to the GND pin. Because of the 4-switch topology, the load is always disconnected from the input during shutdown of the converter.

To drive the high-side switches of the buck and the boost power stages, the buck-boost converter requires external boot-strapping ceramic capacitors with low ESR. These bootstrap capacitors are charged by the VREG supply. The VREG supply requires a low-ESR ceramic capacitor for loop stabilization, and must not be loaded by the external application. The VREG supply is also used to drive the low-side switches of the buck and boost power stages. At device start-up, the VREG pin is supplied by the input voltage. When the buck-boost output voltage is greater than its power-good threshold (the PG pin is high), the VREG pin is supplied by the output voltage to reduce power dissipation.

The device can be enabled with the IGN pin, and, when enabled, the device has a power-latch function which can be selected with the IGN_PWRL pin. This function allows an external MCU to keep TPS5516s-Q1 device on even after the IGN pin goes low.

For the TPS55160-Q1 and TPS55165-Q1 devices, the operation mode of the buck-boost converter can be selected through the PS pin. When the PS pin is low, the buck-boost operates in normal mode with a constant fixed switching frequency. When the PS pin is high, the buck-boost operates in low-power mode with pulse-frequency modulation.

The TPS55160-Q1 and TPS55165-Q1 devices also have a frequency spread-spectrum option that can be enabled or disabled through the SS_EN pin.

The output voltage of the TPS55165-Q1 device is selected as a fixed 5 V or fixed 12 V through the VOS_FB pin. The TPS55160-Q1 and TPS55162-Q1 devices have an adjustable output voltage from 5.7 V to 9 V through an external feedback network.
8.2 Functional Block Diagram
8.3 Feature Description

8.3.1 Spread-Spectrum Feature
The TPS55160-Q1 and TPS55165-Q1 devices have a spread-spectrum feature to modulate the switching frequency through a pseudo-random algorithm.

This spread-spectrum feature is enabled and disabled through the SS_EN pin. When the SS_EN pin is unconnected, the spread-spectrum feature is enabled. The SS_EN pin is internally pulled up with a pullup current between 100 µA and 200 µA. When the SS_EN pin is connected to ground, the spread-spectrum feature is disabled.

This feature can only be enabled when the device is in normal mode with step-down operation. This feature cannot be enabled in low-power mode.

8.3.2 Overcurrent Protection
The buck-boost regulator has two ways of protecting against overcurrent conditions. When the buck-boost is in regulation (essentially the output voltage is at the target voltage), the average current limit provides the protection against overcurrent conditions. When the average current limit is activated (essentially the maximum inductor average current is reached), the output voltage gradually decreases, but the control loop tries to maintain the target output voltage. So when the overcurrent condition clears before the buck-boost control circuit gets too far out of regulation, the output voltage gradually reaches its target voltage level again.

The buck-boost regulator limits the peak-overcurrent in the power MOSFETs. When such a peak-overcurrent event occurs, the buck-boost regulator shuts down and restarts after 5.5 µs. If three peak-overcurrent events occur, and the time between each of these peak-overcurrent events is less than \( 10^{-7} \)s, the device goes into the PRE_RAMP state and a 12-ms time-out is started. The device restarts and goes from the PRE_RAMP state to the RAMP state after this 12-ms time-out expires and the IGN pin is high.

When the device operates in low-power mode, both the average current limit and the peak-current limit protection functions are disabled.

8.3.3 Overtemperature Protection
The internal Power-MOSFETs are protected against excess power dissipation with junction overtemperature protection. In case of a detected overtemperature condition, the TPS55165-Q1 device goes to the PRE_RAMP state (the buck-boost regulator is switched off and the VREG supply is enabled) and a 12-ms time-out is started when the overtemperature condition is cleared. The device restarts in the PRE_RAMP state after this 12-ms time-out expires, the overtemperature condition disappeared, and the IGN pin is high.

When the device operates in low-power mode, this overtemperature protection function is disabled.

8.3.4 Undervoltage Lockout and Minimum Start-Up Voltage
The TPS55165-Q1 device has an undervoltage lockout (UVLO) function. When the device operates in normal mode (the PS pin is low), this UVLO function puts the device in the OFF state when the input voltage is less than the UVLO threshold. The device restarts when the IGN pin is high and the input voltage is greater than or equal to the minimum input voltage for startup, which must be maintained until the output voltage is greater than the PG undervoltage threshold.

When the device operates in low-power mode, this UVLO function is disabled.

8.3.5 Overvoltage Lockout
The TPS55165-Q1 device has an overvoltage lockout (OVLO) function. When the input voltage is greater than the OVLO threshold while the device operates in normal mode (the PS pin is low), this OVLO function puts the device in the PRE_RAMP state (the buck-boost regulator is switched off and the VREG supply is enabled), and a 12-ms time-out starts. The device restarts in the PRE_RAMP state after this 12-ms time-out expires, the input voltage is less than the OVLO threshold, and the IGN pin is high.

When the device operates in low-power mode, this OVLO function is disabled.
Feature Description (continued)

8.3.6 VOUT Overvoltage Protection

When the device operates in normal mode (the PS pin is low) and the output voltage is greater than or equal to the VOUT overvoltage protection, the device goes to the PRE_RAMP state (the buck-boost regulator is switched-off and the VREG supply is enabled) and a 12-ms time-out starts when the output voltage is less than the VOUT overvoltage protection. The device restarts in the PRE_RAMP state after this 12-ms time-out expires, the output voltage is less than the VOUT overvoltage protection, and the IGN pin is high.

When the device operates in low-power mode, this VOUT overvoltage protection function is disabled.

8.3.7 Power-Good Pin

The power-good (PG) pin is a low-side FET open-drain output which is released as soon as the output voltage is greater than the PG undervoltage threshold (essentially the output voltage is rising) and the extension time (PG_exttime) is expired. The intended usage of this pin is to release the reset of an external MCU. Therefore, the logic-input signals (IGN_PWRL and PS) are considered to be valid only when the PG pin reaches the high level.

When the output voltage is less than the PG undervoltage threshold (essentially the output voltage is falling) for a time longer than the PG deglitch filter time, the PG pin is pulled low. When the PG pin is low, the level of the PS and IGN_PWRL pins is interpreted as low, regardless of the actual level. The device goes to the OFF state if the IGN pin is low under this condition. For more information on the behavior of the PG pin for rising and falling output voltage, see Figure 16 through Figure 20.

The PG pin is operational in low-power mode. The PG extension time can be configured by connecting the PG_DLY pin to the VREG pin, the GND pin, or through an external resistor with a value from 10 kΩ to 100 kΩ to the GND pin. The extension time is as follows for the listed configurations:

- When the PG_DLY pin is shorted to the VREG pin, the typical PG extension time is 40 ms.
- When the PG_DLY pin is connected to the GND pin, the typical PG extension time is 0.6 ms.
- When the external resistor between the PG_DLY and GND pins has a value of 10 kΩ, the typical PG extension time is 3 ms.
- When the external resistor between pin the PG_DLY and GND pins has a value of 100 kΩ, the typical PG extension time is 30 ms.

8.4 Device Functional Modes

8.4.1 State Diagram

Figure 15 shows the state diagram.
Pre-Power-Good Off Condition:
- IGN = Low
- OR
- VINL < VIN_startup
- OR
- VREG > VREG_OV

Normal Off Condition:
- (IGN = Low AND IGN_PWRL = Low)
- OR
- VINL < UVLO
- OR
- VREG > VREG_OV

Low-Power Off Condition:
- IGN = Low
- AND
- IGN_PWRL = Low
- AND
- PS = Low

Pre-Ramp Condition:
- VREG < VREG_UV
- OR
- Overtemperature Shutdown
- OR
- I_OUT > I_SW_limit
- OR
- VINL > OVLO
- OR
- VOUT (normal mode) > VOUT_PROT_OV

Valid IGN_PWRL:
- IGN_PWRL = High
- AND
- PG = High
- AND
- PG pin is not pulled down

Valid PS:
- PS = High
- AND
- PG = High
- AND
- PG pin is not pulled down

Note:
- The 12-ms time-out from the PRE_RAMP state to the RAMP state starts only when all conditions for going to the RAMP state are satisfied. As soon as one of these conditions is violated, the 12-ms time-out is reset.
- The oscillator is turned off in low-power mode. The oscillator is turned back on upon detecting a negative edge on the PS pin, or a negative edge on the PG pin which requires the device to go out of low-power mode and enter normal mode again.

Figure 15. State Diagram
8.4.2 Modes of Operation

The operational mode of the buck-boost converter is selected through the PS pin. When the PS pin is low, the buck-boost operates in normal mode with a constant fixed switching frequency. When the PS pin is high, the buck-boost operates in low-power mode with pulse-frequency modulation.

8.4.2.1 Normal Mode

To regulate the output voltage at all possible input voltage conditions, the buck-boost converter automatically switches from step-down operation to boost operation and back as required by the configuration. The regulator always uses one active switch, one rectifying switch, one always-on switch, and one always-off switch. Therefore, the regulator operates as a step-down converter (buck) when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. In normal mode, no mode of operation is available in which all four switches are permanently switching. Controlling the switches in this way allows the converter to maintain high efficiency at the most important point of operation; when the input voltage is close to the output voltage. The RMS current through the switches and the inductor is kept at a minimum to minimize switching and conduction losses. For the remaining two switches, one is kept permanently on and the other is kept permanently off which causes no switching losses.

In normal mode, the converter operates in full continuous mode at a fixed switching frequency of 2 MHz (typical) for the entire load-current range, even with no load at the output. No pulse-skipping should occur for supply voltages from 2 V to 27 V.

8.4.2.2 Low-Power Mode

When the buck-boost converter is in low-power mode, the output voltage is monitored with a comparator with its threshold at the regulation target voltage. When the buck-boost regulator goes to low-power mode, the converter temporarily stops operating and the output voltage drops. The slope of the output voltage depends on the load and output capacitance. As the output voltage decreases to less than the regulation target voltage, the device ramps up the output voltage again by giving one or several pulses until the output voltage exceeds the regulation target voltage. In low-power mode, the buck-boost operates in 4-switch mode, which allows regulation at the target output voltage regardless of whether the input voltage is greater than or less than the target output voltage value.

After the device enters low-power mode, the internal oscillator is turned off. As a result of the oscillator being turned off, all signal de-glitching functions are disabled while the device is in low-power mode. These functions include the \( V_{\text{IN}} \) and VREG OV and UV signal de-glitch functions, and the IGN input signal de-glitch function.
8.4.3 Power-Up and Power-Down Sequences

Figure 16 shows the power-up and power-down sequence without the usage of the IGN_PWRL pin.

The actual ramp-down time of the output voltage depends on external load conditions.

Figure 16. Power-Up and Power-Down Sequence With Normal Mode and Low-Power Mode, Without Usage of IGN_PWRL
Figure 17 shows the power-up and power-down sequence with usage of the IGN_PWRL pin.

A. The actual ramp-down time of the output voltage depends on external load conditions.

Figure 17. Power-Up and Power-Down Sequence With Normal Mode and Low-Power Mode, With Usage of IGN_PWRL
Figure 18 shows a power-up and power-down sequence in low-Power mode with the IGN pin low. Figure 18 shows that after the device is powered on in the OFF state, the device is in low-power mode when the PS pin is high regardless of what was applied on the IGN and IGN_PWRL input pins.

Figure 18. Power-Up and Power-Down Sequence With Low-Power Mode When IGN and IGN_PWRL are low (Essentially When the ECU is in Sleep or Standby mode)

A. The actual ramp-down time of the output voltage depends on external load conditions.
Figure 19 shows that when the device starts in the OFF state, the buck-boost converter always enters normal mode first, even when the PS pin was previously set high. The device can only enter low-power mode when the PG output pin is set high. Figure 19 also shows that the device does not start-up as long as the IGN pin is low.

A. The actual ramp-down time of the output voltage depends on external load conditions.

Note: The buck-boost converter always enters normal mode first after ramp up before it can enter low-power mode.

Figure 19. Power-Up Behavior With PS Pin Previously Set High
Figure 20 shows that the device only can start-up in the OFF state when the IGN pin is high. Setting the IGN_PWRL pin before the IGN pin is high does not start-up the device. Figure 20 also shows that the IGN_PWRL signal is only valid after the PG pin is high and the PG-Deglitch time has elapsed.

The actual ramp-down time of the output voltage depends on external load conditions.

Note: The device does not start-up until the IGN pin is high. The IGN power-latch is only be set after the PG pin is high.

**Figure 20. Power-Up Behavior With IGN_PWRL Set High Prior to High IGN**
8.4.4 Soft-Start Feature

On power up, the device has a soft-start feature which ramps the output of the regulator at a steady slew rate. The soft-start ramp time is 0.5 ms by default. When the device pulls the PG pin low because of a VOUT undervoltage condition while the device is in normal mode, the device stays in normal mode and tries to get to the VOUT level again without soft-start slew-ramp control.

8.4.5 Pulldown Resistor on VOUT

When the buck-boost regulator is disabled (in the OFF state, INIT state, and PRE_RAMP state), an internal active pulldown circuit (specified as \(R_{PD_{VOUT}}\) in the Electrical Characteristics — Reference Voltage (VOS_FB Pin) and Output Voltage (VOUT Pin) table) pulls down the VOUT pin.

8.4.6 Output Voltage Selection

The configuration of the output voltage is selectable through the VOS_FB pin.

The fixed output voltage of the TPS55165-Q1 device is 5 V when the VOS_FB pin is connected to ground and is 12 V when the VOS_FB pin is connected to the VREG pin. For the TPS55165-Q1 device in the 5-V configuration (VOS_FB pin connected to ground), the UVLO threshold is set to less than 2 V. When the TPS55165-Q1 device is in the 12-V configuration (VOS_FB pin connected to the VREG pin), the UVLO threshold is set to less than 3.6 V. For the TPS55162-Q1 device, the UVLO threshold is also set to less than 3.6 V.

For the adjustable output voltage of the TPS55160-Q1 and TPS55162-Q1 devices, connect the VOS_FB pin to the external feedback network. The total resistance of this external feedback network must be less than 1 M\(\Omega\) (essentially, this value must be similar to or less than the implemented total resistance of the implemented internal feedback network for the 12 V setting).
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information
The TPS5516x-Q1 family of devices is a high-voltage synchronous buck-boost DC-DC converter with all four power MOSFETs integrated. Each device in the device family can produce a well-regulated output voltage from a widely-varying input voltage source such as an automotive car battery. If the input voltage is higher than the output voltage, the TPS5516x-Q1 device operates in step-down mode. If the input voltage is lower than the output, the device operates in step-up mode. If the input voltage is equal or close to the output voltage, the device operates between the step-down and step-up mode. The buck-boost overlap control ensures automatic and smooth transition between step-down and step-up (This is ok. Step-up and step-down modes were mentioned in the first page of the spec) modes with optimal efficiency. The output voltage of the TPS55165-Q1 device can be set to a fixed level of 5 V or 12 V. The output voltage of the TPS55160-Q1 and TPS55162-Q1 devices is programmable from 5.7 V to 9 V.

9.1.1 Application Circuits for Output Voltage Configurations
Figure 21 and Figure 22 show the application diagrams for the adjustable output configuration.

Figure 21. TPS55160-Q1 Application Diagram for Adjustable Output Voltage
Figure 22. TPS55162-Q1 Application Diagram for Adjustable Output Voltage

Use Equation 1 to calculate the output voltage.

\[ V_{OUT} = \frac{R1+R2}{R2} \times V_{FB} \]

where

- \( V_{FB} \) is 0.8 V (see Electrical Characteristics — Reference Voltage (VOS_FB Pin) and Output Voltage (VOUT Pin)). (1)
Application Information (continued)

Figure 23 shows the TPS55165-Q1 device in the 5-V configuration.

![Application Diagram for 5-V Voltage](image)

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Figure 23. TPS55165-Q1 Application Diagram for 5-V Voltage
Application Information (continued)

Figure 24 shows the TPS55165-Q1 device in the 12-V configuration.

![Diagram of TPS55165-Q1](image)

**Figure 24. TPS55165-Q1 Application Diagram for 12-V Voltage**

**CAUTION**

For TPS55165-Q1 in 12-V configuration (VOS_FB is shorted to VREG), the PG pin must be tied to an external 5-V supply through a pullup resistor. Tying the PG pin to a supply greater than 5.5 V could damage the device in the unlikely event of a shortage between the PG pin and the adjacent VOS_FB pin, which is tied to the VREG pin in the 12-V output configuration. The absolute-maximum voltage rating of the VREG pin is 5.5 V.
9.2 Typical Application

The TPS5516x-Q1 family of devices requires a minimum number of external components to implement a buck-boost converter. Figure 25 shows the typical schematic for the TPS55165-Q1 device in the 5-V configuration.

![Typical Schematic of TPS55165-Q1 Buck-Boost Converter](image)

Figure 25. TPS55165-Q1 Buck-Boost Converter for Fixed 5-V Output

9.2.1 Design Requirements

Table 1 lists the design requirements for Figure 25.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN_MIN}$</td>
<td>The least input voltage after startup. The $I_{OUT_MAX}$ load current deratings listed in this table apply for $V_{IN} &lt; 5.3$ V.</td>
</tr>
<tr>
<td>$V_{IN_startup}$</td>
<td>The minimum input voltage required for startup.</td>
</tr>
<tr>
<td>$V_{IN_MAX}$</td>
<td>The greatest input voltage after startup.</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>The output voltage.</td>
</tr>
<tr>
<td>$I_{OUT_MAX}$</td>
<td>The maximum output current at $V_{IN} \geq 5.3$ V</td>
</tr>
<tr>
<td></td>
<td>The maximum output current at 3.8 V $\leq V_{IN} &lt; 5.3$ V</td>
</tr>
<tr>
<td></td>
<td>The maximum output current at 2.3 V $\leq V_{IN} &lt; 3.8$ V</td>
</tr>
</tbody>
</table>

9.2.2 Detailed Design Procedure

9.2.2.1 Power-Circuit Selections: $C_{IN}$, $L$, $C_{OUT}$

The TPS5516x-Q1 family of devices integrates not only the power switches but also the loop compensation network as well as many other control circuits which reduces the number of required external components. For the internal loop compensation to be effective, the selection of the external power circuits (power inductor and capacitor) must be confined. TI strongly recommends users selecting the component values as follows: 3.3-µH to 6.2-µH power inductor, 18-µF to 47-µF output capacitor, and 8.2-µF or greater input capacitor. Because the TPS5516x-Q1 device switches at about 2 MHz, a shielded inductor and X5R-type or X7R-type ceramic capacitors should be used for the power circuit.
Considering the component tolerance, the following power component values were selected for this design example:

- \( C_{\text{IN}} = 20 \, \mu\text{F} \)
- \( C_{\text{OUT}} = 22 \, \mu\text{F} \)
- \( L = 4.7 \, \mu\text{H} \)

For the input capacitor \((C_{\text{IN}})\), the voltage rating should be greater than the maximum input voltage \((V_{\text{IN\_MAX}})\). Therefore, two, 10-\(\mu\text{F}\) X7R capacitors rated for 50 V were selected for this design example. Adding a small, high-frequency decoupling ceramic capacitor \((C_{\text{VINP}})\) with a value of 100 nF typical in parallel with the input capacitor is recommended to better filter out the switching noises at the VINP pin. Adding another decoupling ceramic capacitor \((C_{\text{VINL}})\) with a value of 470 nF typical is also recommended for the VINL pin.

The output capacitor \((C_{\text{OUT}})\), receives a voltage of 5 V. Considering some voltage-rating margin, two 10-\(\mu\text{F}\) X7R capacitors rated for 10 V or greater and one, 2.2-\(\mu\text{F}\) X7R-type capacitor rated for 10 V or greater in parallel were selected for the output capacitor. Adding a small, high-frequency decoupling ceramic capacitor \((C_{\text{VOSN}})\) with a value of 100 nF typical in parallel with the output capacitor is recommended to better filter out the switching noises at the VOUT\_SENSE pin.

The power inductor \((L)\) should be a shielded type, and it should not saturate during operation. The inductor should also be able to support the power dissipation under the maximum load. Use the calculations in the following sections to find the required current capabilities for the inductor.

### 9.2.2.1.1 Inductor Current in Step-Down Mode

Use Equation 2 to calculate inductor peak-ripple current in the step-down, or buck, mode \(I_{\text{pk\_buck}}\).

\[
I_{\text{pk\_buck}} = \frac{1}{2} \times \frac{V_{\text{OUT}}}{L} \times \frac{1 - D_{\text{buck}}}{f_{\text{s}}}
\]

where

- \(V_{\text{OUT}}\) is the output voltage.
- \(L\) is the value of the inductor.
- \(D_{\text{buck}}\) is the duty cycle (refer to Equation 3).
- \(f_{\text{s}}\) is the switching frequency.

\[
D_{\text{buck}} = \frac{V_{\text{OUT}}}{V_{\text{IN}}}
\]

The maximum peak-ripple current of the inductor \((I_{\text{pk}})\) occurs when the duty cycle is at the minimum value, specifically when the input voltage \((V_{\text{IN}})\) is at the maximum value which yields the value shown in Equation 4.

\[
D_{\text{buck}} = \frac{5\, \text{V}}{36\, \text{V}} = 0.139
\]

Substitute the values for \(f_{\text{s}}\), \(L\), and \(D_{\text{buck}}\), in Equation 2 to find the peak-ripple current as shown in Equation 5.

\[
I_{\text{pk\_buck}} = \frac{1}{2} \times \frac{5\, \text{V}}{4.7\, \mu\text{H}} \times \frac{1 - 0.139}{2\, \text{MHz}} = 0.458\, \text{A}
\]

The power dissipations can be determined by the RMS current of the inductor. Use Equation 6 to calculate the RMS current of the inductor in buck mode \((I_{\text{rms\_buck}})\).

\[
I_{\text{rms\_buck}} = \sqrt{\frac{1}{2} \times \frac{V_{\text{OUT}}^2}{3} + \frac{1}{3} \times I_{\text{pk\_buck}}^2} = \sqrt{\frac{1}{2} \times 1\, \text{A}^2 + \frac{1}{3} \times 0.458\, \text{A}^2} = 1.1\, \text{A}
\]

Use Equation 7 to calculate the approximate power dissipation of the inductor in buck-mode \((P_{\text{loss\_L\_buck}})\).

\[
P_{\text{loss\_L\_buck}} = I_{\text{rms\_buck}}^2 \times R_{\text{dc}}
\]
9.2.2.1.2 Inductor Current in Step-Up Mode

Use Equation 8 to calculate the inductor peak-ripple current in the step-up, or boost, mode ($I_{\text{pk\_boost}}$).

\[
I_{\text{pk\_boost}} = \frac{1}{2} \times \frac{V_{\text{IN}}}{L} \times \frac{D_{\text{boost}}}{f_{\text{sw}}}
\]

where
- $D_{\text{boost}}$ is the duty cycle in boost mode (refer to Equation 9).

\[
D_{\text{boost}} = \frac{V_{\text{OUT}} - V_{\text{IN}}}{V_{\text{OUT}}}
\]

In general, the maximum peak-ripple current occurs at 50% duty cycle. In this example, because of the power derating versus the input voltage, a few calculations can find that the maximum RMS current occurs when the input voltage is approximately 3.8 V, of which the load current is 0.8 A, according to Table 1. Equation 10 and Equation 11 show the peak-ripple current under this condition.

\[
D_{\text{boost}} = \frac{5\,\text{V} - 3.8\,\text{V}}{5\,\text{V}} = 0.240
\]

\[
I_{\text{pk\_boost}} = \frac{1}{2} \times \frac{3.8\,\text{V}}{4.7\,\mu\text{H}} \times \frac{0.240}{2\,\text{MHz}} = 0.049\,\text{A}
\]

The power dissipation can be determined by the RMS current of the inductor. Use Equation 12 to calculate the RMS current of the inductor in buck mode ($I_{\text{rms\_boost}}$).

\[
I_{\text{rms\_boost}} = \sqrt{\left(\frac{I_{\text{OUT}}}{1 - D_{\text{boost}}}\right)^2 + \frac{1}{3} \times I_{\text{pk\_boost}}^2} = \sqrt{\left(\frac{0.8\,\text{A}}{1 - 0.24}\right)^2 + \frac{1}{3} \times 0.049\,\text{A}^2} = 1.053\,\text{A}
\]

Use Equation 13 to calculate the approximate power dissipation of the inductor in boost mode ($P_{\text{loss\_L\_boost}}$).

\[
P_{\text{loss\_L\_boost}} = I_{\text{rms\_boost}}^2 \times R_{\text{dc}}
\]

9.2.2.1.3 Inductor Current in Buck-Boost Overlap Mode

When input voltage is very close to the output voltage, the device operates in buck-boost overlap mode, and the L1 and L2 pins are switched alternately in consecutive cycles. The small voltage difference between the input and output voltage leads to a small amount of ripple current through the inductor. Therefore, the total inductor current is essentially the load current with small ripples superimposed onto it, and the RMS current is approximately the same as the load current, which is 1 A.

\[
P_{\text{loss\_L\_buckboost}} = I_{\text{dc}}^2 \times R_{\text{dc}}
\]

9.2.2.1.4 Inductor Peak Current

Because the TPS5516x-Q1 device has internal peak current limit ($I_{\text{SW\_limit}}$) of 4.5 A (maximum), this current should be considered when selecting the power inductor. Select the inductor of the saturation current ($I_{\text{SAT}}$) with a minimum value of 4.5 A so that the inductor never gets saturated. TI recommends using a shielded inductor.

9.2.2.1.5 Inductor Peak Current

For this design example, select an AEC-Q200 Grade 0, shielded inductor with the following characteristics:
- Is a surface-mount device (SMD)
- Has an inductance of 4.7 µH
- Supports a saturation current ($I_{\text{SAT}}$) of 4.8 A
- Is rated for an RMS current ($I_{\text{rms}}$) of 1.5 A or larger
- Is rated for a DC load ($R_{\text{dc}}$) of 0.04 Ω or smaller
9.2.2.2 Control-Circuit Selections

9.2.2.2.1 Bootstrap Capacitors
The bootstrap capacitors (C_{BST1} and C_{BST2}) supply the internal high-side MOSFET driver. TI recommends using a 0.1-µF, X7R-type ceramic capacitor rated for 15 V or larger for the bootstrap capacitors.

9.2.2.2.2 VOUT-Sense Bypass Capacitor
To improve noise immunity, connect a 0.1-µF, X7R-type ceramic capacitor rated for 25 V or greater to the VOUT pin.

9.2.2.2.3 VREG Bypass Capacitor
The VREG supplies the internal control circuit as well as the drivers for the integrated low-side driver. To improve noise immunity and stabilize the internal VREG regulator, TI recommends connecting a 4.7-µF, X7R-type ceramic capacitor rated for 25 V or greater between the VREG and GND pins.

9.2.2.2.4 PG Pullup Resistor and Delay Time
The power-good indicator pin (PG) is an open-drain output pin. The PG pin requires an external pullup resistor to flag the power-good status. For this design example, select a 100-kΩ resistor to pull up the PG pin from the output rail.

The PG_DLY pin sets the delay time for the PG status to flip. Follow the instructions listed in the Power-Good Pin to program the delay.

9.2.3 Application Curves

Figure 26. Efficiency vs Load

Figure 27. Start-Up Procedure

Figure 28. Step Load Response

Figure 29. Battery-Voltage Cranking Response
10 Power Supply Recommendations

The TPS5516x-Q1 family of devices is a power-management device. The power supply for the device is any DC-voltage source within the specified input range. The supply should also be capable of supplying sufficient current based on the maximum inductor current in boost-mode operation. When connecting to the power supply and load, try to use short and solid wires. Twisting the pair of wires for the input and output helps minimize the line impedance and avoid adversary interference with the circuit operation.

11 Layout

11.1 Layout Guidelines

The layout of the printed-circuit board (PCB) is critical to achieve low EMI and stable power-supply operation as well as optimal efficiency. Make the high frequency current loops as small as possible, and follow these guidelines of good layout practices;

- The TPS5516x-Q1 family of devices is a high-frequency switching converter. Because the four switch MOSFETs are integrated, the device should be located at the center of the DC-DC power stage. Separate the power ground and analog ground such that the control circuit can be connected to the relatively quieter analog ground without being contaminated by the noisy power ground. Use the PGND pin, GND pin, and the device PowerPAD as the single-point connection between the analog and power grounds.

- Identify the high-frequency switched AC-current loops. In step-down mode, the AC current loop is along the path of the input capacitor (C\text{IN}), L1 pin, internal buck-switch leg, and PGND pin, and closes at the input capacitor. In step-up mode, the AC current loop is along the path of the output capacitor (C\text{OUT}), L2 pin, internal boost-switch leg, and PGND pin, and closes at the output capacitor. These two AC-current loops are both involved in buck-boost overlap mode.

- Optimize component placement and orientation before routing any traces. Place the input and output filter capacitors, the device, and the power inductor close together such that the AC-current loops are short, direct, and the spatial areas enclosed by the loops are minimized. Make the power flow in a straight path rather than a zigzag path on the board.

- Place the high frequency decoupling ceramic capacitors for the input and output as close as possible to the device with the main input and output ceramic capacitors placed next to the high-frequency capacitors. This placement helps confine the high switching noises within a very small area around the device.

- Place the VREG decoupling capacitor close to the VREG pin because it serves as the supply to the internal low-side MOSFETs drivers. Because the VREG pin receives power from the output rail, the ground lead of the VREG decoupling capacitor should connect directly to the C\text{OUT} ground to improve device noise immunity.

- Place the bootstrap capacitors (C\text{BST1} and C\text{BST2}) close to the device with short and direct traces to connect to the corresponding device pins because these capacitors serve as the supplies to the internal high-side MOSFETs drivers.

- Place the VOUT\_SENSE decoupling capacitor (C\text{VOSN}) close to the device. Give the placement of this capacitor priority over the main output capacitors.

- For TPS55160-Q1 or TPS55162-Q1, place the sense-resistor divider for the output voltage close to the device.

- Use eight to nine via holes with a 0.3 mm diameter in the device PowerPAD to help dissipate heat through the layers of the ground plane. Additional via holes around the device PowerPAD can further enhance heat dissipation.

- Use at least ten via holes with a 0.3 mm diameter around the input and output capacitors that are connected to ground-plane layers to minimize the PCB impedance for power current flows.

\textbf{NOTE}

The VREG\_Q pin must always connect to the VREG pin. Both pins should have a Kelvin connection to the decoupling capacitor.
11.2 Layout Example

Figure 30. Example Circuit Layout
12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support
For development support, refer to:
TPS55160-Q1 PSpice Transient Model

12.2 Documentation Support

12.2.1 Related Documentation
For related documentation see the following:
Texas Instruments, TPS5516xQ1-EVM Evaluation Module for 1-A Single-Inductor Buck-Boost-Converter user's guide

12.3 Related Links
The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

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<th>PRODUCT FOLDER</th>
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<th>TECHNICAL DOCUMENTS</th>
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<td>TPS55160-Q1</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
<tr>
<td>TPS55162-Q1</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
<tr>
<td>TPS55165-Q1</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
</tbody>
</table>

12.4 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community**  
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**Design Support**  
*TI's Design Support*  
Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks
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12.6 Electrostatic Discharge Caution
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary
SLYZ022 — *TI Glossary.*
This glossary lists and explains terms, acronyms, and definitions.
13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
### PACKAGING INFORMATION

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<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS55160QPWPRQ1</td>
<td>ACTIVE</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>20</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>TPS55160</td>
<td>Samples</td>
</tr>
<tr>
<td>TPS55160QPWPTQ1</td>
<td>ACTIVE</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>20</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-3-260C-168 HR</td>
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<td>TPS55160</td>
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</tr>
<tr>
<td>TPS55162QPWPRQ1</td>
<td>ACTIVE</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>20</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>TPS55162</td>
<td>Samples</td>
</tr>
<tr>
<td>TPS55162QPWPTQ1</td>
<td>ACTIVE</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>20</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>TPS55162</td>
<td>Samples</td>
</tr>
<tr>
<td>TPS55165QPWPRQ1</td>
<td>ACTIVE</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>20</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>TPS55165</td>
<td>Samples</td>
</tr>
<tr>
<td>TPS55165QPWPTQ1</td>
<td>ACTIVE</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>20</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>TPS55165</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS55160QPWRQ1</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>20</td>
<td>2000</td>
<td>330.0</td>
<td>16.4</td>
<td>6.95</td>
<td>7.1</td>
<td>1.6</td>
<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
<tr>
<td>TPS55160QPWPTQ1</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>20</td>
<td>250</td>
<td>180.0</td>
<td>16.4</td>
<td>6.95</td>
<td>7.1</td>
<td>1.6</td>
<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
<tr>
<td>TPS55162QPWRQ1</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>20</td>
<td>2000</td>
<td>330.0</td>
<td>16.4</td>
<td>6.95</td>
<td>7.1</td>
<td>1.6</td>
<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
<tr>
<td>TPS55162QPWPTQ1</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>20</td>
<td>250</td>
<td>180.0</td>
<td>16.4</td>
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</tr>
<tr>
<td>TPS55165QPWRQ1</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>20</td>
<td>2000</td>
<td>330.0</td>
<td>16.4</td>
<td>6.95</td>
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</tr>
<tr>
<td>TPS55165QPWPTQ1</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>20</td>
<td>250</td>
<td>180.0</td>
<td>16.4</td>
<td>6.95</td>
<td>7.1</td>
<td>1.6</td>
<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

- **All dimensions are nominal.**

*Dimensions:*
- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers
### TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS55160QPWPRQ1</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>20</td>
<td>2000</td>
<td>350.0</td>
<td>350.0</td>
<td>43.0</td>
</tr>
<tr>
<td>TPS55160QPWPTQ1</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>20</td>
<td>250</td>
<td>213.0</td>
<td>191.0</td>
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</tr>
<tr>
<td>TPS55162QPWPRQ1</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>20</td>
<td>2000</td>
<td>350.0</td>
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</tr>
<tr>
<td>TPS55162QPWPTQ1</td>
<td>HTSSOP</td>
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<td>20</td>
<td>250</td>
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</tr>
<tr>
<td>TPS55165QPWPRQ1</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>20</td>
<td>2000</td>
<td>350.0</td>
<td>350.0</td>
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</tr>
<tr>
<td>TPS55165QPWPTQ1</td>
<td>HTSSOP</td>
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<td>20</td>
<td>250</td>
<td>213.0</td>
<td>191.0</td>
<td>55.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
**MECHANICAL DATA**

**PWP (R-PDSO-G20) PowerPAD™ PLASTIC SMALL OUTLINE**

![Diagram of PWP (R-PDSO-G20) PowerPAD™ PLASTIC SMALL OUTLINE](image)

**NOTES:**
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-153

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PowerPAD is a trademark of Texas Instruments.

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**Texas Instruments**

[www.ti.com](http://www.ti.com)
THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

NOTE:  A. All linear dimensions are in millimeters

⚠️ Exposed tie strap features may not be present.

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