TPS552852 22V, 8A Full Integrated Buck-Boost Converter

1 Features

- Wide input and output voltage range
  - Wide input voltage range: 2.4V to 22V
  - Minimum input voltage for start-up: 3.0V
  - Wide output voltage range: 0.8V to 15V
  - Reference voltage accuracy: ±1%
  - Programmable output current limit
- High efficiency over entire load range
  - 94.3% efficiency at V_{IN} = 12V, V_{OUT} = 12V and I_{OUT} = 5A
- Rich protection features
  - Input overvoltage protection
  - Output relative overvoltage protection
  - Hiccup mode for output short-circuit protection
  - Programmable PFM and FPWM mode at light load
  - Thermal shutdown protection
  - Average inductor current limit: 8A
- Small design size
  - Four low $R_{DS(ON)}$ internal MOSFETs
  - High switching frequency: 2.1MHz
  - 2.5mm × 3.5mm HotRod™ WQFN package

2 Applications

- Digital still camera
- Docking station
- Patient monitor
- Hair dryer
- Solid state drive (SSD)

3 Description

The TPS552852 is a fully-integrated ,synchronous buck-boost converter that is optimized for converting battery voltage or adapter voltage into power supply rails. The TPS552852 integrates four 15mΩ MOSFETs to provide a high efficiency and small size design.

The TPS552852 has a wide input voltage range from 2.4V (3.0V rising) to 22V and capable of outputting 0.8V to 15V voltage to support a variety of applications. The device features 8A average inductor current limit and can supply up to 7A output current in buck mode.

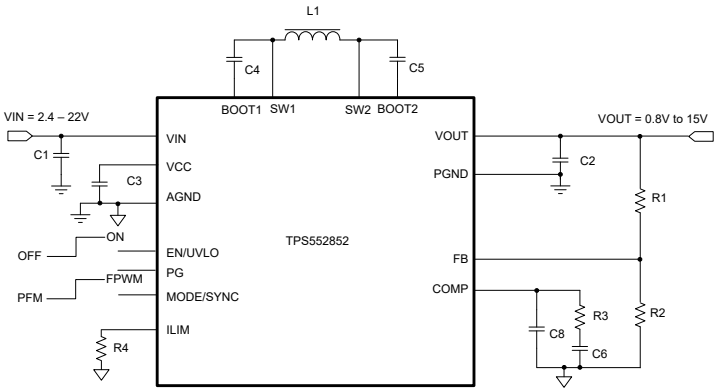
The TPS552852 offers input and output overvoltage protection, average inductor current limit, cycle-by-cycle peak current limit, and output short-circuit protection. The TPS552852 is also designed for safe operating with output current limit without external output current sense resistor and hiccup mode protection in sustained overload conditions.

The TPS552852 allows the use of small inductor and capacitor with high switching frequency. The TPS552852 is available in a 2.5mm × 3.5mm QFN package.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS552852	VAL (WQFN-HR, 15)	3.5mm × 2.5mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit

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4 Pin Configuration and Functions

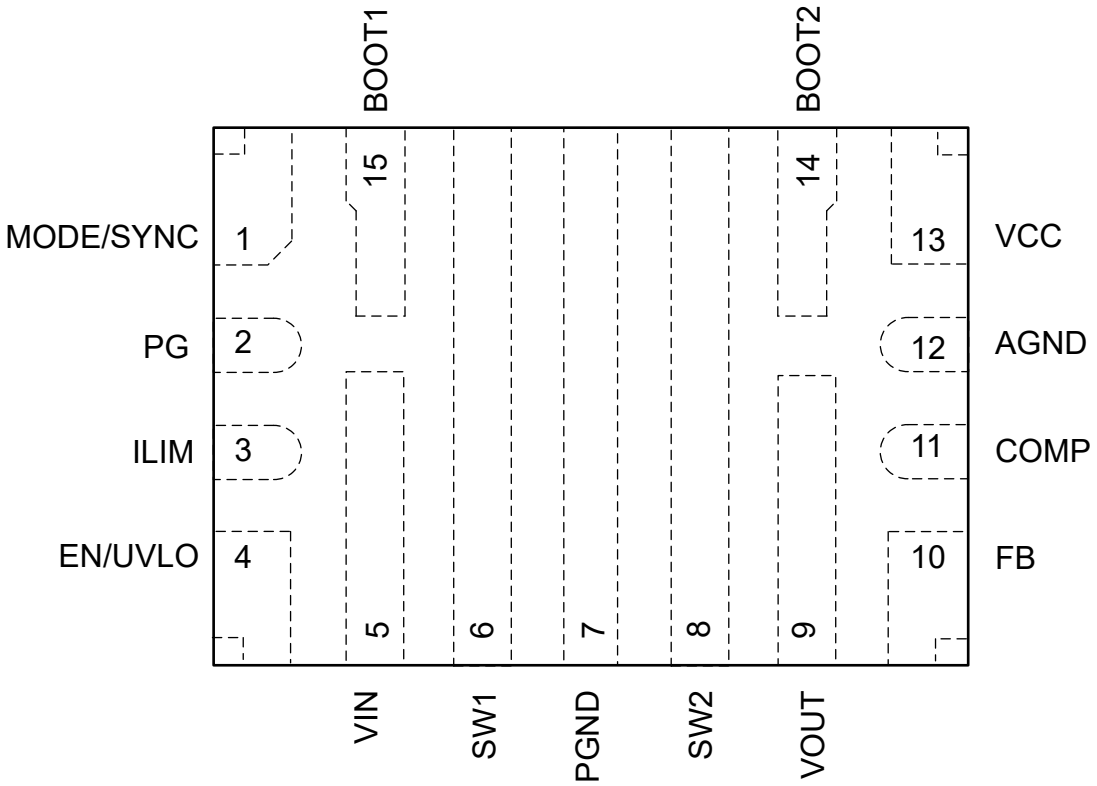


Figure 4-1. 15-Pin WQFN-HR, VAL Package (Transparent Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	MODE/SYNC	I	Mode selection pin. MODE = high, forced PWM mode. MODE = low, auto PFM mode. This pin can also be used to synchronize the external clock. See also Section 6.3.2.
2	PG	O	Power-good indication. When the output voltage is above 95% of the setting output voltage, this pin outputs high impedance. When the output voltage is below 90% of the setting output voltage, this pin outputs low level.
3	ILIM	I	The output current limit is programmed by a resistor between this pin and AGND pin. Connect ILIM to AGND when not using output current limit function.
4	EN/UVLO	I	Enable logic input and programmable input voltage undervoltage lockout (UVLO) input. Logic high level enables the device. Logic low level disables the device and turns the device into shutdown mode. After the voltage at EN/UVLO pin is above the logic high voltage of 1.03V, this pin acts as programmable UVLO input with 1.05V internal reference.
5	VIN	PWR	Input of the buck-boost converter
6	SW1	PWR	The switching node pin of the buck side. This pin is connected to the drain of the internal buck low-side power MOSFET and the source of internal buck high-side power MOSFET.
7	PGND	PWR	Power ground of the device
8	SW2	PWR	The switching node pin of the boost side. This pin is connected to the drain of the internal boost low-side power MOSFET and the source of internal boost high-side power MOSFET.
9	VOUT	PWR	Output of the buck-boost converter
10	FB	I	Connect to the center of a resistor divider to program the output voltage.
11	COMP	O	Output of the internal error amplifier. Connect the loop compensation network between this pin and the AGND pin.

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Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
12	AGND	—	Signal ground of the device
13	VCC	O	Output of the internal regulator. A ceramic capacitor of more than 4.7µF is required between this pin and the AGND pin.
14	BOOT2	O	Power supply for high-side MOSFET gate driver in boost side. A ceramic capacitor of 0.1µF must be connected between this pin and the SW2 pin.
15	BOOT1	O	Power supply for high-side MOSFET gate driver in buck side. A ceramic capacitor of 0.1µF must be connected between this pin and the SW1 pin.

(1) I = input, O = output, PWR = power

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5 Specifications

5.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range at terminals (2)	VIN, SW1	–0.3	27	V
	VOUT, SW2	-0.3	17	V
	BOOT1	SW1 – 0.3	SW1 + 6	V
	BOOT2	SW2 – 0.3	SW2 + 6	V
	EN/UVLO, VCC, PG, ILIM, COMP, FB, MODE/SYNC	–0.3	6	V
	EN/UVLO, PG, ILIM, COMP, FB, MODE /SYNC	–0.3	VCC + 0.3	V
Operating junction temperature	T_J (3)	–40	150	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.
(3) High junction temperatures degrade operating lifetimes. Operating lifetime is derated for junction temperatures greater than 125°C.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002(2)	±500	

(1) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range (Vout ≥ 3.0V)	2.4		22	V
	Input voltage range (Vout < 3.0V)	3		22	V
V_{OUT}	Output voltage range	0.8		15	V
L	Effective inductance range	1	1.5	2.2	µH
C_{IN}	Effective input capacitance range	4.7	22		µF
C_{OUT}	Effective output capacitance range	10	100	1000	µF
T_J	Operating junction temperature	–40		125	°C

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5.4 Thermal Information

THERMAL METRIC(1)		VAL (WQFN-HR) 15 PINS Standard	VAL (WQFN-HR) 15 PINS EVM (2)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.6	33	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.5	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.8	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.6	0.7	°C/W
Y_{JB}	Junction-to-board characterization parameter	6.7	11.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) Measured on TPS552852EVM, 4-layer, 2oz/1oz/1oz/2oz copper PCB.

5.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 12V and V_{OUT} = 15V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.4		22	V
V_{VIN_UVLO}	Undervoltage lockout threshold	V_{IN} rising	2.8	2.9	3.0	V
		V_{IN} falling, V_{OUT} < 3V	2.6	2.7	2.8	V
		V_{IN} falling, V_{OUT} ≥ 3V	2.31	2.33	2.38	V
V_{VIN_OVP}	Input overvoltage protection threshold	Rising threshold	22	22.5	23	V
$V_{VIN_OVP_HYS}$	Input overvoltage protection hysteresis			0.9		V
I_Q	Quiescent current into VIN pin	IC enabled, no load, no switching. V_{IN} = 3.0V to 22V, V_{OUT} = 0.8V, V_{FB} = V_{REF} + 0.1V, Tj up to 125°C		1		mA
	Quiescent current into VOUT pin	IC enabled, no load, no switching, V_{IN} = 3.0V, V_{OUT} = 3V to 15V, V_{FB} = V_{REF} + 0.1V, Tj up to 125°C		1		mA
I_{SD}	Shutdown current into VIN pin	IC disabled, V_{IN} = 3.0V to 22V, Tj up to 125°C		1.3	3.8	µA
V_{CC}	Internal regulator output	V_{IN} = 8V, V_{OUT} = 15V, I_{VCC} = 20mA	5.0	5.2	5.4	V
EN/UVLO						
V_{EN_H}	EN Logic high threshold	V_{CC} = 3.0V to 5.5V			1.03	V
V_{EN_L}	EN Logic low threshold	V_{CC} = 3.0V to 5.5V	0.4			V
V_{EN_HYS}	Enable threshold hysteresis	V_{CC} = 3.0V to 5.5V	0.025			V
V_{UVLO}	UVLO rising threshold at the EN/UVLO pin	V_{CC} = 3.0V to 5.5V	1	1.05	1.1	V
V_{UVLO_HYS}	UVLO threshold hysteresis	V_{CC} = 3.0V to 5.5V		13		mV
I_{UVLO}	Sourcing current at the EN/UVLO pin	$V_{EN/UVLO}$ = 1.3V	4.5	5	5.5	µA
OUTPUT						
V_{OUT}	Output voltage range		0.8		15	V
$V_{VOUT_OVP_FB}$	Detected with respect to FB rising		110.5	115	120	%
$V_{VOUT_OVP_FB_HYS}$	hysteresis			2.3		%
I_{FB_LKG}	Leakage current at FB pin	Tj up to 125°C			100	nA

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5.5 Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 12V and V_{OUT} = 15V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VOUT_LKG}	Leakage current into VOUT pin	IC disabled, V_{OUT} = 15V, V_{SW2} = 0V, Tj up to 125°C		0.13	20	µA
REFERENCE VOLTAGE						
V_{REF}	Reference voltage at the FB pin	PWM operation	1.188	1.2	1.212	V
POWER SWITCH						
$R_{DS(on)}$	Low-side MOSFET on resistance on buck side	V_{OUT} = 15V, V_{CC} = 5.2V		15.5		mΩ
	High-side MOSFET on resistance on buck side	V_{OUT} = 15V, V_{CC} = 5.2V		14.5		mΩ
	Low-side MOSFET on resistance on boost side	V_{OUT} = 15V, V_{CC} = 5.2V		15.5		mΩ
	High-side MOSFET on resistance on boost side	V_{OUT} = 15V, V_{CC} = 5.2V		14.5		mΩ
INTERNAL CLOCK						
f_{SW}	Switching frequency		1900	2100	2300	kHz
t_{OFF_min}	Min. off time	Boost mode		90	145	ns
t_{ON_min}	Min. on time	Buck mode		90	130	ns
CURRENT LIMIT						
I_{LIM_AVG}	Average inductor current limit	V_{IN} = 8V, V_{OUT} = 15V, FPWM	7	8		A
		V_{IN} = 8V, V_{OUT} = 15V, PFM	7	8		A
I_{LIM_PK}	Peak inductor current limit at boost high side	V_{IN} = 8V, V_{OUT} = 15V, FPWM		13		A
		V_{IN} = 8V, V_{OUT} = 15V, PFM		13		A
OUTPUT CURRENT LIMIT						
I_{OUT_LIMIT}	Output current limit	Rlimit = 60.4kΩ		3		A
		Rlimit = 34kΩ		5		A
ERROR AMPLIFIER						
I_{SINK}	COMP pin sink current	V_{FB} = V_{REF} + 400mV, V_{COMP} = 1.1V, V_{CC} = 5V		20		µA
I_{SOURCE}	COMP pin source current	V_{FB} = V_{REF} – 400mV, V_{COMP} = 1.1V, V_{CC} = 5V		60		µA
V_{CCLPH}	High clamp voltage at the COMP pin			1.2		V
V_{CCLPL}	Low clamp voltage at the COMP pin			0.7		V
G_{EA}	Error amplifier transconductance			190		µA/V
SOFT START						
t_{SS}	Soft-start time		2.5	3.9	5.7	ms
SYNCHRONOUS CLOCK						
V_{SNYC_H}	Sync clock high voltage threshold				1.2	V
V_{SYNC_L}	Sync clock low voltage threshold		0.4			V
t_{SYNC_MIN}	Minimum sync clock pulse width		50			ns
HICCUP						
t_{HICCUP}	Hiccup off time			76		ms
MODE						
V_{MODE}	MODE logic high threshold				1.2	V
V_{MODE}	MODE logic low threshold		0.4			V
PROTECTION						
T_{SD}	Thermal shutdown threshold	T_J rising		175		°C

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5.5 Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 12V and V_{OUT} = 15V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD_HYS}	Thermal shutdown hysteresis	T_J falling below Tsd		20		°C

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5.6 Typical Characteristics

V_{IN} = 12V, T_A = 25°C, f_{SW} = 2100kHz, unless otherwise noted.

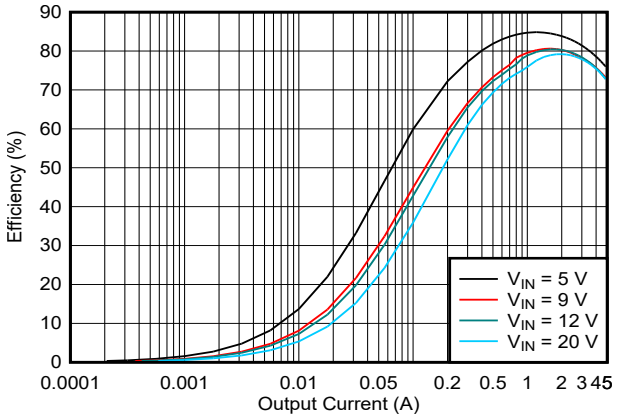


Figure 5-1. Efficiency vs Output Current, V_{OUT} = 1.2V, FPWM

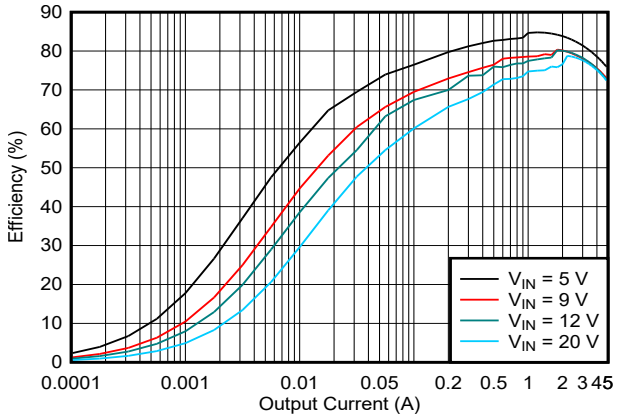


Figure 5-2. Efficiency vs Output Current, V_{OUT} = 1.2V, PFM

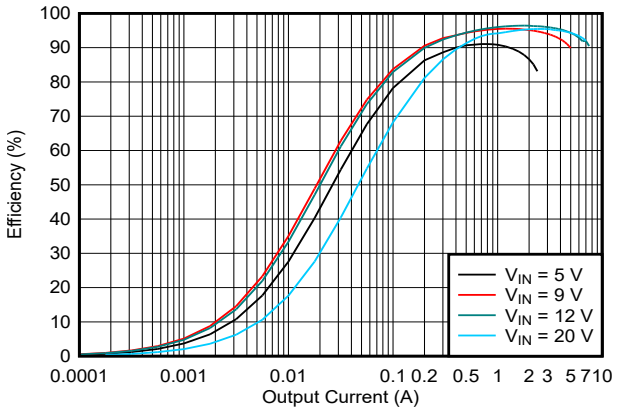


Figure 5-3. Efficiency vs Output Current, V_{OUT} = 12V, FPWM

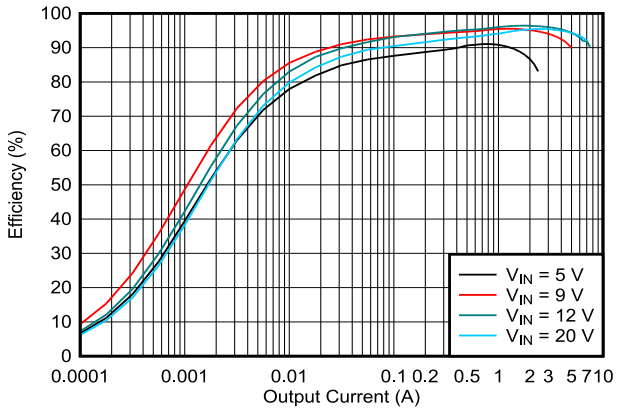


Figure 5-4. Efficiency vs Output Current, V_{OUT} = 12V, PFM

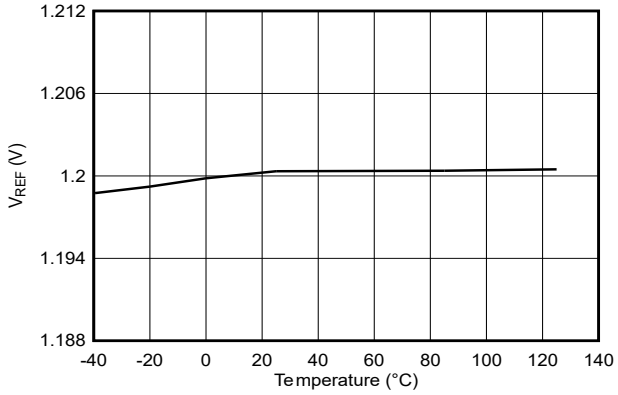


Figure 5-5. Reference Voltage vs Temperature

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6 Detailed Description

6.1 Overview

The TPS552852 is an 8A, buck-boost DC to DC converter with integrated four MOSFETs. The TPS552852 can operate over a wide range of 2.4V to 22V input voltage and output 0.8V to 15V. The device can transition among buck mode, buck-boost mode, and boost mode smoothly according to the input voltage and the setting output voltage. The TPS552852 operates in the buck mode when the input voltage is greater than the output voltage and in the boost mode when the input voltage is less than the output voltage. When the input voltage is close to the output voltage, the TPS552852 operates in one-cycle buck and one-cycle boost mode alternately.

The TPS552852 uses an average current mode control scheme. Current mode control provides simplified loop compensation, rapid response to the load transients and inherent line voltage rejection. An error amplifier compares the feedback voltage of the output voltage with the internal reference voltage. The output of the error amplifier determines the average inductor current.

The TPS552852 works in fixed-frequency PWM mode at moderate to heavy load currents. In the light load condition, the TPS552852 can be configured to automatically transition to PFM mode or be forced in PWM mode with MODE/SYNC pin.

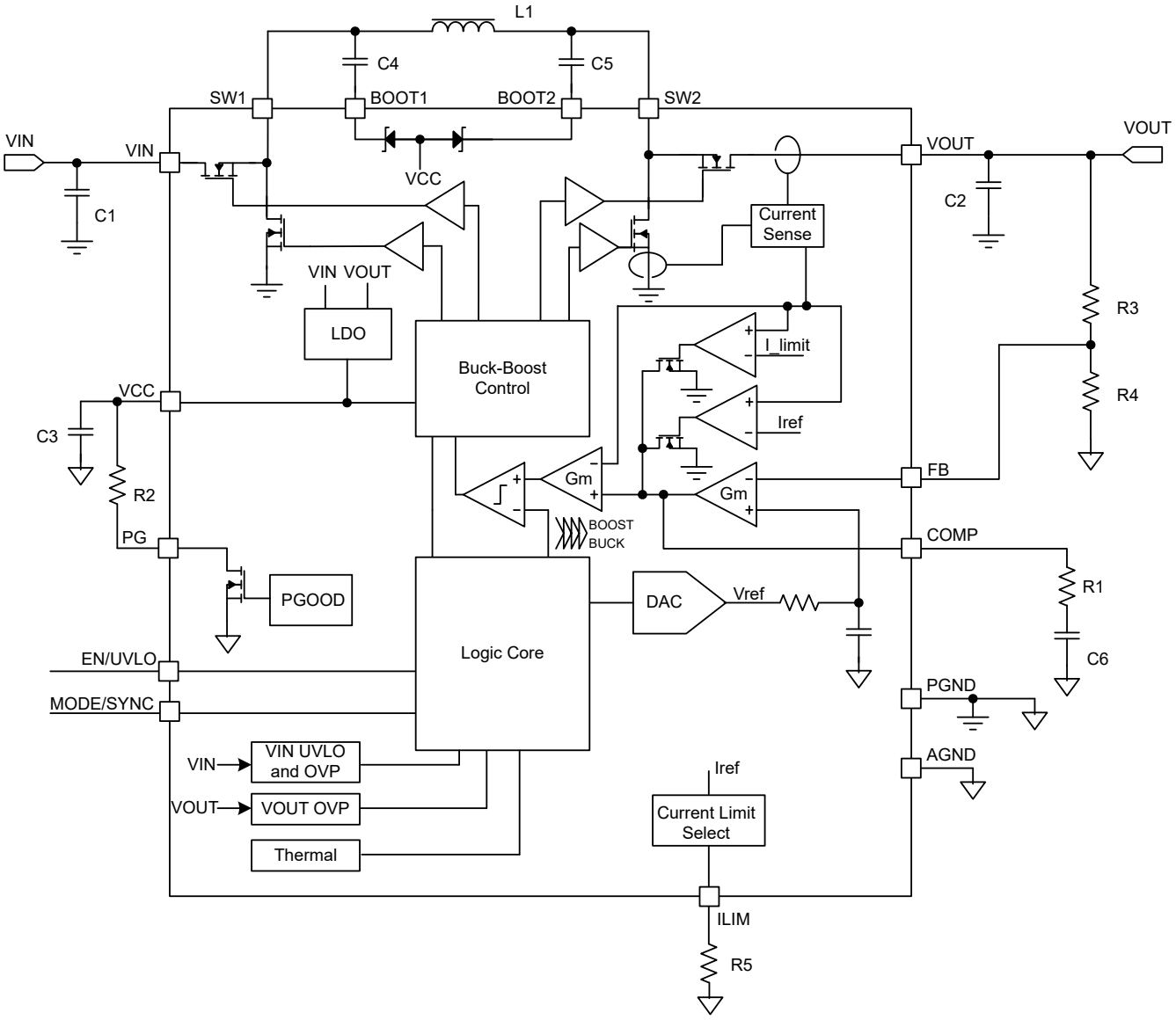
The TPS552852 provides typical 8A average inductor current limit. In addition, the TPS552852 provides cycle-by-cycle peak inductor current limit as well when the inductor peak current is above peak current limit.

A precision voltage threshold of 1.05V with 5µA sourcing current at the EN/UVLO pin supports programmable input undervoltage lockout (UVLO) with hysteresis. When input voltage is higher than 22.5V, the input overvoltage protection (OVP) feature turns off the device to prevent damage. The output overvoltage protection (OVP) feature turns off the high side FETs to prevent damage to the devices powered by the TPS552852.

The TPS552852 provides a hiccup mode protection to reduce the heating in the power components when the output short circuit happens. With hiccup feature, the TPS552852 turns off for 76ms and restarts soft start-up.

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6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 VCC Power Supply

An internal LDO to supply the TPS552852 outputs regulated 5.2V voltage at the VCC pin. When V_{IN} is less than V_{OUT}, the internal LDO selects the power supply source by comparing V_{IN} to a rising threshold of 6.2V with 0.3V hysteresis. When V_{IN} is higher than 6.2V, the supply for LDO is V_{IN}. When V_{IN} is lower than 5.9V, the supply for LDO is V_{OUT}. When V_{OUT} is less than V_{IN}, the internal LDO selects the power supply source by comparing V_{OUT} to a rising threshold of 6.2V with 0.3V hysteresis. When V_{OUT} is higher than 6.2V, the supply for LDO is V_{OUT}. When V_{OUT} is lower than 5.9V, the supply for LDO is V_{IN}. Table 6-1 shows the supply source selection for the internal LDO.

Table 6-1. V_{CC} Power Supply Logic

V_{IN}	V_{OUT}	INPUT FOR V_{CC} LDO
V_{IN} > 6.2V	V_{OUT} > V_{IN}	V_{IN}
V_{IN} < 5.9V	V_{OUT} > V_{IN}	V_{OUT}
V_{IN} > V_{OUT}	V_{OUT} > 6.2V	V_{OUT}
V_{IN} > V_{OUT}	V_{OUT} < 5.9V	V_{IN}

6.3.2 Mode/SYNC Pin Configuration

By forcing a constant voltage on MODE/SYNC pin, the TPS552852 can select different light load operation mode. Auto PFM mode can be selected by forcing a constant low voltage (< 0.4V) on the MODE/SYNC pin. Forced PWM mode can be selected by forcing a constant high voltage (> 1.2V) on the MODE/SYNC pin.

For noise-sensitive applications, the TPS552852 can be synchronized to an external clock signal applied to the MODE/SYNC pin. TI recommends the duty cycle of the external clock in the range of 30% to 70%. The external clock at the MODE/SYNC pin must have lower than 0.4V low level voltage and the clock frequency must be within ±20% of the default switching frequency.

When clock input is forced on the MODE/SYNC pin and the synchronization function works, TPS552852 automatically enters forced PWM mode at light load.

Table 6-2. MODE/SYNC Pin Configuration

MODE/SYNC VOLTAGE	LIGHT LOAD OPERATION MODE	SYNC TO EXTERNAL CLOCK
Low < 0.4V	Auto PFM	No
High > 1.2V	Forced PWM	No
Clock Input	Forced PWM	Yes

6.3.3 Input Undervoltage Lockout

When the input voltage is below 2.4V, the TPS552852 is disabled. When the input voltage is above 3V, the TPS552852 can be enabled by pulling the EN pin to a high voltage above 1.1V.

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6.3.4 Enable and Programmable UVLO

The TPS552852 has a dual function enable and undervoltage lockout (UVLO) circuit. When the input voltage at the VIN pin is above the input UVLO rising threshold of 3V and the EN/UVLO pin is pulled above V_{EH_H} but less than the enable UVLO threshold of V_{UVLO}, the TPS552852 is enabled but still in standby mode. The TPS552852 starts to detect the resistance between the MODE pin and ground.

The EN/UVLO pin has an accurate UVLO voltage threshold to support programmable input undervoltage lockout with hysteresis. When the EN/UVLO pin voltage is greater than the UVLO threshold of 1.05V, the TPS552852 is enabled for switching operation. A hysteresis current I_{UVLO_HYS} is sourced out of the EN/UVLO pin to provide hysteresis that prevents on and off chattering in the presence of noise with a slowly changing input voltage.

By using the resistor divider as shown in Figure 6-1, calculate the turn-on threshold using Equation 1.

$$V_{IN\,(UVLO_ON)} = V_{UVLO} \times (1 + \frac{R1}{R2}) \tag{1}$$

where

- V_{UVLO} is the UVLO threshold of 1.05V at the EN/UVLO pin.

The hysteresis between the UVLO turn-on threshold and turn-off threshold is set by the upper resistor in the EN/UVLO resistor divider and is caculated using Equation 2.

$$\Delta V_{IN\,(UVLO)} = I_{UVLO_HYS} \times R1 \tag{2}$$

where

- I_{UVLO_HYS} is the sourcing current from the EN/UVLO pin when the voltage at the EN/UVLO pin is above V_{UVLO}.

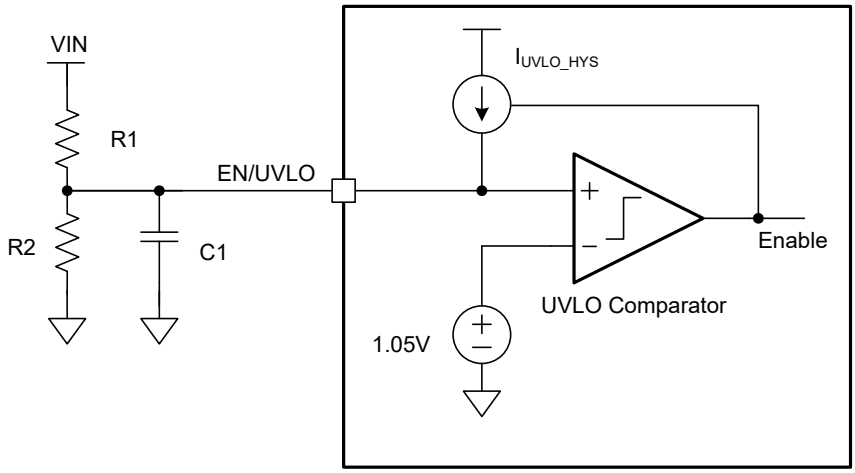


Figure 6-1. Programmable UVLO With Resistor Divider at the EN/UVLO Pin

Using an NMOSFET together with a resistor divider can implement both logic enable and programmable UVLO as shown in Figure 6-2. The EN logic high level must be greater than enable threshold plus the V_{th} of the NMOSFET. The NMOSFET also eliminates the leakage current from VIN to ground through the UVLO resistor divider during shutdown mode.

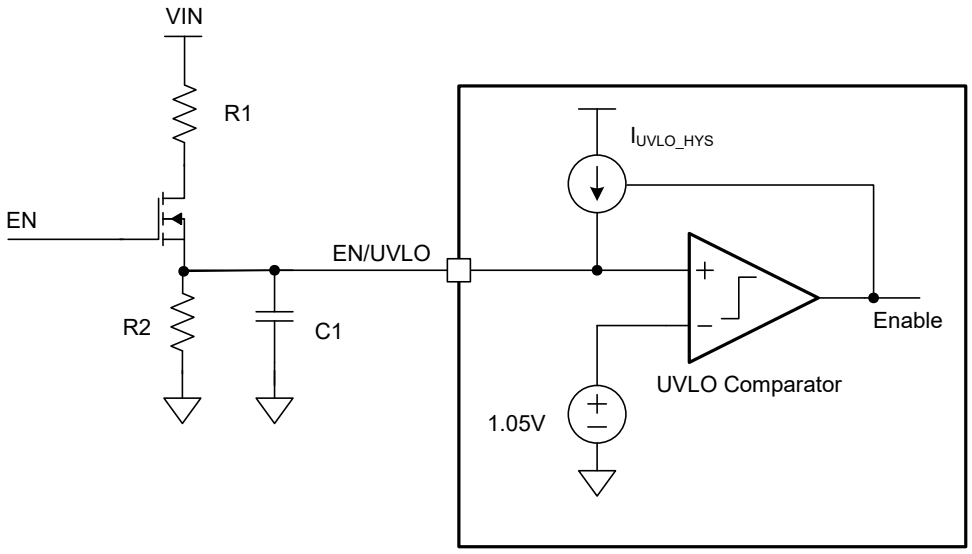


Figure 6-2. Logic Enable and Programmable UVLO

6.3.5 Soft Start

When the input voltage is above the UVLO threshold and the voltage at the EN/UVLO pin is above the enable UVLO threshold, the TPS552852 starts to ramp up the output voltage by ramping an internal reference voltage from 0V to 1.2V within typical 3.9ms.

6.3.6 Shutdown

When the EN/UVLO pin voltage is pulled below 0.4V, the TPS552852 is in shutdown mode, and all functions are disabled.

6.3.7 Switching Frequency

The TPS552852 uses a fixed frequency average current control scheme. The switching frequency is 2.1MHz for the optimization of the design size.

6.3.8 Inductor Current Limit

The TPS552852 implements both peak current and average inductor current limit. The average current mode control loop uses the current sense information at the high-side MOSFET of the boost leg to clamp the maximum average inductor current to 8A (typical).

Besides the average current limit, a peak current limit protection is implemented during transient to protect the device against an overcurrent condition beyond the capability of the device.

6.3.9 Internal Charge Path

Each of the two high-side MOSFET drivers is biased from the floating bootstrap capacitor, which is normally recharged by V_{CC} through both the external and internal bootstrap diodes when the low-side MOSFET is turned on. When the TPS552852 operates exclusively in the buck or boost regions, one of the high-side MOSFETs is constantly on. An internal charge path, from VOUT and BOOT2 to BOOT1 or from VIN and BOOT1 to BOOT2 charges the bootstrap capacitor to V_{CC} so that the high-side MOSFET remains on.

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6.3.10 Output Voltage Setting

TPS552852 output voltage is configured with feedback resistors as shown in Figure 6-3, use Equation 3 to calculate the output voltage with the reference voltage at the FB pin.

$$V_{OUT} = V_{REF} \times (1 + \frac{R_{FB_UP}}{R_{FB_BT}}) \quad (3)$$

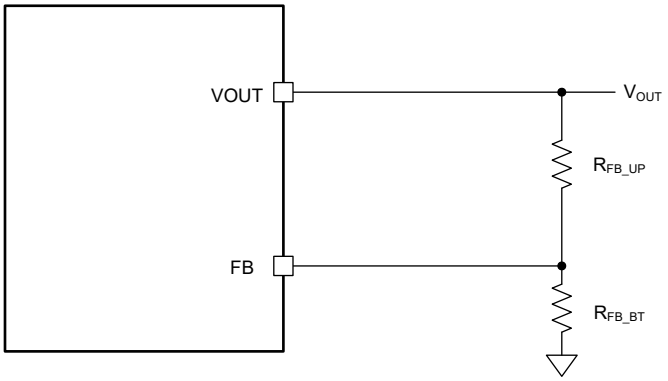


Figure 6-3. Output Voltage Setting by External Resistor Divider

TI recommends using 100kΩ for the up resistor R_{FB_UP}. The reference voltage V_{REF} is 1.2V.

6.3.11 Output Current Limit

The TPS552852 supports output current limit function in buck, buck-boost and boost mode without external current sense resistor. The output current limit is programmable by a resistor R_{ILIM} between the ILIM pin and the AGND pin. The detailed equation is updated in the following.

$$R_{ILIM}(ohm) = \frac{0.9}{I_{LIM}(A) - 0.5} \times 169000 \quad (4)$$

If the set I_{LIM} is lower than 500mA or the ILIM pin is left floating, the I_{LIM} is clamped at minimum value 500mA.

If not using this function, connect ILIM to AGND directly and the output current limit function is disabled.

6.3.12 Input Overvoltage Protection

The TPS552852 has input overvoltage protection which avoids any damage to the device in case the current flows from the output to the input and the input source cannot sink current in FPWM mode. When the input voltage at the VIN pin is detected above 22.5V typically, the internal soft-start circuit is reset when VIN OVP is triggered. The converter automatically restarts when the input voltage drops the hysteresis value lower than the input overvoltage protection threshold.

6.3.13 Output Overvoltage Protection

The TPS552852 monitors a resistor-divided feedback voltage to detect output overvoltage condition. When the feedback voltage is over 115% of the target voltage, the device stops switching until output voltage drops the 2.3% hysteresis value. This function secures the circuits connected to the output from excessive overvoltage.

6.3.14 Output Short-Circuit Protection

In addition to the average inductor current limit, the TPS552852 implements the output short-circuit protection by entering hiccup mode. After a soft start-up time of 3.9ms, the TPS552852 monitors the average inductor current and output voltage. Whenever the output short circuit happens, causing the average inductor current hitting the set limit and the output voltage below 0.8V, the TPS552852 shuts down the switching for 76ms (typical) and then

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repeats the soft start for 3.9ms. The hiccup mode helps reduce the total power dissipation on the TPS552852 in the output short-circuit or overcurrent condition.

6.3.15 Thermal Shutdown

The TPS552852 is protected by a thermal shutdown circuit that shuts down the device when the internal junction temperature exceeds 175°C (typical). The internal soft start circuit is reset when thermal shutdown is triggered. The converter automatically restarts when the junction temperature drops below the thermal shutdown hysteresis of 20°C below the thermal shutdown threshold.

6.4 Device Functional Modes

In light load condition, the TPS552852 can work in PFM or forced PWM mode to meet different application requirements. PFM mode decreases switching frequency to reduce the switching loss, thus, gets high efficiency at light load condition. The FPWM mode keeps the switching frequency unchanged to avoid undesired low switching frequency, but the efficiency becomes lower than that of PFM mode.

The functional mode is selected by MODE/SYNC pin as introduced in Section 6.3.2.

6.4.1 PWM Mode

In FPWM mode, the TPS552852 keeps the switching frequency unchanged in light load condition. When the load current decreases, the output of the internal error amplifier decreases as well to reduce the average inductor current down to deliver less power from input to output. When the output current further reduces, the current through the inductor decreases to zero during the switch-off time. The high-side N-MOSFET is not turned off even if the current through the MOSFET is zero. Thus, the inductor current changes direction after running to zero. The power flow is from output side to input side. The efficiency is low in this condition. However, with the fixed switching frequency, there is no audible noise or other problems that can be caused by low switching frequency in light load condition.

6.4.2 Power Save Mode

The TPS552852 improves the efficiency at light load condition with PFM mode. When the TPS552852 operates at light load condition, the output of the internal error amplifier decreases to make the inductor peak current down to deliver less power to the load. When the output current further reduces, the current through the inductor decreases to zero during the switch-off time. When the TPS552852 works in buck mode, after the inductor current becomes zero, the low-side switch of the buck side is turned off to prevent the reverse current from output to ground. When the TPS552852 works in boost mode, after the inductor current becomes zero, the high side-switch of the boost side is turned off to prevent the reverse current from output to input. The TPS552852 resumes switching until the output voltage drops. Thus, PFM mode reduces switching cycles and eliminates the power loss by the reverse inductor current to get high efficiency in light load condition.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS552852 can operate over a wide range of 2.4V to 22V input voltage and output 0.8V to 15V. The TPS552852 can transition among buck mode, buck-boost mode, and boost mode smoothly according to the input voltage and the setting output voltage. The TPS552852 operates in buck mode when the input voltage is greater than the output voltage and in boost mode when the input voltage is less than the output voltage. When the input voltage is close to the output voltage, the TPS552852 operates in one-cycle buck and one-cycle boost mode alternately.

7.2 Typical Application

The TPS552852 provides a small size design for power supply application with the input voltage ranging from 3V to 22V.

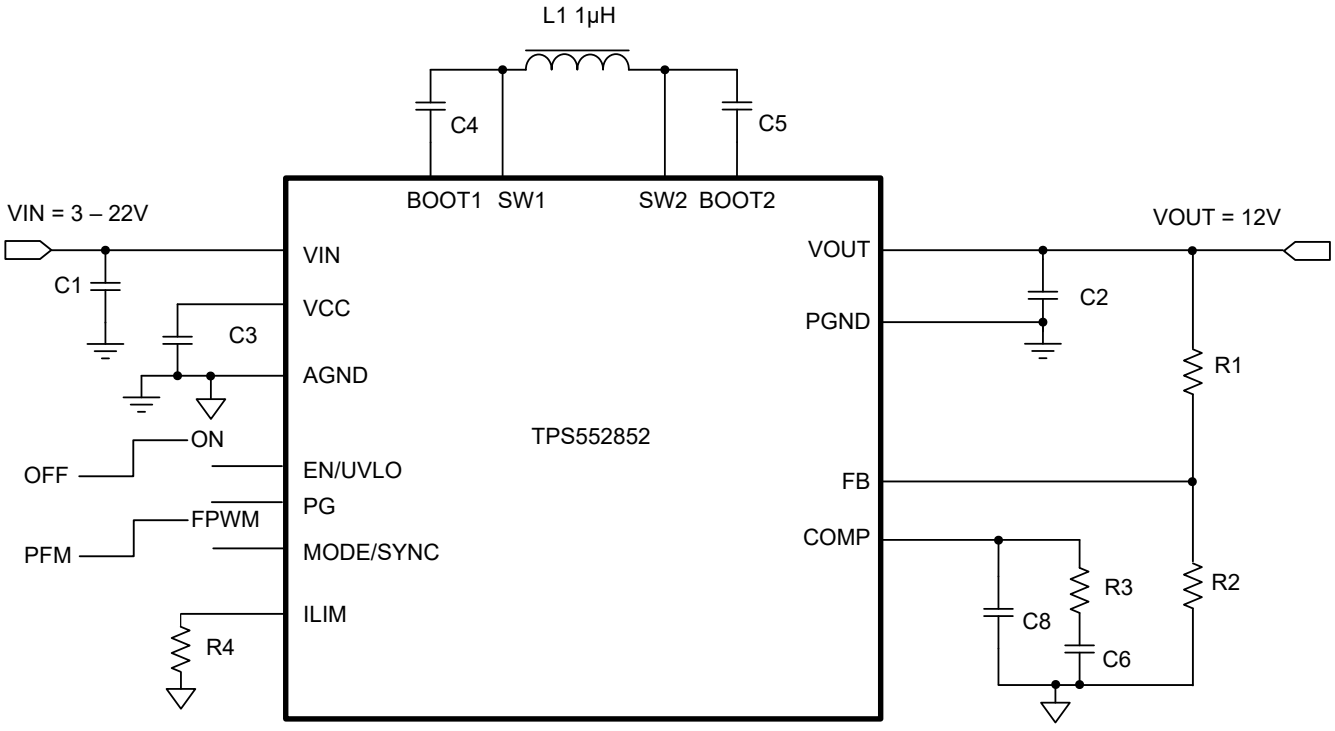


Figure 7-1. Power Supply With 3V to 22V Input Voltage

7.2.1 Design Requirements

Table 7-1 lists the design parameters:

Table 7-1. Design Parameters

PARAMETERS	VALUES
Input voltage	3V to 22V
Output voltage	12V
Output voltage ripple	±50mV
Operating mode at light load	PFM

7.2.2 Detailed Design Procedure

7.2.2.1 Inductor Selection

Because the selection of the inductor affects steady state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. There are three important inductor specifications: inductance, saturation current, and DC resistance.

The TPS552852 is designed to work with inductor values between 1µH and 2.2µH. The inductor selection is based on consideration of both buck and boost modes of operation.

The inner current loop uses internal compensation and requires the inductor value larger than $1.2/f_{SW}$

For buck mode, the inductor selection is based on limiting the peak-to-peak current ripple to the maximum inductor current at the maximum input voltage. In CCM, Equation 5 shows the relationship between the inductance and the inductor ripple current.

$$L=\frac{(V_{IN(MAX)}-V_{OUT})\times V_{OUT}}{\Delta I_{L(P-P)}\times f_{SW}\times V_{IN(MAX)}} \quad (5)$$

where

- $V_{IN(MAX)}$ is the maximum input voltage
- V_{OUT} is the output voltage
- $\Delta I_{L(P-P)}$ is the peak to peak ripple current of the inductor
- f_{SW} is the switching frequency

For a certain inductor, the inductor ripple current achieves maximum value when VOUT equals half of the maximum input voltage. Choosing higher inductance gets smaller inductor current ripple while smaller inductance gets larger inductor current ripple.

For boost mode, the inductor selection is based on limiting the peak-to-peak current ripple to the maximum inductor current at the maximum output voltage. In CCM, Equation 6 shows the relationship between the inductance and the inductor ripple current.

$$L=\frac{V_{IN}\times(V_{OUT(MAX)}-V_{IN})}{\Delta I_{L(P-P)}\times f_{SW}\times V_{OUT(MAX)}} \quad (6)$$

where

- V_{IN} is the input voltage
- $V_{OUT(MAX)}$ is the maximum output voltage
- $\Delta I_{L(P-P)}$ is the peak to peak ripple current of the inductor
- f_{SW} is the switching frequency

For a certain inductor, the inductor ripple current achieves maximum value when V_{IN} equals to the half of the maximum output voltage. Choosing higher inductance gets smaller inductor current ripple while smaller inductance gets larger inductor current ripple.

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For this application example, a 1µH inductor is selected, which produces approximate maximum inductor current ripple of 50% of the highest average inductor current in buck mode and 50% of the highest average inductor current in boost mode.

In buck mode, the inductor DC current equals to the output current. In boost mode, use Equation 7 to calculate the inductor DC current.

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (7)$$

where

- V_{OUT} is the output voltage
- I_{OUT} is the output current
- V_{IN} is the input voltage
- η is the power conversion efficiency

For a given maximum output current of the buck-boost converter TPS552852, the maximum inductor DC current happens at the minimum input voltage and maximum output voltage. Set the inductor current limit of the TPS552852 higher than the calculated maximum inductor DC current to make sure the TPS552852 has the desired output current capability.

In boost mode, use Equation 8 to calculate the inductor ripple current.

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{L \times f_{SW} \times V_{OUT}} \quad (8)$$

where

- $\Delta I_{L(P-P)}$ is the inductor ripple current
- L is the inductor value
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Therefore, use Equation 9 to caclualte the inductor peak current.

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \quad (9)$$

Normally, working with an inductor peak-to-peak current of less than 40% of the average inductor current for maximum output current is advisable. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI, but in the same way, load transient response time is increased. The selected inductor must have higher saturation current than the calculated peak current.

The conversion efficiency is dependent on the resistance of the current path. The switching loss associated with the switching MOSFETs, and the inductor core loss. Therefore, the overall efficiency is affected by the inductor DC resistance (DCR), equivalent series resistance (ESR) at the switching frequency, and the core loss. Table 7-2 lists recommended inductors for the TPS552852. In this application example, the Coilcraft inductor XGL6030-102MEC is selected for small size, high saturation current, and small DCR.

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Table 7-2. Recommended Inductors

PART NUMBER	L (µH)	DCR (MAXIMUM) (mΩ)	SATURATION CURRENT / HEAT RATING CURRENT (A)	SIZE (L x W x H mm)	VENDOR(1)
XGL6030-102MEC	1	4.9	17.7/18.1	6.7 × 6.5 × 3.1	Coilcraft
VCHA085D-1R0MS6	1	4.8	22/18	8.7 × 8.2 × 5.2	Cyntec
IHLP4040DZER1R0M01	1	2.5	20/25	10.2 × 10.2 × 4.0	Vishay

(1) See the *Third-Party Products Disclaimer*.

7.2.2.2 Input Capacitor

In buck mode, the input capacitor supplies high ripple current. Equation 10 gives the RMS current in the input capacitors.

$$I_{CIN(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times V_{IN}}} \quad (10)$$

where

- $I_{CIN(RMS)}$ is the RMS current through the input capacitor
- I_{OUT} is the output current

The maximum RMS current occurs at the output voltage is half of the input voltage, which gives $I_{CIN(RMS)} = I_{OUT} / 2$. Ceramic capacitors are recommended for thei low ESR and high ripple current capability. A total of 20µF effective capacitance is a good starting point for this application.

7.2.2.3 Output Capacitor

In boost mode, the output capacitor conducts high ripple current. Equation 11 calculates the output capacitor RMS ripple, where the minimum input voltage and the maximum output voltage correspond to the maximum capacitor current.

$$I_{COUT(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} - 1} \quad (11)$$

where

- $I_{COUT(RMS)}$ is the RMS current through the output capacitor
- I_{OUT} is the output current

The ESR of the output capacitor causes an output voltage ripple given by Equation 12 in boost mode.

$$V_{RIPPLE(ESR)} = \frac{I_{OUT} \times V_{OUT}}{V_{IN}} \times R_{COUT} \quad (12)$$

where

- R_{COUT} is the ESR of the output capacitance

The capacitance also causes a capacitive output voltage ripple given by Equation 13 in boost mode. When input voltage reaches the minimum value and the output voltage reaches the maximum value, there is the largest output voltage ripple caused by the capacitance.

$$V_{RIPPLE(CAP)} = \frac{I_{OUT} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right)}{C_{OUT} \times f_{SW}} \quad (13)$$

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Typically, a combination of ceramic capacitors and bulk electrolytic capacitors is needed to provide low ESR, high ripple current, and small output voltage ripple. From the required output voltage ripple, use Equation 12 and Equation 13 to calculate the minimum required effective capacitance of the C_{OUT}.

7.2.2.4 Output Current Limit

The output current limit is implemented by setting a resistor between the ILIM pin and AGND pin.

7.2.2.5 Loop Stability

The TPS552852 uses average current control scheme. The inner current loop uses internal compensation and requires the inductor value must be larger than $1.2/f_{SW}$. The outer voltage loop requires an external compensation. The COMP pin is the output of the internal voltage error amplifier. An external compensation network comprised of resistor and ceramic capacitors is connected to the COMP pin.

The TPS552852 operates in buck mode or boost mode. Therefore, both buck and boost operating modes require loop compensations. The restrictive one of both compensations is selected as the overall compensation from a loop stability point of view. Typically for a converter designed either work in buck mode or boost mode, the boost mode compensation design is more restrictive due to the presence of a right half plane zero (RHPZ).

The power stage in boost mode can be modeled by Equation 14.

$$G_{PS}(s) = \frac{R_{LOAD} \times (1-D)}{2 \times R_{SENSE}} \times \frac{\left(1 + \frac{s}{2\pi \times f_{ESRZ}}\right) \times \left(1 - \frac{s}{2\pi \times f_{RHPZ}}\right)}{1 + \frac{s}{2\pi \times f_P}} \tag{14}$$

where

- R_{LOAD} is the output load resistance
- D is the switching duty cycle in boost mode
- R_{SENSE} is the equivalent internal current sense resistor, which is 0.055Ω

The power stage has two zeros and one pole generated by the output capacitor and load resistance. Use Equation 15 to Equation 17 to calculate them.

$$f_P = \frac{2}{2\pi \times R_{LOAD} \times C_{OUT}} \tag{15}$$

$$f_{ESRZ} = \frac{1}{2\pi \times R_{COUT} \times C_{OUT}} \tag{16}$$

$$f_{RHPZ} = \frac{R_{LOAD} \times (1-D)^2}{2\pi \times L} \tag{17}$$

The internal transconductance amplifier together with the compensation network at the COMP pin constitutes the control portion of the loop. Equation 18 shows the transfer function of the control portion.

$$G_C(s) = \frac{G_{EA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{\left(1 + \frac{s}{2\pi \times f_{COMZ}}\right)}{\left(1 + \frac{s}{2\pi \times f_{COMP1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{COMP2}}\right)} \tag{18}$$

where

- G_{EA} is the transconductance of the error amplifier
- R_{EA} is the output resistance of the error amplifier
- V_{REF} is the reference voltage input to the error amplifier
- V_{OUT} is the output voltage

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- f_{COMP1} and f_{COMP2} are the pole's frequency of the compensation network
- f_{COMZ} is the zero's frequency of the compensation network

The total open-loop gain is the product of one or more G_{PS} and G_C. The next step is to select the loop crossover frequency, f_C, at which the total open-loop gain is 1, namely 0dB. The higher in frequency that the loop gain stays above 0dB before crossing over, the faster the loop response. The loop gain crossing over 0dB at the frequency no higher than the lower of either 1/10 of the switching frequency, f_{SW} or 1/5 of the RHPZ frequency, f_{RHPZ} is generally accepted.

Then, set the value of R_C, C_C, and C_P by Equation 19 to Equation 21.

$$R_C = \frac{2\pi \times V_{OUT} \times R_{SENSE} \times C_{OUT} \times f_C}{(1-D) \times V_{REF} \times G_{EA}} \quad (19)$$

where

- f_C is the selected crossover frequency

$$C_C = \frac{R_{LOAD} \times C_{OUT}}{2 \times R_C} \quad (20)$$

$$C_P = \frac{R_{COUT} \times C_{OUT}}{R_C} \quad (21)$$

If the calculated C_P is less than 10pF, the position of C_P can be left open.

Designing the loop for greater than 45° of phase margin and greater than 10dB gain margin eliminates output voltage ringing during the line and load transient.

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7.2.3 Application Curves

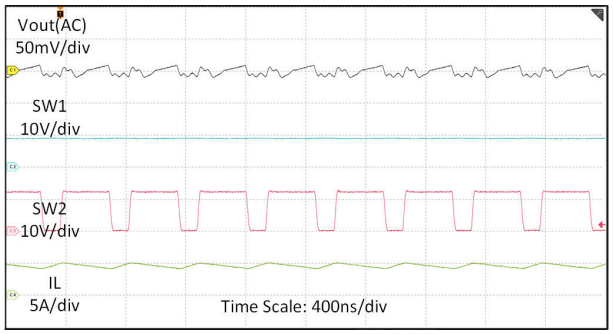


Figure 7-2. Switching Waveforms in V_{IN} = 9V, V_{OUT} = 12V, I_O = 3A, FPWM

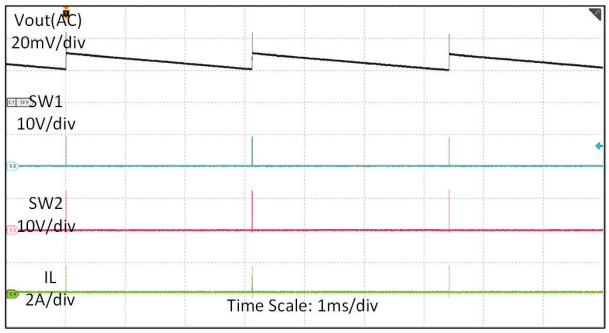


Figure 7-3. Switching Waveforms in V_{IN} = 9V, V_{OUT} = 12V, I_O = 0A, PFM

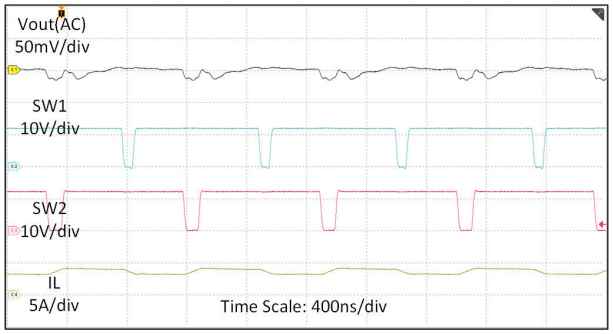


Figure 7-4. Switching Waveforms in V_{IN} = 12V, V_{OUT} = 12V, I_O = 3A, FPWM

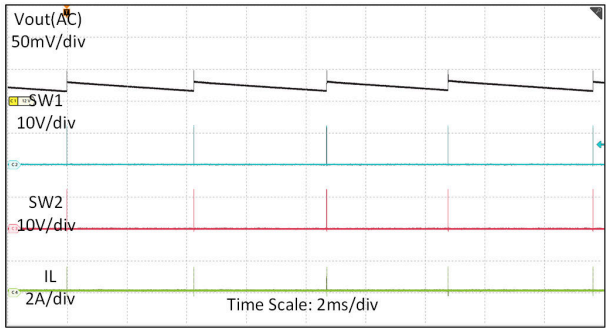


Figure 7-5. Switching Waveforms in V_{IN} = 12V, V_{OUT} = 12V, I_O = 0A, PFM

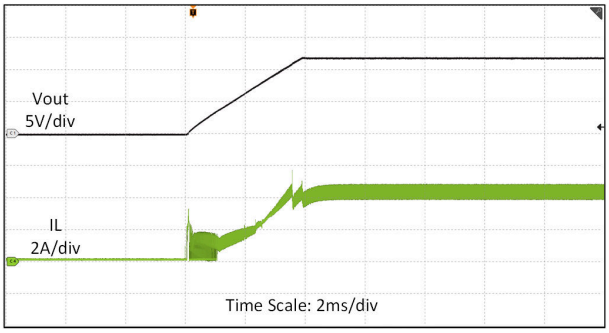


Figure 7-6. Start-up Waveforms in V_{IN} = 9V, V_{OUT} = 12V, R_{LOAD} = 4Ω, FPWM

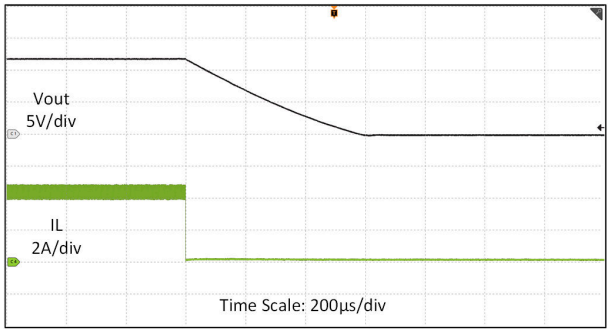


Figure 7-7. Shutdown Waveforms in V_{IN} = 9V, V_{OUT} = 12V, R_{LOAD} = 4Ω, FPWM

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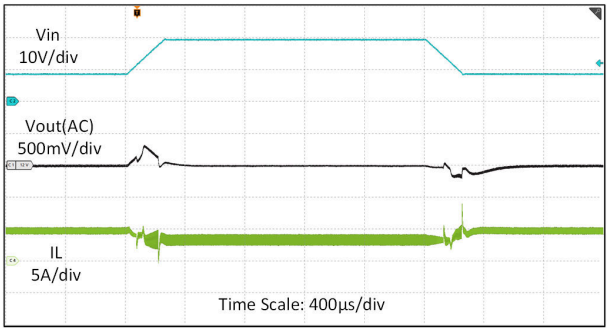


Figure 7-8. Line Transient Waveforms in V_{IN} = 9V to 20V, V_{OUT} = 12V, I_O = 3A with 200µs Slew Rate, FPWM

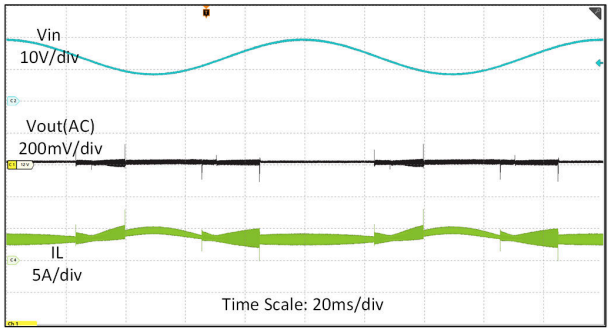


Figure 7-9. Line Sweep Waveforms in V_{IN} = 9V to 20V, V_{OUT} = 12V, I_O = 3A, FPWM

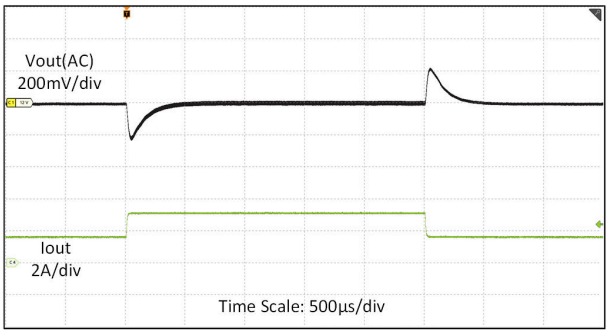


Figure 7-10. Load Transient Waveforms in V_{IN} = 9V, V_{OUT} = 12V, I_O = 1.5A to 3A, FPWM

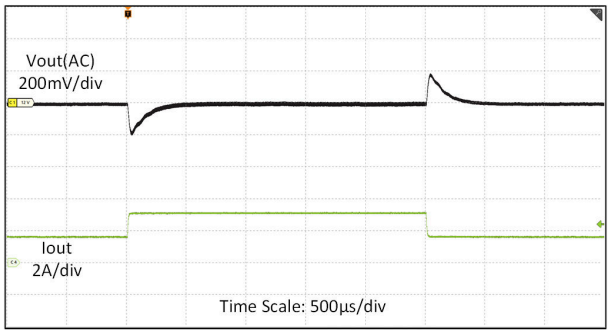


Figure 7-11. Load Transient Waveforms in V_{IN} = 12V, V_{OUT} = 12V, I_O = 1.5A to 3A, FPWM

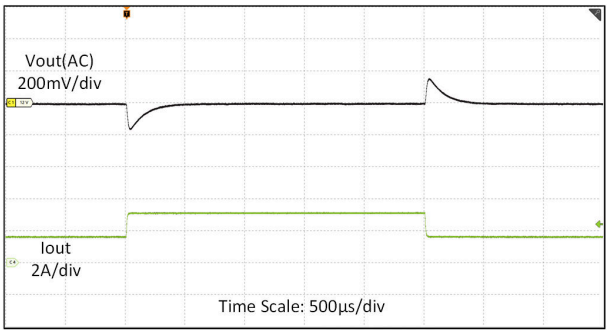


Figure 7-12. Load Transient Waveforms in V_{IN} = 12V, V_{OUT} = 12V, I_O = 1.5A to 3A, FPWM

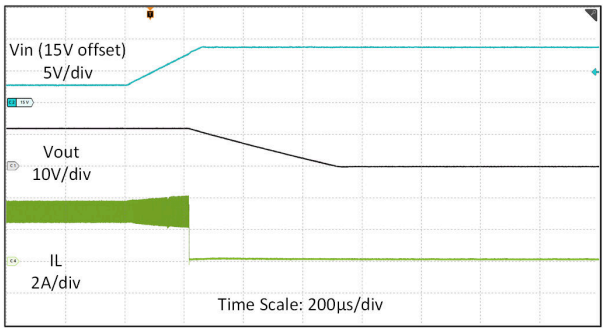


**Figure 7-13. VIN OVP Waveforms in V_{IN} = 18V to 24V,
V_{OUT} = 12V, I_{OUT} = 3A**

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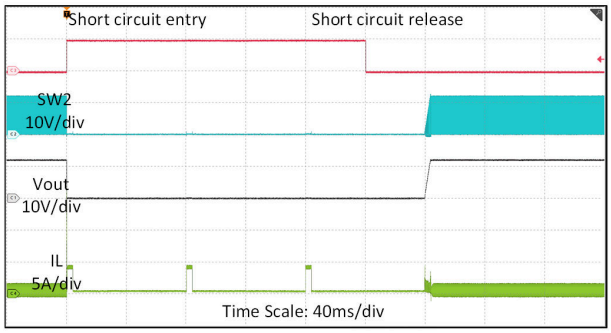


Figure 7-14. Short-Circuit Protection in V_{IN} = 9V, V_{OUT} = 12V

7.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 3.0V to 22V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. A typical choice is an aluminum electrolytic capacitor with a value of 100µF.

7.4 Layout

7.4.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully done, the regulator can suffer from instability and noise problems.

1. Place the 0.1µF small package (0402) ceramic capacitors close to the VIN/VOUT pins to minimize high frequency current loops. This action improves the radiation of high-frequency noise (EMI) and efficiency.
2. Use multiple GND vias near PGND pin to connect the PGND to the internal ground plane. This action also improves thermal performance.
3. Minimize the SW1 and SW2 loop areas as these are high dv/dt nodes. Use a ground plane under the switching regulator to minimize interplane coupling.
4. Place the BOOT1 bootstrap capacitor close to the IC and connect directly to the BOOT1 to SW1 pins. Place the BOOT2 bootstrap capacitor close to the IC and connect directly to the BOOT2 and SW2 pins.
5. Place the VCC capacitor close to the IC with wide and short trace. The GND terminal of the VCC capacitor must be directly connected with PGND plane through three to four vias.
6. Isolate the power ground from the analog ground. The PGND plane and AGND plane are connected at the terminal of the VCC capacitor. Then the noise caused by the MOSFET driver and parasitic inductance does not interface with the AGND and internal control circuit.
7. Place the compensation components as close to the COMP pin as possible. Keep the compensation components, feedback components, and other sensitive analog circuitry far away from the power components, switching nodes SW1 and SW2, and high-current trace to prevent noise coupling into the analog signals.
8. To improve thermal performance, TI recommends to use thermal vias close to the VIN pin to a large VIN area, and the VOUT pin to a large VOUT area separately.

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7.4.2 Layout Example

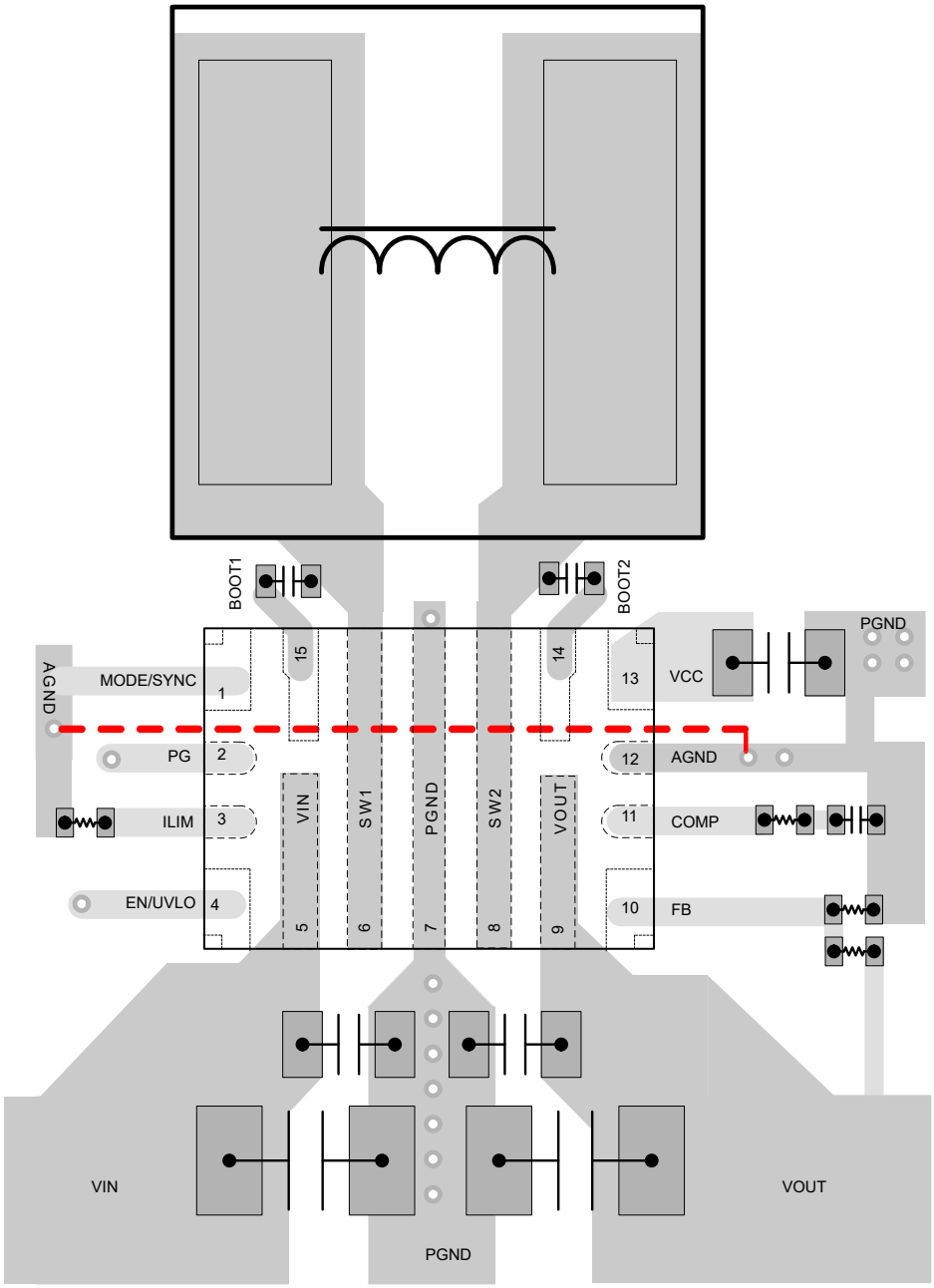


Figure 7-15. Layout Example

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8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

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8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

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8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

DATE	REVISION	NOTES
March 2026	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS552852VALR	Active	Production	WQFN-HR (VAL) | 15	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	552852

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

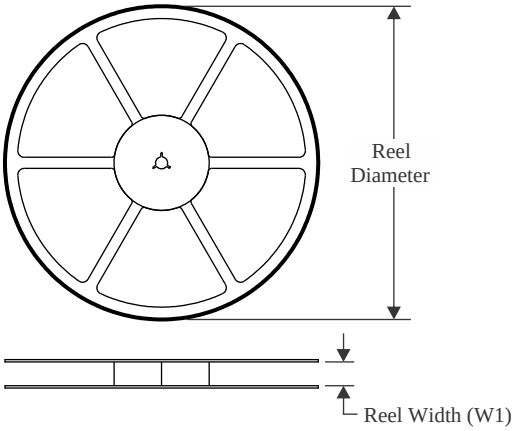
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

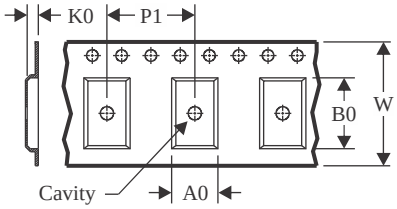
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

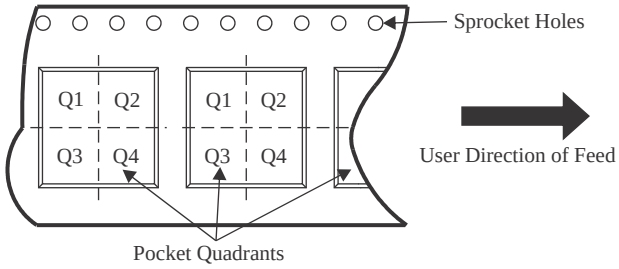


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

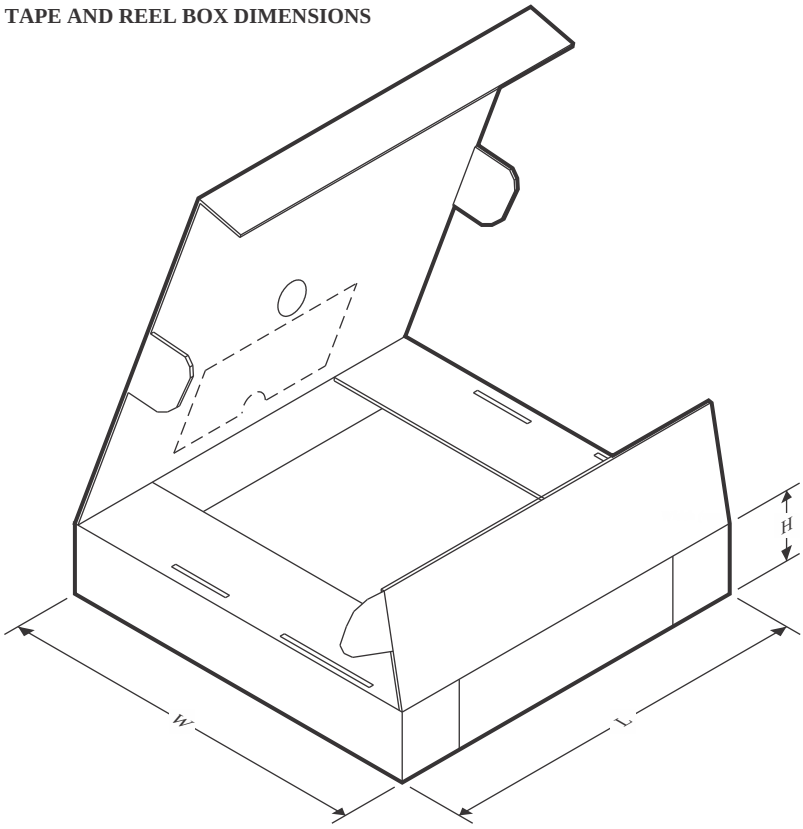
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS552852VALR	WQFN-HR	VAL	15	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

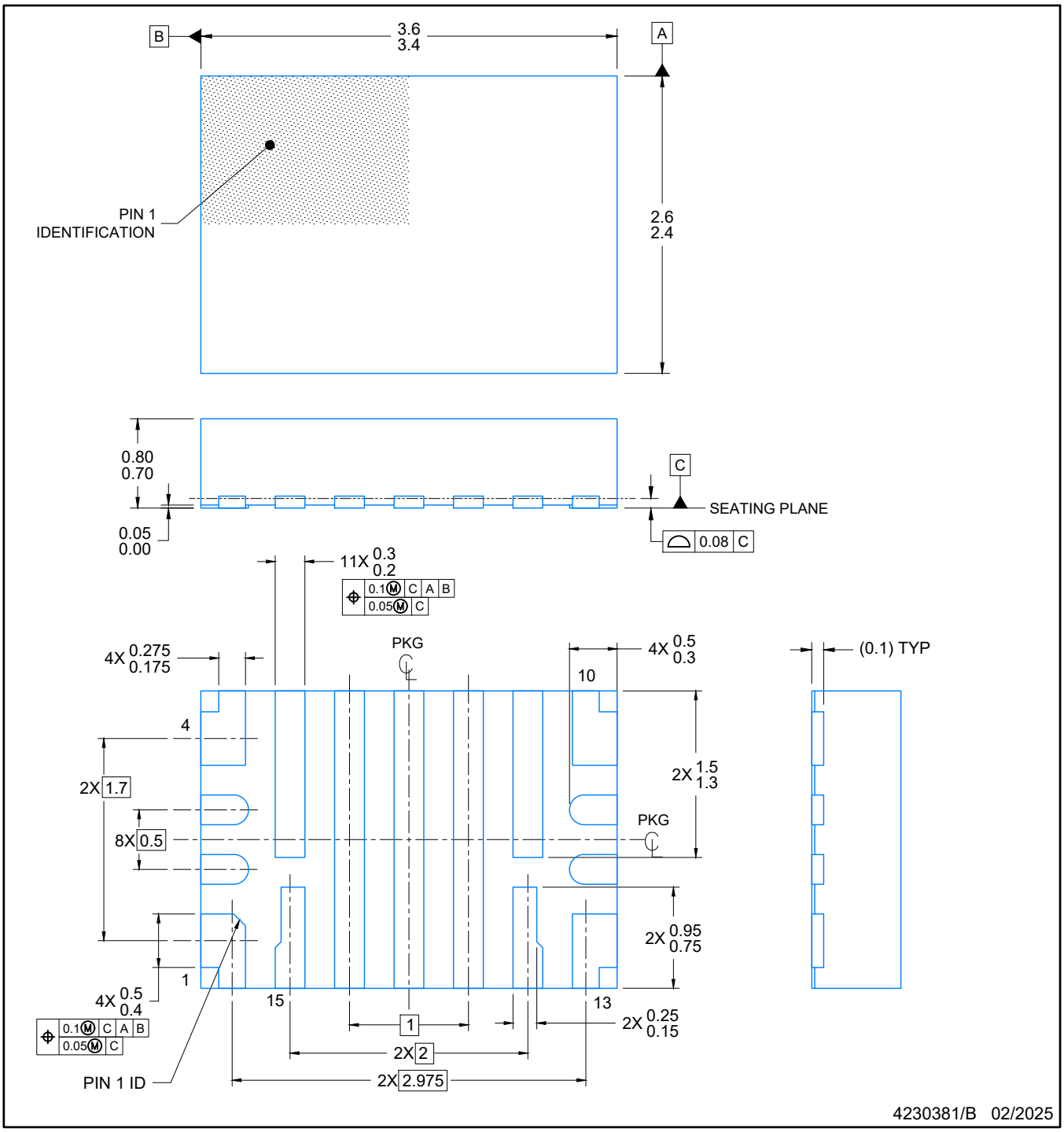
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS552852VALR	WQFN-HR	VAL	15	3000	210.0	185.0	35.0

PACKAGE OUTLINE

VAL0015A

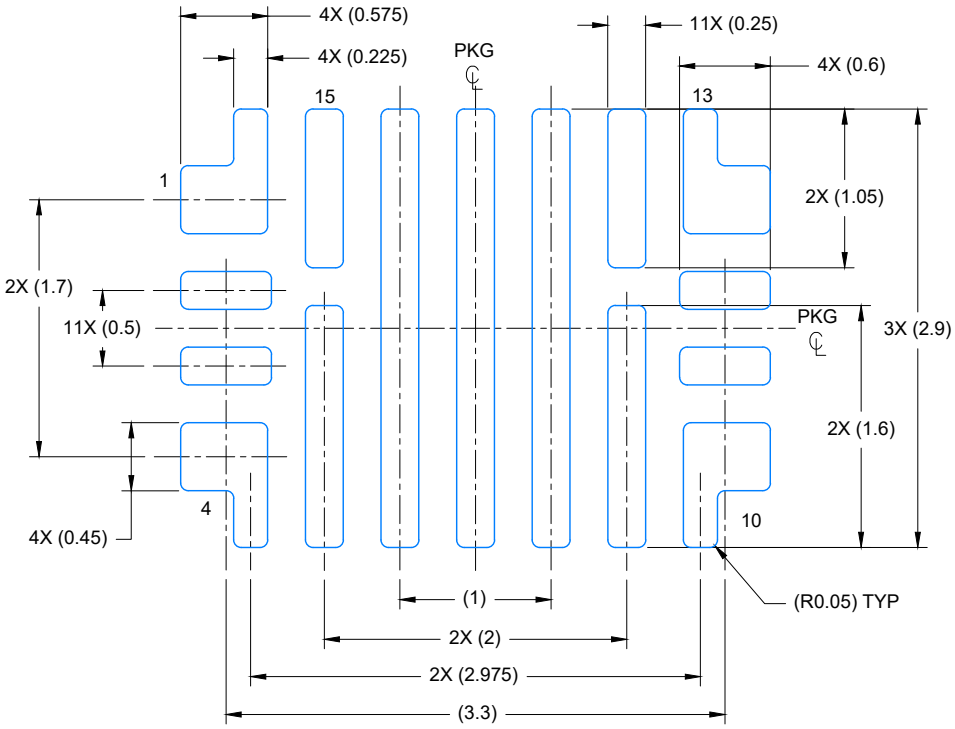
WQFN-HR - 0.8 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

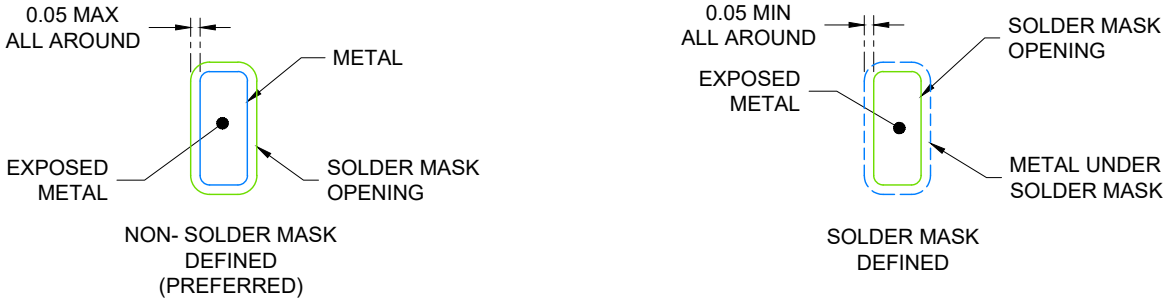


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

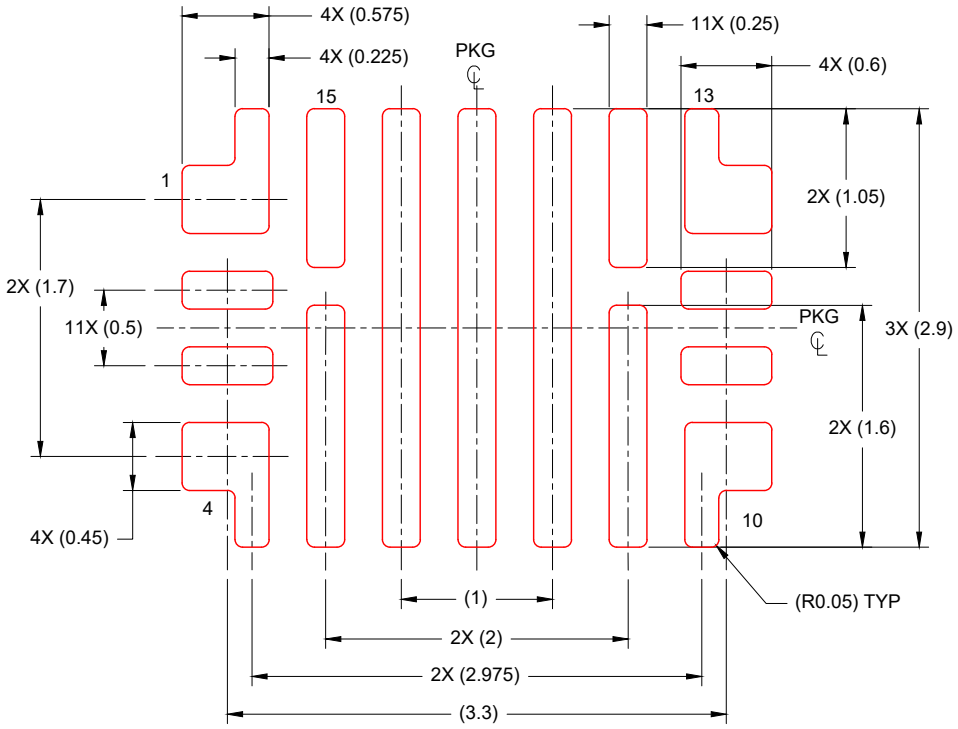


SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025