TPS561300 4.5V to 30V, 1A, EMI-Friendly, Synchronous Step-Down Converter

1 Features

- Configured for a wide range of applications
  - 4.5V to 30V input voltage range
  - Up to 1A continuous output current
  - 0.6V ± 1.5% reference voltage (25°C)
  - Supports low drop out mode
- High efficiency
  - Integrated 100mΩ and 60mΩ MOSFETs
  - Low 2µA shutdown, 26µA quiescent current
  - Pulse frequency modulation (PFM) for high light load efficiency
- Ease of use
  - Peak current mode control with internal loop compensation
  - Fixed 1200kHz switching frequency
  - Internal 5ms soft start
  - Frequency spread spectrum to reduce electromagnetic interference (EMI)
  - Overcurrent protection for both MOSFETs with hiccup mode protection
  - Non-latched protection for over temperature protection (OTP), overcurrent protection (OCP), overvoltage protection (OVP), and undervoltage lockout (UVLO)
  - SOT-23 (6) package

2 Applications

- 12V, 24V distributed power-bus supply
- Industry application
  - White goods
- Consumer application
  - Audio
  - Set-top box (STB), digital television (DTV)
  - Printer

3 Description

The TPS561300 is a 4.5V to 30V input voltage range, 1A, synchronous buck converter. The device includes two integrated switching FETs, internal loop compensation, and 5ms internal soft start to reduce component count.

By integrating the MOSFETs and employing the SOT-23 package, the TPS561300 achieves the high power density and offers a small footprint on the PCB.

The TPS561300 operates in pulse frequency modulation for high light load efficiency and reduces the power loss. The frequency spread spectrum operation is introduced for EMI reduction.

Cycle-by-cycle current limit in both high-side MOSFET protects the converter in an overload condition and is enhanced by a low-side MOSFET freewheeling current limit which prevents current runaway. Hiccup mode protection is triggered if the overcurrent condition has persisted for longer than the present time.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS561300	DDC (SOT-23-THN, 6)	2.9mm × 2.8mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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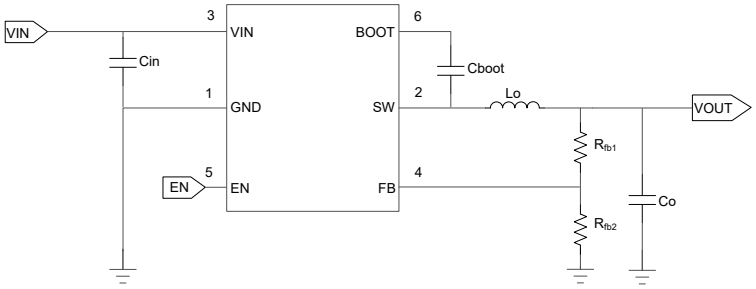
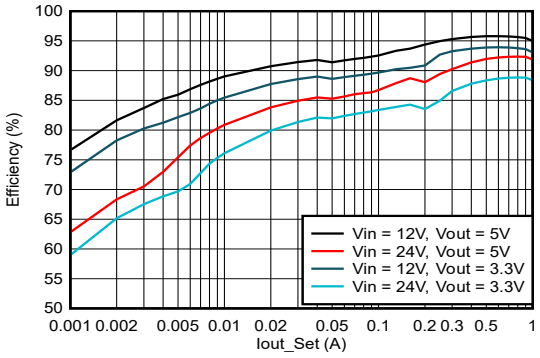


TPS561300 Simplified Schematic



Efficiency vs Output Current

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4 Pin Configuration and Functions

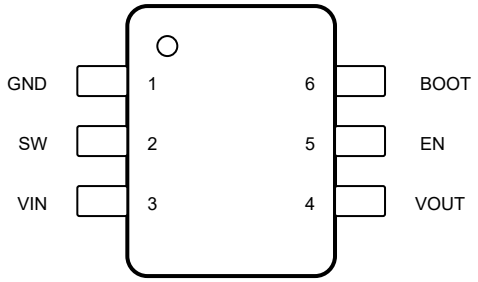

Figure 4-1. 6-Pin SOT-23-THN, DDC Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
BOOT	6	O	Supply input for the high-side NFET gate drive circuit. Connect a 0.1µF capacitor between BOOT and SW pins.
EN	5	I	This pin is the enable pin. Float the EN pin to enable.
FB	4	I	Converter feedback input. Connect to output voltage with feedback resistor divider for TPS542021, connect to output capacitors to get fixed 5V for TPS542025.
GND	1	—	Ground pin. Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	O	Switch node connection between high-side NFET and low-side NFET.
VIN	3	—	Input voltage supply pin. The drain terminal of high-side power NFET.

(1) O = Output; I = Input

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5 Specifications

5.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to +150°C , unless otherwise noted(1)

		MIN	MAX	UNIT
Input voltage range, V_I	VIN	–0.3	32	V
	EN	–0.3	7	V
	FB	–0.3	7	V
Output voltage range, V_O	BOOT-SW	–0.3	7	V
	SW	–0.3	32	V
	SW (20ns transient)	–5	32	V
Operating junction temperature(2), T_J		–40	150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. A*Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Operating at junction temperatures greater than 150°C, although possible, degrades the lifetime of the device.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_I	Input voltage range	VIN	4.5	30	V
		EN	–0.1	5.5	V
		FB	–0.1	5.5	V
V_O	Output voltage range	BOOT-SW	–0.1	5.5	V
		SW	–0.1	30	V
T_J	Operating junction temperature		–40	150	°C

5.4 Thermal Information

THERMAL METRIC (1)		TPS561300 DDC (SOT-23-THN, 6)		UNIT
		JEDEC(2)	EVM(3)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118.6	N/A	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.6	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.4	N/A	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.5	N/A	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.7	N/A	°C/W
$R_{\theta JA\_EVM}$	Junction-to-ambient thermal resistance on official EVM board	N/A	57.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were simulated on a standard JEDEC board. These values do not represent the performance obtained in an actual application.

(3) The real $R_{\theta JA}$ is tested on TI EVM.

5.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product. T_J = –40°C to +150°C, V_{IN} = 4.5V to 30V, (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input voltage range		4.5		30	V
I_Q	Non switching quiescent current	EN = 5V, VFB = 1V		26		µA
I_{OFF}	Shut down current	EN = GND		2		µA
$V_{IN(UVLO)}$	VIN undervoltage lockout	Rising V_{IN}	3.9	4.2	4.5	V
		Falling V_{IN}	3.4	3.7	4	V
	Hysteresis		400	480	650	mV
ENABLE (EN PIN)						
$V_{(EN\_RISING)}$	Enable threshold	Rising		1.21	1.28	V
$V_{(EN\_FALLING)}$		Falling	1.1	1.19		V
$I_{(EN\_INPUT)}$	Input current	V_{EN} = 1V		0.7		µA
$I_{(EN\_HYS)}$	Hysteresis current	V_{EN} = 1.5V		1.55		µA
FEEDBACK AND ERROR AMPLIFIER						
V_{FB}	Feedback voltage	V_{IN} = 12V	0.587	0.596	0.605	V
PULSE SKIP MODE						
$I_{(SKIP)}$ (1)	Pulse skip mode peak inductor current threshold	V_{IN} = 24V, V_{OUT} = 5V, L = 15µH		300		mA
POWER STAGE						
$R_{(HSD)}$	High-side FET on resistance	T_A = 25°C, V_{BST} – SW = 6V		100		mΩ
$R_{(LSD)}$	Low-side FET on resistance	T_A = 25°C, V_{IN} = 12V		60		mΩ
CURRENT LIMIT						
$I_{(LIM\_HS)}$	High side current limit		1.6	1.8	2.2	A
$I_{(LIM\_LS)}$	Low side source current limit		1.3	1.6	1.9	A
OSCILLATOR						
F_{sw}	Centre switching frequency		1050	1200	1350	kHz
OVER TEMPERATURE PROTECTION						
Thermal Shutdown(1)	Rising temperature			160		°C
	Hysteresis			10		°C
	Hiccup time			32768		Cycles

(1) Not production tested

5.6 Timing Requirements

		MIN	TYP	MAX	UNIT
OVERCURRENT PROTECTION					
t_{HIC_WAIT}	Hiccup up wait time		512		Cycles
$t_{HIC\_RESTART}$	Hiccup up time before restart		16384		Cycles
t_{SS}	Soft-start time		5		mS
ON TIME CONTROL					
t_{MIN_ON} (1)	Minimum on time, measured at 90% to 90% and 1A loading		110		ns

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5.7 Typical Characteristics

V_{IN} = 12V, unless otherwise specified

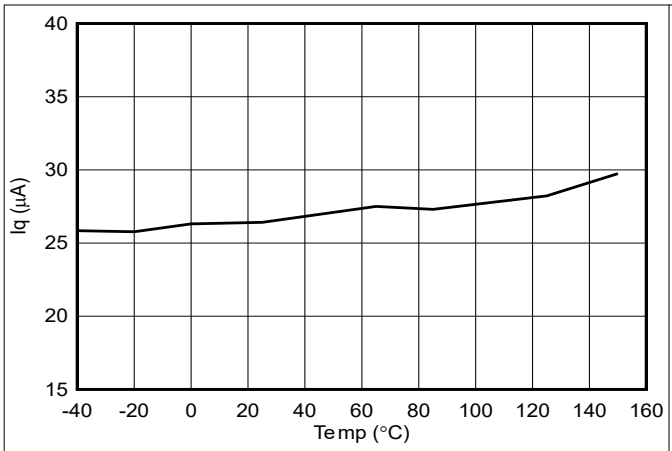

Figure 5-1. Non-Switching Operating Quiescent Current vs Junction Temperature

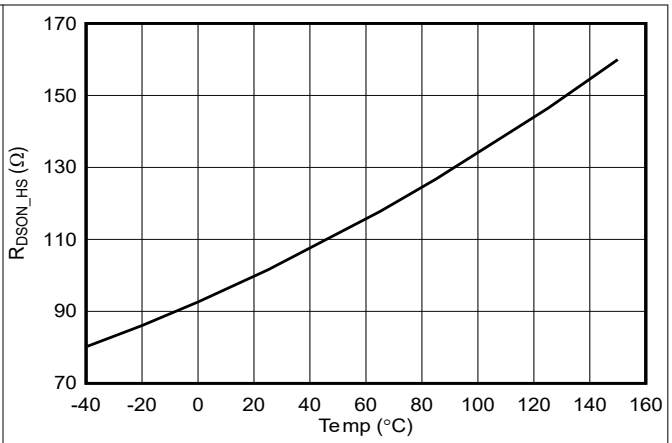

Figure 5-2. High-Side Resistance vs Junction Temperature

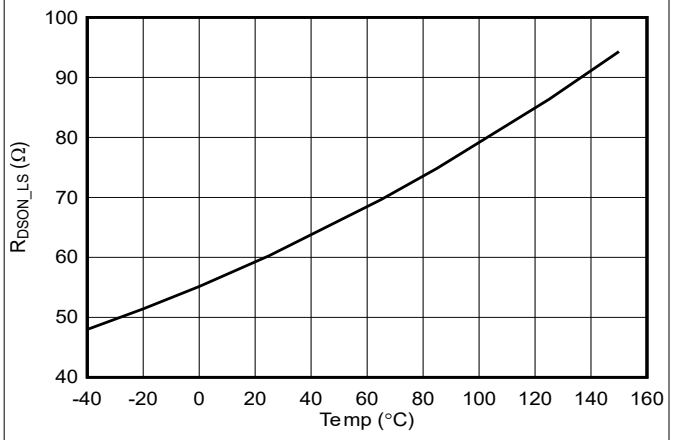

Figure 5-3. Low-Side FET On Resistance vs Junction Temperature

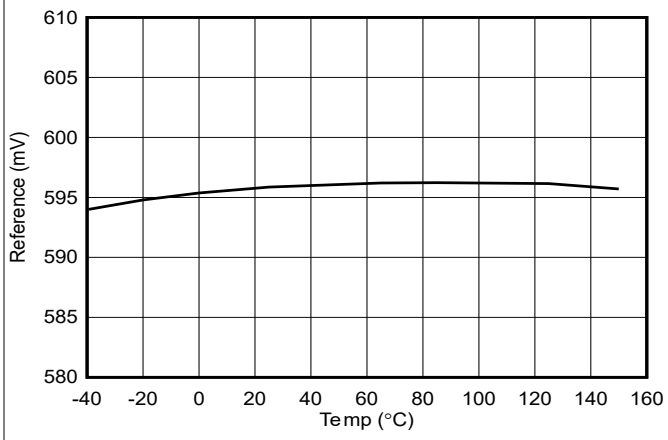

Figure 5-4. Reference Voltage vs Junction Temperature

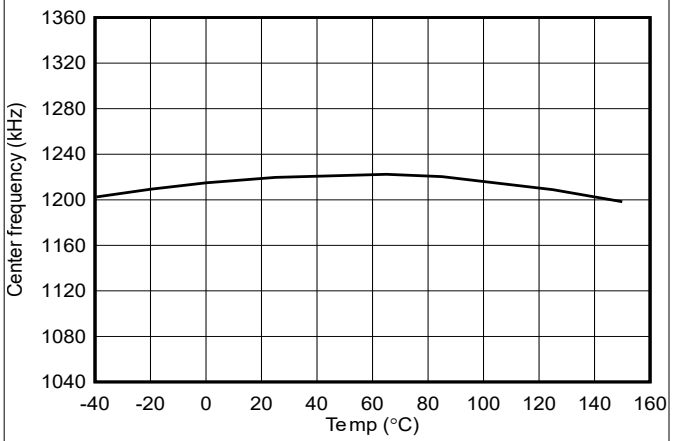

Figure 5-5. Centre Switching Frequency vs Junction Temperature

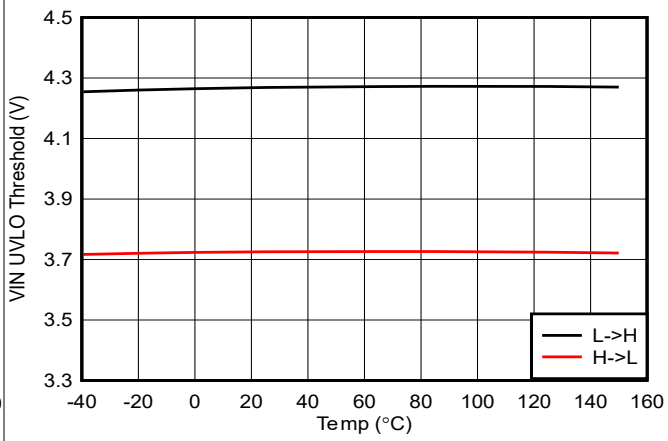

Figure 5-6. VIN UVLO Threshold vs Junction Temperature

5.7 Typical Characteristics (continued)

V_{IN} = 12V, unless otherwise specified

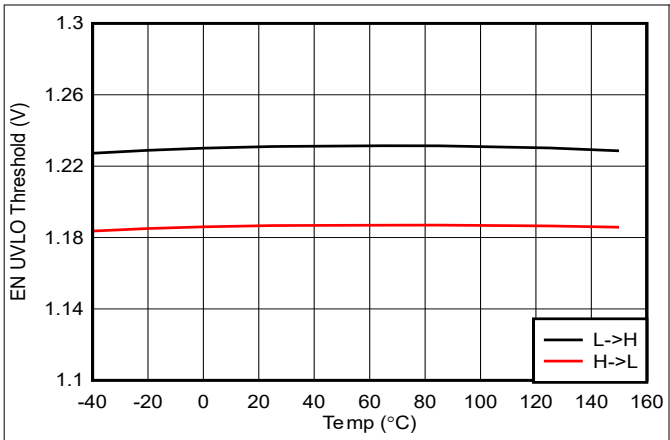

Figure 5-7. EN Threshold vs Junction Temperature

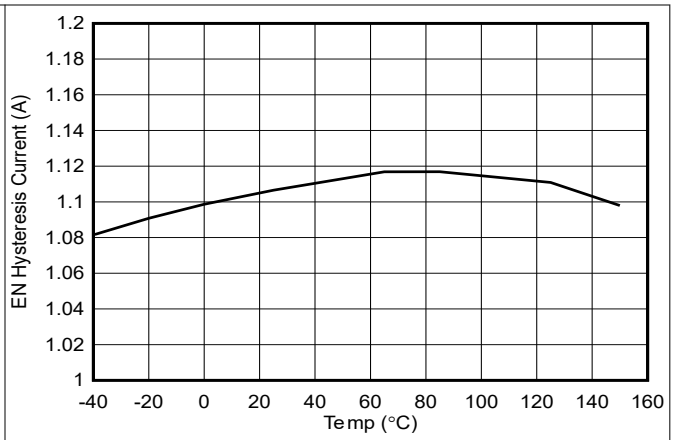

Figure 5-8. EN Hysteresis Current vs Junction Temperature

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6 Detailed Description

6.1 Overview

The TPS561300 device is a 30V, 1A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients the device implements a constant-frequency, peak current mode control which reduces output capacitance. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

The switching frequency is fixed to 1200kHz. The device begins switching at VIN equal to 4.5V. The operating current is 26µA typically when not switching and under no load. When the device is disabled, the supply current is 2µA typically.

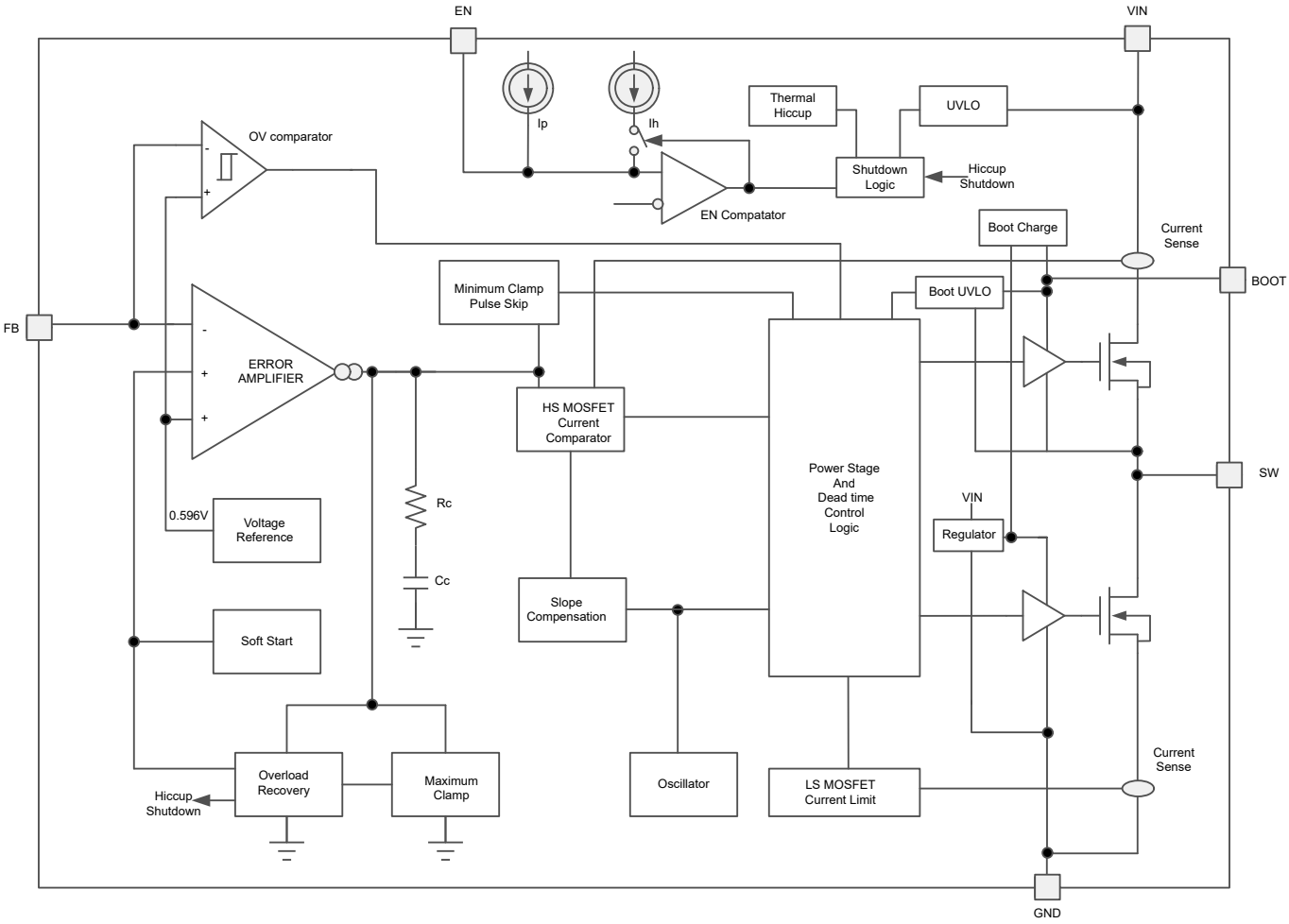
The integrated 100mΩ high-side MOSFET and 60mΩ low-side allow for high efficiency power supply designs with continuous output currents up to 1A.

The device reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by an external capacitor on the BOOT to PH pins. The boot capacitor voltage is monitored by an UVLO circuit and turns the high-side MOSFET off when the voltage falls below a preset threshold of 2.1V typically.

The device minimizes excessive output overvoltage transients by taking advantage of the overvoltage comparator. When the regulated output voltage is greater than 108% of the nominal voltage, the overvoltage comparator is activated, and the high-side MOSFET is turned off and masked from turning on until the output voltage is lower than 104%.

The device has internal 5ms soft-start time to minimize inrush currents.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Fixed-Frequency PWM Control

The device uses a fixed-frequency, peak current-mode control. The output voltage is compared through external resistors on the FB pin to an internal voltage reference by an error amplifier. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is compared to the current of the high-side power switch. When the power-switch current reaches the error amplifier output voltage level, the high side power switch is turned off and the low-side power switch is turned on. The error amplifier output voltage increases and decreases as the output current increases and decreases. The device implements a current-limit by clamping the error amplifier voltage to a maximum level and also implements a minimum clamp for improved transient-response performance.

6.3.2 Pulse Frequency Mode

The TPS561300 is designed to operate in pulse frequency mode at light load currents to boost light load efficiency. When the peak inductor current is lower than 300mA typically, the device enters pulse frequency mode. When the device is in pulse frequency mode, the error amplifier output voltage is clamped which prevents the high side integrated MOSFET from switching. The peak inductor current must rise above 300mA and exit pulse frequency mode. Because the integrated current comparator catches the peak inductor current only, the average load current entering pulse frequency mode varies with the applications and external output filters.

6.3.3 Error Amplifier

The device has a transconductance amplifier as the error amplifier. The error amplifier compares the FB voltage to the lower of the internal soft-start voltage or the internal 0.596V voltage reference. The transconductance of the error amplifier is 240µA/V typically. The frequency compensation components are placed internal between the output of the error amplifier and ground.

6.3.4 Slope Compensation and Output Current

The device adds a compensating ramp to the signal of the switch current. This slope compensation prevents sub-harmonic oscillations as the duty cycle increases. The available peak inductor current remains constant over the full duty-cycle range.

6.3.5 Enable and Adjusting Undervoltage Lockout

The EN pin provides electrical on and off control of the device. When the EN pin voltage exceeds the threshold voltage, the device begins operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters the low-quiescent (IQ) state.

The EN pin has an internal pullup-current source, which allows the user to float the EN pin to enable the device. If an application requires control of the EN pin, use open-drain or open-collector output logic to interface with the pin.

The device implements internal undervoltage-lockout (UVLO) circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 480mV.

If an application requires a higher UVLO threshold on the VIN pin, then the EN pin can be configured as shown in Figure 6-1. When using the external UVLO function, TI recommends setting the hysteresis at a value greater than 500mV.

The EN pin has a small pullup current, Ip, which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function because the pullup current increases by Ih when the EN pin crosses the enable threshold. Use Equation 1 and Equation 2 to calculate the values of R4 and R5 for a specified UVLO threshold.

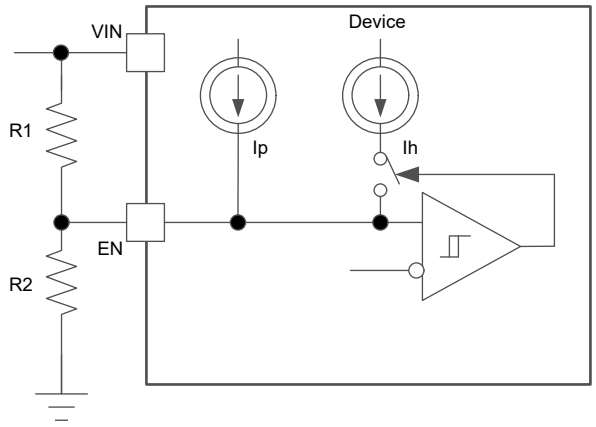

Figure 6-1. Adjustable VIN Undervoltage Lockout

$$R_4 = \frac{\frac{V_{ENfalling}}{V_{ENrising}} \times V_{START} - V_{STOP}}{I_p \times \left(1 - \frac{V_{ENfalling}}{V_{ENrising}}\right) + I_h} \quad (1)$$

$$R_5 = \frac{R_4 \times V_{ENfalling}}{V_{STOP} - V_{ENfalling} + \left(I_h + I_p\right) \times R_4} \quad (2)$$

Where:

I_p = 0.7µA
I_h = 1.55µA
$V_{ENfalling}$ = 1.19V
$V_{ENrising}$ = 1.22V

6.3.6 Safe Start-Up into Prebiased Outputs

The device has been designed to prevent the low-side MOSFET from discharging a prebiased output. During monotonic prebiased start-up, both high-side and low-side MOSFETs are not allowed to be turned on until the internal soft-start voltage is higher than the FB pin voltage.

6.3.7 Voltage Reference

The voltage reference system produces a precise ±2% voltage-reference overtemperature by scaling the output of a temperature stable bandgap circuit. The typical voltage reference is designed at 0.596V.

6.3.8 Adjusting Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends to use divider resistors with 1% tolerance or better. Start with a 100kΩ for the upper resistor divider, and use Equation 3 to calculate the output voltage. To improve efficiency at light loads consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable.

$$V_{OUT} = V_{ref} \times \left(\frac{R_2}{R_3} + 1\right) \quad (3)$$

6.3.9 Internal Soft Start

The TPS561300 uses the internal soft-start function. The internal soft start time is set to 5ms typically.

6.3.10 Bootstrap Voltage (BOOT)

The TPS561300 has an integrated boot regulator and requires a 0.1µF ceramic capacitor between the BOOT and SW pins to provide the gate drive voltage for the high-side MOSFET. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage. To improve drop out, the device is designed to operate at 100% duty cycle as long as the BOOT to SW pin voltage is greater than 2.1V typically.

6.3.11 Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

6.3.11.1 High-Side MOSFET Overcurrent Protection

The device implements current mode control which uses the internal COMP voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle-by-cycle basis. During each cycle, the switch current and the current reference generated by the internal COMP voltage are compared. When the peak switch current intersects the current reference, the high-side switch turns off.

6.3.11.2 Low-Side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on, the conduction current is monitored by the internal circuitry. During normal operation, the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current-limit. The inductor valley current is exceeded the low-side source current limit, the high-side MOSFET does not turn on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET turns on again when the inductor valley current is below the low-side sourcing current-limit at the start of a cycle.

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Furthermore, if an output overload condition occurs for more than the hiccup wait time, which is programmed for 512 switching cycles, the device shuts down and restarts after the hiccup time of 16384 cycles. The hiccup mode helps to reduce the device power dissipation under severe overcurrent conditions.

6.3.12 Spread Spectrum

To reduce EMI, TPS561300 introduces frequency spread spectrum. The jittering span is ±6% of the switching frequency with 1/512 swing frequency.

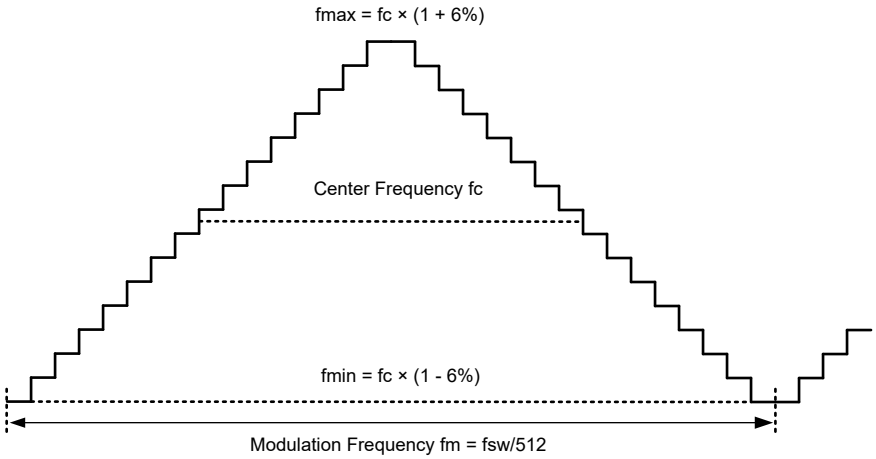

Figure 6-2. Frequency Spread Spectrum Diagram

6.3.13 Output Overvoltage Protection (OVP)

The TPS561300 incorporates an overvoltage transient protection (OVTP) circuit to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. The OVP circuit includes an overvoltage comparator to compare the FB pin voltage and internal thresholds. When the FB pin voltage goes above 108% × Vref, the high-side MOSFET is forced off. When the FB pin voltage falls below 104% × Vref, the high-side MOSFET is enabled again.

6.3.14 Thermal Shutdown

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C typically. When the junction temperature drops below 150°C typically, the internal thermal-hiccup timer begins to count. The device re-initiates the power-up sequence after the built-in thermal-shutdown hiccup time (32768 cycles) is over.

6.4 Device Functional Modes

6.4.1 Normal Operation

When the input voltage is above the UVLO threshold, the TPS561300 can operate in the normal switching modes. Normal continuous conduction mode (CCM) occurs when inductor peak current is above 0A. In CCM, the device operates at a fixed frequency.

6.4.2 Eco-mode Operation

The devices are designed to operate in high-efficiency pulse-skipping mode under light load conditions. Pulse skipping initiates when the switch current falls to 0A. During pulse skipping, the low-side FET turns off when the switch current falls to 0A. The switching node (the SW pin) waveform takes on the characteristics of discontinuous conduction mode (DCM) operation and the apparent switching frequency decreases. As the output current decreases, the perceived time between switching pulses increases.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS561300 device is typically used as a step-down converter, which converts an input voltage from 5V to 30V to fixed output voltage 5V.

7.2 Typical Application

7.2.1 TPS561300 5V to 30V Input, 5V Output Converter

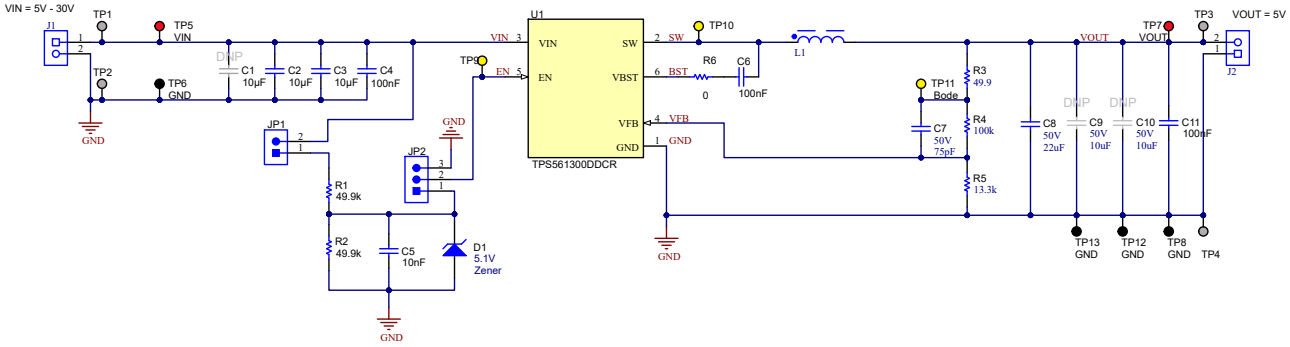

Figure 7-1. 5V, 1A Reference Design

7.2.2 Design Requirements

For this design example, use the parameters in the following table.

Table 7-1. Design Parameters

PARAMETER	VALUE
Input voltage range	5V to 30V
Output voltage	5V
Output current	1A
Transient response, 1A load step	ΔV_{OUT} = ±5 %
Output voltage ripple	10mVpp
Switching frequency	1200kHz

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7.2.3 Detailed Design Procedure

7.2.3.1 Input Capacitor Selection

The device requires an input decoupling capacitor, and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10µF for the decoupling capacitor. An additional 0.1µF capacitor (C4) from VIN to GND is optional to provide additional high frequency filtering. The capacitor voltage rating must be greater than the maximum input voltage.

Use the following equation to calculate the input ripple voltage (ΔV_{IN}).

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{SW}} + I_{OUT(MAX)} \times ESR_{MAX} \quad (4)$$

where:

- C_{BULK} is the bulk capacitor value
- f_{SW} is the switching frequency
- $I_{OUT(MAX)}$ is the maximum loading current
- ESR_{MAX} is maximum series resistance of the bulk capacitor

The maximum RMS (root mean square) ripple current must also be checked. For worst case conditions, use the following equation to calculate $I_{CIN(RMS)}$.

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{2} \quad (5)$$

The actual input-voltage ripple is greatly affected by parasitic associated with the layout and the output impedance of the voltage source. *Design Requirements* shows the actual input voltage ripple for this circuit, which is larger than the calculated value. The maximum voltage across the input capacitors is VIN (MAX) + ΔVIN/2. The selected bypass capacitor is rated for 50V and the ripple current capacity is greater than 2A. Both values provide ample margin. The maximum ratings for voltage and current must not be exceeded under any circumstance.

7.2.3.2 Bootstrap Capacitor Selection

Connect a 0.1µF ceramic capacitor between the BOOT to SW pin for proper operation. TI recommends to use a ceramic capacitor.

7.2.3.3 Output Voltage Setpoint

The output voltage of the TPS561300 device is externally adjustable using a resistor divider network. The divider network is comprised of R4 and R5. Use the following equations to calculate the relationship of the output voltage to the resistor divider.

$$R_5 = \frac{R_4 \times V_{ref}}{V_{OUT} - V_{ref}} \quad (6)$$

$$V_{OUT} = V_{ref} \times \left(\frac{R_4}{R_5} + 1\right) \quad (7)$$

Select a value of R4 to be approximately 100kΩ. Slightly increasing or decreasing R5 can result in closer output voltage matching when using standard value resistors. In this design, R4 = 100kΩ and R5 = 13.3kΩ, which results in a 5V output voltage. The 49.9Ω resistor, R3, is provided as a convenient location to break the control loop for stability testing.

7.2.3.4 Undervoltage Lockout Setpoint

The UVLO setpoint can be adjusted using the external-voltage divider network of R1 and R2. R1 is connected between the VIN and EN pins of the TPS561300 device. R2 is connected between the EN and GND pins. The UVLO has two thresholds, one for power up when he input voltage is rising and one for power down or brown

outs when the input voltage is falling. Use Equation 1 and Equation 2 to calculate the values for the upper and lower resistor values of R1 and R2.

7.2.3.5 Inductor Selection

Use the following equation to calculate the minimum value of the output inductor (L_{MIN}).

$$L_{MIN} = \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times f_{SW}} \quad (8)$$

Where:

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current.

In general, the value of K_{IND} is at the discretion of the designer; however, the following guidelines can be used. For designs using low-ESR output capacitors, such as ceramics, a value as high as K_{IND} = 0.3 can be used.

For this design example, use K_{IND} = 0.3. The minimum inductor value is calculated as 11.57µH. For this design, a close standard value of 12µH was selected for L_{MIN}.

For the output filter inductor, the RMS current and saturation current ratings must not be exceeded. Use the following equation to calculate the RMS inductor current ($I_{L(RMS)}$).

$$I_{L(MAX)} = \sqrt{I_{OUT(MAX)}^{2} + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_O \times f_{SW} \times 0.8}\right)^{2}} \quad (9)$$

Use the following equation to calculate the peak inductor current ($I_{L(PK)}$).

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_O \times f_{SW} \times 1.6} \quad (10)$$

Smaller or larger inductor values can be used depending on the amount of ripple current the designer wants to allow so long as the other design requirements are met. Larger value inductors have lower AC current and result in lower output voltage ripple. Smaller inductor values increase AC current and output voltage ripple.

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7.2.4 Application Curves

The following data is tested with V_{IN} = 24V, V_{OUT} = 5V, T_A = 25°C, unless otherwise specified.

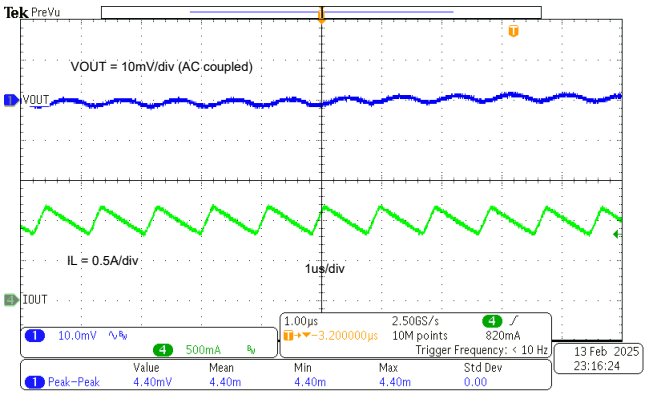

Figure 7-2. TPS561300EVM Output Voltage Ripple, I_{OUT} = 1A

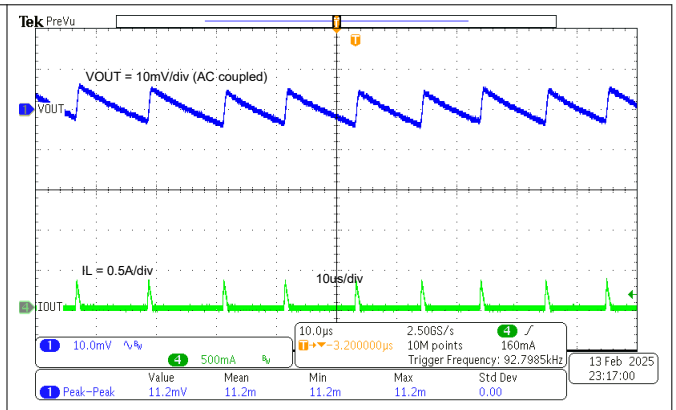

Figure 7-3. TPS561300EVM Output Voltage Ripple, I_{OUT} = 0.01A

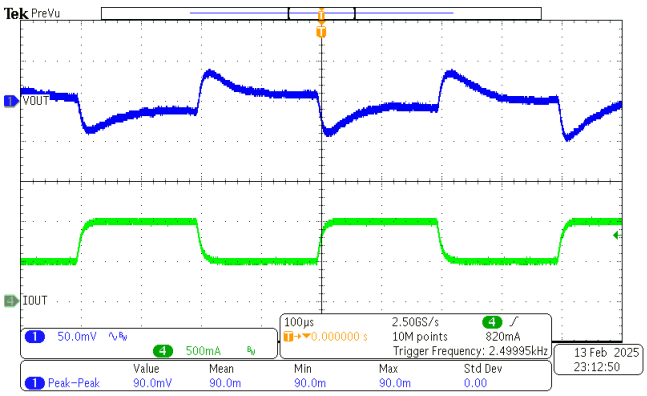

Figure 7-4. TPS561300EVM Load Transient Response, 0.5A to 1A Load Step

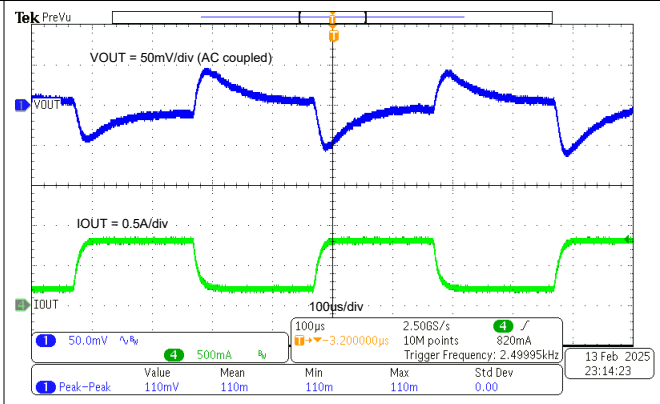

Figure 7-5. TPS561300EVM Load Transient Response, 0.2A to 0.8A Load Step

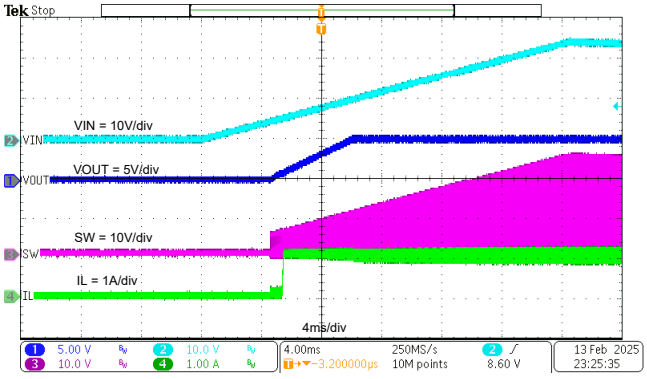

Figure 7-6. TPS561300EVM Start-Up Relative to V_{IN}

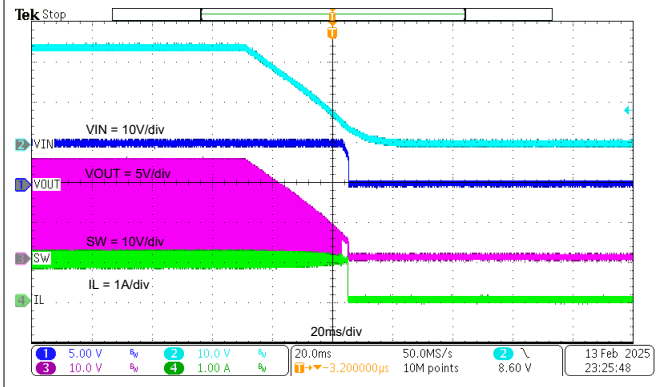

Figure 7-7. TPS561300EVM Shutdown Relative to V_{IN}

7.3 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4.5V and 30V. This input supply must be well regulated. If the input supply is located more than a few inches from the device or converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47µF is a typical choice.

7.4 Layout

7.4.1 Layout Guidelines

- Make VIN and GND traces as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
- Place the input capacitor and output capacitor as close to the device as possible to minimize trace impedance.
- Provide sufficient vias for the input capacitor and output capacitor.
- Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
- Do not allow switching current to flow under the device.
- Connect a separate VOUT path to the upper feedback resistor.
- Make a Kelvin connection to the GND pin for the feedback path.
- Place the voltage feedback loop away from the high-voltage switching trace, and preferably have ground shield.
- Make the trace of the VFB node as small as possible to avoid noise coupling.
- Make the GND trace between the output capacitor and the GND pin as wide as possible to minimize the trace impedance.

7.4.2 Layout Example

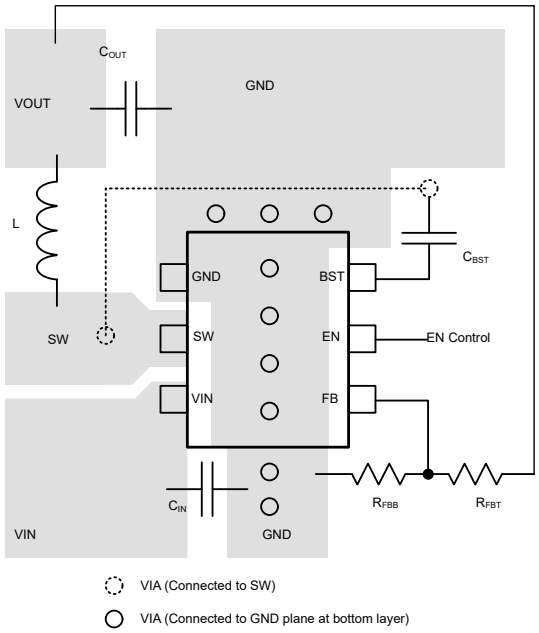

Figure 7-8. Board Layout

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8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

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8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feedforward Capacitor* application report

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

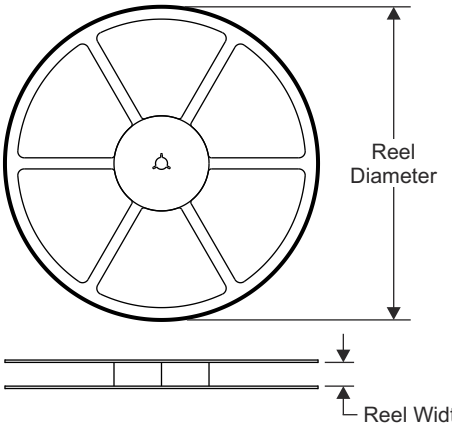
DATE	REVISION	NOTES
February 2025	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

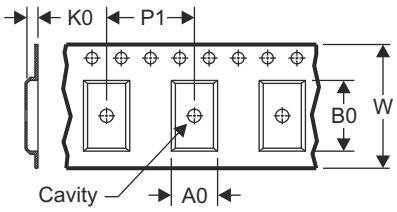
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Tape and Reel Information

REEL DIMENSIONS

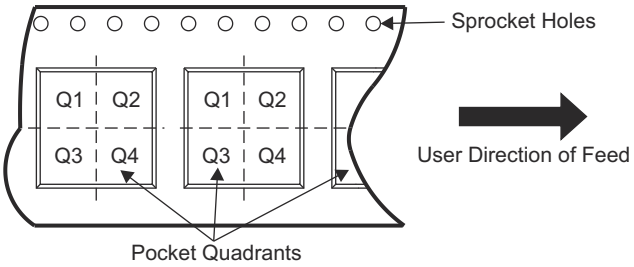


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTPS561300DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

ADVANCE INFORMATION

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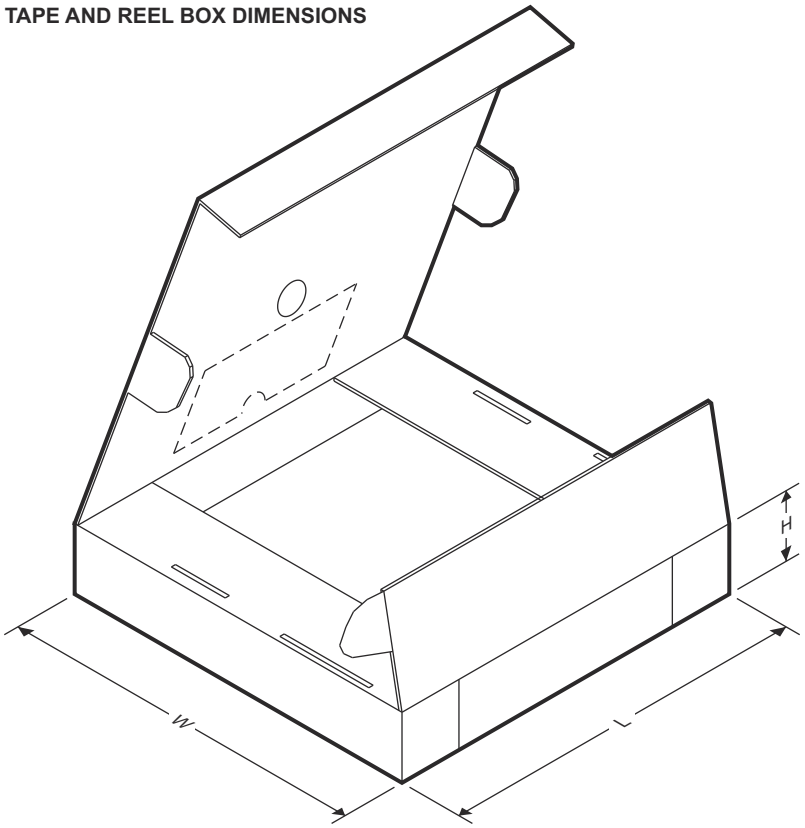
TAPE AND REEL BOX DIMENSIONS



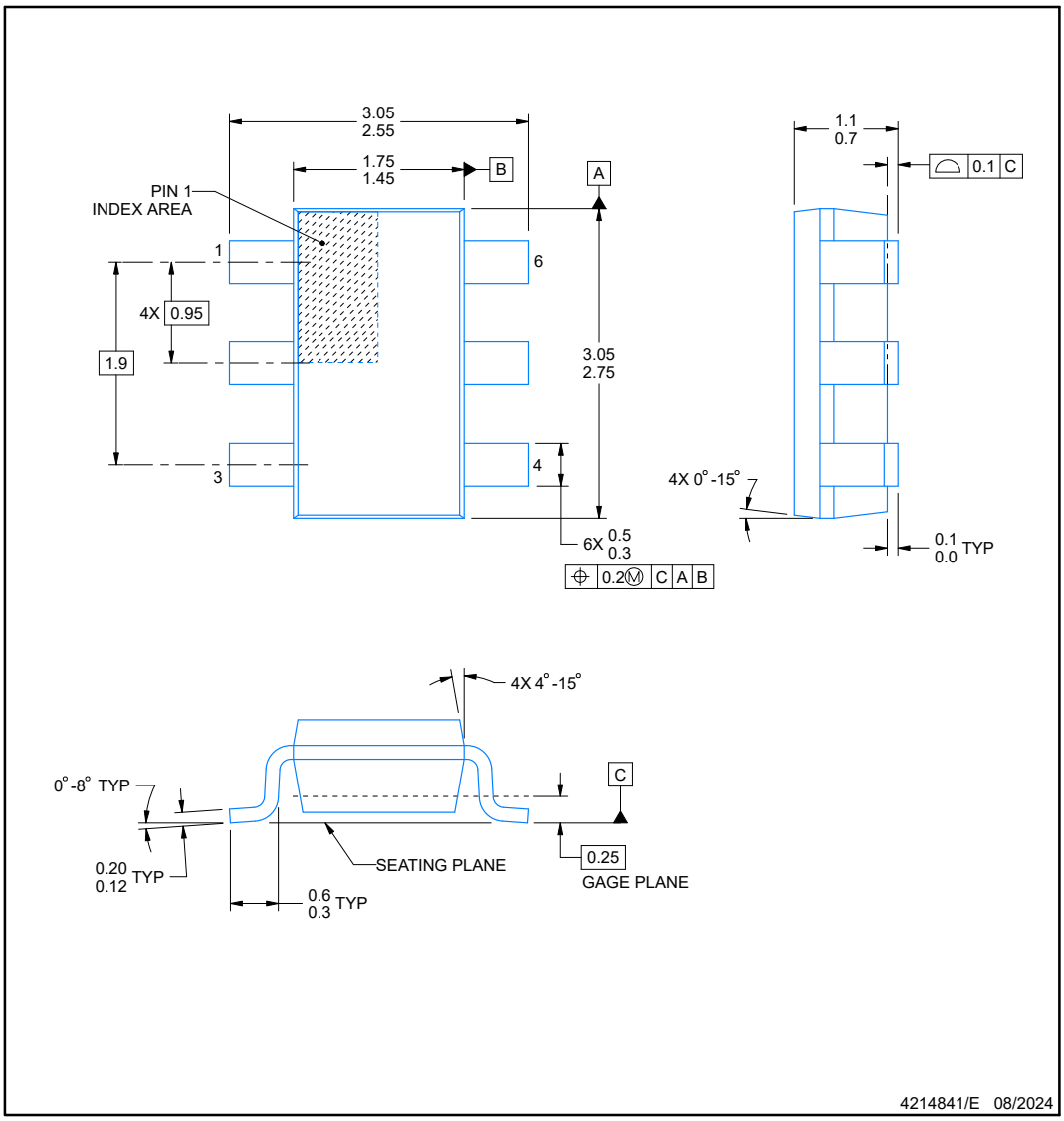
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTPS561300DDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.

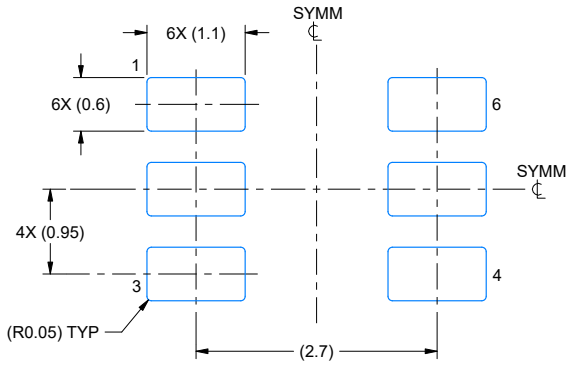
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

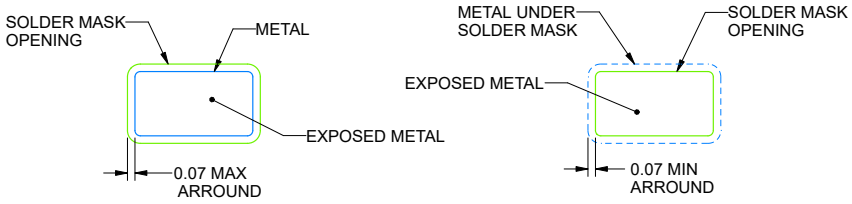
DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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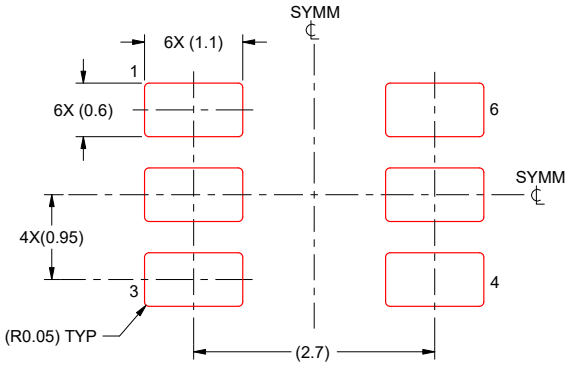
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDC0006A — **SOT-23 - 1.1 max height**

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS561300DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	TBD	Call TI	Call TI	-40 to 150		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

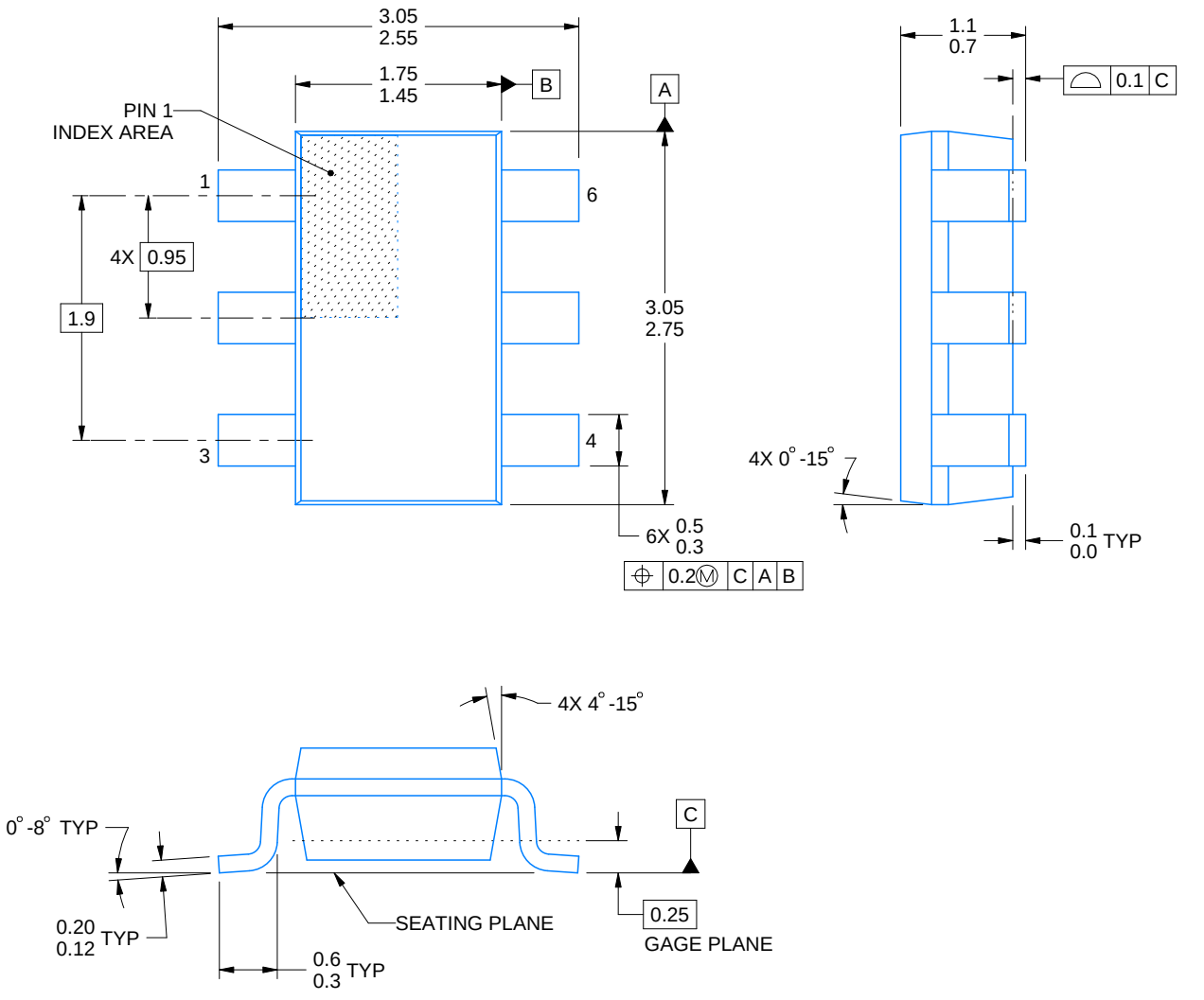
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



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NOTES:

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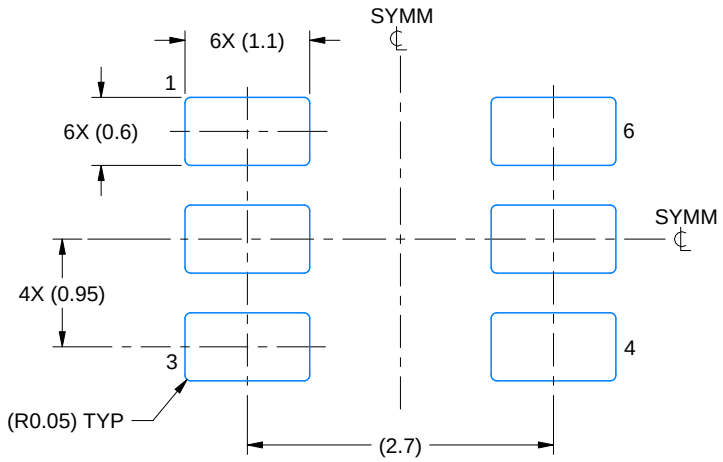
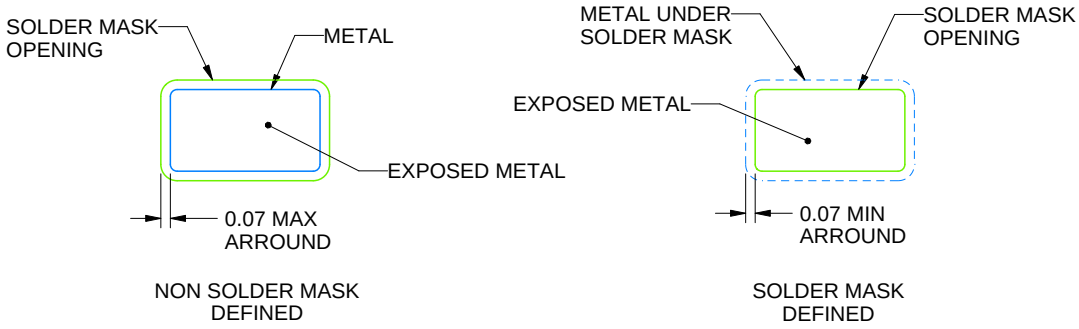
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

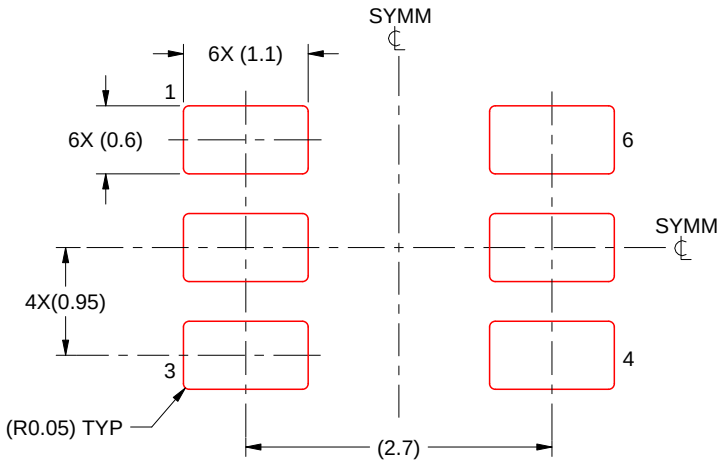


SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

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7. Board assembly site may have different recommendations for stencil design.

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