TPS56325x 3-V to 16-V Input, 3-A Synchronous Buck Converters in SOT-563 Package

1 Features

• Configured for a wide range of applications
  – 3-V to 16-V input voltage range
  – 0.6-V to 7-V output voltage range
  – 0.6-V reference voltage
  – ±1% reference accuracy at 25°C
  – ±1.5% reference accuracy at –40°C to 125°C
  – Integrated 55.2-mΩ and 24.3-mΩ MOSFETs
  – 100-µA low quiescent current
  – 1.4-MHz switching frequency
  – Maximum 93% large duty cycle operation
  – Precision EN threshold voltage
  – 1.6-ms fixed typical soft-start time
• Ease of use and small solution size
  – TPS563252 Eco-mode, TPS563257 FCCM mode at light loading
  – D-CAP3™ control topology
  – Easy layout with integrated bootstrap capacitor
  – Support start-up with prebiased output
  – Open-drain power-good indicator
  – Non-latch for OV, OT, and UVLO protection
  – Hiccup mode for UV protection
  – Cycle-by-cycle OC and NOC protection
  – 1.6-mm × 1.6-mm SOT-563 package
• Create a custom design using the TPS563252 with the WEBENCH® Power Designer
• Create a custom design using the TPS563257 with the WEBENCH® Power Designer

2 Applications

• WLAN/Wi-Fi access point, switch, router
• Pro-audio, surveillance, drone
• DTV, STB and DVR, smart speaker

3 Description

The TPS56325x is a simple, easy-to-use, high efficiency, high power density, synchronous buck converter with input voltage ranging from 3-V to 16-V and supports up to 3-A continuous current at output voltages between 0.6 V and 7 V.

The TPS56325x employs DCAP3 topology to provide a fast transient response and to support low-ESR output capacitors with no requirement for external compensation. The device can support up to 93% duty cycle operation. Integrated bootstrap capacitor helps achieve single layer PCB and can save total BOM cost.

The TPS563252 operates in Eco-mode, which maintains high efficiency during light loading. The TPS563257 operates in FCCM mode, which keeps the same frequency and lower output ripple during all load conditions. The device integrates complete protection through OVP, OCP, UVLO, OTP, and UVP with hiccup.

The device is available in 1.6-mm × 1.6-mm SOT-563 package. The junction temperature is specified from –40°C to 125°C.

Device Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Mode</th>
<th>Package(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS563252</td>
<td>ECO</td>
<td>DRL (SOT-563, 6)</td>
</tr>
<tr>
<td>TPS563257</td>
<td>FCCM</td>
<td></td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
Table of Contents

1 Features ................................................................. 1
2 Applications ............................................................ 1
3 Description .............................................................. 1
4 Revision History ...................................................... 2
5 Pin Configuration and Functions .................................. 3
6 Specifications .......................................................... 4
   6.1 Absolute Maximum Ratings ................................... 4
   6.2 ESD Ratings ........................................................ 4
   6.3 Recommended Operating Conditions ......................... 4
   6.4 Thermal Information .............................................. 4
   6.5 Electrical Characteristics ....................................... 5
   6.6 Typical Characteristics .......................................... 7
7 Detailed Description .................................................. 10
   7.1 Overview .......................................................... 10
   7.2 Functional Block Diagram ....................................... 11
   7.3 Feature Description .............................................. 11
7.4 Device Functional Modes ........................................ 13
8 Application and Implementation ................................. 14
   8.1 Application Information ........................................ 14
   8.2 Typical Application .............................................. 14
   8.3 Power Supply Recommendations ............................. 20
   8.4 Layout ............................................................. 20
9 Device and Documentation Support ............................... 22
   9.1 Receiving Notification of Documentation Updates .......... 22
   9.2 Support Resources ............................................... 22
   9.3 Trademarks ........................................................ 22
   9.4 Electrostatic Discharge Caution ............................... 22
   9.5 Glossary .......................................................... 22
10 Mechanical, Packaging, and Orderable Information .......... 22
   10.1 Tape and Reel Information .................................... 23

4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>August 2022</td>
<td></td>
<td>Advance Information</td>
</tr>
</tbody>
</table>
## 5 Pin Configuration and Functions

![Figure 5-1. 6-Pin SOT563 DRL Package (Top View)](image)

### Table 5-1. Pin Functions

<table>
<thead>
<tr>
<th>Pin</th>
<th>Type(1)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>P</td>
<td>Input voltage supply pin. Connect the input decoupling capacitors between VIN and GND.</td>
</tr>
<tr>
<td>SW</td>
<td>P</td>
<td>Switch node pin. Connect the output inductor to this pin.</td>
</tr>
<tr>
<td>GND</td>
<td>G</td>
<td>GND pin for the controller circuit and the internal circuitry</td>
</tr>
<tr>
<td>PG</td>
<td>A</td>
<td>Open-drain power-good indicator</td>
</tr>
<tr>
<td>EN</td>
<td>A</td>
<td>Enable input control. Driving EN high enables the converter</td>
</tr>
<tr>
<td>FB</td>
<td>A</td>
<td>Converter feedback input. Connect to output voltage with a feedback resistor divider.</td>
</tr>
</tbody>
</table>

(1) A = Analog, P = Power, G = Ground
6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Pin voltage(^{(2)})</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>–0.3</td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>FB, EN, PG</td>
<td>–0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>GND</td>
<td>–0.3</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>SW, DC</td>
<td>–2</td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>SW (transient &lt; 20 ns)</td>
<td>–5.5</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>Operating junction temperature, (T_J)</td>
<td>–40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature, (T_{stg})</td>
<td>–55</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

\(^{(2)}\) All voltage values are with respect to the network ground pin.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>(V_{\text{ESD}})</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrostatic discharge</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)}), all pins</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(^{(2)})</td>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

\(^{(1)}\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

\(^{(2)}\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Pin voltage</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>3</td>
<td>16</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>FB, EN, PG</td>
<td>–0.1</td>
<td>5.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>GND</td>
<td>–0.1</td>
<td>0.1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>SW, DC</td>
<td>–1</td>
<td>16</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>SW (transient &lt; 20 ns)</td>
<td>–5</td>
<td>18</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output current, (I_{\text{OUT}})</td>
<td>0</td>
<td>3</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Operating junction temperature, (T_J)</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage temperature, (T_{stg})</td>
<td>–40</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>DRL (SOT-563)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction-to-ambient thermal resistance</td>
<td>137.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-ambient thermal resistance on EVM board</td>
<td>74</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-case (top) thermal resistance</td>
<td>58.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-board thermal resistance</td>
<td>29.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-top characterization parameter</td>
<td>1.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-board characterization parameter</td>
<td>29.4</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
6.5 Electrical Characteristics

$T_J = -40°C$ to $125°C$, $V_{IN} = 12$ V (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT SUPPLY VOLTAGE</td>
<td>$V_{IN}$ Input voltage range</td>
<td>3</td>
<td>16</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{VIN}$ VIN supply current</td>
<td>No load, $V_{EN} = 5\text{ V}$, $V_{FB} = 0.65\text{ V}$, non-switching, ECO version</td>
<td>100</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>No load, $V_{EN} = 5\text{ V}$, $V_{FB} = 0.65\text{ V}$, non-switching, FCCM version</td>
<td>360</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{NSDN}$ VIN shutdown current</td>
<td>No load, $V_{EN} = 0\text{ V}$</td>
<td>2</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>UVLO</td>
<td>$V_{IN,UVLO}$ Input undervoltage lockout threshold</td>
<td>2.92</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Rising threshold</td>
<td>2.72</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Falling threshold</td>
<td>200</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FEEDBACK VOLTAGE</td>
<td>$V_{REF}$ FB voltage</td>
<td>$T_J = 25°C$</td>
<td>594</td>
<td>600</td>
<td>606</td>
</tr>
<tr>
<td></td>
<td>$T_J = -40°C$ to $125°C$</td>
<td>591</td>
<td>600</td>
<td>609</td>
<td>mV</td>
</tr>
<tr>
<td>INTEGRATED POWER MOSFETS</td>
<td>$R_{DSON,HS}$ (1) High-side MOSFET on-resistance</td>
<td>$T_J = 25°C, V_{IN} \geq 5\text{ V}$</td>
<td>55.2</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_J = 25°C, V_{IN} = 3\text{ V}$</td>
<td>67.5</td>
<td>mΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_{DSON,LS}$ Low-side MOSFET on-resistance</td>
<td>$T_J = 25°C, V_{IN} \geq 5\text{ V}$</td>
<td>24.3</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_J = 25°C, V_{IN} = 3\text{ V}$</td>
<td>30.2</td>
<td>mΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SWITCHING FREQUENCY</td>
<td>$f_{sw}$ Switching frequency</td>
<td>$T_J = 25°C, V_{OUT} = 3.3\text{ V}$</td>
<td>1400</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{ON(MIN)}$ (1) Minimum on time</td>
<td>$T_J = 25°C$</td>
<td>60</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{OFF(MIN)}$ (1) Minimum off time</td>
<td>$V_{FB} = 0.5\text{ V}$</td>
<td>110</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>LOGIC THRESHOLD</td>
<td>$V_{ENH}$ EN threshold high level</td>
<td>Rising enable threshold</td>
<td>1.15</td>
<td>1.19</td>
<td>1.25</td>
</tr>
<tr>
<td></td>
<td>$V_{ENL}$ EN threshold low level</td>
<td>Falling disable threshold</td>
<td>0.9</td>
<td>1</td>
<td>1.1</td>
</tr>
<tr>
<td></td>
<td>$V_{ENHYS}$ EN hysteresis</td>
<td>Hysteresis</td>
<td>190</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_{EN}$ EN pulldown resistor</td>
<td>2</td>
<td>MΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CURRENT LIMIT</td>
<td>$I_{OCL,LS}$ Overcurrent threshold</td>
<td>Valley current set point</td>
<td>3.1</td>
<td>4.1</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>$I_{NOC}$ Negtive overcurrent threshold</td>
<td>1.5</td>
<td>2.1</td>
<td>2.5</td>
<td>A</td>
</tr>
<tr>
<td>SOFT START</td>
<td>$I_S$ Internal soft start time</td>
<td>1.6</td>
<td>ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OUTPUT OVERVOLTAGE AND UNDERRVOLTAGE PROTECTION</td>
<td>$V_{OVP}$ OVP trip threshold</td>
<td>$V_{FB}$ rising</td>
<td>110%</td>
<td>115%</td>
<td>120%</td>
</tr>
<tr>
<td></td>
<td>$I_{VPDLY}$ OVP prop deglitch</td>
<td>24</td>
<td>µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{UVP}$ UVP trip threshold</td>
<td>$V_{FB}$ falling</td>
<td>55%</td>
<td>60%</td>
<td>65%</td>
</tr>
<tr>
<td></td>
<td>$I_{UPDLY}$ UVP prop deglitch</td>
<td>256</td>
<td>µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{VPDFEL}$ Hiccup delay relative to SS time</td>
<td>UVP detect</td>
<td>256</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{VPDEN}$ Hiccup enable delay relative to SS time</td>
<td>UVP detect</td>
<td>14</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>POWER GOOD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
$T_J = -40^\circ\text{C} \text{ to } 125^\circ\text{C}$, $V_{IN} = 12\text{ V}$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{PGTH}$</td>
<td>Power good threshold</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>FB falling, PG from high to low</td>
<td>80%</td>
<td>85%</td>
<td>90%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>FB rising, PG from low to high</td>
<td>85%</td>
<td>90%</td>
<td>95%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>FB falling, PG from low to high</td>
<td>105%</td>
<td>110%</td>
<td>115%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>FB rising, PG from high to low</td>
<td>110%</td>
<td>115%</td>
<td>120%</td>
<td></td>
</tr>
<tr>
<td>$V_{PG(OL)}$</td>
<td>PG pin output low-level voltage</td>
<td></td>
<td></td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$I_{OL} = 4\text{ mA}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{PG(LKG)}$</td>
<td>PG pin leakage current when</td>
<td></td>
<td></td>
<td>1</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>open drain output is high</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{PG} = 5.5\text{ V}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{PG(R)}$</td>
<td>PG delay going from low to high</td>
<td>1</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>$I_{PG(F)}$</td>
<td>PG delay going from high to low</td>
<td>32</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
</tbody>
</table>

**THERMAL SHUTDOWN**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{SDN}$</td>
<td>Thermal shutdown threshold</td>
<td></td>
<td>155</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{OTPHSY}$</td>
<td>Hysteresis</td>
<td></td>
<td>20</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Specified by design
6.6 Typical Characteristics

\( T_J = -40°C \) to \( 125°C \), \( V_{IN} = 12 \) V (unless otherwise noted)

Figure 6-1. TPS563252 Quiescent Current

Figure 6-2. TPS563257 Quiescent Current

Figure 6-3. Enable On Threshold Voltage

Figure 6-4. Enable Off Threshold Voltage

Figure 6-5. Low-Side \( R_{DS(ON)} \)

Figure 6-6. High-Side \( R_{DS(ON)} \)

Copyright © 2022 Texas Instruments Incorporated

Submit Document Feedback
Junction Temperature (°C)

\[ V_{\text{ref}} (V) \]

\[ -40 \quad -20 \quad 0 \quad 20 \quad 40 \quad 60 \quad 80 \quad 100 \quad 120 \quad 140 \]

\[ 0.5985 \quad 0.599 \quad 0.5995 \quad 0.6 \quad 0.6005 \quad 0.601 \quad 0.6015 \]

Figure 6-7. VREF Voltage

\[ \text{Vin} (V) \quad \text{Frequency (kHz)} \]

\[ 2 \quad 4 \quad 6 \quad 8 \quad 10 \quad 12 \quad 14 \quad 16 \]

\[ 400 \quad 600 \quad 800 \quad 1000 \quad 1200 \quad 1400 \quad 1600 \]

\[ \text{Vout} = 1.05V \quad \text{Vout} = 3.3V \quad \text{Vout} = 5V \quad \text{Vout} = 7V \]

Figure 6-8. Frequency vs Input Voltage, \( I_{\text{OUT}} = 3 \text{ A} \)

\[ \text{Iout (A)} \quad \text{Frequency (kHz)} \]

\[ 0.001 \quad 0.005 \quad 0.02 \quad 0.05 \quad 0.1 \quad 0.2 \quad 0.5 \quad 1 \quad 2 \quad 3 \]

\[ 0 \quad 1000 \quad 2000 \quad 3000 \quad 4000 \quad 5000 \quad 6000 \quad 7000 \quad 8000 \quad 9000 \quad 10000 \]

\[ \text{Vout} = 1.05V \quad \text{Vout} = 3.3V \quad \text{Vout} = 5V \quad \text{Vout} = 7V \]

Figure 6-9. TPS563252 Frequency vs Loading, \( \text{V}_{\text{IN}} = 12 \text{ V} \)

\[ \text{Iout (A)} \quad \text{Efficiency} \]

\[ 0.001 \quad 0.005 \quad 0.02 \quad 0.05 \quad 0.1 \quad 0.2 \quad 0.5 \quad 1 \quad 2 \quad 3 \]

\[ 0 \quad 10% \quad 20% \quad 30% \quad 40% \quad 50% \quad 60% \quad 70% \quad 80% \quad 90% \quad 100% \]

\[ \text{Vin} = 3V \quad \text{Vin} = 6V \quad \text{Vin} = 12V \quad \text{Vin} = 16V \]

Figure 6-11. TPS563252 Efficiency at 0.6 V\text{OUT} with a 0.68-μH Inductor

\[ \text{Iout (A)} \quad \text{Efficiency} \]

\[ 0.001 \quad 0.005 \quad 0.02 \quad 0.05 \quad 0.1 \quad 0.2 \quad 0.5 \quad 1 \quad 2 \quad 3 \]

\[ 0 \quad 10% \quad 20% \quad 30% \quad 40% \quad 50% \quad 60% \quad 70% \quad 80% \quad 90% \quad 100% \]

\[ \text{Vin} = 3V \quad \text{Vin} = 6V \quad \text{Vin} = 12V \quad \text{Vin} = 16V \]

Figure 6-12. TPS563257 Efficiency at 0.6 V\text{OUT} with a 0.68-μH Inductor
Figure 6-13. TPS563252 Efficiency at 1.05 V<sub>OUT</sub> with a 0.82-μH Inductor

Figure 6-14. TPS563257 Efficiency at 1.05 V<sub>OUT</sub> with a 0.82-μH Inductor

Figure 6-15. TPS563252 Efficiency at 3.3 V<sub>OUT</sub> with a 2.2-μH Inductor

Figure 6-16. TPS563257 Efficiency at 3.3 V<sub>OUT</sub> with a 2.2-μH Inductor

Figure 6-17. TPS563252 Efficiency at 5 V<sub>OUT</sub> with a 2.2-μH Inductor

Figure 6-18. TPS563257 Efficiency at 5 V<sub>OUT</sub> with a 2.2-μH Inductor
7 Detailed Description

7.1 Overview

The TPS56325x is a 3-A integrated FET synchronous buck converter that operates from 3-V to 16-V input voltage and 0.6-V to 7-V output voltage. This device also integrates the BST pin in an internal IC, which is helpful for easy layout. The device employs a D-CAP3 topology that provides fast transient response with no external compensation components and an accurate feedback voltage. The proprietary D-CAP3 mode enables low external component count, ease of design, and optimization of the power design for cost, size, and efficiency. The topology provides a seamless transition between CCM operating mode at higher load condition and DCM operation mode at lighter load condition.

The Eco-mode version allows the TPS563252 to maintain high efficiency at light load. The FCCM version allows the TPS563257 to maintain a fixed switching frequency and lower voltage output ripple. The TPS56325x is able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.
7.3 Feature Description

7.3.1 PWM Operation and D-CAP3 Control

The main control loop of the buck is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary DCAP3 mode control. The DCAP3 mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. The device is stable even with virtually no ripple at the output. The TPS56325x also includes an error amplifier that makes the output voltage very accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after an internal one-shot timer expires. This one-shot duration is set proportional to the output voltage, $V_{OUT}$, and is inversely proportional to the converter input voltage, $V_{IN}$, to maintain a pseudo-fixed frequency over the input voltage.
range, hence, it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ripple generation circuit is added to reference voltage to emulate the output ripple, enabling the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for DCAP3 control topology.

7.3.2 Eco-Mode Control

The TPS563252 is designed with advanced Eco-mode to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction mode. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on time is kept almost the same as it was in continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The transition point to the light load operation \( I_{OUT(LL)} \) current can be calculated in Equation 1.

\[
I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \left( \frac{V_{IN} - V_{OUT}}{V_{IN}} \right) \times V_{OUT}
\]

7.3.3 Soft Start and Prebiased Soft Start

The TPS56325x has an internal fixed 1.6-ms soft-start time. The EN default status is low. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator. If the output capacitor is prebiased at start-up, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage, \( V_{FB} \). This scheme makes sure that the converter ramps up smoothly into the regulation point.

7.3.4 Overvoltage Protection

The TPS56325x has the overvoltage protection feature. When the output voltage becomes higher than the OVP threshold, the OVP is triggered in which, the deglitch time is 24 μs. Both the high-side MOSFET and the low-side MOSFET drivers are turned off. When the overvoltage condition is removed, the device returns to switching.

7.3.5 Large Duty Operation

The TPS56325x can support large duty operations up to 93% by smoothly dropping down the switching frequency. When \( V_{IN} / V_{OUT} < 1.6 \) and \( V_{FB} \) is lower than internal \( V_{REF} \), the switching frequency is allowed to smoothly drop to make \( t_{ON} \) extended to implement the large duty operation and improve the performance of the load transient performance. Please refer frequency test waveform in Figure 6-8. The minimum switching frequency is limited to approximately 600 kHz.

7.3.6 Current Protection and Undervoltage Protection

The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the off state by measuring the low-side FET drain-to-source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated. During the on time of the high-side FET switch, the switch current increases at a linear rate determined by the following:

- \( V_{IN} \)
- \( V_{OUT} \)
- On time
- Output inductor value

During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current, \( I_{OUT} \). If the monitored valley current is above the OCL level, the converter maintains a low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until

\[
I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \left( \frac{V_{IN} - V_{OUT}}{V_{IN}} \right) \times V_{OUT}
\]
the current level becomes OCL level or lower. In subsequent switching cycles, the on time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. The load current is higher than the overcurrent threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current can be higher than the current available from the converter, which can cause the output voltage to fall. When the FB voltage falls below the UVP threshold voltage, the UVP comparator detects it and the device shuts down after the UVP delay time (typically 256 µs) and restarts after the hiccup wait time (typically 14 ms).

When the overcurrent condition is removed, the output voltage returns to the regulated value.

The TPS563257 is a FCCM mode part. In this mode, the device has negative inductor current at light loading. The device has NOC (negative overcurrent) protection to avoid too large negative current. NOC protection detects the valley of inductor current. When the valley value of inductor current exceeds the NOC threshold, the IC turns off the low side then turns on the high side. When the NOC condition is removed, the device returns to normal switching.

Because the TPS563257 is a FCCM mode port, if the inductance is so small that the device trigger NOC, it causes the output voltage to be higher than target value. The minimum inductance is identified as Equation 2.

\[
L = \frac{V_{out} \times (1 - \frac{V_{out}}{V_{in}})}{2 \times \text{Frequency} \times NOC_{min}}
\]

(2)

7.3.7 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This is a non-latch protection.

7.3.8 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value, the device is shut off. This is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Eco-mode Operation

The TPS563252 operates in Eco-mode, which maintains high efficiency at light loading. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction mode. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on time is kept almost the same as it was in continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high.

7.4.2 FCCM Mode Operation

The TPS563257 operates in forced CCM (FCCM) mode, which keeps the converter operating in continuous current mode during light load conditions and allows the inductor current to become negative. During FCCM mode, the switching frequency is maintained at an almost constant level over the entire load range, which is suitable for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load.
8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The device is a typical buck DC-DC converter that is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 3 A. The following design procedure can be used to select component values for TPS56325x. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

The application schematic in Figure 8-1 was developed to meet the requirements in Table 8-1. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

Figure 8-1 shows the TPS56325x 12-V input, 1.05-V output converter schematic.

Figure 8-1. Schematic

8.2.1 Design Requirements

Table 8-1 shows the design parameters for this application.

Table 8-1. Design Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>Output voltage</td>
<td></td>
<td>1.05</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>I&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>Output current</td>
<td></td>
<td>3</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>ΔV&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>Transient response, 0.3 A - 2.7 A load step, 0.8-A/μs slew rate</td>
<td>±3% × V&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>Input voltage</td>
<td>3</td>
<td>12</td>
<td>16</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;OUT(ripple)&lt;/sub&gt;</td>
<td>Output voltage ripple, CCM condition</td>
<td></td>
<td>20</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>F&lt;sub&gt;SW&lt;/sub&gt;</td>
<td>Switching frequency</td>
<td>1.4 MHz</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>T&lt;sub&gt;A&lt;/sub&gt;</td>
<td>Ambient temperature</td>
<td></td>
<td>25</td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>
8.2.2 Detailed Design Procedure
8.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends using 1% tolerance or better divider resistors. Start by using Equation 3 to calculate $V_{\text{OUT}}$.

To improve efficiency at very light loads, consider using larger value resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable. Use a 10-kΩ or 30-kΩ resistor for $R_5$ to start the design.

$$V_{\text{OUT}} = 0.6 \times \left( 1 + \frac{R_4}{R_5} \right)$$

(3)

8.2.2.2 Output Filter Selection

The LC filter used as the output filter has a double pole at Equation 4. In this equation, $C_{\text{OUT}}$ uses its effective value after derating, not its nominal value.

$$f_p = \frac{1}{2\pi \sqrt{L_{\text{OUT}} \times C_{\text{OUT}}}}$$

(4)

For any control topology that is compensated internally, there is a range of the output filter it can support. At low frequency, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops has a 180 degree drop. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40 dB to –20 dB per decade and leads the 90 degree phase boost. The internal ripple injection high-frequency zero is about 156 kHz. The inductor and capacitor selected for the output filter is recommended such that the double pole is located approximately 40 kHz, so that the phase boost provided by this high-frequency zero provides adequate phase margin for the stability requirement. The crossover frequency of the overall system should usually be targeted to be less than one-third of the switching frequency ($f_{\text{SW}}$).

<table>
<thead>
<tr>
<th>Table 8-2. Recommended Component Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage (V)</td>
</tr>
<tr>
<td>---------------------</td>
</tr>
<tr>
<td>0.6</td>
</tr>
<tr>
<td>1.05</td>
</tr>
<tr>
<td>3.3</td>
</tr>
<tr>
<td>5</td>
</tr>
<tr>
<td>7</td>
</tr>
</tbody>
</table>

The inductor peak-to-peak ripple current, peak current, and RMS current are calculated using Equation 5, Equation 6, and Equation 7. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$I_{\text{P-P}} = \frac{V_{\text{OUT}}}{V_{\text{IN(MAX)}}} \times \frac{V_{\text{IN(MAX)}} - V_{\text{OUT}}}{L_{\text{O}} \times f_{\text{SW}}}$$

(5)

$$I_{\text{PEAK}} = I_{\text{O}} + \frac{I_{\text{P-P}}}{2}$$

(6)

$$I_{\text{LO(RMS)}} = \sqrt{I_{\text{O}}^2 + \frac{1}{12}I_{\text{P-P}}^2}$$

(7)
For this design example, the calculated peak current is 3.4 A and the calculated RMS current is 3.01 A. The inductor used is 744383660082 with 8.8-A rated current and 11-A saturation current.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS56325x are intended for use with ceramic or other low-ESR capacitors. Use Equation 8 to determine the required RMS current rating for the output capacitor.

\[
I_{\text{CO(RMS)}} = \frac{V_{\text{OUT}} \times (V_{\text{IN}} - V_{\text{OUT}})}{\sqrt{12} \times V_{\text{IN}} \times L \times f_{\text{SW}}}
\]

(8)

For this design, one MuRata GRM21BR61A226ME44L 22-µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.25 A and each output capacitor is rated for 4 A.

### 8.2.2.3 Input Capacitor Selection

The TPS56325x requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. An additional 0.1-µF capacitor from the VIN pin to ground is recommended to provide high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.
8.2.3 Application Curves

The following data is tested with $V_{IN} = 12\, \text{V}$, $V_{OUT} = 1.05\, \text{V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

![Figure 8-2. TPS563252 Frequency vs Loading](image1)

![Figure 8-3. TPS563257 Frequency vs Loading](image2)

![Figure 8-4. TPS563252 Load Regulation vs Loading](image3)

![Figure 8-5. TPS563257 Load Regulation vs Loading](image4)

![Figure 8-6. TPS563252 Line Regulation vs $V_{IN}$](image5)

![Figure 8-7. TPS563257 Line Regulation vs $V_{IN}$](image6)

---

Copyright © 2022 Texas Instruments Incorporated

Submit Document Feedback

Product Folder Links: [TPS563252](#) [TPS563257](#)
Figure 8-8. TPS563252 Output Voltage Ripple with 0.01-A Loading

Figure 8-9. TPS563257 Output Voltage Ripple with 0.01-A Loading

Figure 8-10. Output Voltage Ripple with 3-A Loading

Figure 8-11. TPS563252 Transient Response with 0.3 A to 2.7 A

Figure 8-12. TPS563252 Transient Response with 0.1 A to 3 A

Figure 8-13. TPS563257 Transient Response with 0.3 A to 2.7 A
Figure 8-14. TPS563257 Transient Response with 0.1 A to 3 A

Figure 8-15. Start-Up Through EN, IOUT = 3 A

Figure 8-16. Shutdown Through EN, IOUT = 3 A

Figure 8-17. Start-Up with VIN Rising, IOUT = 3 A

Figure 8-18. Shutdown with VIN Falling, IOUT = 3 A

Figure 8-19. TPS563252 Normal Operation to Output Hard Short
8.3 Power Supply Recommendations

The TPS56325x are designed to operate from input supply voltages in the range of 3 V to 16 V. Buck converters require the input voltage to be higher than the output voltage for proper operation.

8.4 Layout

8.4.1 Layout Guidelines

- VIN and GND traces must be as wide as possible to reduce trace impedance. The wide areas are also an advantage from the view point of heat dissipation.
- Place the input capacitor and output capacitor as close to the device as possible to minimize trace impedance.
- Provide sufficient vias for the input capacitor and output capacitor.
- Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
- Do not allow switching current to flow under the device.
- Connect a separate VOUT path to the upper feedback resistor.
- Make a Kelvin connection to the GND pin for the feedback path.
- Place a voltage feedback loop away from the high-voltage switching trace, and preferably has ground shield.
- The trace of the FB node must be as small as possible to avoid noise coupling.
- The GND trace between the output capacitor and the GND pin must be as wide as possible to minimize its trace impedance.
8.4.2 Layout Example

Figure 8-22. Suggested Layout
9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on Subscribe to updates to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer’s go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided “AS IS” by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI’s views; see TI’s Terms of Use.

9.3 Trademarks

D-CAP3™ and TI E2E™ are trademarks of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
10.1 Tape and Reel Information

**REEL DIMENSIONS**

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

**TAPE DIMENSIONS**

- A0
- B0
- K0
- W

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS563252DRLR</td>
<td>SOT-5X3</td>
<td>DRL</td>
<td>6</td>
<td>4000</td>
<td>180.0</td>
<td>8.4</td>
<td>2.0</td>
<td>1.8</td>
<td>0.75</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>TPS563257DRLR</td>
<td>SOT-5X3</td>
<td>DRL</td>
<td>6</td>
<td>4000</td>
<td>180.0</td>
<td>8.4</td>
<td>2.0</td>
<td>1.8</td>
<td>0.75</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
</tbody>
</table>
## TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS563252DRLR</td>
<td>SOT-5X3</td>
<td>DRL</td>
<td>6</td>
<td>4000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPS563257DRLR</td>
<td>SOT-5X3</td>
<td>DRL</td>
<td>6</td>
<td>4000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/ Ball material (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>XTPS563252DRLR</td>
<td>ACTIVE</td>
<td>SOT-5X3</td>
<td>DRL</td>
<td>6</td>
<td>4000</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 125</td>
<td></td>
<td>Samples</td>
</tr>
<tr>
<td>XTPS563257DRLR</td>
<td>ACTIVE</td>
<td>SOT-5X3</td>
<td>DRL</td>
<td>6</td>
<td>4000</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 125</td>
<td></td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated