TPS56C215 3.8V to 17V Input, 12A, Synchronous, Step-Down SWIFT™ Converter

1 Features

- Integrated 7.8mΩ and 3.2mΩ MOSFETs
- Supports 12A continuous I_{OUT}
- 4.5V start-up without external 5.0V bias
- 0.6V ±-1% reference voltage across full temperature range
- 0.6V to 5.5V output voltage range
- Supports ceramic output capacitors
- D-CAP3™ control mode for fast transient response
- Selectable forced continuous conduction mode (FCCM) for tight output voltage ripple or auto-skipping Eco-mode for high light-load efficiency
- Selectable F_{SW} of 400kHz, 800kHz, and 1.2MHz
- Monotonic start-up into prebiased outputs
- Two adjustable current limit settings with hiccup re-start
- Optional external 5V bias for enhanced efficiency
- Adjustable soft start with a default 1ms soft-start time
- –40°C to 150°C operating junction temperature
- Small 3.5mm × 3.5mm HotRod™ QFN package
- Pin-to-pin compatible with 8A TPS568215
- Create a custom design using TPS56C215 with the WEBENCH® Power Designer

2 Applications

- Server, cloud-computing, storage
- Telecom and networking, point-of-load (POL)
- IPCs, factory automation, PLC, test measurement
- High-end DTV

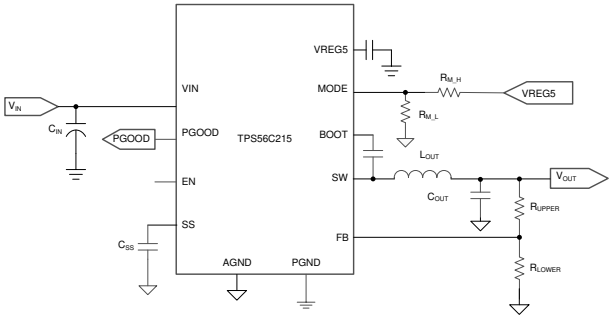
3 Description

The TPS56C215 is a small monolithic 12A synchronous buck converter with an adaptive on-time D-CAP3 control mode. The device integrates low R_{DS}(on) power MOSFETs that enable high efficiency and offers ease-of-use with minimum external component count for space-conscious power systems. Competitive features include a very accurate reference voltage, fast load transient response, auto-skip mode operation for light load efficiency, adjustable current limit and no requirement for external compensation. A forced continuous conduction mode helps meet tight voltage regulation accuracy requirements for performance DSPs and FPGAs. The TPS56C215 is available in a thermally enhanced, 18-pin, HotRod QFN package and is designed to operate from –40°C to 150°C junction temperature.

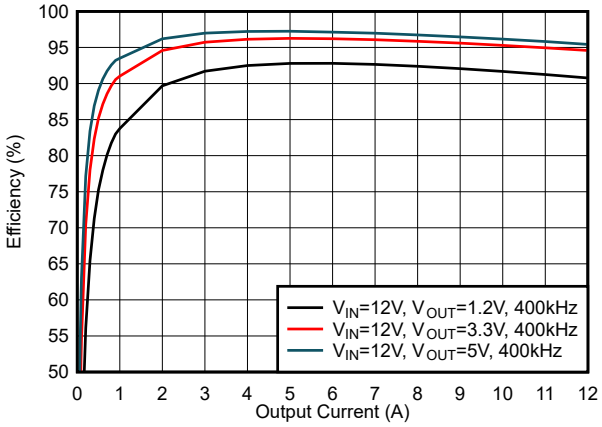
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS56C215	RNN (VQFN-HR, 18)	3.5mm × 3.5mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application



Efficiency vs Output Current

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

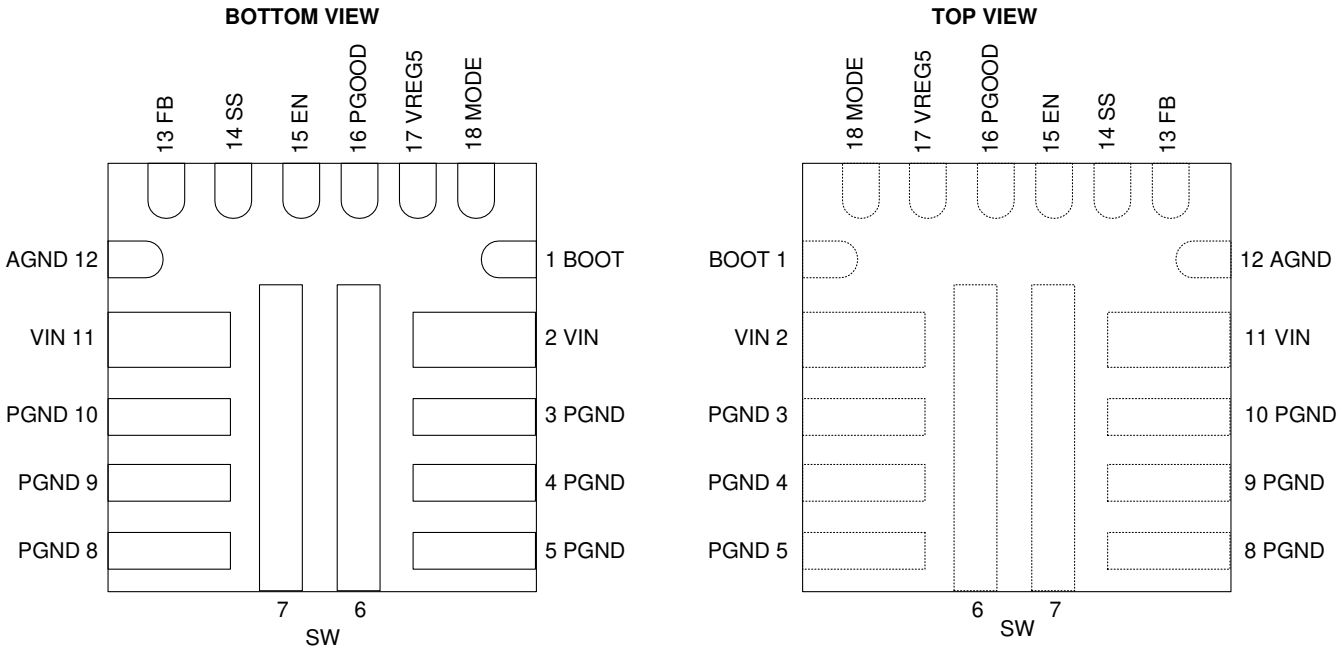

Figure 4-1. RNN Package, 18-Pin VQFN

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
BOOT	1	I	Supply input for the gate drive voltage of the high-side MOSFET. Connect the bootstrap capacitor between BOOT and SW.
VIN	2,11	P	Input voltage supply pin for the control circuitry. Connect the input decoupling capacitors between VIN and PGND.
PGND	3, 4, 5, 8, 9, 10	G	Power GND terminal for the controller circuit and the internal circuitry. Connect to AGND with a short trace.
SW	6, 7	O	Switch node terminal. Connect the output inductor to this pin.
AGND	12	G	Ground of internal analog circuitry. Connect AGND to PGND plane with a short trace.
FB	13	I	Converter feedback input. Connect to the center tap of the resistor divider between output voltage and AGND.
SS	14	O	Soft-Start time selection pin. Connecting an external capacitor sets the soft-start time and if no external capacitor is connected, the converter starts up in 1 ms.
EN	15	I	Enable input control, leaving this pin floating enables the converter. This pin can also be used to adjust the input UVLO by connecting to the center tap of the resistor divider between VIN and EN.
PGOOD	16	O	Open-drain power good indicator, this pin asserted low if output voltage is out of PGOOD threshold, overvoltage, or if the device is under thermal shutdown, EN shutdown or during soft start.
VREG5	17	I/O	4.7-V internal LDO output which can also be driven externally with a 5-V input. This pin supplies voltage to the internal circuitry and gate driver. Bypass this pin with a 4.7-µF capacitor.
MODE	18	I	Switching frequency, current limit selection and light load operation mode selection pin. Connect this pin to a resistor divider from VREG5 and AGND for different MODE options shown in Table 6-3.

(1) I = input, P = power, G = ground, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	V_{IN}	–0.3	20	V
	SW	–2	19	
	SW (10-ns transient)	–5	25	
	V_{IN}-SW		22	
	V_{IN}-SW (10-ns transient)		25	
	EN	–0.3	6.5	
	BOOT –SW	–0.3	6.5	
	BOOT –SW (10 ns transient)	–0.3	7.5	
	BOOT	–0.3	25.5	
	SS, MODE, FB	–0.3	6.5	
	VREG5	–0.3	6	
Output voltage	PGOOD	–0.3	6.5	V
Output current(2)	I_{OUT}		14	A
Operating junction temperature	T_J	–40	150	°C
Storage temperature	T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) to be consistent with the TI reliability requirement of 100k Power-On-Hours at 105°C junction temperature, the output current must not exceed 14A continuously under 100% duty operation as to prevent electromigration failure in the solder. Higher junction temperature or longer power-on hours are achievable at lower than 14A continuous output current.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	V_{IN}	3.8		17	V
	SW	–1.8		17	V
	BOOT	–0.1		23.5	V
	VREG5	–0.1		5.2	V
Output current	I_{LOAD}	0		12	A
Operating junction temperature	T_J	-40		150	°C

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5.4 Thermal Information

THERMAL METRIC[1]		RNN (VQFN-HR) 18 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

T_J = –40°C to 150°C, V_{IN} = 12V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{IN}	VIN supply current	T_J = 25°C, V_{EN} = 5 V, non switching		146		µA
I_{VINSDN}	VIN shutdown current	T_J = 25°C, V_{EN} = 0 V		9.3		µA
LOGIC THRESHOLD						
V_{ENH}	EN H-level threshold voltage		1.175	1.225	1.3	V
V_{ENL}	EN L-level threshold voltage		1.025	1.104	1.15	V
V_{ENHYS}				0.121		V
I_{ENp1}	EN pullup current	V_{EN} = 1.0 V	0.35	1.91	2.95	µA
I_{ENp2}		V_{EN} = 1.3 V	3	4.197	5.5	µA
FEEDBACK VOLTAGE						
V_{FB}	FB voltage	T_J = 25°C	598	600	602	mV
		T_J = 0°C to 85°C	597.5	600	602.5	mV
		T_J = –40°C to 85°C	594	600	602.5	mV
		T_J = –40°C to 150°C	594	600	606	mV
LDO VOLTAGE						
VREG5	LDO output voltage	T_J = –40°C to 150°C	4.58	4.7	4.83	V
ILIM5	LDO output current limit	T_J = –40°C to 150°C	100	150	200	mA
MOSFET						
$R_{DS(on)H}$	High side switch resistance	T_J = 25°C, V_{VREG5} = 4.7 V		7.8		mΩ
$R_{DS(on)L}$	Low side switch resistance	T_J = 25°C, V_{VREG5} = 4.7 V		3.2		mΩ
SOFT START						
I_{ss}	Soft-start charge current	T_J = –40°C to 150°C	4.9	6	7.1	µA
CURRENT LIMIT						
I_{OCL}	Current Limit (Low side sourcing)	ILIM-1 option, valley current	9.775	11.5	13.225	A
		ILIM option, valley current	11.73	13.8	15.87	A
	Current limit (low side negative)	Valley current		4		A
POWER GOOD						
$V_{PGOODTH}$	PGOOD threshold	V_{FB} falling (fault)		84%		
		V_{FB} rising (good)		93%		
		V_{FB} rising (fault)		116%		
		V_{FB} falling (good)		108%		

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5.5 Electrical Characteristics (continued)

T_J = –40°C to 150°C, V_{IN} = 12V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP threshold	OVP detect		121% × V_{FB}		
V_{UVP}	Output UVP threshold	Hiccup detect		70% × V_{FB}		
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature		160		°C
		Hysteresis		15		°C
UVLO						
UVLO	UVLO threshold	VREG5 rising voltage		4.25		V
		VREG5 falling voltage		3.52		V
		VREG5 hysteresis		730		mV
UVLO, VREG5 = 4.7V	UVLO threshold, VREG5 = 4.7V	VIN rising voltage, VREG5 = 4.7V		3.32		V
		VIN falling voltage, VREG5 = 4.7V		3.24		V
		VIN hysteresis, VREG5 = 4.7V		80		mV

5.6 Timing Requirements

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
ON-TIME TIMER CONTROL						
t_{ON}	SW on time[1]	V_{IN} = 12 V, V_{OUT} = 3.3 V, F_{SW} = 800 kHz	310	340	380	ns
$t_{ON\ min}$	SW Minimum on time	V_{IN} = 17 V, V_{OUT} = 0.6 V, F_{SW}= 1200 kHz		60		ns
t_{OFF}	SW Minimum off time	25°C, V_{FB} = 0.5 V			310	ns
SOFT START						
t_{SS}	Soft-start time	Internal soft-start time		1.2		ms
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
t_{UVPDEL}	Output hiccup delay relative to SS time	UVP detect		1		cycle
t_{UVPEN}	Output hiccup enable delay relative to SS time	UVP detect		14		cycle

(1) Specified by design

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5.7 Typical Characteristics

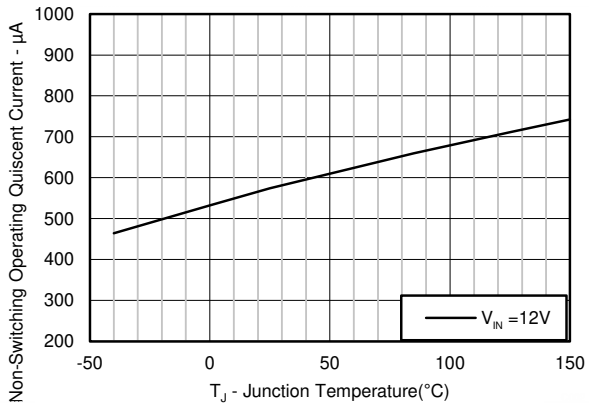

Figure 5-1. Quiescent Current vs Temperature

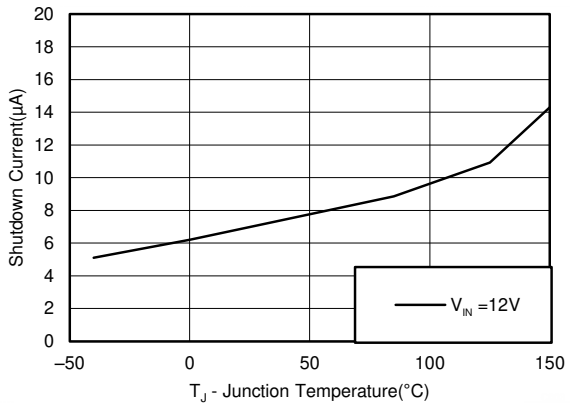

Figure 5-2. Shutdown Current vs Temperature

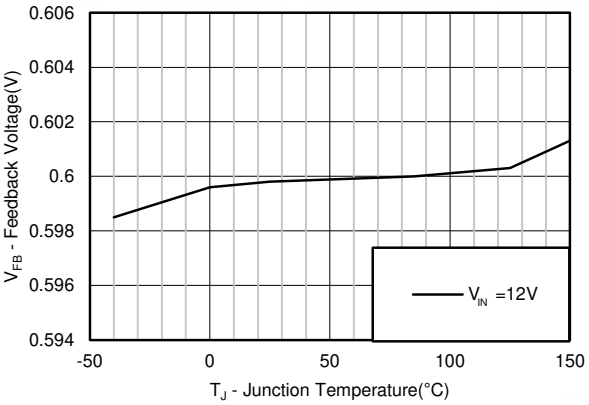

Figure 5-3. Feedback Voltage vs Temperature

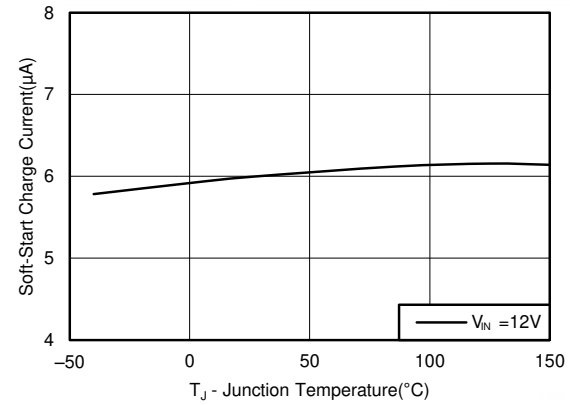

Figure 5-4. Soft-Start Charge Current vs Temperature

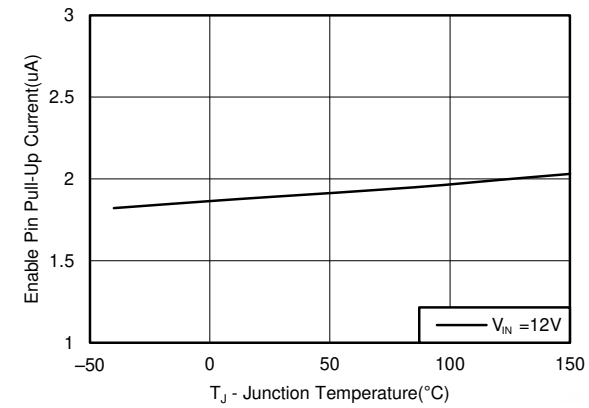

Figure 5-5. Enable Pullup Current, V_{EN} = 1.0 V

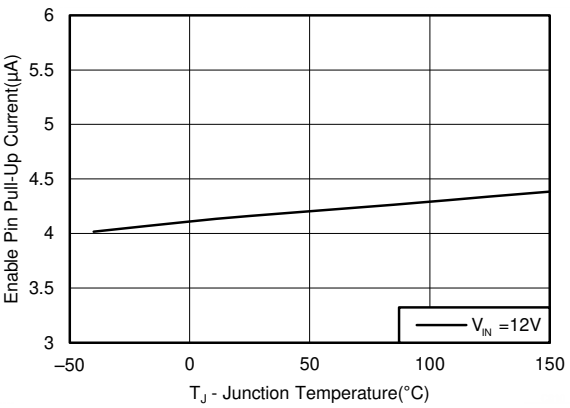

Figure 5-6. Enable Pullup Current, V_{EN} = 1.3 V

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5.7 Typical Characteristics (continued)

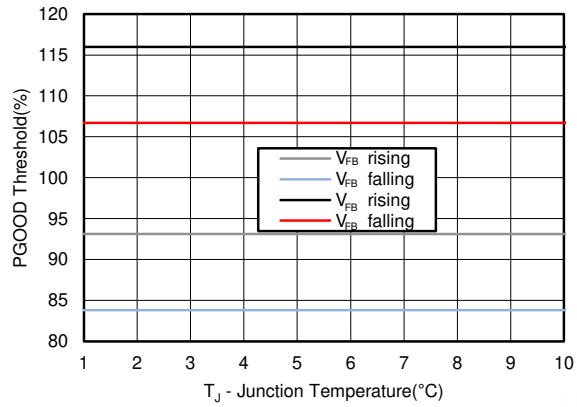

Figure 5-7. PGOOD Threshold vs Temperature

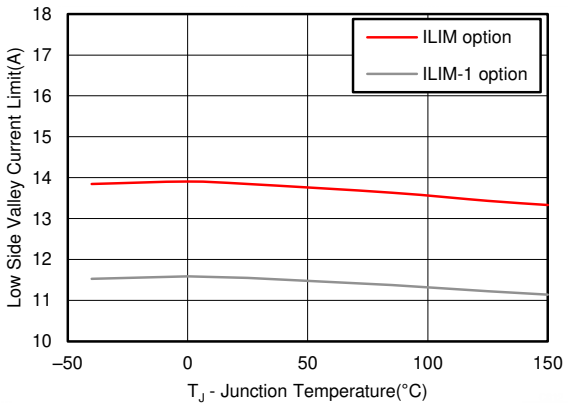

Figure 5-8. Current Limit vs Temperature

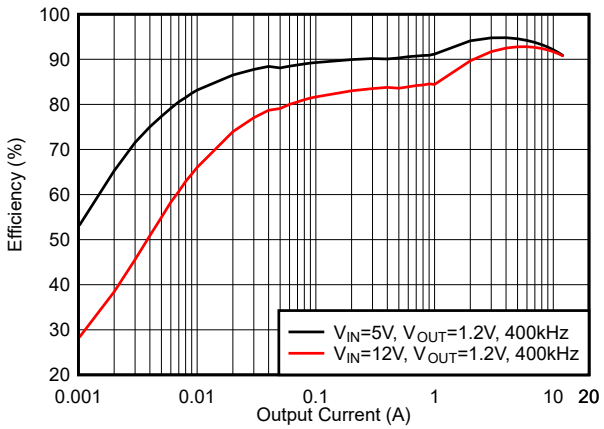

Figure 5-9. Efficiency, DCM Mode, f_{SW} = 400 kHz

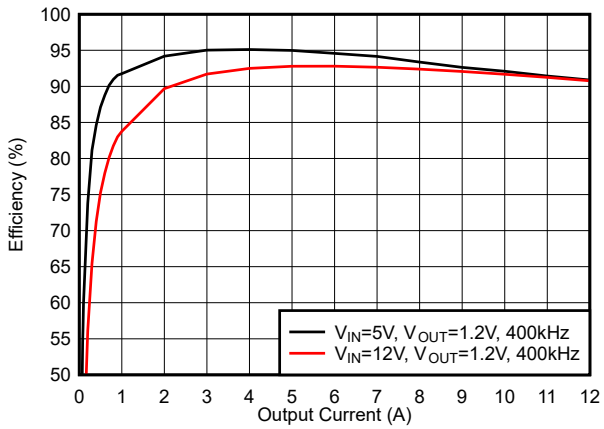

Figure 5-10. Efficiency, FCCM Mode, f_{SW} = 400 kHz

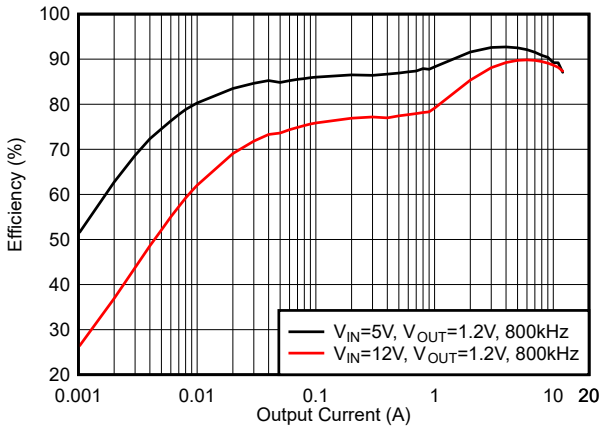

Figure 5-11. Efficiency, DCM Mode, f_{SW} = 800 kHz

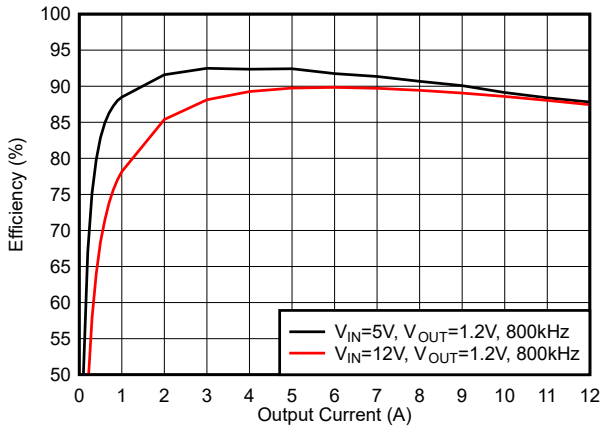

Figure 5-12. Efficiency, FCCM Mode, f_{SW} = 800 kHz

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5.7 Typical Characteristics (continued)

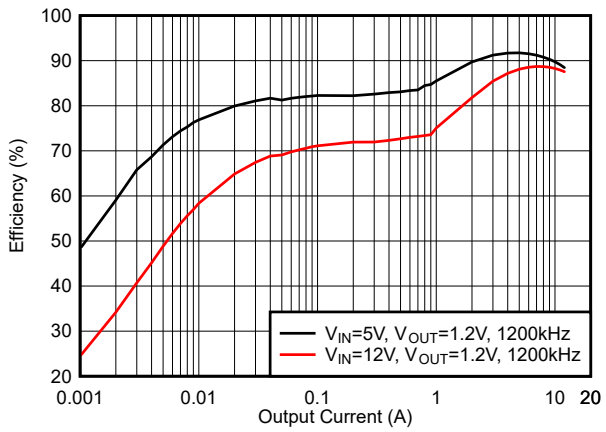

Figure 5-13. Efficiency, DCM Mode, f_{SW} = 1200 kHz

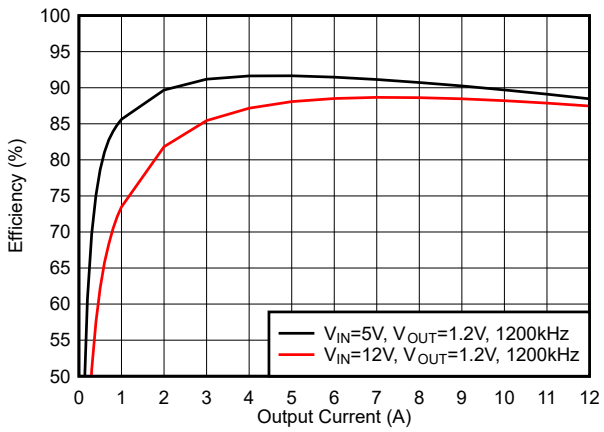

Figure 5-14. Efficiency, FCCM Mode, f_{SW} = 1200 kHz

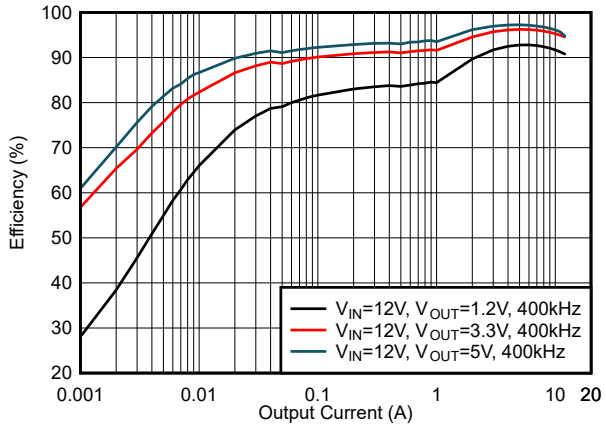

Figure 5-15. Efficiency, DCM Mode, f_{SW} = 400 kHz

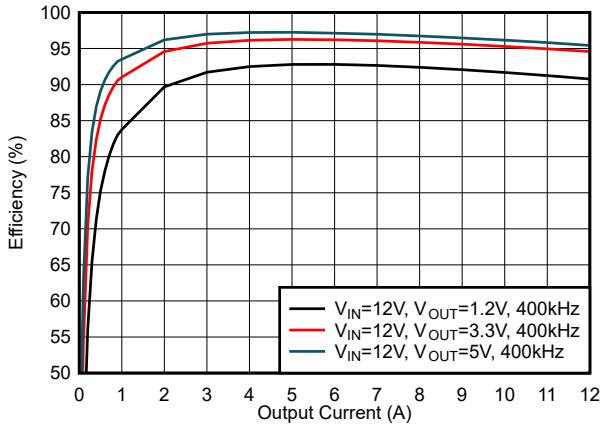

Figure 5-16. Efficiency, FCCM Mode, f_{SW} = 400 kHz

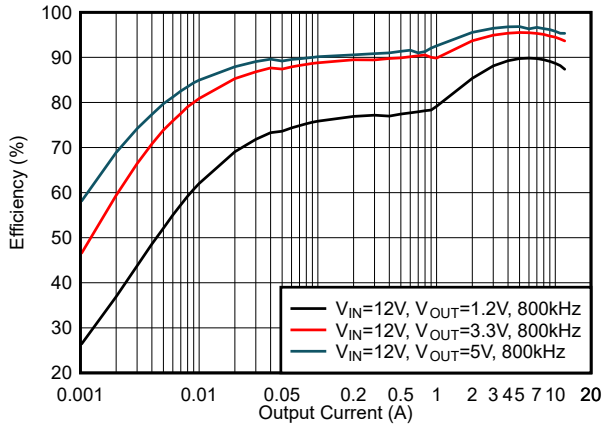

Figure 5-17. Efficiency, DCM Mode, f_{SW} = 800 kHz

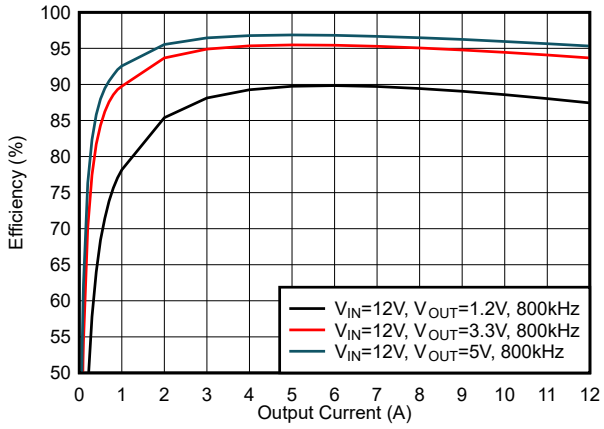

Figure 5-18. Efficiency, FCCM Mode, f_{SW} = 800 kHz

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5.7 Typical Characteristics (continued)

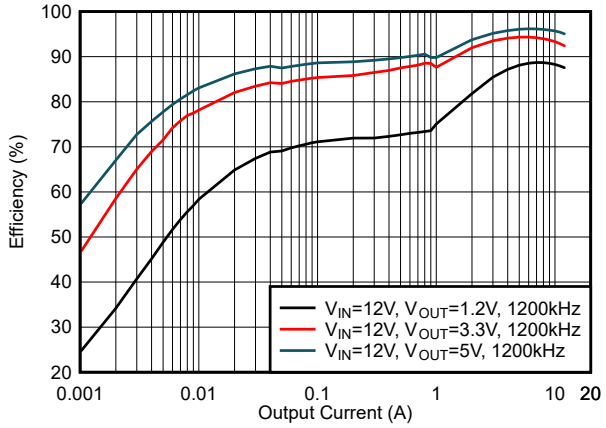

Figure 5-19. Efficiency, DCM Mode, f_{SW} = 1200 kHz

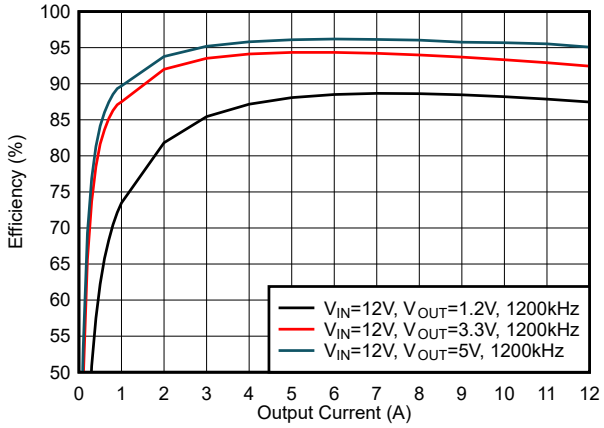

Figure 5-20. Efficiency, FCCM Mode, f_{SW} = 1200 kHz

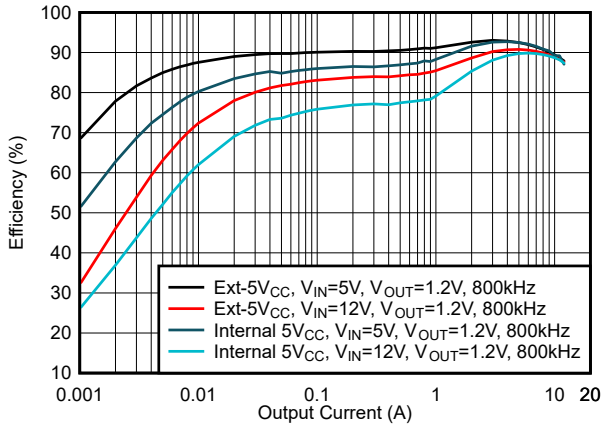

Figure 5-21. Efficiency, Ext-VCC vs Internal-VCC, DCM Mode, f_{SW} = 800 kHz

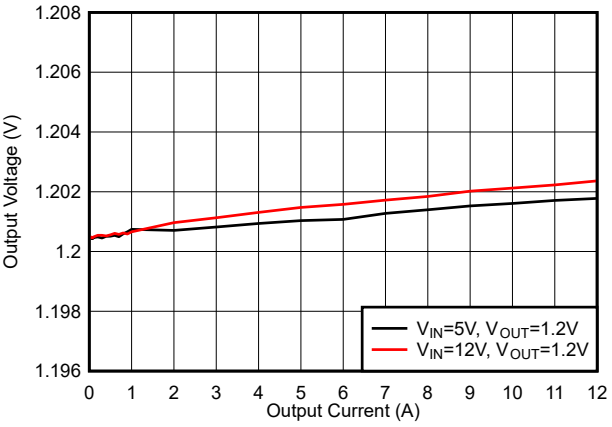

Figure 5-22. Load Regulation, F_{SW} = 800 kHz

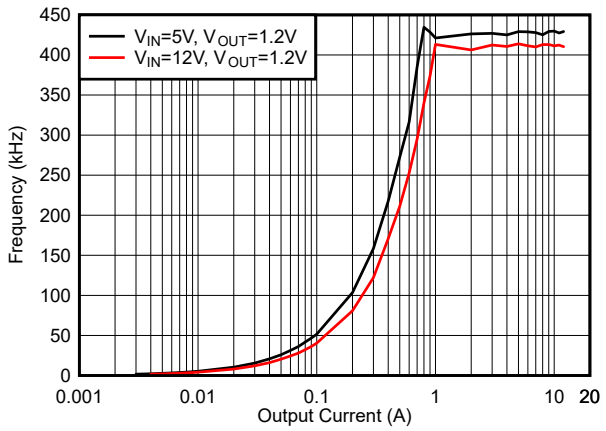

Figure 5-23. F_{SW} Load Regulation, Mode = DCM, F_{SW} = 400 kHz

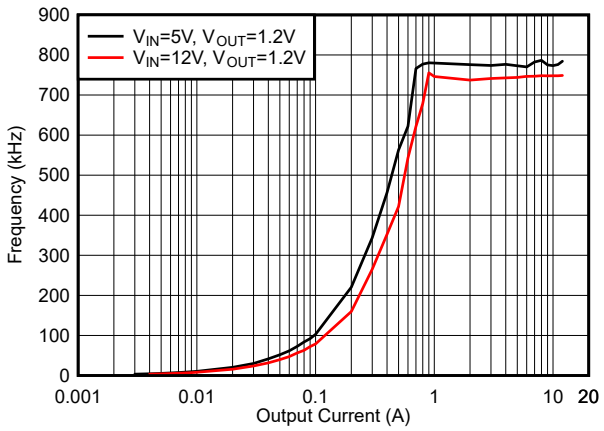

Figure 5-24. F_{SW} Load Regulation, Mode = DCM, F_{SW} = 800 kHz

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5.7 Typical Characteristics (continued)

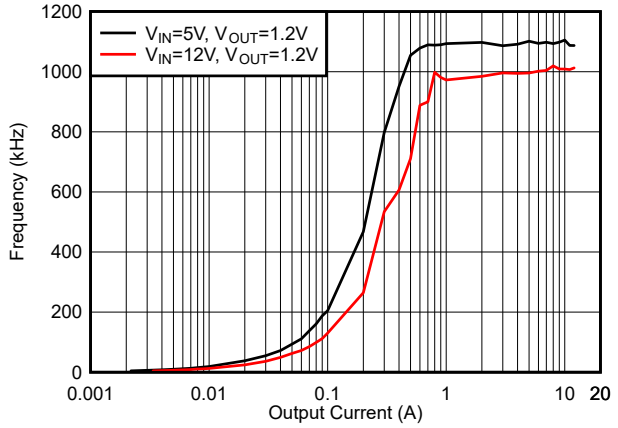

Figure 5-25. F_{SW} Load Regulation, Mode = DCM, F_{SW} = 1200 kHz

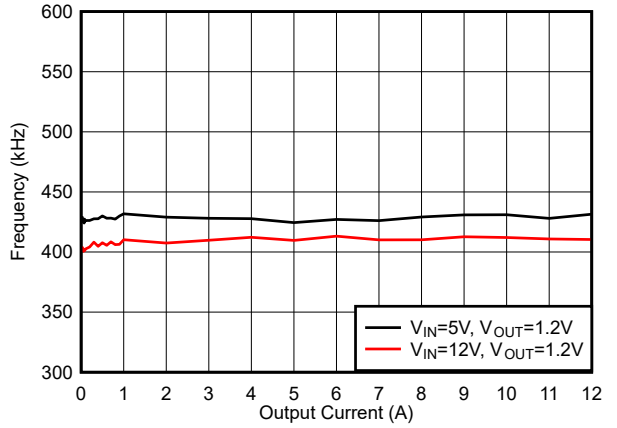

Figure 5-26. F_{SW} Load Regulation, Mode =FCCM, F_{SW} = 400 kHz

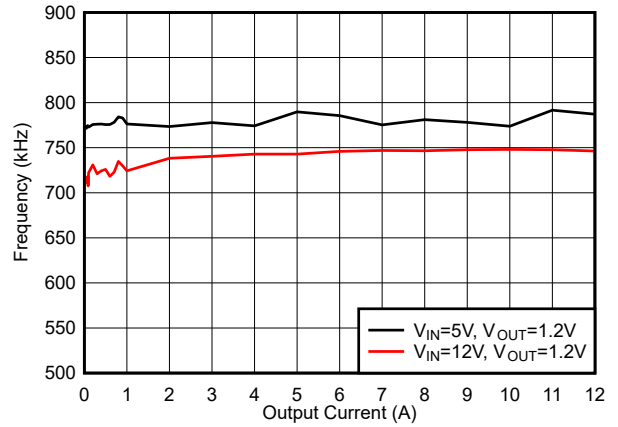

Figure 5-27. F_{SW} Load Regulation, Mode = FCCM, F_{SW} = 800 kHz

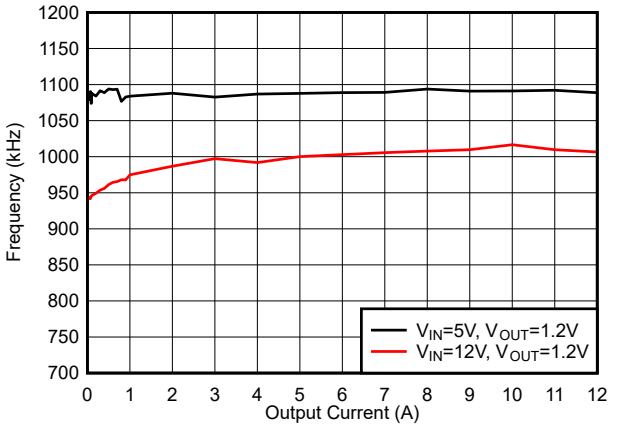

Figure 5-28. F_{SW} Load Regulation, Mode = FCCM, F_{SW} = 1200 kHz

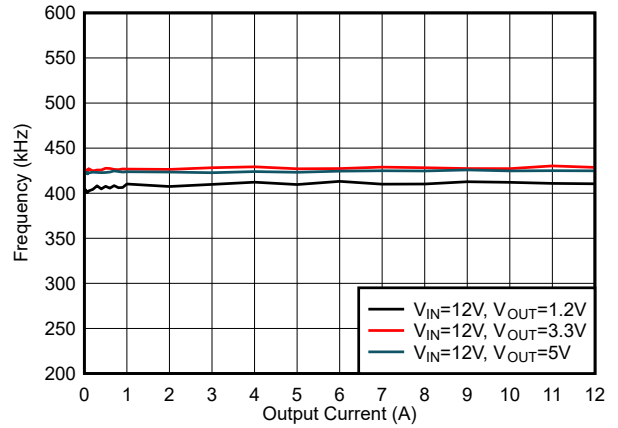

Figure 5-29. F_{SW} Load Regulation, Mode = FCCM, F_{SW} = 400 kHz

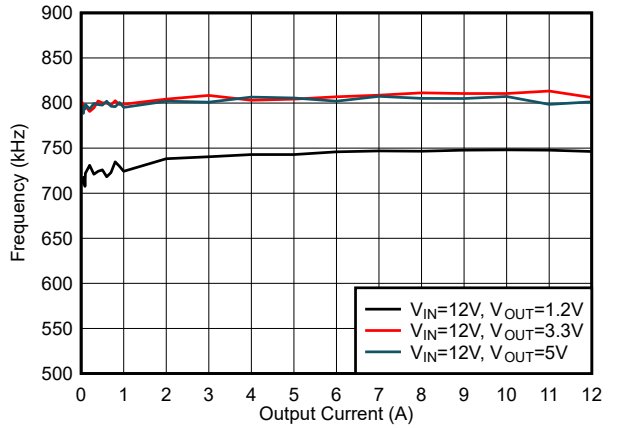

Figure 5-30. F_{SW} Load Regulation, Mode = FCCM, F_{SW} = 800 kHz

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5.7 Typical Characteristics (continued)

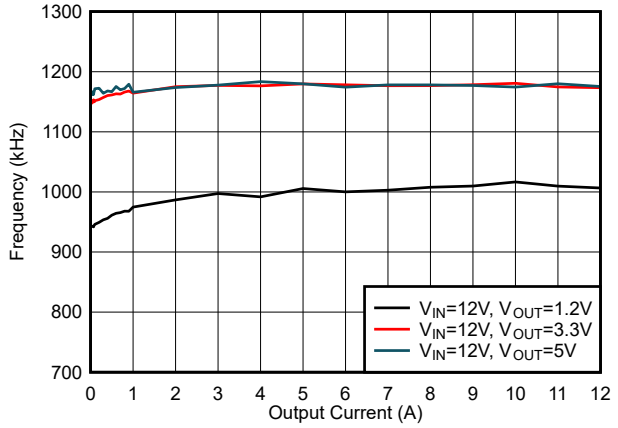

Figure 5-31. F_{SW} Load Regulation, Mode = FCCM, F_{SW} = 1200 kHz

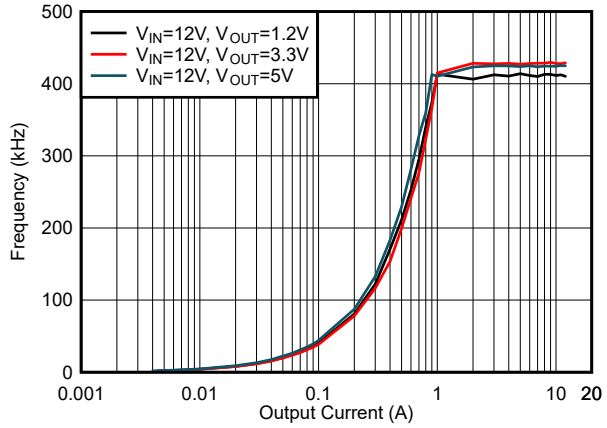

Figure 5-32. F_{SW} Load Regulation, Mode = DCM, F_{SW} = 400 kHz

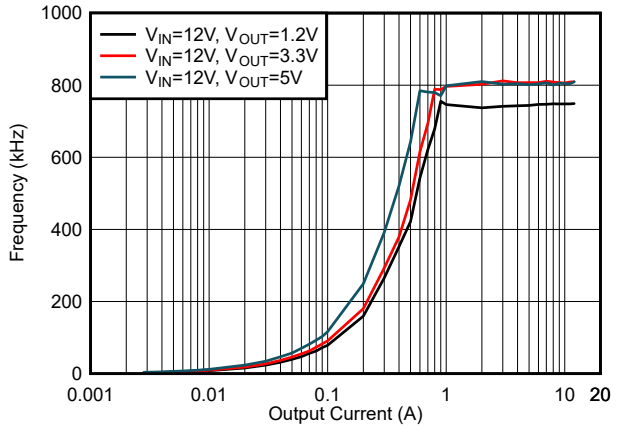

Figure 5-33. F_{SW} Load Regulation, Mode = DCM, F_{SW} = 800 kHz

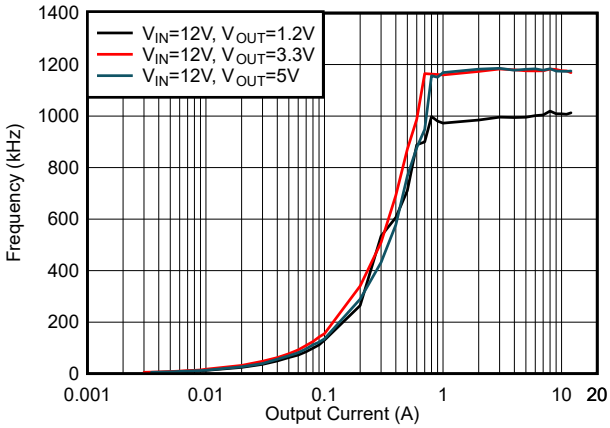

Figure 5-34. F_{SW} Load Regulation, Mode = DCM, F_{SW} = 1200 kHz

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6 Detailed Description

6.1 Overview

The TPS56C215 is a high-density, synchronous, step-down buck converter which can operate from 3.8-V to 17-V input voltage (V_{IN}). The device has 7.8-mΩ and 3.2-mΩ integrated MOSFETs that enable high efficiency up to 12 A. The device employs D-CAP3 control mode that provides fast transient response with no external compensation components and an accurate feedback voltage. The control topology provides seamless transition between FCCM operating mode at higher load condition and DCM/Eco-mode operation at lighter load condition. DCM/Eco-mode allows the TPS56C215 to maintain high efficiency at light load. The TPS56C215 is able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

The TPS56C215 has three selectable switching frequencies (F_{SW}) (400 kHz, 800 kHz, and 1200 kHz), which gives the flexibility to optimize the design for higher efficiency or smaller size. There are two selectable current limits. All these options are configured by choosing the right voltage on the MODE pin.

The TPS56C215 has a 4.7-V internal LDO that creates bias for all internal circuitry. There is a feature to overdrive this internal LDO with an external voltage on the VREG5 pin which improves the efficiency of the converter. The undervoltage lockout (UVLO) circuit monitors the VREG5 pin voltage to protect the internal circuitry from low input voltages. The device has an internal pullup current source on the EN pin which can enable the device even with the pin floating.

Soft-start time can be selected by connecting a capacitor to the SS pin. The device is protected from output short, undervoltage, and overtemperature conditions.

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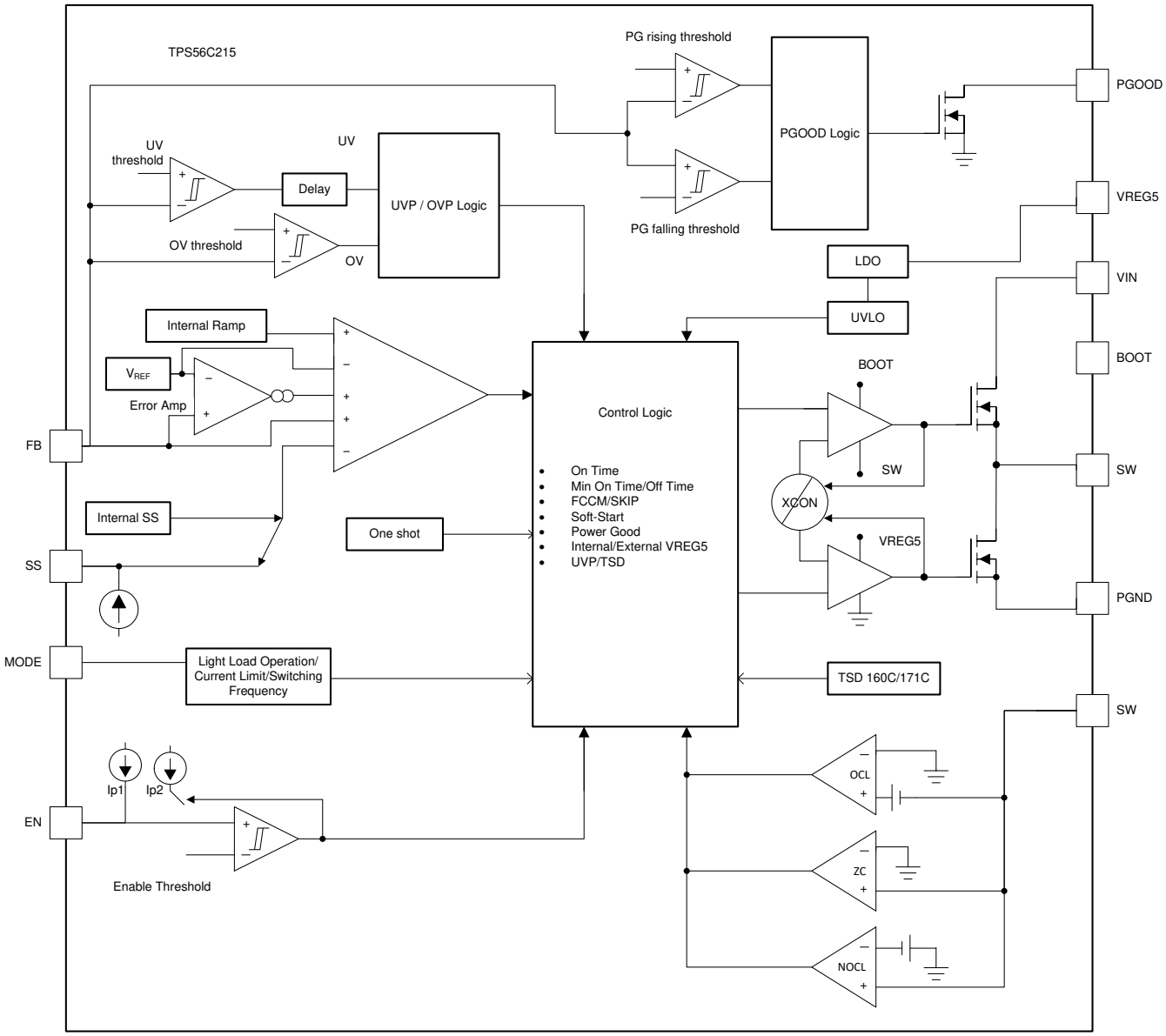
6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 PWM Operation and D-CAP3™ Control Mode

The TPS56C215 operates using the adaptive on-time PWM control with a proprietary D-CAP3 control mode which enables low external component count with a fast load transient response while maintaining a good output voltage accuracy. At the beginning of each switching cycle, the high-side MOSFET is turned on for an on-time set by an internal one shot timer. This on-time is set based on the input voltage of the converter, output voltage of the converter, and the pseudo-fixed frequency, hence this type of control topology is called an adaptive on-time control. The one-shot timer resets and turns on again after the feedback voltage (V_{FB}) falls below the internal reference voltage (V_{REF}). An internal ramp is generated which is fed to the FB pin to simulate the output voltage ripple. This enables the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for DCAP3 control topology.

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The TPS56C215 includes an error amplifier that makes the output voltage very accurate. This error amplifier is absent in other flavors of D-CAP3. For any control topology that is compensated internally, there is a range of the output filter the control topology can support. The output filter used with the TPS56C215 is a low-pass L-C circuit. This L-C filter has double pole that is described in Equation 1.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS56C215. The low frequency L-C double pole has a 180 degree in-phase. At the output filter frequency, the gain rolls off at a –40-dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40-dB to –20-dB per decade and increases the phase to 90 degree one decade above the zero frequency. The internal ripple injection high frequency zero is changed according to the switching frequency selected as shown in Table 6-1. The inductor and capacitor selected for the output filter must be such that the double pole is located close enough to the high-frequency zero so that the phase boost provided by this high-frequency zero provides adequate phase margin for the stability requirement. The crossover frequency of the overall system must usually be targeted to be less than one-fifth of the switching frequency (F_{SW}).

Table 6-1. Ripple Injection Zero

SWITCHING FREQUENCY (kHz)	ZERO LOCATION (kHz)
400	17.8
800	27.1
1200	29.8

Table 6-2 lists the inductor values and part numbers that are used to plot the efficiency curves in *Section 5.7*.

Table 6-2. Inductor Values

V_{OUT}(V)	F_{SW}(kHz)	L_{OUT}(µH)	WÜRTH PART NUMBER(1)
1.2	400	1.2	744325120
	800	0.68	744311068
	1200	0.47	744314047
3.3	400	2.4	744325240
	800	1.5	7443552150
	1200	1.2	744325120
5.5	400	3.3	744325330
	800	2.4	744325240
	1200	1.5	7443552150

(1) See Third-Party Products disclaimer.

6.3.2 Eco-mode Control

The TPS56C215 is designed with Eco-mode control to increase efficiency at light loads. This option can be chosen using the MODE pin as shown in Table 6-3. As the output current decreases from heavy load condition, the inductor current is also reduced. If the output current is reduced enough, the valley of the inductor current reaches the zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side MOSFET is turned off when a zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept approximately the same as in continuous conduction mode. The off-time increases as discharging the output with a smaller load current takes more time. The light load current where the transition to Eco-mode operation happens ($I_{OUT(LL)}$) can be calculated from Equation 2.

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$$I_{OUT(LL)} = \frac{1}{2 \times L_{OUT} \times F_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

After identifying the application requirements, design the output inductance (L_{OUT}) so that the inductor peak-to-peak ripple current is approximately between 20% and 30% of the $I_{OUT(max)}$ (peak current in the application). Sizing the inductor properly so that the valley current does not hit the negative low-side current limit is important.

6.3.3 4.7-V LDO

The VREG5 pin is the output of the internal 4.7-V linear regulator that creates the bias for all the internal circuitry and MOSFET gate drivers. The VREG5 pin needs to be bypassed with a 4.7-µF capacitor. An external voltage that is above the internal output voltage of the LDO can override the internal LDO, switching the internal LDO to the external rail after a higher voltage is detected. This enhances the efficiency of the converter because the quiescent current now runs off this external rail instead of the input power supply. The UVLO circuit monitors the VREG5 pin voltage and disables the output when VREG5 falls below the UVLO threshold. When using an external bias on the VREG5 rail, any power-up and power-down sequencing can be applied but understanding that if there is a discharge path on the VREG5 rail that can pull a current higher than the internal current limit of the LDO (ILIM5) from the VREG5, then the VREG5 LDO turns off thereby shutting down the output of TPS56C215 is important. If such condition does not exist and if the external VREG5 rail is turned off, the VREG5 voltage switches over to the internal LDO voltage which is 4.7 V typically in a few nanoseconds. Figure 6-1 shows this transition of the VREG5 voltage from an external bias of 5.5 V to the internal LDO output of 4.7 V when the external bias to VREG5 is disabled while the output of TPS56C215 remains unchanged.

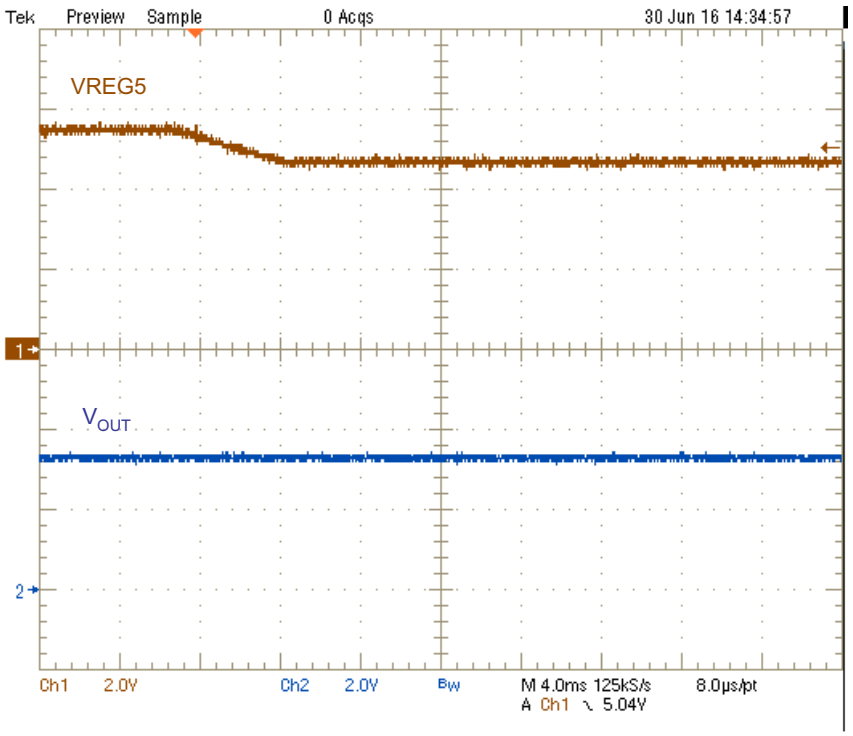

Figure 6-1. VREG5 Transition

6.3.4 MODE Selection

The TPS56C215 has a MODE pin that can offer 12 different states of operation as a combination of current limit, switching frequency, and light load operation. The device can operate at two different current limits ILIM-1 and ILIM to support an output continuous current of 10 A and 12 A, respectively. The TPS56C215 is designed to compare the valley current of the inductor against the current limit thresholds so understand that the output current is half the ripple current higher than the valley current. For example, with the ILIM current limit selection,

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the OCL threshold is 11.73-A minimum, which means that a pk-pk inductor ripple current of 0.54-A minimum is needed to be able to draw 12 A out of the converter without entering an overcurrent condition. The TPS56C215 can operate at three different frequencies of 400 kHz, 800 kHz, and 1200 kHz and also can choose between Eco-mode and FCCM mode. The device reads the voltage on the MODE pin during start-up and latches onto one of the MODE options listed in Table 6-3. The voltage on the MODE pin can be set by connecting this pin to the center tap of a resistor divider connected between VREG5 and AGND. A guideline for the top resistor (R_{M_H}) and the bottom resistor (R_{M_L}) in 1% resistors is shown in Table 6-3. Make sure that the voltage for the MODE pin is derived from the VREG5 rail only because internally this voltage is referenced to detect the MODE option. The MODE pin setting can be reset only by a VIN power cycling.

Table 6-3. MODE Pin Resistor Settings

R_{M_L} (kΩ)	R_{M_H} (kΩ)	LIGHT LOAD OPERATION	CURRENT LIMIT	FREQUENCY (kHz)
5.1	300	FCCM	ILIM-1	400
10	200	FCCM	ILIM	400
20	160	FCCM	ILIM-1	800
20	120	FCCM	ILIM	800
51	200	FCCM	ILIM-1	1200
51	180	FCCM	ILIM	1200
51	150	DCM	ILIM-1	400
51	120	DCM	ILIM	400
51	91	DCM	ILIM-1	800
51	82	DCM	ILIM	800
51	62	DCM	ILIM-1	1200
51	51	DCM	ILIM	1200

Figure 6-2 shows the typical start-up sequence of the device after the EN pin voltage crosses the EN turn-on threshold. After the voltage on VREG5 pin crosses the rising UVLO threshold, reading the first MODE setting takes 100 µs and approximately 100 µs from there to finish the last MODE setting. The output voltage starts ramping after the MODE setting reading is completed.

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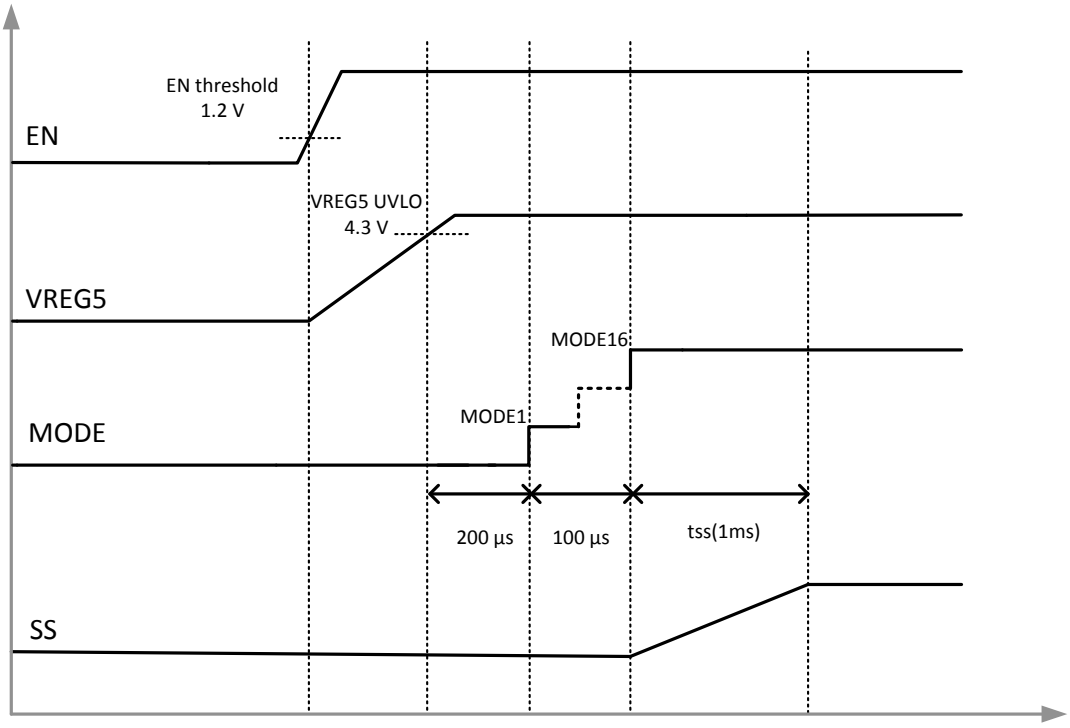

Figure 6-2. Power-Up Sequence

6.3.5 Soft Start and Prebiased Soft Start

The TPS56C215 has an adjustable soft start time that can be set by connecting a capacitor on SS pin. When the EN pin becomes high, the soft-start charge current (I_{SS}) begins charging the external capacitor (C_{SS}) connected between SS and AGND. The devices tracks the lower of the internal soft-start voltage or the external soft-start voltage as the reference. The equation for the soft-start time (T_{SS}) is shown in Equation 3:

$$T_{SS(S)} = \frac{C_{SS} \times V_{REF}}{I_{SS}} \quad (3)$$

where

- V_{REF} is 0.6 V and I_{SS} is 6 µA

If the output capacitor is prebiased at start-up, the device initiates switching and starts ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme makes sure that the converters ramp up smoothly into regulation point.

6.3.6 Enable and Adjustable UVLO

The EN pin controls the turn-on and turnoff of the device. When EN pin voltage is above the turn-on threshold which is around 1.2 V, the device starts switching, and when the EN pin voltage falls below the turn-off threshold, which is around 1.1 V, the device stops switching. If the user application requires a different turn-on (V_{START}) and turnoff thresholds (V_{STOP}) respectively, the EN pin can be configured as shown in Figure 6-3 by connecting a resistor divider between VIN and EN. The EN pin has a pullup current I_{p1} that sets the default state of the pin when floating. This current increases to I_{p2} when the EN pin voltage crosses the turn-on threshold. The UVLO thresholds can be set by using Equation 4 and Equation 5.

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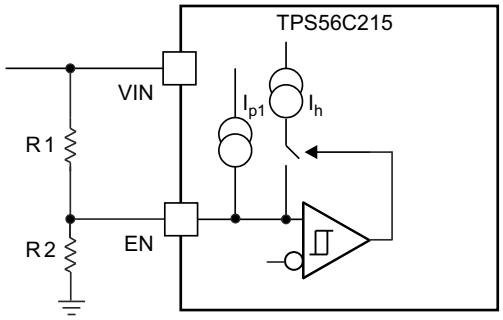

Figure 6-3. Adjustable VIN Undervoltage Lockout

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_{p1}\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (4)$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1\ I_{p2}} \quad (5)$$

where

- I_{p2} = 4.197 µA
- I_{p1} = 1.91 µA
- I_h = 2.287 µA
- $V_{ENRISING}$ = 1.225 V
- $V_{ENFALLING}$ = 1.104 V

6.3.7 Power Good

The Power Good (PGOOD) pin is an open-drain output. After the FB pin voltage is between 93% and 107% of the internal reference voltage (V_{REF}), the PGOOD is deasserted and floats after a 200-µs deglitch time. TI recommends a pullup resistor of 10 kΩ to pull up to VREG5. The PGOOD pin is pulled low when the FB pin voltage is lower than V_{UVP} or greater than V_{OVP} threshold, in an event of thermal shutdown, or during the soft-start period.

6.3.8 Overcurrent Protection and Undervoltage Protection

The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by input voltage, output voltage, the on-time, and the output inductor value. During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the measured drain-to-source voltage of the low-side FET is above the voltage proportional to current limit, the low-side FET stays on until the current level becomes lower than the OCL level which reduces the output current available. When the current is limited the output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 68% of the target voltage, the UVP comparator detects the fall and shuts down the device after a wait time of 1 × t_{SS}. The device re-starts after a hiccup time of 14 × t_{SS}. In this type of valley detect control, the load current is higher than the OCL threshold by one half of the peak-to-peak inductor ripple current. When the overcurrent condition is removed, the output voltage returns to the regulated value. If an OCL condition happens during start-up, then the device enters hiccup-mode immediately without a wait time of 1 soft-start cycle.

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6.3.9 Transient Response Enhancement

The PSM deglitch feature activates whenever the device transitions from a heavy load in Continuous Conduction Mode (CCM) to a light load in Discontinuous Conduction Mode (DCM). During this transition, the system enters Forced Continuous Conduction Mode (FCCM) for 16 cycles before switching to DCM. This feature is designed to provide fast recovery in load transients during DCM operation.

Figure 6-4 shows 16-cycle and 32-cycle FCCM operation during load release and dynamic COMP pin positioning. Figure 6-5 shows steady-state Auto-skip mode operation with the dynamic COMP pin clamp.

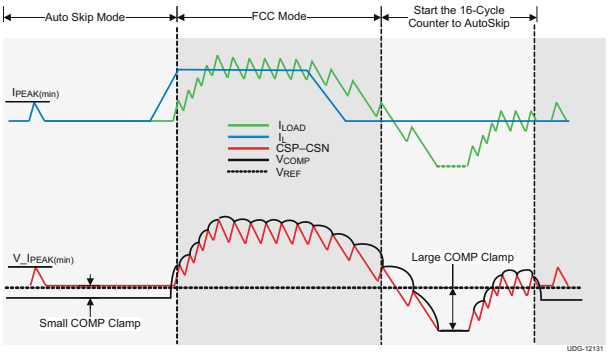

Figure 6-4. FCCM Transient Response

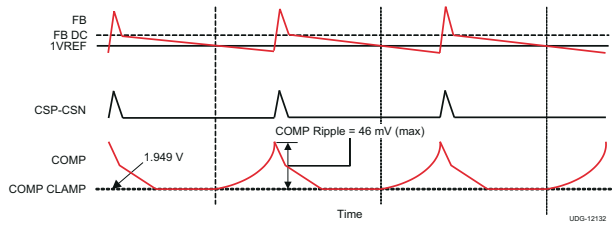

Figure 6-5. Auto-skip Mode Transient Response

6.3.10 UVLO Protection

Undervoltage lockout protection (UVLO) monitors the internal VREG5 regulator voltage. When the VREG5 voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

6.3.11 Thermal Shutdown

The device monitors the internal die temperature. If this temperature exceeds the thermal shutdown threshold value (T_{SDN} typically 160°C), the device shuts off. This protection is a non-latch protection. During start-up, if the device temperature is higher than 160°C, the device does not start switching and does not load the MODE settings. If the device temp goes higher than T_{SDN} threshold after start-up, the device stops switching with SS reset to ground and an internal discharge switch turns on to quickly discharge the output voltage. The device re-starts switching when the temperature goes below the thermal shutdown threshold but the MODE settings are not re-loaded again.

6.3.12 Output Voltage Discharge

The device has a 500-Ω discharge switch that discharges the output V_{OUT} through SW node during any event of fault like output overvoltage, output undervoltage, TSD, if VREG5 voltage below the UVLO and when the EN pin voltage (V_{EN}) is below the turn-on threshold.

6.4 Device Functional Modes

6.4.1 Light Load Operation

When the MODE pin is selected to operate in FCCM mode, the converter operates in continuous conduction mode (FCCM) during light-load conditions. During FCCM, the switching frequency (F_{SW}) is maintained at an almost constant level over the entire load range which is designed for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load. If the MODE pin is selected to operate in DCM/Eco-mode, the device enters pulse skip mode after the valley of the inductor ripple current crosses zero. The Eco-mode maintains higher efficiency at light load with a lower switching frequency.

6.4.2 Standby Operation

The TPS56C215 can be placed in standby mode by pulling the EN pin low. The device operates with a shut-down current of 7 µA when in standby condition.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The schematic of Figure 7-1 shows a typical application for TPS56C215. This design converts an input voltage range of 4.5 V to 17 V down to 1.2 V with a maximum output current of 12 A.

7.2 Typical Application

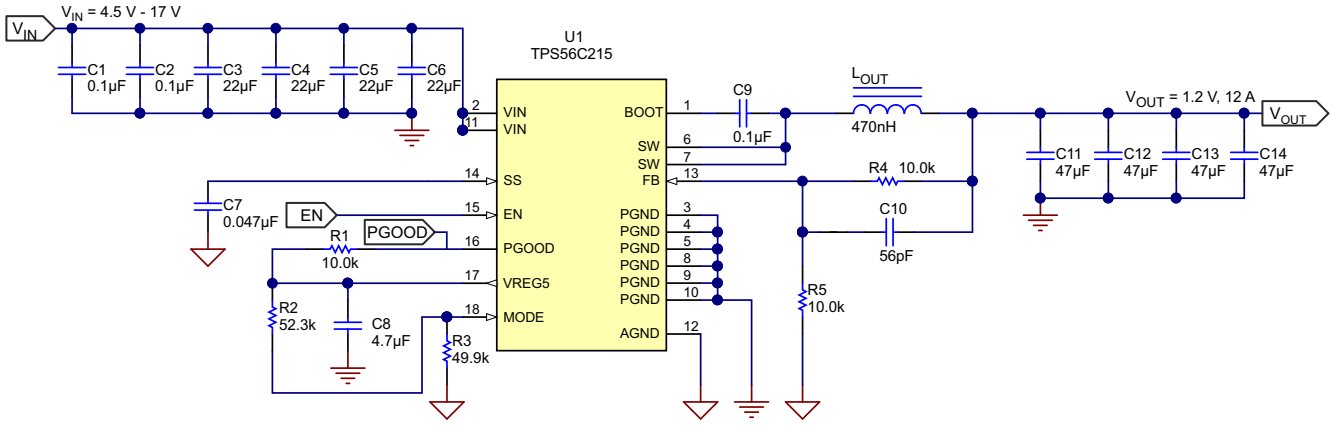

Figure 7-1. Application Schematic

7.2.1 Design Requirements

Table 7-1. Design Parameters

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage			1.2		V
I_{OUT}	Output current			12		A
ΔV_{OUT}	Transient response	9-A load step		40		mV
V_{IN}	Input voltage		4.5	12	17	V
$V_{OUT(ripple)}$	Output voltage ripple			20		$mV_{(P-P)}$
	Start input voltage	Input voltage rising		Internal UVLO		V
	Stop input voltage	Input voltage falling		Internal UVLO		V
F_{SW}	Switching frequency			1.2		MHz
Operating mode				DCM		
T_A	Ambient temperature			25		°C

7.2.2 Detailed Design Procedure

7.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS56C215 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (VIN), output voltage (VOUT), and output current (IOUT) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.

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3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability. In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.2.2 External Component Selection

7.2.2.2.1 Output Voltage Set Point

To change the output voltage of the application, changing the value of the upper feedback resistor is necessary. By changing this resistor the user can change the output voltage above 0.6 V. See Equation 6.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{UPPER}}{R_{LOWER}}\right) \tag{6}$$

7.2.2.2.2 Switching Frequency and MODE Selection

Switching Frequency, current limit, and switching mode (DCM or FCCM) are set by a voltage divider from VREG5 to GND connected to the MODE pin. See Table 6-3 for possible MODE pin configurations. Switching frequency selection is a tradeoff between higher efficiency and smaller system design size. Lower switching frequency yields higher overall efficiency but relatively bigger external components. Higher switching frequencies cause additional switching losses which impact efficiency and thermal performance. For this design, 1.2 MHz is chosen as the switching frequency, the switching mode is DCM and the output current is 12 A.

7.2.2.2.3 Inductor Selection

The inductor ripple current is filtered by the output capacitor. A higher inductor ripple current means the output capacitor must have a ripple current rating higher than the inductor ripple current. See Table 7-2 for recommended inductor values.

The RMS and peak currents through the inductor can be calculated using Equation 7 and Equation 8. MAke sure that the inductor is rated to handle these currents.

$$I_{L(rms)} = \sqrt{\left(I^2_{OUT} + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times L_{OUT} \times F_{SW}}\right)^2\right)} \tag{7}$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{OUT(ripple)}}{2} \tag{8}$$

During transient, short circuit conditions, the inductor current can increase up to the current limit of the device so choosing an inductor with a saturation current higher than the peak current under current limit condition is safe.

7.2.2.2.4 Output Capacitor Selection

After selecting the inductor, the output capacitor needs to be optimized. In DCAP3, the regulator reacts within one cycle to the change in the duty cycle so the good transient performance can be achieved without needing large amounts of output capacitance. The recommended output capacitance range is given in Table 7-2

Ceramic capacitors have very low ESR, otherwise the maximum ESR of the capacitor must be less than $V_{OUT(ripple)}/I_{OUT(ripple)}$.

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Table 7-2. Recommended Component Values

V_{OUT} (V)	R_{LOWER} (kΩ)	R_{UPPER} (kΩ)	F_{SW} (kHz)	L_{OUT} (µH)	$C_{OUT(min)}$ (µF)	$C_{OUT(max)}$ (µF)	C_{FF} (pF)
0.6	10	0	400	0.68	300	500	–
			800	0.47	100	500	–
			1200	0.33	88	500	–
1.2		10	400	1.2	100	500	–
			800	0.68	88	500	–
			1200	0.47	88	500	–
3.3		45.3	400	2.4	88	500	100–220
			800	1.5	88	500	100–220
			1200	1.2	88	500	100–220
5.5		82.5	400	3.3	88	500	100–220
			800	2.4	88	500	100–220
			1200	1.5	88	700	100–220

7.2.2.2.5 Input Capacitor Selection

The minimum input capacitance required is given in Equation 9.

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{INripple} \times V_{IN} \times F_{SW}} \tag{9}$$

TI recommends using a high quality X5R or X7R input decoupling capacitors of 40 µF on the input voltage pin. The voltage rating on the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. The input ripple current is calculated by Equation 10:

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{(V_{IN(min)} - V_{OUT})}{V_{IN(min)}}} \tag{10}$$

7.2.3 Application Curves

Figure 7-2 through Figure 7-8 apply to the circuit of Figure 7-1 . V_{IN} = 12 V, f_{SW} = 800 kHz, T_a = 25°C unless otherwise specified.

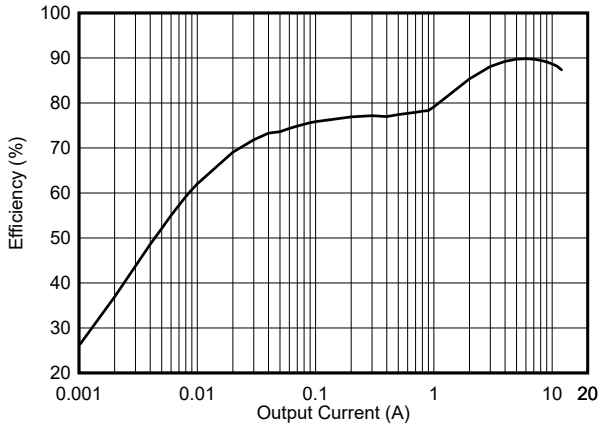

Figure 7-2. Efficiency

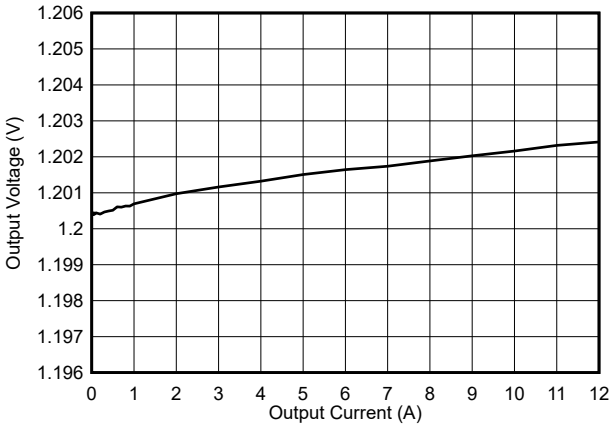

Figure 7-3. Load Regulation

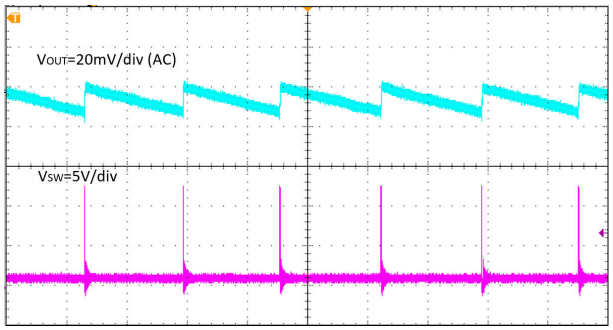

Figure 7-4. Output Voltage Ripple, I_{OUT} = 10 mA, Time = 80 µS/div

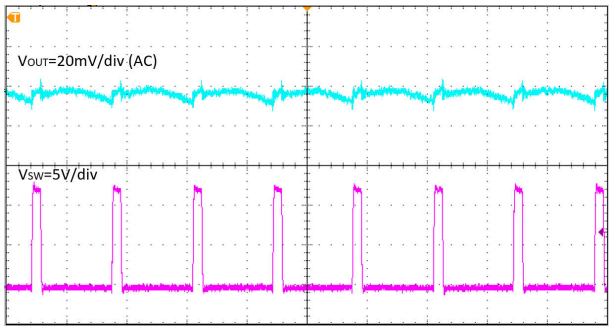

Figure 7-5. Output Voltage Ripple, I_{OUT} = 12 A, Time = 1 µS/div

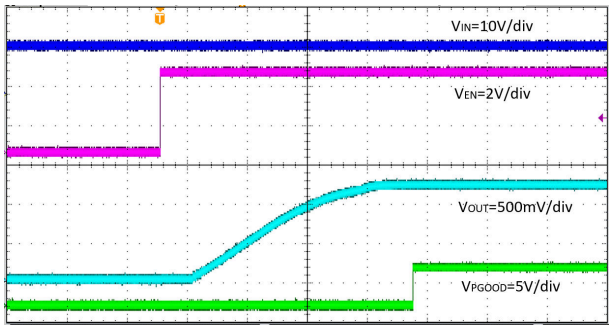

Figure 7-6. Start-Up Relative to EN Rising, Time = 2 ms/div

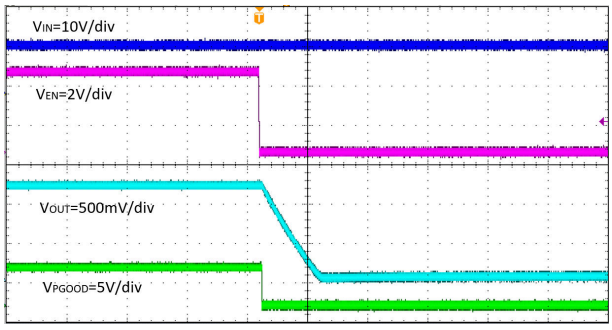

Figure 7-7. Shutdown Relative to EN Falling, Time = 200 µS/div

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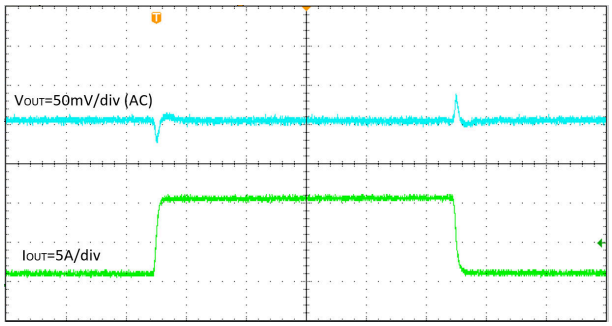

Figure 7-8. Transient Response, Load Step = 3 A – 9 A – 3 A, Slew Rate Setting = 2.5 A/µS, Time = 100 uS/div

7.3 Power Supply Recommendations

The TPS56C215 is intended to be powered by a well regulated dc voltage. The input voltage range is 3.8 to 17 V. TPS56C215 is a buck converter. The input supply voltage must be greater than the desired output voltage for proper operation. Input supply current must be appropriate for the desired output current. If the input voltage supply is located far from the TPS56215 circuit, some additional input bulk capacitance is recommended. Typical values are 100 µF to 470 µF.

7.4 Layout

7.4.1 Layout Guidelines

- Recommend a four-layer or six-layer PCB for good thermal performance and with maximum ground plane. 3" × 3", four-layer PCB with 2-oz. copper used as example.
- Recommend having equal caps on each side of the IC. Place them right across VIN as close as possible.
- Inner layer 1 is ground with the PGND to AGND net tie
- Inner layer2 has VIN copper pour that has vias to the top layer VIN. *Place multiple vias under the device near VIN and PGND and near input capacitors* to reduce parasitic inductance and improve thermal performance
- Bottom later is GND with the BOOT trace routing.
- Reference feedback to the quite AGND and routed away from the switch node.
- Make VIN trace wide to reduce the trace impedance.

7.4.2 Layout Example

Figure 7-9 shows the recommended top side layout. Component reference designators are the same as the circuit shown in Figure 7-1. Resistor divider for EN is not used in the circuit of Figure 7-1, but are shown in the layout for reference.

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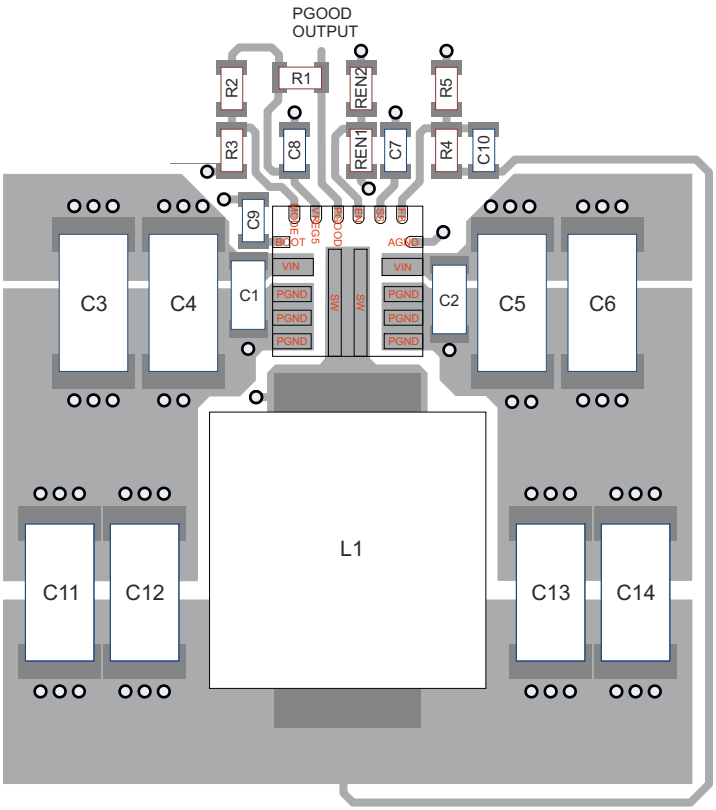

Figure 7-9. Top Side Layout

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Figure 7-10 shows the recommended layout for the first internal layer. The figure is comprised of a large PGND plane and a smaller ANGD island. AGND and PGND are connected at a single point to reduce circulating currents.

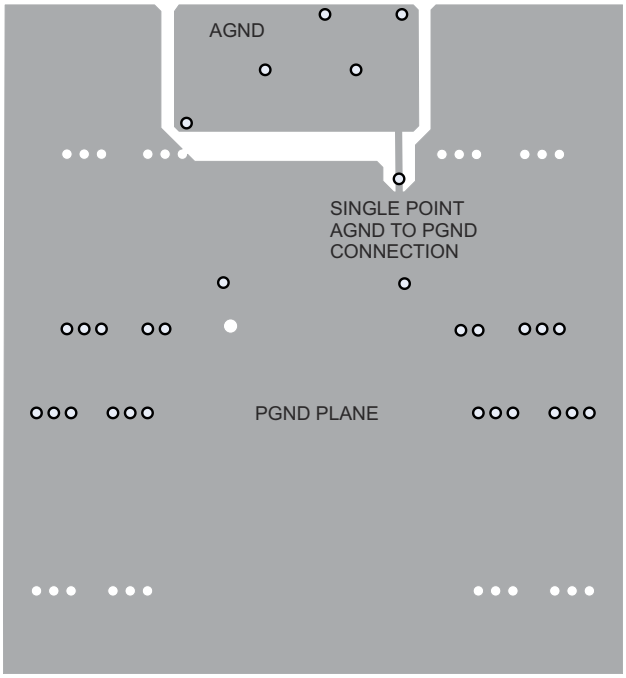

Figure 7-10. Mid Layer 1 Layout

Figure 7-11 shows the recommended layout for the second internal layer. The figure is comprised of a large PGND plane, a smaller copper fill area to connect the two top side V_{IN} copper areas and a second V_{OUT} copper fill area.

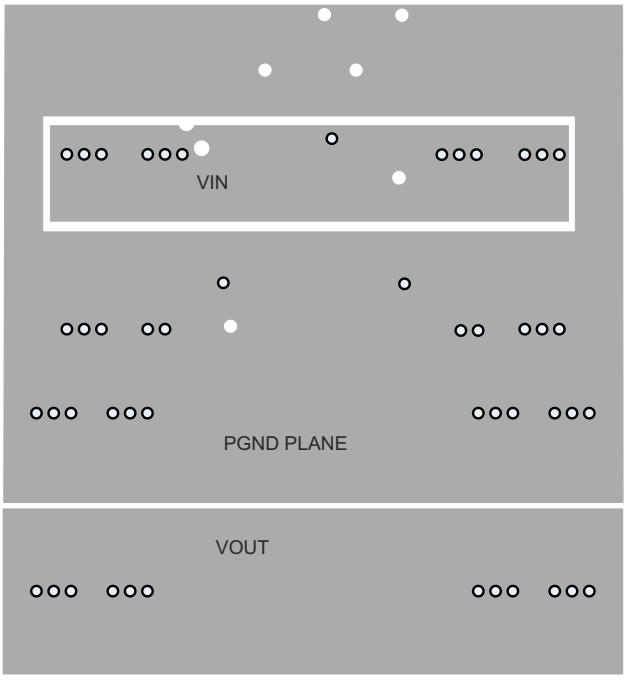

Figure 7-11. Mid Layer 2 Layout

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Figure 7-12 shows the recommended layout for the bottom layer. The figure is comprised of a large PGND plane and a trace to connect the BOOT capacitor to the SW node.

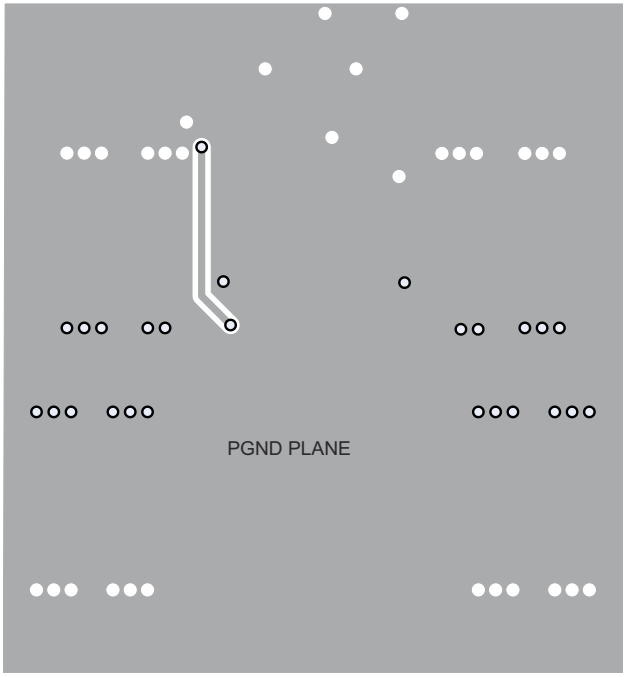

Figure 7-12. Bottom Layer Layout

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8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

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8.1.2 Development Support

The evaluation module for system validation in shown in Figure 8-1.

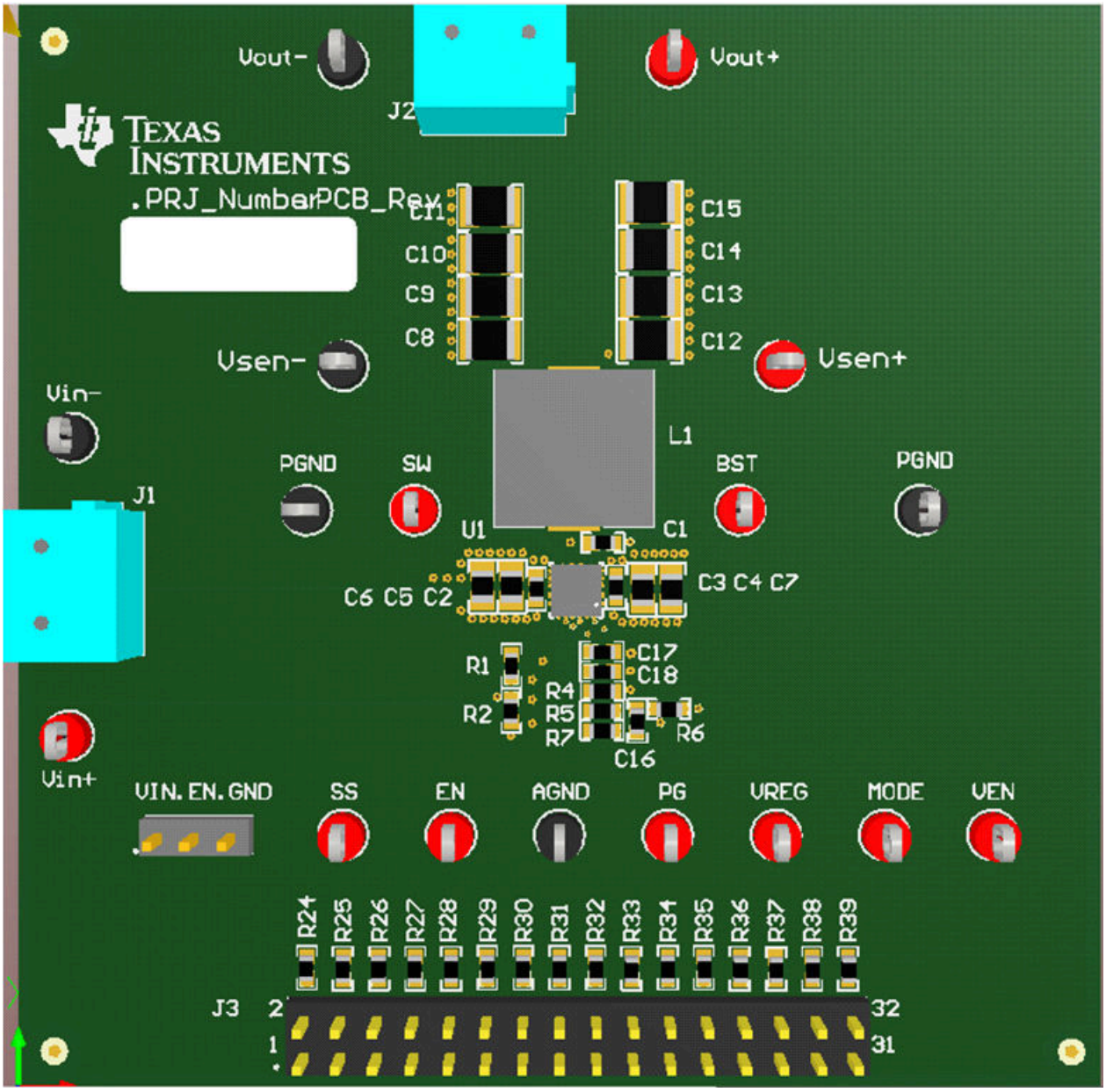

Figure 8-1. System Validation EVM Board

8.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS56C215 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (VIN), output voltage (VOUT), and output current (IOUT) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability. In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (August 2024) to Revision H (June 2025) **Page**

- Changed MOSFET values from 13.5mΩ and 4.5mΩ to 7.8mΩ and 3.2mΩ....1
- Added WEBENCH link in the *Features* 1
- Updated Efficiency vs Output Current figure to include the most recent data for the device....1
- Updated $R_{DS(on)H}$ from 13.5 mΩ to 7.8 mΩ , $R_{DS(on)L}$ from 4.5 mΩ to 3.2 mΩ and t_{UVPEN} hiccup time from 7 cycles to 14 cycles....5
- Changed I_{IN} typ value from 600µA to 146µA and deleted I_{IN} max value....5
- Changed I_{VINSDN} typ value from 7µA to 9.3µA....5
- Changed $V_{PGOODTH}$ VFB falling (good) value from 107% to 108%....5
- Changed V_{UVP} value from 68% to 70%....5
- Changed UVLO VREG5 rising voltage value from 4.3V to 4.25V....5
- Changed UVLO VREG5 falling voltage value from 3.57V to 3.52....5
- Changed UVLO, VREG5 = 4.7V VIN falling voltage, VREG5 = 4.7V value from 3.26V to 3.24V....5
- Changed UVLO, VREG5 = 4.7V VIN hysteresis, VREG5 = 4.7V value from 60mV to 80mV....5
- Changed t_{ON} min value from 54ns to 60ns....6
- Changed t_{SS} value from 1.045ms to 1.2ms....6
- Updated Figure 5-9 to Figure 5-34 to include the most recent data for the device....7
- Deleted High-side RDS(on) vs Temperature and Low-side RDS(on) vs Temperature figures....7
- Changes MOSFET values from 13.5-mΩ to 7.8-mΩ and 4.5-mΩ to 3.2-mΩ....13
- Changed "Zero Location" values in Table 6-1 from 7.1 to 17.8, from 14.3 to 27.1, from 21.4 to 29.8....14
- Changed wait time from 1 ms to 1 × t_{SS} and hiccup time from 7ms to 14 × t_{SS} 19
- Added the *Transient Response Enhancement* section....20
- Added *Custom Design With WEBENCH® Tools* section....21
- Updated *Application Curves* to include the most recent data for the device....24
- Added *Custom Design With WEBENCH® Tools* section....30

Changes from Revision F (August 2023) to Revision G (August 2024) **Page**

- Changed description "TI's smallest" to "a small" with updated products portfolio. 1
- Deleted $T_{SDN\ VREG5}$ spec....5
- Added note "Specified by design" for the SW On Time parameter....6
- Removed Out-of-Bounds Operation section....14
- Updated Thermal Shutdown section....20

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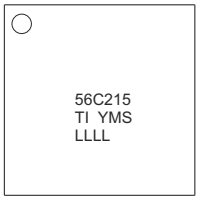
10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Package Marking



TI = TI Letters
YM = Year Month Date Code
S = Assembly Site Code
LLLL = Assembly Lot Code

Y : Year Code (1, 2, 3, 4, 5, 6, 7, 8, 9, 0)
M : Month Code (1, 2, 3, 4, 5, 6, 7, 8, 9, 0, A, B, C)

Figure 10-1. Symbolization

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS56C215RNNR	Active	Production	VQFN-HR (RNN) | 18	3000 | LARGE T&R	Yes	Call TI | Sn	Level-2-260C-1 YEAR	-40 to 125	56C215
TPS56C215RNNR.A	Active	Production	VQFN-HR (RNN) | 18	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	56C215
TPS56C215RNNT	Active	Production	VQFN-HR (RNN) | 18	250 | SMALL T&R	Yes	Call TI | Sn	Level-2-260C-1 YEAR	-40 to 125	56C215
TPS56C215RNNT.A	Active	Production	VQFN-HR (RNN) | 18	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	56C215

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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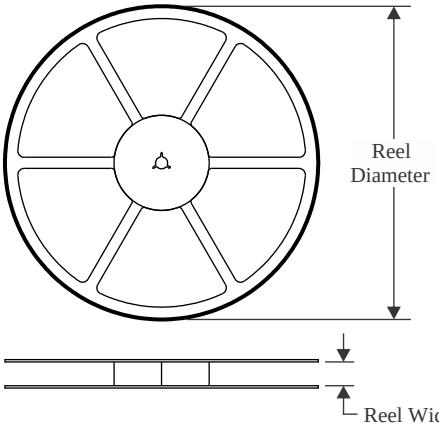
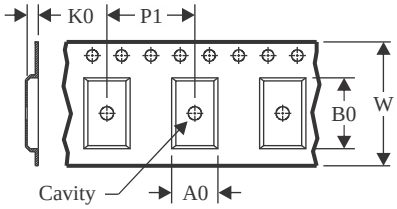
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

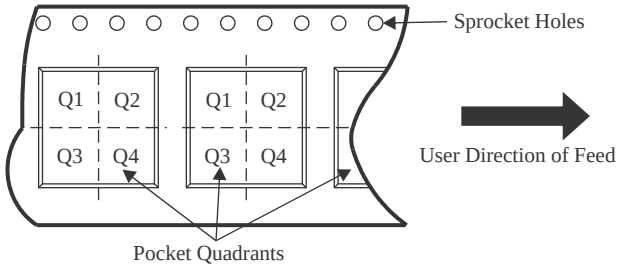


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

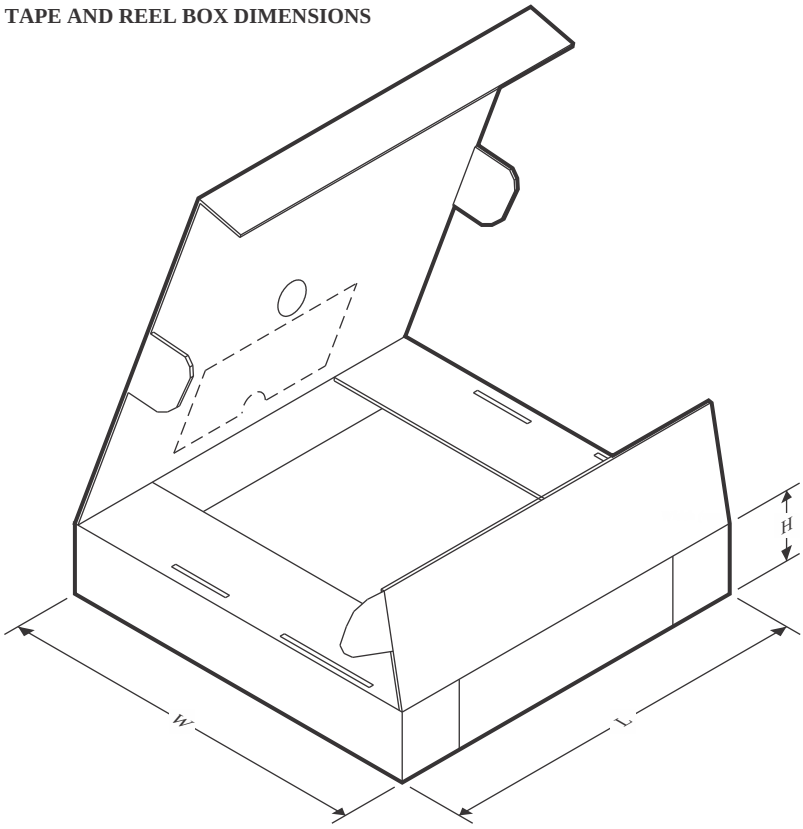
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS56C215RNNR	VQFN-HR	RNN	18	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TPS56C215RNNT	VQFN-HR	RNN	18	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TPS56C215RNNT	VQFN-HR	RNN	18	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

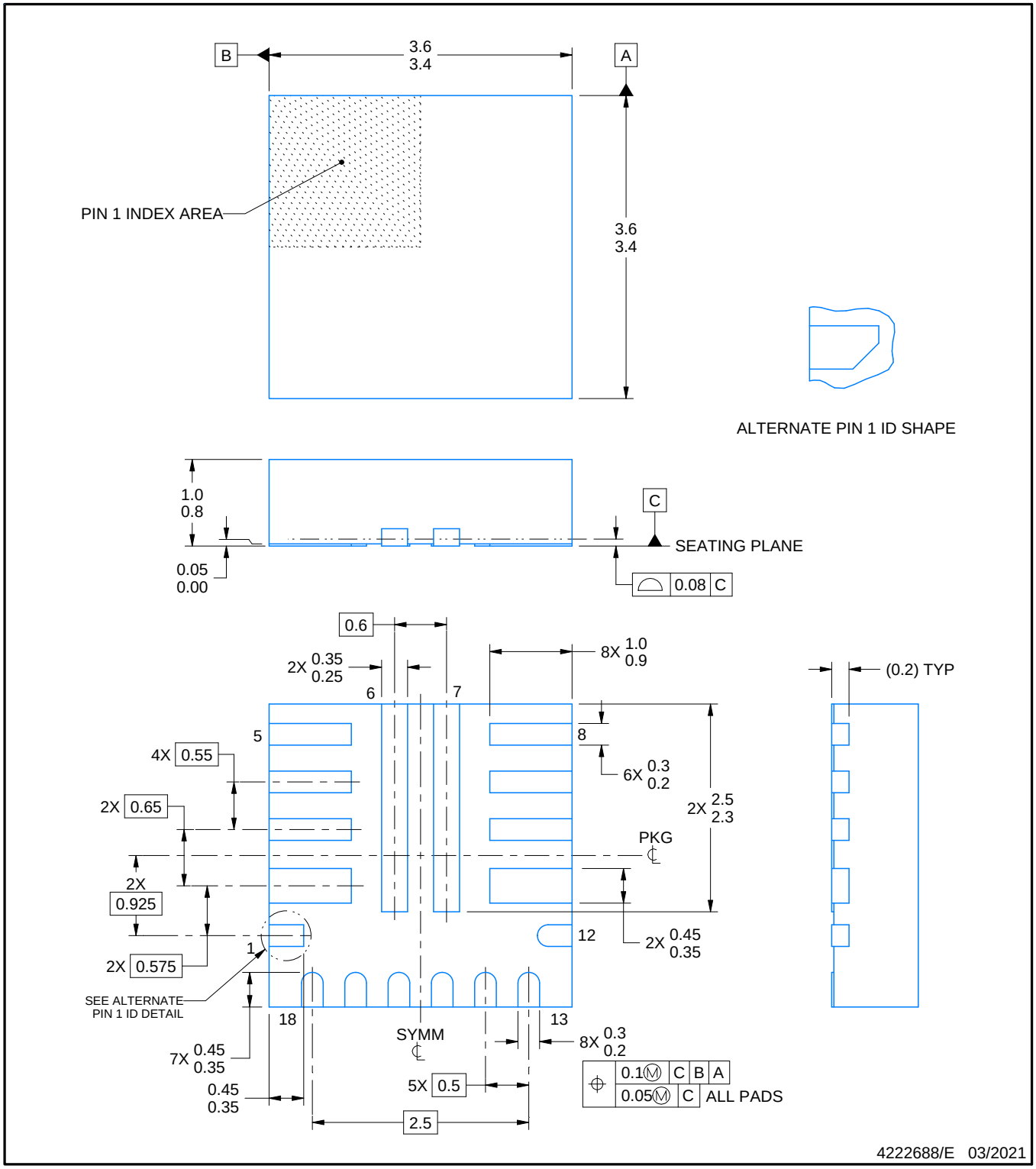
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS56C215RNNR	VQFN-HR	RNN	18	3000	367.0	367.0	35.0
TPS56C215RNNT	VQFN-HR	RNN	18	250	210.0	185.0	35.0
TPS56C215RNNT	VQFN-HR	RNN	18	250	213.0	191.0	35.0

PACKAGE OUTLINE

RNN0018A

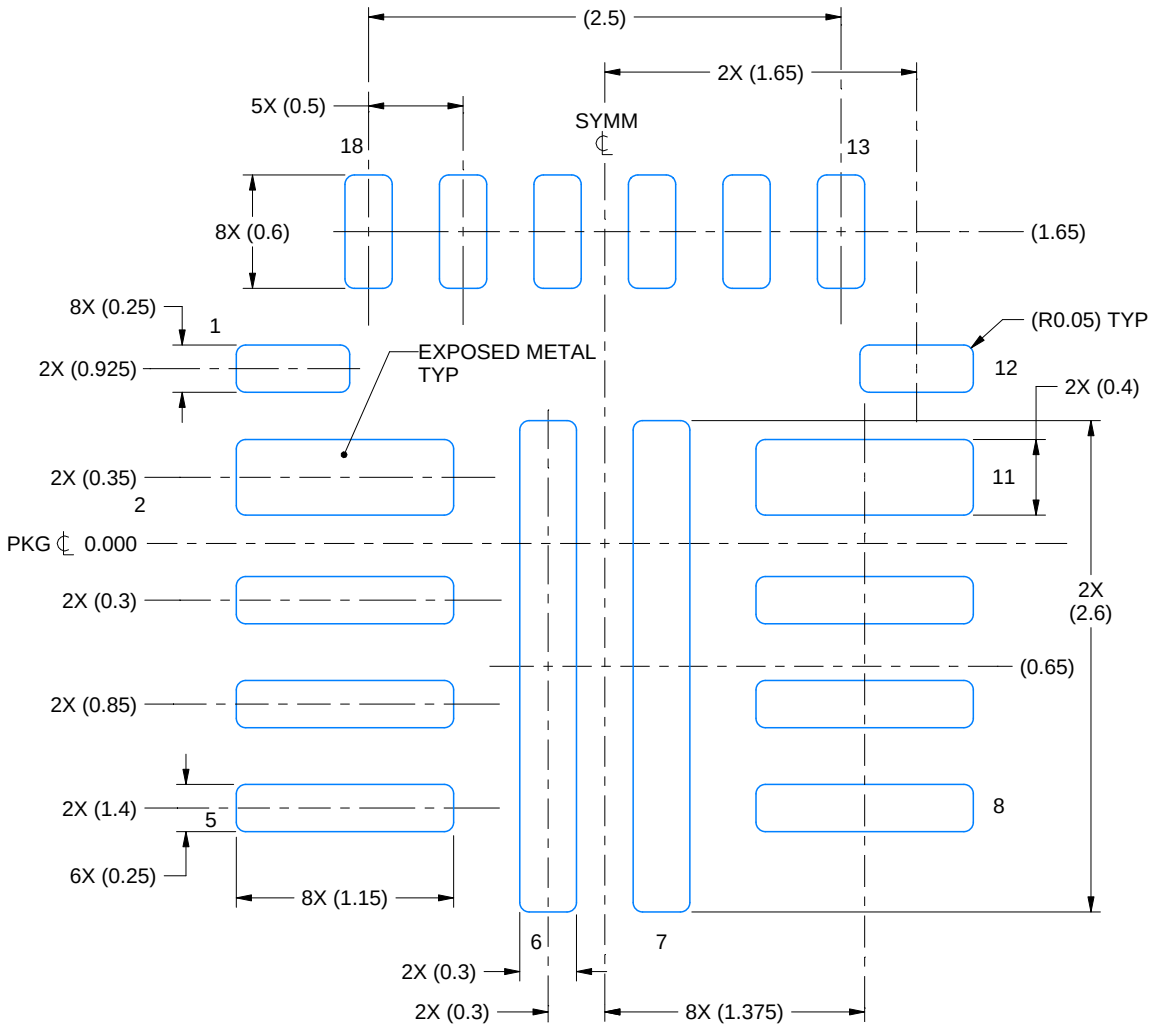
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

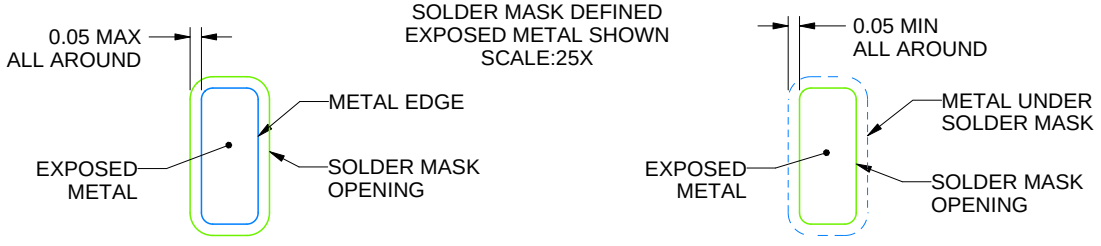


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
EXPOSED METAL SHOWN
SCALE:25X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

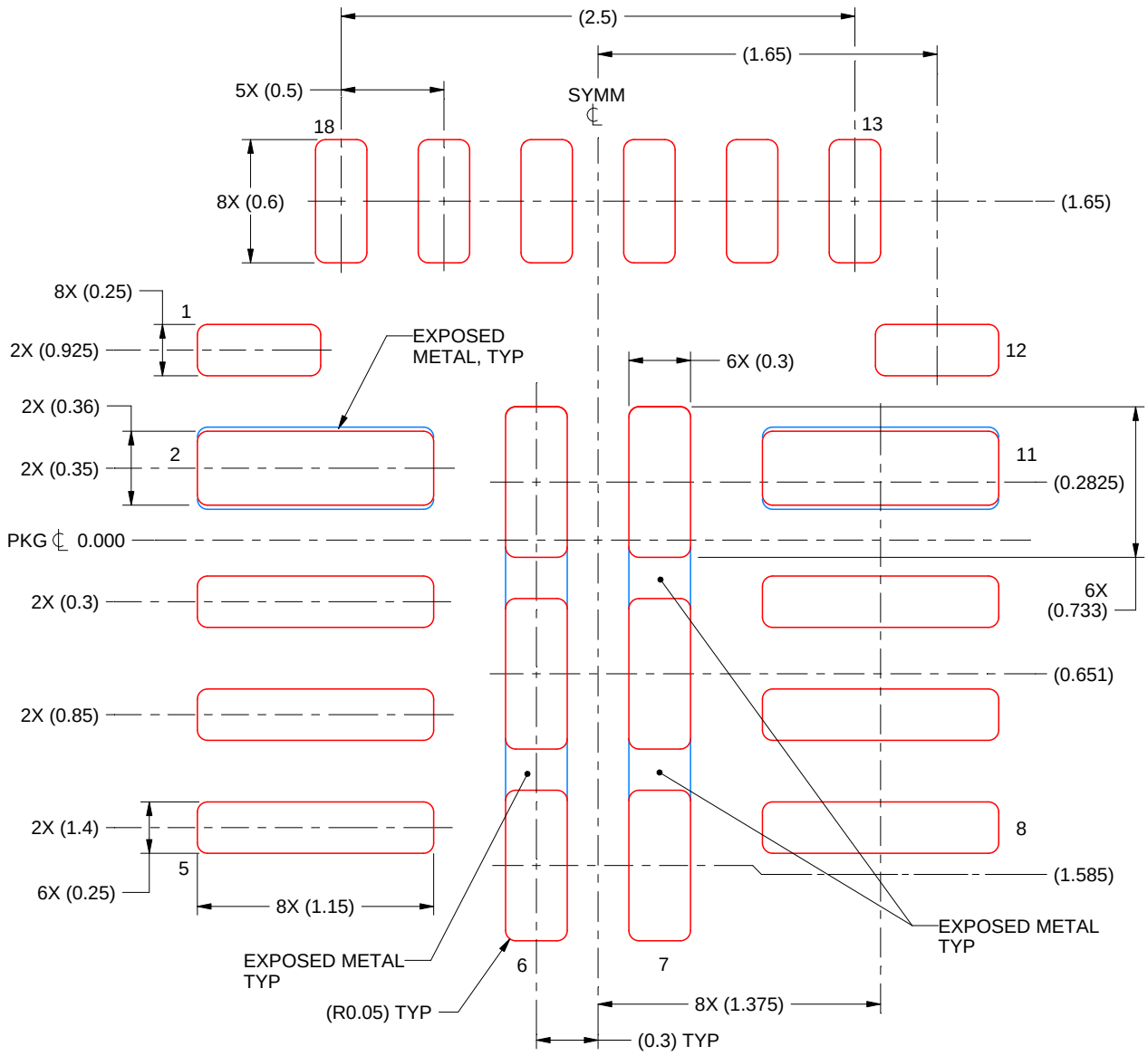
3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

RNN0018A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 6 & 7: 83% - PADS 2 & 11: 90%
SCALE:30X

4222688/E 03/2021

NOTES: (continued)

5. For alternate stencil design recommendations, see IPC-7525 or board assembly site preference.

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