TPS61378-Q1 25-µA Quiescent Current Synchronous Boost Converter with Load Disconnect

1 Features
- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
- Input voltage range: 2.3 V to 14 V
- Programmable output voltage range: 4.0 V to 18.5 V
- 5 V, 5.25 V, 5.5 V fixed output options
- Programmable switching frequency: 200 kHz to 2.2 MHz
- Programmable switch peak current limit: 1 A to 4.8 A
- 25-µA Quiescent current into VIN pin
- 0.5-µA Shutdown current into VIN pin
- ±1.5% Reference voltage accuracy
- Spread spectrum frequency modulation
- Selectable auto PFM and forced PWM mode
- True load disconnect during shutdown
- Support VIN close VOUT operation
- Input under-voltage lockout and output over-voltage protection
- Hiccup output short circuit protection
- Power good indicator
- Higher than 90% efficiency under 0.8-A load from 3.3-V to 9-V conversion
- Thermal shutdown protection at 175°C
- 3-mm x 3-mm 16-pin QFN package

2 Applications
- Advanced driver-assistance system (ADAS)
- Automotive infotainment and cluster
- Body electronics and lighting
- Emergency call (E-call)

3 Description
The TPS61378-Q1 is a fully-integrated synchronous boost converter with load disconnect function integrated. The device is suitable as a post-boost for automotive applications with a programmable current limit up to 4.8-A and maximum 18.5 V output voltage. It supports an input voltage from 2.3 V to 14 V and 25-µA low quiescent current.

The TPS61378-Q1 employs the peak current-mode control with the switching frequency programmable from 200 kHz to 2.2 MHz. In medium to heavy load, the TPS61378-Q1 works in fixed frequency PWM operation with the frequency set by an external resistor. In light load, the TPS61378-Q1 offers two optional modes: Auto PFM or Forced PWM which is configured by the mode pin externally. In Auto PFM mode, the switching frequency is lowered at light load to improve the efficiency. In Forced PWM mode, the switching frequency is kept constant across the entire load range. The switching frequency can be synchronized to an external clock. The TPS61378-Q1 uses the spread spectrum of the internal clock to optimize the EMI performance if the device is configured in Forced PWM mode. In addition, there is an internal soft-start time to limit the inrush current.

The TPS61378-Q1 also has robust protection features including the output short protection, output over voltage and thermal shutdown protection. The TPS61378-Q1 is available in a 3-mm x 3-mm 16-pin QFN package with wettable flank.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS61378QRTE</td>
<td>VQFN-16</td>
<td>3.0-mm x 3.0-mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
Table of Contents

1 Features .................................................................. 1
2 Applications ........................................................... 1
3 Description ............................................................. 1
4 Revision History ..................................................... 2
5 Device Comparison Table ........................................ 3
6 Pin Configuration and Functions ............................... 3
7 Specifications ........................................................ 5
  7.1 Absolute Maximum Ratings ................................. 5
  7.2 ESD Ratings ....................................................... 5
  7.3 Recommended Operating Conditions ..................... 5
  7.4 Thermal Information ........................................... 6
  7.5 Electrical Characteristics ..................................... 6
  7.6 Typical Characteristics ........................................ 8
8 Detailed Description ................................................ 9
  8.1 Overview .......................................................... 9
  8.2 Functional Block Diagrams ................................. 10
8.3 Feature Description .............................................. 10
9 Application and Implementation ............................. 14
  9.1 Application Information ...................................... 14
  9.2 Typical Application ........................................... 14
10 Power Supply Recommendations ......................... 21
11 Layout ............................................................... 22
  11.1 Layout Guidelines ............................................ 22
  11.2 Layout Example ............................................... 22
12 Device and Documentation Support ....................... 23
  12.1 Device Support ............................................... 23
  12.2 Receiving Notification of Documentation Updates .... 23
  12.3 Support Resources .......................................... 23
  12.4 Trademarks ..................................................... 23
  12.5 Electrostatic Discharge Caution ......................... 23
  12.6 Glossary ........................................................ 23
13 Mechanical, Packaging, and Orderable Information .... 23

4 Revision History

<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>May 2020</td>
<td>*2</td>
<td>Second Release of Advance Information</td>
</tr>
<tr>
<td>April 2020</td>
<td></td>
<td>Advance Information release.</td>
</tr>
</tbody>
</table>
5  Device Comparison Table

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>Output Voltage (V)</th>
<th>Resistor from FB to GND (R_FB_LOW)</th>
<th>Spread Spectrum</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS61378-Q1</td>
<td>5</td>
<td>R_FB_LOW ≤ 2 kΩ</td>
<td>Enable</td>
</tr>
<tr>
<td></td>
<td>5.25</td>
<td>2 kΩ &lt; R_FB_LOW ≤ 4 kΩ</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5.5</td>
<td>4 kΩ &lt; R_FB_LOW ≤ 8 kΩ</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Adjustable</td>
<td>R_FB_LOW ≥ 16 kΩ</td>
<td></td>
</tr>
<tr>
<td>TPS613781-Q1(1)</td>
<td>5.7</td>
<td>R_FB_LOW ≤ 2 kΩ</td>
<td>Enable</td>
</tr>
<tr>
<td>TPS613782-Q1(1)</td>
<td>6.2</td>
<td>2 kΩ &lt; R_FB_LOW ≤ 4 kΩ</td>
<td>Enable</td>
</tr>
<tr>
<td>TPS613783-Q1(1)</td>
<td>7</td>
<td>4 kΩ &lt; R_FB_LOW ≤ 8 kΩ</td>
<td></td>
</tr>
<tr>
<td></td>
<td>8</td>
<td>R_FB_LOW ≥ 16 kΩ</td>
<td></td>
</tr>
<tr>
<td></td>
<td>9</td>
<td>R_FB_LOW ≤ 2 kΩ</td>
<td>Enable</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>2 kΩ &lt; R_FB_LOW ≤ 4 kΩ</td>
<td>Enable</td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>4 kΩ &lt; R_FB_LOW ≤ 8 kΩ</td>
<td></td>
</tr>
<tr>
<td></td>
<td>12</td>
<td>R_FB_LOW ≥ 16 kΩ</td>
<td></td>
</tr>
<tr>
<td>TPS613784-Q1(1)</td>
<td>5</td>
<td>R_FB_LOW ≤ 2 kΩ</td>
<td>Disable</td>
</tr>
<tr>
<td></td>
<td>5.25</td>
<td>2 kΩ &lt; R_FB_LOW ≤ 4 kΩ</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5.5</td>
<td>4 kΩ &lt; R_FB_LOW ≤ 8 kΩ</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Adjustable</td>
<td>R_FB_LOW ≥ 16 kΩ</td>
<td></td>
</tr>
</tbody>
</table>

(1) Product Preview. Contact TI factory for more information.

6  Pin Configuration and Functions

RTE Package
16-Pin WQFN
Transparent Top View

Exposed Thermal Pad

Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>NAME</th>
<th>NO.</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>I</td>
<td>VIN</td>
<td>1</td>
<td>IC power supply input</td>
</tr>
<tr>
<td>2</td>
<td>I</td>
<td>BST</td>
<td>2</td>
<td>Power supply for high-side N-MOSFET gate driver. A capacitor must be connected between this pin and SW pin.</td>
</tr>
<tr>
<td>3,4</td>
<td>PWR</td>
<td>SW</td>
<td>3,4</td>
<td>The switching node pin of the converter. It is connected to the drain of the internal low-side FET and the source of the high-side FET.</td>
</tr>
</tbody>
</table>
## Pin Functions (continued)

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAME</td>
<td>NO.</td>
<td>DESCRIPTION</td>
</tr>
<tr>
<td>MODE/SYNC</td>
<td>5</td>
<td>Mode selection pin. MODE = High, Forced PWM mode. MODE = Low or left floating, Auto PFM Mode. This pin can also be used to synchronize the external clock. Refer to Table 1 for details.</td>
</tr>
<tr>
<td>VCC</td>
<td>6</td>
<td>Output of internal regulator. A ceramic capacitor with more than 1uF must be connected between this pin and GND.</td>
</tr>
<tr>
<td>GND</td>
<td>7, 8</td>
<td>Power ground of the IC. It is connected to the source of the low-side FET.</td>
</tr>
<tr>
<td>VO</td>
<td>9</td>
<td>Isolation power FET is between this pin and OUT pin. Connect load to this pin to achieve input/output isolation</td>
</tr>
<tr>
<td>OUT</td>
<td>10</td>
<td>Boost converter output.</td>
</tr>
<tr>
<td>PG</td>
<td>11</td>
<td>Power good indicator, open drain output.</td>
</tr>
<tr>
<td>ILIM</td>
<td>12</td>
<td>Current limit setting pin. Use a resistor to set the desired peak current limit. Refer to Adjustable Peak Current Limit for details.</td>
</tr>
<tr>
<td>FB</td>
<td>13</td>
<td>Feedback pin. Use a resistor divider to set the desired output voltage. Refer to Programming the Output Voltage for details.</td>
</tr>
<tr>
<td>COMP</td>
<td>14</td>
<td>Output of the internal trans-conductance error amplifier. An external RC network is connected to this pin for optimizing the loop stability and response time.</td>
</tr>
<tr>
<td>EN</td>
<td>15</td>
<td>Enable logic input.</td>
</tr>
<tr>
<td>FREQ</td>
<td>16</td>
<td>Frequency setting pin. Connect a resistor between this pin and GND pin to set the desired frequency. Customer can also use an external signal to set the switching frequency between 200-kHz and 2.2-MHz. Refer to Switching Frequency Setting for details.</td>
</tr>
<tr>
<td>Thermal Pad</td>
<td>-</td>
<td>The thermal pad should be connected to power ground plane for good power dissipation.</td>
</tr>
</tbody>
</table>
7 Specifications

**NOTICE**

The pre-production samples with PTPS61378QWRTERQ1 orderable part number (top marking: X378Q) have following specification differences with the production units:(1)

- Peak switching current limit at soft start and short circuit is changed to 0.9A typical vs 1.2A typical
- Typical soft start time is changed to 2.5ms
- Hiccup on time is changed to 2ms typical, while hiccup off time remains unchanged

All other functions of the converter can be evaluated.

Production unit samples will be available in 3Q20.

For detailed information, contact bcs_request_TPS61378@list.ti.com

(1) See Electrical Characteristics table

### 7.1 Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted)(1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>-0.3</td>
<td>16</td>
<td>V</td>
</tr>
<tr>
<td>VO, SW, OUT</td>
<td>-0.3</td>
<td>23</td>
<td>V</td>
</tr>
<tr>
<td>BST</td>
<td>-0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>MODE, FB, PG, FREQ / SYNC, ILIMIT, VCC, COMP, EN</td>
<td>-0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>TJ</td>
<td>-40</td>
<td>175</td>
<td>°C</td>
</tr>
<tr>
<td>Tstg</td>
<td>-65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

### 7.2 ESD Ratings

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;(ESD)&lt;/sub&gt; (1)</td>
<td>Electrostatic discharge</td>
<td>Human-body model (HBM), per AEC Q100-002 (2)</td>
<td>±2000</td>
</tr>
<tr>
<td>V&lt;sub&gt;(ESD)&lt;/sub&gt; (1)</td>
<td>Electrostatic discharge</td>
<td>Charged-device model (CDM), per AEC Q100-011, all pins (3)</td>
<td>±500</td>
</tr>
<tr>
<td>V&lt;sub&gt;(ESD)&lt;/sub&gt; (1)</td>
<td>Electrostatic discharge</td>
<td>Charged-device model (CDM), per AEC Q100-011, corner pins (1,4,5,8,9,12,13,16) (3)</td>
<td>±750</td>
</tr>
</tbody>
</table>

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

### 7.3 Recommended Operating Conditions over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>2.3</td>
<td>14</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOUT</td>
<td>3.0</td>
<td>18.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>TA</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

(1) See Electrical Characteristics table
7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TPS61378-Q1</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{JA}</td>
<td>46.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>R_{JC(top)}</td>
<td>43.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>R_{JC(bot)}</td>
<td>18.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>ψ_{JT}</td>
<td>1.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>ψ_{JB}</td>
<td>18.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>R_{JCQV0}</td>
<td>8.8</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

7.5 Electrical Characteristics

T_{J} = -40 to 125°C, V_{IN} = 3.3 V and V_{OUT} = 9 V (V{O pin}). Typical values are at T_{J} = 25°C, (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{IN}</td>
<td>Input voltage range</td>
<td>2.3</td>
<td>14</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_{IN,UVLO}</td>
<td>VIN under voltage lockout threshold</td>
<td>V_{IN} rising</td>
<td>2.1</td>
<td>2.3</td>
<td>V</td>
</tr>
<tr>
<td>V_{IN,HYS}</td>
<td>VIN UVLO hysteresis</td>
<td>150</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{CC,UVLO}</td>
<td>VCC UVLO threshold</td>
<td>V_{CC} rising</td>
<td>2.2</td>
<td>2.4</td>
<td>V</td>
</tr>
<tr>
<td>V_{CC,HYS}</td>
<td>VCC UVLO hysteresis</td>
<td>150</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{CC}</td>
<td>VCC regulation</td>
<td>4.8</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{Q}</td>
<td>Quiescent current into V_{IN} pin</td>
<td>IC enabled, no load, V_{IN} = 3.3 V, V_{OUT} = 18.5 V, V_{FB} = V_{REF} + 0.1 V</td>
<td>25</td>
<td>35</td>
<td>µA</td>
</tr>
<tr>
<td>I_{Q}</td>
<td>Quiescent current into OUT pin</td>
<td>IC enabled, no load, V_{IN} = 3.3 V, V_{OUT} = 18.5 V, V_{FB} = V_{REF} + 0.1 V</td>
<td>10</td>
<td>35</td>
<td>µA</td>
</tr>
<tr>
<td>I_{SD}</td>
<td>Shutdown current into VIN pin</td>
<td>IC disabled, V_{IN} = 14 V, EN = GND</td>
<td>0.5</td>
<td>5</td>
<td>µA</td>
</tr>
<tr>
<td>I_{SW,LKG}</td>
<td>Reverse leakage current into SW</td>
<td>IC disabled, V_{IN} = 5 V, OUT = SW = 18.5 V, VO = 0</td>
<td>5</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>I_{VO,LKG}</td>
<td>Reverse leakage current into VO</td>
<td>IC disabled, OUT = VO = 5 V, SW = 0</td>
<td>5</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>V_{OUT}</td>
<td>Output voltage range</td>
<td>Freq = 2200 kHz</td>
<td>4.0</td>
<td>18.5</td>
<td>V</td>
</tr>
<tr>
<td>V_{OPP}</td>
<td>Output over-voltage protection threshold</td>
<td>V_{IN} = 3.3 V, V_{OUT} rising</td>
<td>19.5</td>
<td>20</td>
<td>20.5</td>
</tr>
<tr>
<td>V_{OPP,HYS}</td>
<td>Output over-voltage protection hysteresis</td>
<td>V_{IN} = 3.3 V, OVP threshold</td>
<td>0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_{REF}</td>
<td>Reference Voltage at FB pin</td>
<td>T_{J} = -40 to 125°C, FB to GND resistance ≥ 16 kΩ</td>
<td>0.788</td>
<td>0.8</td>
<td>0.812</td>
</tr>
<tr>
<td>V_{OUT,5V}</td>
<td></td>
<td>T_{J} = -40 to 125°C, R_{FB} = 2.0 kΩ</td>
<td>4.920</td>
<td>5.000</td>
<td>5.080</td>
</tr>
<tr>
<td>V_{OUT,5.25V}</td>
<td></td>
<td>T_{J} = -40 to 125°C, R_{FB} = 4.0 kΩ</td>
<td>5.148</td>
<td>5.238</td>
<td>5.328</td>
</tr>
<tr>
<td>V_{OUT,5.5V}</td>
<td></td>
<td>T_{J} = -40 to 125°C, R_{FB} = 8.0 kΩ</td>
<td>5.410</td>
<td>5.500</td>
<td>5.590</td>
</tr>
<tr>
<td>I_{FB,LKG}</td>
<td>Leakage current into FB pin</td>
<td>50</td>
<td>nA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_{DS(th)}</td>
<td>Low-side MOSFET on resistance</td>
<td>V_{CC} = 4.85 V</td>
<td>50</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>R_{DS(iso)}</td>
<td>Isolation MOSFET on resistance</td>
<td>V_{CC} = 4.85 V</td>
<td>100</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>R_{DS(iso)}</td>
<td>High-side MOSFET on resistance</td>
<td>V_{CC} = 4.85 V</td>
<td>50</td>
<td>mΩ</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CURRENT LIMIT</th>
<th>T_{J} = -40 to 125°C, Duty cycle = 90%</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_{LIM,SW}</td>
<td>P_{LIM} = 20 kW, Duty cycle = 90%</td>
</tr>
<tr>
<td>I_{LIM,SW}</td>
<td>3.8</td>
</tr>
<tr>
<td>I_{LIM,SW}</td>
<td>P_{LIM} = 20 kW, Duty cycle = 90%</td>
</tr>
<tr>
<td>I_{LIM,SW}</td>
<td>3.8</td>
</tr>
<tr>
<td>I_{LIM,SW}</td>
<td>P_{LIM} = 100 kW, Duty cycle = 90%</td>
</tr>
<tr>
<td>I_{LIM,SW}</td>
<td>0.8</td>
</tr>
<tr>
<td>I_{LIM,SW}</td>
<td>P_{LIM} = 100 kW, Duty cycle = 90%</td>
</tr>
<tr>
<td>I_{LIM,SW}</td>
<td>0.8</td>
</tr>
<tr>
<td>I_{LIM,SW}</td>
<td>P_{LIM} = 20 kW</td>
</tr>
<tr>
<td>I_{LIM,SW}</td>
<td>0.96</td>
</tr>
<tr>
<td>I_{LIM,SW}</td>
<td>P_{LIM} = 20 kW</td>
</tr>
<tr>
<td>I_{LIM,SW}</td>
<td>0.24</td>
</tr>
</tbody>
</table>

(1) Peak switching current limit at soft start and short circuit is changed to 0.9A typical vs 1.2A typical for the PTPS61378QWRTERQ1.
Electrical Characteristics (continued)

\( T_J = -40 \text{ to } 125°C, \ V_{IN} = 3.3 \text{ V and } V_{OUT} = 9 \text{ V (VO pin). Typical values are at } T_J = 25°C, \text{ (unless otherwise noted)} \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SWITCHING FREQUENCY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( F_{SW} )</td>
<td>Switching frequency</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( R_{FREQ} = 18 \text{ kΩ} )</td>
<td>2000</td>
<td>2200</td>
<td>2400</td>
<td>kHz</td>
</tr>
<tr>
<td>( F_{SW} )</td>
<td>Switching frequency</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( R_{FREQ} = 200 \text{ kΩ} )</td>
<td>180</td>
<td>200</td>
<td>220</td>
<td>kHz</td>
</tr>
<tr>
<td>( D_{MAX} )</td>
<td>Maximum Duty Cycle</td>
<td></td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>( R_{FREQ} = 18 \text{ kΩ} )</td>
<td>80</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( F_{DITHER} )</td>
<td></td>
<td>10%</td>
<td></td>
<td></td>
<td>Fsw</td>
</tr>
<tr>
<td>( F_{DITHER} )</td>
<td></td>
<td>0.39%</td>
<td></td>
<td></td>
<td>Fsw</td>
</tr>
<tr>
<td><strong>ERROR AMPLIFIER</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{SINK} )</td>
<td>COMP pin sink current</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{FB}=V_{REF} + 0.2V, \ V_{COMP}=1.2V )</td>
<td>6</td>
<td></td>
<td></td>
<td>uA</td>
</tr>
<tr>
<td>( I_{SOURCE} )</td>
<td>COMP pin source current</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{FB}=V_{REF} - 0.2V, \ V_{COMP}=1.2V )</td>
<td>6</td>
<td></td>
<td></td>
<td>uA</td>
</tr>
<tr>
<td>( V_{OCCLPH} )</td>
<td>COMP pin high clamp voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{FB}=V_{REF} - 0.2V, \ ILIM = 4.8 \text{ A} )</td>
<td>1.25</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{OCCLPL} )</td>
<td>COMP pin high low voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{FB}=V_{REF} + 0.2V, )</td>
<td>0.6</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( G_{MEA} )</td>
<td>Error amplifier trans conductance</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{COMP} = 1.0 \text{ V} )</td>
<td>70</td>
<td></td>
<td></td>
<td>uS</td>
</tr>
<tr>
<td>( V_{PG, TH} )</td>
<td>PG threshold for rising FB voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>90%</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{PG, HYS} )</td>
<td>PG hysteresis</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>5%</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{PG, DELAY} )</td>
<td>PG delay time</td>
<td>2</td>
<td>4</td>
<td>TBD</td>
<td>ms</td>
</tr>
<tr>
<td>( t_{PG, SINK} )</td>
<td>PG pin sink current capability</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{PG} = 0.4 \text{ V} )</td>
<td>10</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td><strong>DOWN MODE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( f_{SYNC, MIN} )</td>
<td></td>
<td>200</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>( f_{SYNC, MAX} )</td>
<td></td>
<td>2200</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>( t_{EN, DELAY} )</td>
<td>Delay time between EN high and device working</td>
<td>0.7</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>( t_{ISS} )</td>
<td>Softstart time</td>
<td>2(2)</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>( t_{HCP, ON} )</td>
<td>Hiccup on time</td>
<td>4(3)</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>( t_{HCP, OFF} )</td>
<td>Hiccup off time</td>
<td>70</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td><strong>EN / SYNC LOGIC</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{H} )</td>
<td>EN, MODE/SYNC pins Logic high threshold</td>
<td>1.2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{L} )</td>
<td>EN, MODE/SYNC pins Logic Low threshold</td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( R_{DOWN} )</td>
<td>EN, MODE/SYNC pins internal pull down resistor</td>
<td>800</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td><strong>THERMAL SHUTDOWN</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{IDR} )</td>
<td>Thermal shutdown rising threshold</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( TJ \text{ rising} )</td>
<td>175</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>( t_{IDF} )</td>
<td>Thermal shutdown falling threshold</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( TJ \text{ falling} )</td>
<td>155</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

(2) Typical soft start time is changed to 2.5ms for the PTPS61378QWRTERQ1 orderable part
(3) Hiccup on time is changed to 2ms typical, while hiccup off time remain unchanged for the PTPS61378QWRTERQ1 orderable part
7.6 Typical Characteristics

Figure 1. Efficiency vs Output Current

Figure 2. Load regulation
8 Detailed Description

8.1 Overview

The TPS61378-Q1 is a fully integrated synchronous boost converter with load disconnect function. It supports output voltage up to 18.5 V with maximum 4.8 A programmable switching peak current limit. The input voltage ranges from 2.3 V to 14 V while consuming 25-µA quiescent current.

The TPS61378-Q1 utilizes fixed frequency peak current control scheme, which has an internal oscillator and supports adjustable switching frequency from 200 kHz to 2.2 MHz.

The TPS61378-Q1 operates with fixed frequency pulse width modulation (PWM) from medium to heavy load. At the beginning of each switching cycle, the low-side N-MOSFET switch is turned on, and the inductor current ramps up to a peak current that is determined by the output of the internal error amplifier (EA). Once the switching peak current triggers the output of the EA, the low-side N-MOSFET is turned off and the high-side N-MOSFET is turned on after a short dead time. The high-side N-MOSFET switch is not turned off until the next cycle as determined by the internal oscillator. The low-side switch turns on again after a short dead time and the switching cycle is repeated.

The TPS61378-Q1 provides either Auto PFM or Forced PWM option for the light load operation by configuration of the MODE / SYNC pin. In Forced PWM mode, the switching frequency remains constant across the entire load range, which helps to avoid the frequency variation with load. The internal oscillator can be synchronized with an external clock applied to the MODE / SYNC pin. Spread spectrum modulation of the frequency in Forced PWM mode helps to optimize the EMI performance for automotive applications. In Auto PFM mode, the switching frequency may decreases resulting in higher efficiency.

The TPS61378-Q1 implements a cycle-by-cycle current limit to protect the device from overload during the boost operation phase. If the output current further increases and triggers the output voltage to fall below the input voltage, the TPS61378-Q1 enters into hiccup mode short protection.

There is a built-in soft start time which prevents the inrush current during the startup. The TPS61378-Q1 also provides a power good (PG) indicator to enable the power sequence control for startup.

The TPS61378-Q1 also has a number of protection features including output short protection, output over voltage protection (OVP), and thermal shutdown protection (OTP).
8.2 Functional Block Diagrams

![Functional Block Diagram](image)

Figure 3. Functional Block Diagram

8.3 Feature Description

8.3.1 VCC Power Supply

The internal LDO in the TPS61378-Q1 outputs a regulated voltage of 4.8 V with 10 mA output current capability. A ceramic capacitor is connected between the VCC pin and GND pin to stabilize the VCC voltage and also decouple the noise on the VCC pin. The value of this ceramic capacitor should be above 1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating higher than 10 V is recommended.

8.3.2 Input Undervoltage Lockout (UVLO)

An under-voltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the UVLO threshold of 2.15 V. A hysteresis of 150 mV is added so that the device cannot be enabled again until the input voltage exceeds 2.3 V. This function is implemented in order to prevent malfunctioning of the device when the input voltage is between 2.15 V and 2.3 V.
Feature Description (continued)

8.3.3 Enable and Soft Start
When the input voltage is above the UVLO threshold and the EN pin is pulled above 1.2 V. The TPS61378-Q1 is enabled. The TPS61378-Q1 starts to monitor the FB pin. With a typical 700 μs delay time after EN is pulled high, the TPS61378-Q1 starts switching. There is an internal built-in startup time which is typically 2 ms to limit the inrush current during startup.

8.3.4 Shut Down
When the input voltage is below the UVLO threshold or the EN pin is pulled low. The TPS61378-Q1 is in shutdown mode and all the functions are disabled. The input voltage is isolated from the output to minimize the leakage currents.

8.3.5 Switching Frequency Setting
The TPS61378-Q1 uses a fixed frequency control scheme and the switching frequency can be programmed between 200kHz and 2.2 MHz using a resistor from the FREQ pin to GND. The resistor also must be connected when the oscillator is synchronized by an external clock. The resistance is defined by the Equation 1

\[ R_{\text{FREQ}} = \frac{1}{K_{\text{FREQ}} \times F_{\text{SW}} \times C_{\text{FREQ}}} \]  

Where
- \( R_{\text{FREQ}} \) is the resistance between the FREQ pin and the GND pin
- \( C_{\text{FREQ}} \) is the internal capacitance, it’s 5 pF typically.
- \( K \) is the current ratio, which is 5 typically

For instance, the switching frequency is 2.2MHz if the resistance between the FREQ pin and GND is 18kΩ. This pin cannot be left floating or tied to VCC.

8.3.6 Spread Spectrum Frequency Modulation
The TPS61378-Q1 uses a triangle waveform to spread the switching frequency with ±10% of normal frequency. The frequency of the triangle waveform is typically 0.4% of the switching frequency. For example, if the normal switching frequency of TPS61378-Q1 is programmed to 2.2MHz, the spread spectrum function will modulate the switching frequency in the range of 1.98 MHz to 2.42 MHz in a triangle behavior with 8.5 kHz rate.

The spread spectrum is only available while the clock of the TPS61378-Q1 is free running at its natural frequency. Any of the following conditions overrides spread spectrum, turning it off:
- An external clock is applied to the MODE/SYNC pin
- The device works in the PFM operation at light load.
8.3.7 Adjustable Peak Current Limit

The TPS61378-Q1 adopts a cycle-by-cycle peak current limit internally. The low-side switch is turned off immediately as soon as the switch peak current triggers the limit threshold. The peak switch current limit can be set by a resistor from the ILIM pin to ground. The relationship between the current limit and the resistor is shown in Equation 2.

\[ I_{\text{ILIM}} = \frac{K}{R_{\text{ILIM}}} \] (2)

Where
- \( R_{\text{ILIM}} \) is the resistance between the ILIM pin and the GND pin
- \( I_{\text{ILIM}} \) is switch peak current limit.
- \( K \) is 96k typically.

For instance, the current limit is set to 4.8A if the \( R_{\text{ILIM}} \) is 20 k\( \Omega \); This pin cannot be left floating or connected to VCC.

8.3.8 Bootstrap

The TPS61378-Q1 has an integrated bootstrap regulator circuit. A small ceramic capacitor is needed between the BST pin and SW pin to provide the gate driving supply voltage for the high-side switch. The bootstrap capacitor is charged during the time when the low-side switch is in the ON state. The value of this ceramic capacitor should be above 0.1\( \mu \)F. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating higher than 6.3V is recommended.

8.3.9 Load Disconnect

The TPS61378-Q1 integrates a load disconnect function, which completely cut off the path between the input side and the output side during shutdown. The output disconnect function also allows the output short protection and minimize the inrush current at startup.

8.3.10 MODE/SYNC configuration

Table 1 summarizes the MODE/SYNC function and the entry condition.

<table>
<thead>
<tr>
<th>MODE/SYNC Pin Configuration</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Low</td>
<td>Auto PFM Mode</td>
</tr>
<tr>
<td>Logic High</td>
<td>Forced PWM Mode</td>
</tr>
<tr>
<td>External Synchronization</td>
<td>Forced PWM Mode</td>
</tr>
</tbody>
</table>

The TPS61378-Q1 could be synchronized to an external clock applied to the MODE / SYNC pin.

8.3.10.1 Forced PWM Mode

The TPS61378-Q1 enters Forced PWM Mode by pulling the MODE / SYNC pin to logic high for more than 5 switching cycles. In Forced PWM mode, the TPS61378-Q1 keeps the switching frequency constant at light load condition. When the load current decreases, the output of the internal error amplifier will also decrease to keep the inductor peak current down. When the output current decreases further, the high-side switch is not turned off even if the current of the high-side switch goes negative to keep the frequency constant.

8.3.10.2 Auto PFM Mode

The TPS61378-Q1 enters Auto PFM Mode by pulling the MODE/SYNC pin to logic low for more than 5 switching cycles or leave the pin floating. The TPS61378-Q1 improves the efficiency at light load when operating in PFM mode. When the output current decreases to a certain level, the output voltage of the error amplifier is clamped by the internal circuit. If the output current reduces further, the inductor through the high-side switch will be clamped but not further lowered. Pulses are skipped to improve the efficiency at light load.
8.3.10.3 External Clock Synchronization

The TPS61378-Q1 supports external clock synchronization with a range of 200 kHz to 2.2 MHz. The TPS61378-Q1 remains in the Forced PWM Mode and operates in CCM across the entire load range if the oscillator is synced by an external clock. External clock synchronization can also be achieved by varying the external clock if desired.

8.3.11 Over-voltage Protection (OVP)

If the output voltage exceeds the OVP threshold (typical 20 V), the TPS61378-Q1 stops switching immediately until the output voltage drops below the recovery threshold (typical 19.5 V). This function protects the device against excessive voltage.

8.3.12 Output Short Protection

In addition to the cycle-by-cycle current limit function, the TPS61378-Q1 also has the output short protection. If the output current is too high to pull the output voltage drops below the input voltage, the device enters into short circuit protection mode. In hiccup mode, the device limits the current to a relative lower level with 4ms and then shuts down. After 70 ms, it will restart. If the short condition disappears, the device will automatically restart.

8.3.13 Power Good Indicator

The TPS61378-Q1 integrates a power good indicator function. The PG pin asserts when the output voltage rises above 90% of the target output voltage. The PG pin is an open drain output before the VOUT reaches the 90% target output voltage. The PG pin becomes active low after a typical 4 ms delay time after the VOUT reaches 90% of the target output voltage. When the output voltage drops below 85% of the target output voltage, the PG logic goes low.

8.3.14 Thermal Shutdown

A thermal shutdown is implemented to prevent damage due to the excessive heat and power dissipation. Typically, the thermal shutdown occurs at the junction temperature exceeding 175°C. When the thermal shutdown is triggered, the device stops switching and recovers when the junction temperature falls below 155°C (typical).
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information
The TPS61378-Q1 is a 25-µA quiescent current boost converter which supports 2.3V to 14V input voltage range. It also supports load disconnect in order to minimize the leakage current. The following design procedure can be used to select component values for the TPS61378-Q1.

9.2 Typical Application

9.2.1 Design Requirements
A typical application example is dual cameras powered via a coax cable, which normally requires 9.0-V output as its bias voltage and consumes less than 600 mA current. The following design procedure can be used to select external component values for the TPS61378-Q1.

9.2.1.1 Detailed Design Procedure

9.2.1.1.1 Programming the Output Voltage
There are two ways to set the output voltage of the TPS61378-Q1, adjustable or fixed. If the resistance between FB and GND is higher than 16 kΩ during startup, the TPS61378-Q1 works as an adjustable output version. The FB pin is connected to the negative input of the internal error amplifier directly. The output voltage can be programmed by adjusting the external resistor divider \(R_{\text{upper}}\) and \(R_{\text{lower}}\) according to the equation . When the output voltage is in well regulation, the typical voltage at the FB pin is \(V_{\text{REF}}\) of 0.8 V.

\[
V_{\text{OUT}} = V_{\text{REF}} \times \frac{(R_{\text{upper}} + R_{\text{lower}})}{R_{\text{lower}}}
\]
Typical Application (continued)

For some application where the resistor needs to be as low as possible, the low side divider could be 20 kΩ. The reference voltage is 0.8 V, the high side divider is 205 kΩ for 9 V output voltage.

For other application without specific requirement on divider resistance, we can choose $R_{\text{down}}$ to be approximately 80.6 kΩ. Slightly increasing or decreasing $R_{\text{down}}$ can result in closer output voltage matching when using standard values.

For the best accuracy, $R_{\text{down}}$ is recommended to be smaller than 100 kΩ to ensure that the current following through $R_{\text{down}}$ is at least 100 times larger than FB pin leakage current. Changing $R_{\text{down}}$ towards the lower value increases the robustness against noise injection. Changing the $R_{\text{down}}$ to higher values reduces the quiescent current for achieving higher efficiency at light load.

If the resistance between FB and GND is less than 16 kΩ during startup, the TPS61378-Q1 works as a fixed output voltage version. The TPS61378-Q1 uses the internal resistor divider.

For the 5 V fixed output voltage, the FB pin can be connected to the GND directly or use a $R_{\text{lower}}$ with less than 2 kΩ resistance.

For the 5.25 V fixed output voltage, the $R_{\text{lower}}$ is between 2.0 kΩ and 4.0 kΩ and no $R_{\text{upper}}$ is needed.

For 5.5 V fixed output voltage, the $R_{\text{lower}}$ is between 4.0 kΩ and 8.0 kΩ and no $R_{\text{upper}}$ is needed.

9.2.1.1.2 Setting the Switching Frequency

The switching frequency of the TPS61378-Q1 is set at 2.2 MHz. Use to calculate the required resistor value. The calculated value is 18 kΩ to get the frequency of 2.2 MHz.

9.2.1.1.3 Setting the Current Limit

The current limit of the TPS61378-Q1 can be programmed by an external resistor. Use For a target current limit of 4.8 A, the calculated resistor value is 20 kΩ.

9.2.1.1.4 Selecting the Inductor

A boost converter normally requires two main passive components for storing the energy during the power conversion: an inductor and an output capacitor. The inductor affects the steady state efficiency (including the ripple and efficiency) as well as the transient behavior and loop stability, which makes the inductor to be the most critical component in application.

When selecting the inductor, as well as the inductance, the other parameters of importance are:

• The maximum current rating (RMS and peak current should be considered),
• The series resistance,
• Operating temperature

Choosing the inductor ripple current with the low ripple percentage of the average inductor current results in a larger inductance value, maximizes the converter’s potential output current and minimizes EMI. The larger ripple results in a smaller inductance value, and a physically smaller inductor, improves transient response but results in potentially higher EMI.

The rule of thumb to choose the inductor is to make the inductor ripple current ($\Delta I_L$) a certain percentage of the average current. The inductance can be calculated by Equation 4, Equation 5, and Equation 6:

$$\Delta I_L = \frac{V_{\text{IN}} \times D}{L \times f_{\text{SW}}}$$  \hspace{1cm} (4)

$$\Delta I_{L-R} = \text{Ripple\%} \times \frac{V_{\text{OUT}} \times I_{\text{OUT}}}{\eta \times V_{\text{IN}}}$$  \hspace{1cm} (5)

$$L = \frac{1}{\text{Ripple \%}} \times \frac{\eta \times V_{\text{IN}}}{V_{\text{OUT}} \times I_{\text{OUT}}} \times \frac{V_{\text{IN}} \times D}{f_{\text{SW}}}$$

where

• $\Delta I_L$ is the peak-peak inductor current ripple
• $V_{\text{IN}}$ is the input voltage
Typical Application (continued)

- D is the duty cycle
- L is the inductor
- \( f_{SW} \) is the switching frequency
- Ripple % is the ripple ratio versus the DC current
- \( V_{OUT} \) is the output voltage
- \( I_{OUT} \) is the output current
- \( \eta \) is the efficiency

The current flowing through the inductor is the inductor ripple current plus the average input current. During power-up, load faults, or transient load conditions, the inductor current can increase above the peak inductor current calculated.

Inductor values can have \( \pm 20\% \) or even \( \pm 30\% \) tolerance with no current bias. When the inductor current approaches the saturation level, its inductance can decrease 20% to 35% from the value at 0-A bias current depending on how the inductor vendor defines saturation. When selecting an inductor, make sure its rated current, especially the saturation current, is larger than its peak current during the operation.

The inductor peak current varies as a function of the load, the switching frequency, the input and output voltages and it can be calculated by Equation 7 and Equation 8.

\[
I_{PEAK} = I_{IN} + \frac{1}{2} \times \Delta I_L
\]

where
- \( I_{PEAK} \) is the peak current of the inductor
- \( I_{IN} \) is the input average current
- \( \Delta I_L \) is the ripple current of the inductor

The input DC current is determined by the output voltage, the output current and efficiency can be calculated by:

\[
I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta}
\]

where
- \( I_{IN} \) is the input current of the inductor
- \( V_{OUT} \) is the output voltage
- \( V_{IN} \) is the input voltage
- \( \eta \) is the efficiency

While the inductor ripple current depends on the inductance, the frequency, the input voltage and duty cycle calculated by Equation 4, replace Equation 4, Equation 8 into Equation 7 and get the inductor peak current:

\[
I_{PEAK} = \frac{I_{OUT}}{(1 - D) \times \eta} + \frac{1}{2} \times \frac{V_{IN} \times D}{L \times f_{SW}}
\]

where
- \( I_{PEAK} \) is the peak current of the inductor
- \( I_{OUT} \) is the output current
- \( D \) is the duty cycle
- \( \eta \) is the efficiency
- \( V_{IN} \) is the input voltage
- \( L \) is the inductor
- \( f_{SW} \) is the switching frequency
Typical Application (continued)

The heat rating current (RMS) is as below:

\[ I_{L\_RMS} = \sqrt{I_{IN}^2 + \frac{1}{12}(\Delta I_L)^2} \]

where
- \( I_{L\_RMS} \) is the RMS current of the inductor
- \( I_{IN} \) is the input current of the inductor
- \( \Delta I_L \) is the ripple current of the inductor

It is important that the peak current does not exceed the inductor saturation current and the RMS current is not over the temperature related rating current of the inductors.

For a given physical inductor size, increasing inductance usually results in an inductor with lower saturation current. The total losses of the coil consists of the DC resistance (DCR) loss and the following frequency dependent loss:
- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)

For a certain inductor, the larger current ripple (smaller inductor) generates the higher DC and also the frequency-dependent loss. An inductor with lower DCR is basically recommended for higher efficiency. However, it is usually a tradeoff between the loss and foot print.

### Table 2. Recommended Inductors

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>L (μH)</th>
<th>DCR Typ (mΩ) Max</th>
<th>SATURATION CURRENT / Heat Rating Current (A)</th>
<th>SIZE (L x W x H mm)</th>
<th>VENDOR(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>XEL4030-471MEB</td>
<td>0.47</td>
<td>4.1</td>
<td>15.5</td>
<td>4 x 4 x 3</td>
<td>Coilcraft</td>
</tr>
<tr>
<td>XEL4030-102MEB</td>
<td>1</td>
<td>8.9</td>
<td>9</td>
<td>4 x 4 x 3</td>
<td>Coilcraft</td>
</tr>
</tbody>
</table>

(1) See Third-party Products Disclaimer

### 9.2.1.1.5 Selecting the Output Capacitors

The output capacitor is mainly selected to meet the requirements at load transient or steady state. Then the loop is compensated for the output capacitor selected. The output ripple voltage is related to the equivalent series resistance (ESR) of the capacitor and its capacitance. Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by Equation 11:

\[ C_{OUT} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f_{SW} \times \Delta V \times V_{OUT}} \]

where
- \( C_{OUT} \) is the output capacitor
- \( I_{OUT} \) is the output current
- \( V_{OUT} \) is the output voltage
- \( V_{IN} \) is the input voltage
- \( \Delta V \) is the output voltage ripple required
- \( f_{SW} \) is the switching frequency

The additional output ripple component caused by ESR is calculated by Equation 12:

\[ \Delta V_{ESR} = I_{OUT} \times R_{ESR} \]

where
- \( \Delta V_{ESR} \) is the output voltage ripple caused by ESR
- \( R_{ESR} \) is the resistor in series with the output capacitor

For the ceramic capacitor, the ESR ripple can be neglected. However, for the tantalum or electrolytic capacitors, it must be considered if used.
The minimum ceramic output capacitance needed to meet a load transient requirement can be estimated using Equation 13:

\[ C_{OUT} = \frac{\Delta I_{STEP}}{2\pi \times f_{BW} \times \Delta V_{TRAN}} \]

where

- \( \Delta I_{STEP} \) is the transient load current step
- \( \Delta V_{TRAN} \) is the allowed voltage dip for the load current step
- \( f_{BW} \) is the control loop bandwidth (i.e., the frequency where the control loop gain crosses zero)

(13)

Care must be taken when evaluating a ceramic capacitor’s derating under the DC bias. Ceramic capacitors can derate by as much as 70% of its capacitance at its rated voltage. Therefore, enough margins on the voltage rating should be considered to ensure adequate capacitance at the required output voltage.

9.2.1.1.6 Selecting the Input Capacitors

Multilayer ceramic capacitors are an excellent choice for the input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. While a 22-µF input capacitor or equivalent is sufficient for the most applications, larger values may be used to reduce input current ripple.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the \( V_{IN} \) pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional “bulk” capacitance (electrolytic or tantalum) in this circumstance, should be placed between \( C_{IN} \) and the power source lead to reduce ringing that can occur between the inductance of the power source leads and \( C_{IN} \).

9.2.1.1.7 Loop Stability and Compensation

9.2.1.1.7.1 Small Signal Model

The TPS61378-Q1 uses the fixed frequency peak current mode control; there is an internal adaptive slope compensation to avoid the sub-harmonic oscillation. With the inductor current information sensed, the small-signal model of the power stage reduces from a two-pole system, created by \( L \) and \( C_{OUT} \), to a single-pole system, created by \( R_{OUT} \) and \( C_{OUT} \). The single-pole system is easily used with the loop compensation. Figure 4 shows the equivalent small signal elements of a boost converter.
The small signal of power stage including the slope compensation is:

\[
K_{PS}(S) = \frac{R_{OUT} \times (1-D)}{2 \times R_{SENSE}} \times \frac{\left(1 + \frac{s}{2 \pi F_{SWE}}\right) \left(1 - \frac{s}{2 \pi F_{BW}}\right)}{(1 + \frac{s}{2 \pi f_p})} \times H_{c}(S)
\]

where
- \( D \) is the duty cycle
- \( R_{OUT} \) is the output load resistor
- \( R_{SENSE} \) is the equivalent internal current sense resistor, which is typically 118 m\( \Omega \)

The single pole of the power stage is:

\[
f_p = \frac{2}{2 \pi \times R_{OUT} \times C_{OUT}}
\]

where
- \( C_{OUT} \) is the output capacitance, for a boost converter having multiple, identical output capacitors in parallel, simply combine the capacitors with the equivalent capacitance

The zero created by the ESR of the output capacitor is:

\[
f_{ESR} = \frac{1}{2 \pi \times R_{ESR} \times C_{OUT}}
\]

where
- \( R_{ESR} \) is the equivalent resistance in series of the output capacitor.

The right-hand plane zero is:

\[
f_{RHP} = \frac{R_{OUT} \times (1-D)^2}{2 \pi \times L}
\]

where
• D is the duty cycle
• \( R_{\text{OUT}} \) is the output load resistor
• \( L \) is the inductance

Equation 18 shows the equation for feedback resistor network and the error amplifier.

\[
H_{\text{EA}}(S) = G_{\text{EA}} \times R_{\text{EA}} \times \frac{R_{\text{DOWN}}}{R_{\text{UP}} + R_{\text{DOWN}}} \times \frac{S}{2 \times \pi \times f_z} \times \left(1 + \frac{S}{2 \times \pi \times f_{p1}}\right) \times \left(1 + \frac{S}{2 \times \pi \times f_{p2}}\right)
\]

where
• \( R_{\text{EA}} \) is the output impedance of the error amplifier and typical \( R_{\text{EA}} = 500 \, \text{M\text{\ohm}} \).
• \( f_{p1}, f_{p2} \) is the pole's frequency of the compensation, \( f_z \) is the zero's frequency of the compensation network. (18)

\[
f_{p1} = \frac{1}{2\pi \times R_{\text{EA}} \times C_c}
\]

where
• \( C_c \) is the zero capacitor compensation (19)

\[
f_{p2} = \frac{1}{2\pi \times R_C \times C_p}
\]

where
• \( C_p \) is the pole capacitor compensation
• \( R_C \) is the resistor of the compensation network

\[
f_z = \frac{1}{2\pi \times R_C \times C_c}
\]

9.2.1.1.7.2 Loop Compensation Design Steps

With the small signal models coming out, the next step is to calculate the compensation network parameters with the given inductor and output capacitance.

1. Set the Cross Over Frequency, \( f_C \)
   - The first step is to set the loop crossover frequency, \( f_C \). The higher crossover frequency, the faster the loop response is. It is generally accepted that the loop gain cross over no higher than the lower of either \( 1/10 \) of the switching frequency, \( f_{SW} \), or \( 1/5 \) of the RHPZ frequency, \( f_{RHPZ} \). Then calculate the loop compensation network values of \( R_C, C_c, \) and \( C_p \) by following below equations.

2. Set the Compensation Resistor, \( R_C \)
   - By placing \( f_z \) below \( f_C \), for frequencies above \( f_C \), \( R_C \| R_{\text{EA}} \approx R_C \) and so \( R_C \times G_{\text{EA}} \) sets the compensation gain. Setting the compensation gain, \( K_{\text{COMP-dB}} \) at \( f_z \), results in the total loop gain, \( T(s) = G_{\text{PS}}(s) \times H_{\text{EA}}(s) \times H_e(s) \) being zero at \( f_C \).
   - Therefore, to approximate a single-pole roll-off up to \( f_{p2} \), rearrange Equation 18 to solve for \( R_C \) so that the compensation gain, \( K_{\text{EA}} \), at \( f_C \) is the negative of the gain, \( K_{\text{PS}} \), read at frequency \( f_C \) for the power stage bode plot or more simply:

\[
K_{\text{EA}}(f_C) = 20 \times \log(G_{\text{EA}} \times R_C \times \frac{R_{\text{DOWN}}}{R_{\text{UP}} + R_{\text{DOWN}}}) = - K_{\text{PS}}(f_C)
\]

where
• \( K_{\text{EA}} \) is gain of the error amplifier network
• \( K_{\text{PS}} \) is the gain of the power stage
• \( G_{\text{EA}} \) is the amplifier’s trans-conductance, the typical value of \( G_{\text{EA}} = 70 \, \mu\text{A} / \text{V} \) (22)

3. Set the compensation zero capacitor, \( C_c \)
   - Place the compensation zero at the power stage \( R_{\text{OUT}} \), \( C_{\text{OUT}} \) pole’s position, so to get:
\[
f_Z = \frac{1}{2\pi R_C C_C}
\]

- Set \(f_Z = f_P\), and get the
\[
C_C = \frac{R_{OUT} \times C_{OUT}}{2R_C}
\]

4. Set the compensation pole capacitor, \(C_P\)
- Place the compensation pole at the zero produced by the \(R_{ESR}\) and the \(C_{OUT}\), it is useful for canceling unhelpful effects of the ESR zero.

\[
f_{P2} = \frac{1}{2\pi R_C C_P}
\]

\[
f_{ESR} = \frac{1}{2\pi R_{ESR} C_{OUT}}
\]

- Set \(f_{P2} = f_{ESR}\), and get the
\[
C_P = \frac{R_{ESR} \times C_{OUT}}{R_C}
\]

9.2.1.7.3 Selecting the Bootstrap Capacitor

The bootstrap capacitor between the BST and SW pin supplies the gate current to charge the high-side FET device gate during each cycle’s turn-on and also supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is 0.1 µF to 1 µF. \(C_{BST}\) should be a good quality, low ESR, ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. A value of 0.1 µF was selected for this design example.

9.2.1.7.4 \(V_{CC}\) Capacitor

The primary purpose of the \(V_{CC}\) capacitor is to supply the peak transient currents of the driver and bootstrap capacitor as well as provide stability for the \(V_{CC}\) regulator. The value of \(C_{VCC}\) should be at least 10 times greater than the value of \(C_{BST}\), and should be a good quality, low ESR, ceramic capacitor. \(C_{VCC}\) should be placed close to the pins of the IC to minimize potentially damaging voltage transients caused by the trace inductance. A value of 2.2 µF was selected for this design example.

10 Power Supply Recommendations

The TPS61378-Q1 is designed to operate from an input voltage supply range between 2.3 V to 14 V. This input supply should be well regulated. If the input supply is located more than a few inches from the device, the bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.
11 Layout

11.1 Layout Guidelines
As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitor, as well as the inductor should be placed as close as possible to the IC.

11.2 Layout Example
The bottom layer is a large GND plane connected by vias.

Figure 5. Recommended Layout
12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer
TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources
TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks
E2E is a trademark of Texas Instruments.

12.5 Electrostatic Discharge Caution
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
EXAMPLE STENCIL DESIGN

RTE0016K

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

SYMM

METAL ALL AROUND

(R0.05) TYP

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.
# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>PTPS61378QWRTERQ1</td>
<td>ACTIVE</td>
<td>WQFN</td>
<td>RTE</td>
<td>16</td>
<td>3000</td>
<td>TBD</td>
<td>Call TI</td>
<td>-40 to 125</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPS61378QWRTERQ1</td>
<td>PREVIEW</td>
<td>WQFN</td>
<td>RTE</td>
<td>16</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>2ELH</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

- **RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

- **Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
RTE (S-PWQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
   The package thermal pad must be soldered to the board for thermal and mechanical performance.
   See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO-220.
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated