1 Features
• DCS-Control™ topology
• Qualified for automotive applications
• Functional Safety-Capable
  – Documentation available to aid functional safety system design
• AEC-Q100 qualified with the following results:
  – Device temperature grade: −40°C to 125°C operating junction temperature range
  – Device HBM ESD classification level 2
  – Device CDM ESD classification level C4B
• Input voltage range: 3 to 17 V
• Adjustable output voltage from 0.9 to 6 V
• Pin-selectable output voltage (nominal, + 5%)
• Programmable soft start and tracking
• Seamless power save mode transition
• Quiescent current of 17 µA (typ.)
• Selectable operating frequency
• Power good output
• 100% Duty cycle mode
• Short circuit protection
• Overtemperature protection
• Pin-to-pin compatible with TPS62150A-Q1
• Available in a 3-mm × 3-mm, VQFN-16 package
• Create a custom design using the TPS62130A-Q1 with the WEBENCH® Power Designer

2 Applications
• ADAS camera
• Sensor fusion
• Infotainment telematics
• Infotainment, CAN-, USB- power supply

3 Description
The TPS6213XA-Q1 devices are easy-to-use synchronous step-down DC-DC converters optimized for applications with high power density. A high switching frequency of typically 2.5 MHz allows the use of small inductors and provides fast transient response as well as high output-voltage accuracy through the use of the DCS-Control™ topology.

With a wide operating input-voltage range of 3 to 17 V, the devices are ideally suited for systems powered from intermediate bus power rails. The devices support up to 3-A continuous output current at output voltages between 0.9 V and 6 V (with 100% duty cycle mode). The output-voltage startup ramp is controlled by the soft-start pin, which allows operation as either a standalone power supply or in tracking configurations. Power sequencing is also possible by configuring the enable and open-drain power-good pins.

In power save mode, the devices show quiescent current of about 17 µA from VIN. Power save mode which is entered automatically and seamlessly if the load is small, maintains high efficiency over the entire load range. In shutdown mode, the devices are turned off and shutdown current consumption is less than 2 µA. The devices are packaged in a 16-pin VQFN package measuring 3 × 3 mm (RGT).

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS62130A-Q1</td>
<td>VQFN (16)</td>
<td>3.00 mm x 3.00 mm</td>
</tr>
<tr>
<td>TPS62133A-Q1</td>
<td>VQFN (16)</td>
<td>3.00 mm x 3.00 mm</td>
</tr>
<tr>
<td>TPS6213013A-Q1</td>
<td>VQFN (16)</td>
<td>3.00 mm x 3.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
Table of Contents

1 Features .............................................................. 1
2 Applications ......................................................... 1
3 Description ........................................................... 1
4 Revision History ..................................................... 2
5 Device Comparison Table .......................................... 4
6 Pin Configuration and Functions ............................. 4
7 Specifications .......................................................... 5
   7.1 Absolute Maximum Ratings ............................. 5
   7.2 ESD Ratings .................................................. 5
   7.3 Recommended Operating Conditions ................. 5
   7.4 Thermal Information ........................................ 5
   7.5 Electrical Characteristics ............................... 6
   7.6 Typical Characteristics ..................................... 7
8 Parameter Measurement Information ....................... 7
9 Detailed Description ............................................... 9
   9.1 Overview ...................................................... 9
   9.2 Functional Block Diagram ............................... 9
   9.3 Feature Description ........................................ 10
10 Application and Implementation ............................ 14
   10.1 Application Information ................................ 14
   10.2 Typical Application ....................................... 14
   10.3 System Examples ......................................... 26
11 Power Supply Recommendations ............................ 29
12 Layout .................................................................. 30
   12.1 Layout Guidelines ......................................... 30
   12.2 Layout Example ............................................ 30
13 Device and Documentation Support ......................... 31
   13.1 Device Support .............................................. 31
   13.2 Related Links ............................................... 31
   13.3 Receiving Notification of Documentation Updates 31
   13.4 Support Resources ......................................... 31
   13.5 Trademarks .................................................. 31
   13.6 Electrostatic Discharge Caution ........................ 31
   13.7 Glossary ...................................................... 31
14 Mechanical, Packaging, and Orderable Information .... 31

4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (January 2018) to Revision E .......................... Page
  • Added functional safety capable bullet in the Features ............................................................. 1

Changes from Revision C (July 2017) to Revision D ............................... Page
  • Changed pin 7 from "LOG" to "FSW" in the Pin Functions table for clarification ....................... 4
  • Deleted extra text string "or 1.25 MHz, selectable with the FSW" after 1st paragraph of Pulse Width Modulation (PWM) Operation section .......................................................... 10
  • Deleted extra text ".with FSW=Low" preceding Equation 1 ...................................................... 11

Changes from Revision B (October 2016) to Revision C ........................ Page
  • Added WEBENCH® links throughout document ................................................................. 1
  • Changed "LOG" pin to "FSW" pin on the Pin Configuration drawing, and added FSW description throughout the document .................................................. 4
  • Added SW (AC) spec to the Absolute Maximum Ratings (1) table .................................... 5
  • Added Power Good Pin Logic Table table and Frequency Selection (FSW) section regarding pin control .................. 12

Changes from Revision A (October 2016) to Revision B ........................ Page
  • Deleted "Product Preview " status from TPS6213013A-Q1 device ........................................ 1
  • Added text to Frequency Selection (FSW) section regarding pin control .................. 13
  • Added Receiving Notification of Documentation Updates and Support Resources sections .................................. 31
Changes from Original (May 2014) to Revision A

- Added TPS6213013A-Q1 device ................................................................. Page 1
- Added TPS6213013A-Q1 to Device Comparison Table ................................................. Page 4
- Moved Storage temperature spec., T_{stg} to Absolute Maximum Ratings table, and re-named Handling Ratings table to ESD Ratings .......................................................................................... Page 5
- Corrected Thermal Information table ........................................................................ Page 5
- Added Figure 27, Figure 28, Figure 31, and Figure 32 ..................................................... Page 22
- Added Figure 33, Figure 34 ..................................................................................... Page 23
- Added Figure 52 .................................................................................................. Page 29
- Changed Figure 55 ............................................................................................. Page 30
5 Device Comparison Table

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>OUTPUT VOLTAGE</th>
<th>PACKAGE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS62130A-Q1</td>
<td>Adjustable</td>
<td>PA6IQ</td>
</tr>
<tr>
<td>TPS62133A-Q1</td>
<td>5 V</td>
<td>PA6JQ</td>
</tr>
<tr>
<td>TPS6213013A-Q1</td>
<td>1.3 V</td>
<td>13013Q</td>
</tr>
</tbody>
</table>

6 Pin Configuration and Functions

### Pin Functions

#### RGT Package
16-Pin VQFN
Top View

- PGND
- PGND
- VOS
- EN
- SW 1
- Exposed Thermal Pad
- SW 2
- SW 3
- PG 4
- FB
- AGND
- FSW
- DEF
- EN
- VOS
- PVIN
- AVIN
- SW 5,6,7,8
- SW 9
- SS/TR
- PVIN
- PVIN
- SS/TR
- PGND

#### Pin Functions

<table>
<thead>
<tr>
<th>PIN(1)</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NO.</td>
<td>NAME</td>
<td>DESCRIPTION</td>
</tr>
<tr>
<td>1,2,3</td>
<td>SW</td>
<td>O Switch node, which is connected to the internal MOSFET switches. Connect inductor between SW and output capacitor.</td>
</tr>
<tr>
<td>4</td>
<td>PG</td>
<td>O Output power good (High = VOUT ready, Low = VOUT below nominal regulation) ; open drain (requires pullup resistor)</td>
</tr>
<tr>
<td>5</td>
<td>FB</td>
<td>I Voltage feedback of adjustable version. Connect resistive voltage divider to this pin. It is recommended to connect FB to AGND on fixed output voltage versions for improved thermal performance.</td>
</tr>
<tr>
<td>6</td>
<td>AGND</td>
<td>Analog Ground. Must be connected directly to the Exposed Thermal Pad and common ground plane.</td>
</tr>
<tr>
<td>7</td>
<td>FSW</td>
<td>I Switching Frequency Select (Low = 2.5 MHz, High = 1.25 MHz for typical operation)(2)</td>
</tr>
<tr>
<td>8</td>
<td>DEF</td>
<td>I Output Voltage Scaling (Low = nominal, High = nominal + 5%)(2)</td>
</tr>
<tr>
<td>9</td>
<td>SS/TR</td>
<td>I Soft-Start / Tracking Pin. An external capacitor connected to this pin sets the internal voltage reference rise time. It can be used for tracking and sequencing.</td>
</tr>
<tr>
<td>10</td>
<td>AVIN</td>
<td>I Supply voltage for control circuitry. Connect to same source as PVIN.</td>
</tr>
<tr>
<td>11,12</td>
<td>PVIN</td>
<td>I Supply voltage for power stage. Connect to same source as AVIN.</td>
</tr>
<tr>
<td>13</td>
<td>EN</td>
<td>I Enable input (High = enabled, Low = disabled)(2)</td>
</tr>
<tr>
<td>14</td>
<td>VOS</td>
<td>I Output voltage sense pin and connection for the control loop circuitry.</td>
</tr>
<tr>
<td>15,16</td>
<td>PGND</td>
<td>Power Ground. Must be connected directly to the Exposed Thermal Pad and common ground plane.</td>
</tr>
<tr>
<td>Exposed Thermal Pad</td>
<td>–</td>
<td>Must be connected to AGND (pin 6), PGND (pin 15,16) and common ground plane(3). Must be soldered to achieve appropriate power dissipation and mechanical reliability.</td>
</tr>
</tbody>
</table>

(1) For more information about connecting pins, see Detailed Description and Application and Implementation sections.
(2) An internal pulldown resistor keeps logic level low, if pin is floating.
(3) See Figure 55.
7 Specifications

7.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Pin voltage</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVIN, PVIN</td>
<td>–0.3</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>EN, SS/TR, SW (DC)</td>
<td>–0.3</td>
<td>V_{IN}+0.3</td>
<td>V</td>
</tr>
<tr>
<td>SW (AC), less than 10 ns</td>
<td>–2</td>
<td>24.5</td>
<td>V</td>
</tr>
<tr>
<td>DEF, FSW, FB, PG, VOS</td>
<td>–0.3</td>
<td>7</td>
<td>V</td>
</tr>
</tbody>
</table>

Power Good sink current | PG | 10 mA
Temperature | Operating junction temperature, T_J | –40 | 150 °C
Storage temperature | T_{STG} | –65 | 150 °C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network ground terminal.

(3) While switching.

7.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

7.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>17</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>0.9</td>
<td>6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>–40</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC</th>
<th>TPS6213xA-Q1</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{JA} Junction-to-ambient thermal resistance</td>
<td>45</td>
<td>°C/W</td>
</tr>
<tr>
<td>R_{JC(top)} Junction-to-case (top) thermal resistance</td>
<td>53.6</td>
<td>°C/W</td>
</tr>
<tr>
<td>R_{JB} Junction-to-board thermal resistance</td>
<td>17.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>ψ_{JT} Junction-to-top characterization parameter</td>
<td>1.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>ψ_{JB} Junction-to-board characterization parameter</td>
<td>17.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>R_{JC(bot)} Junction-to-case (bottom) thermal resistance</td>
<td>4.5</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report.
## 7.5 Electrical Characteristics

over junction temperature range ($T_J = -40^\circ C$ to $+125^\circ C$), typical values at $V_{IN} = 12$ V and $T_A = 25^\circ C$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>Input voltage range</td>
<td>3</td>
<td>17</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_Q$</td>
<td>Operating quiescent current</td>
<td>EN = High, $I_{OUT} = 0$ mA, device not switching</td>
<td>17</td>
<td>30</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{SD}$</td>
<td>Shutdown current</td>
<td>EN = Low</td>
<td>1.5</td>
<td>25</td>
<td>µA</td>
</tr>
<tr>
<td>$V_{UVLO}$</td>
<td>Undervoltage lockout threshold</td>
<td>Failing Input Voltage (PWM mode operation)</td>
<td>2.6</td>
<td>2.7</td>
<td>2.8</td>
</tr>
<tr>
<td>$T_{SD}$</td>
<td>Thermal shutdown temperature</td>
<td>Hysteresis</td>
<td>200</td>
<td></td>
<td>mV</td>
</tr>
</tbody>
</table>

### CONTROL (EN, DEF, FSW, SS/TR, PG)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_H$</td>
<td>High level input threshold voltage (EN, DEF, FSW)</td>
<td>0.9</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_L$</td>
<td>Low level input threshold voltage (EN, DEF, FSW)</td>
<td>EN = $V_IN$ or GND; DEF, FSW=GND</td>
<td>0.01</td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{LKG}$</td>
<td>Input leakage current (EN, DEF, FSW)</td>
<td>Rising ($%V_{OUT}$)</td>
<td>92%</td>
<td>95%</td>
<td>98%</td>
</tr>
<tr>
<td>$V_{TH,PG}$</td>
<td>Power good threshold voltage</td>
<td>Failing ($%V_{OUT}$)</td>
<td>87%</td>
<td>90%</td>
<td>94%</td>
</tr>
<tr>
<td>$V_{OL,PG}$</td>
<td>Power good output low</td>
<td>$I_{PG} = -2$ mA</td>
<td>0.07</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>$I_{LKG,PG}$</td>
<td>Input leakage current (PG)</td>
<td>$V_{PG} = 1.8$ V</td>
<td>1</td>
<td>400</td>
<td>nA</td>
</tr>
<tr>
<td>$I_{SS/TR}$</td>
<td>SS/TR pin source current</td>
<td>2.3</td>
<td>2.5</td>
<td>2.7</td>
<td>µA</td>
</tr>
</tbody>
</table>

### POWER SWITCH

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{DS(ON)}$</td>
<td>High-side MOSFET ON-resistance</td>
<td>$V_{IN} \geq 6$ V</td>
<td>90</td>
<td>170</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td>Low-side MOSFET ON-resistance</td>
<td>$V_{IN} = 3$ V</td>
<td>120</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{LIMF}$</td>
<td>High-side MOSFET forward current limit</td>
<td>$V_{IN} = 12$ V, $T_A = 25^\circ C$</td>
<td>3.6</td>
<td>4.2</td>
<td>4.9</td>
</tr>
</tbody>
</table>

### OUTPUT

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{REF}$</td>
<td>Internal reference voltage</td>
<td>0.8</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{LKG, FB}$</td>
<td>Input leakage current (FB)</td>
<td>$V_{FB} = 0.8$ V</td>
<td>1</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Output voltage range (TPS62130A-Q1)</td>
<td>$V_{IN} \geq V_{OUT}$</td>
<td>0.9</td>
<td>6.0</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>DEF (Output voltage programming)</td>
<td>DEF = $0$ (GND)</td>
<td>$V_{OUT}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output voltage accuracy$^2$</td>
<td>PWM mode operation, $V_{IN} \geq V_{OUT} +1$ V</td>
<td>$-1.8%$</td>
<td>1.8%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Load regulation</td>
<td>Power Save Mode operation, $C_{OUT} = 22$ µF</td>
<td>$-2.3%$</td>
<td>2.8%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Line regulation</td>
<td>$3$ V $\leq V_{IN} \leq 17$ V, $V_{OUT} = 3.3$ V, PWM mode operation</td>
<td>0.05</td>
<td>%/A</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3 V $\leq V_{IN} \leq 17$ V, $V_{OUT} = 3.3$ V, $I_{OUT} = 1$ A, PWM mode operation</td>
<td>0.02</td>
<td>%/V</td>
<td></td>
</tr>
</tbody>
</table>

(1) Current into AVIN+PVIN pin
(2) This is the regulation accuracy of the voltage at the FB pin (adjustable version) and of the output voltage (fixed version).
7.6 Typical Characteristics

8 Parameter Measurement Information

Table 1. List of Components

<table>
<thead>
<tr>
<th>REFERENCE</th>
<th>DESCRIPTION</th>
<th>MANUFACTURER</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC</td>
<td>17-V, 3-A Step-Down Converter, QFN</td>
<td>TPS62130AQRGT, Texas Instruments</td>
</tr>
<tr>
<td>L1</td>
<td>2.2 µH, 0.165 x 0.165 in</td>
<td>XFL4020-222MEB, Coilcraft</td>
</tr>
</tbody>
</table>
Parameter Measurement Information (continued)

Table 1. List of Components (continued)

<table>
<thead>
<tr>
<th>REFERENCE</th>
<th>DESCRIPTION</th>
<th>MANUFACTURER</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>10 µF, 25 V, Ceramic, 1210</td>
<td>Standard</td>
</tr>
<tr>
<td>C3</td>
<td>22 µF, 6.3 V, Ceramic, 0805</td>
<td>Standard</td>
</tr>
<tr>
<td>C5</td>
<td>3300 pF, 25 V, Ceramic, 0603</td>
<td>Standard</td>
</tr>
<tr>
<td>C7</td>
<td>0.1 µF, 25 V, Ceramic, 0603</td>
<td>Standard</td>
</tr>
<tr>
<td>R1</td>
<td>Depending on V_{OUT}</td>
<td>Standard</td>
</tr>
<tr>
<td>R2</td>
<td>Depending on V_{OUT}</td>
<td>Standard</td>
</tr>
<tr>
<td>R3</td>
<td>100 kΩ, Chip, 0603, 1/16W, 1%</td>
<td>Standard</td>
</tr>
</tbody>
</table>

Figure 6. Measurement Setup (High Switching Frequency)

Figure 7. Measurement Setup (Low Switching Frequency)
9 Detailed Description

9.1 Overview

The TPS6213xA-Q1 synchronous switched mode power converters are based on DCS-Control™ (Direct Control with Seamless Transition into Power Save Mode), an advanced regulation topology, that combines the advantages of hysteretic, voltage mode, and current mode control including an AC loop directly associated to the output voltage. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. It sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

The DCS-Control topology supports PWM (Pulse Width Modulation) mode for medium and heavy load conditions and a Power Save Mode at light loads. During PWM, it operates at its nominal switching frequency in continuous conduction mode. This frequency is typically about 2.5 MHz or 1.25 MHz with a controlled frequency variation, depending on the input voltage. If the load current decreases, the converter enters Power Save Mode to sustain high efficiency down to very light loads. In Power Save Mode, the switching frequency decreases linearly with the load current. Since DCS-Control supports both operation modes within one single building block, the transition from PWM to Power Save Mode is seamless without effects on the output voltage.

9.2 Functional Block Diagram

![Diagram of TPS62130A-Q1 (Adjustable Output Voltage)]

*This pin is connected to a pull down resistor internally (see Feature Description section).

Copyright © 2017, Texas Instruments Incorporated
9.3 Feature Description

9.3.1 Pulse Width Modulation (PWM) Operation
The TPS6213xA-Q1 operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of 2.5 MHz or 1.25 MHz, selectable with the FSW pin. The frequency variation in PWM is controlled and depends on \( V_{IN} \), \( V_{OUT} \), and the inductance. The device operates in PWM mode as long the output current is higher than half the ripple current of the inductor. To maintain high efficiency at light loads, the device enters Power Save Mode at the boundary to discontinuous conduction mode (DCM). PSM operation occurs if the output current becomes smaller than half the ripple current of the inductor.

9.3.2 Power Save Mode Operation
The built-in Power Save Mode of the TPS6213xA-Q1 is entered seamlessly, if the load current decreases. This secures a high efficiency in light load operation. The device remains in Power Save Mode as long as the inductor current is discontinuous.

In Power Save Mode, the switching frequency decreases linearly with the load current maintaining high efficiency. The transition into and out of Power Save Mode happens within the entire regulation scheme and is seamless in both directions.

* This pin is connected to a pull down resistor internally (see Feature Description section).

Copyright © 2017, Texas Instruments Incorporated
Feature Description (continued)

TPS6213xA-Q1 includes a fixed on-time circuitry. This on-time, in steady-state operation with FSW=Low, can be estimated as:

\[ t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 400\text{ns} \]  

(1)

For very small output voltages, an absolute minimum on-time of about 80 ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, keeping efficiency high. Also the off-time can reach its minimum value at high duty cycles. The output voltage remains regulated in such case. Using \(t_{ON}\), the typical peak inductor current in Power Save Mode can be approximated by:

\[ I_{LPSM(peak)} = \frac{(V_{IN} - V_{OUT})}{L} \cdot I_{ON} \]  

(2)

When \(V_{IN}\) decreases to typically 15% above \(V_{OUT}\), the TPS6213xA-Q1 does not enter Power Save Mode, regardless of the load current. The device maintains output regulation in PWM mode.

9.3.3 100% Duty-Cycle Operation

The duty cycle of the buck converter is given by \(D = \frac{V_{OUT}}{V_{IN}}\) and increases as the input voltage comes close to the output voltage. In this case, the device starts 100% duty cycle operation turning on the high-side switch 100% of the time. The high-side switch stays turned on as long as the output voltage is below the internal set point. This allows the conversion of small input to output voltage differences (for example, for the longest operation time of battery-powered applications). In 100% duty cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, can be calculated as:

\[ V_{IN(min)} = V_{OUT(min)} + I_{OUT}(R_{DS(on)} + R_L) \]

where

- \(I_{OUT}\) is the output current
- \(R_{DS(on)}\) is the \(R_{DS(on)}\) of the high-side FET
- \(R_L\) is the DC resistance of the inductor used

(3)

9.3.4 Enable / Shutdown (EN)

When Enable (EN) is set High, the device starts operation. Shutdown is forced if EN is pulled Low with a shutdown current of typically 1.5 µA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off. The internal resistive divider pulls down the output voltage smoothly. The EN signal must be set externally to High or Low. The typical threshold values are 0.65 V (rising) and 0.45 V (falling). An internal pulldown resistor of about 400 kΩ is connected and keeps EN logic low, if Low is set initially and then the pin gets floating. It is disconnected if the pin is set High.

Connecting the EN pin to an appropriate output signal of another power rail provides sequencing of multiple power rails.

9.3.5 Soft Start / Tracking (SS/TR)

The internal soft-start circuitry controls the output voltage slope during start-up, avoiding excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high-impedance power sources or batteries. When EN is set to start device operation, the device starts switching after a delay of about 50 µs and \(V_{OUT}\) rises with a slope controlled by an external capacitor connected to the SS/TR pin. See Figure 41 and Figure 42 for typical start-up operation.
Feature Description (continued)

Using a very small capacitor (or leaving SS/TR pin un-connected) provides the fastest start-up behavior. The TPS6213xA-Q1 can start into a pre-biased output. During monotonic pre-biased start-up, both of the power MOSFETs are not allowed to turn on until the internal ramp of the device sets an output voltage above the pre-bias voltage. As long as the output is below about 0.5 V, a reduced current limit of typically 1.6 A is set internally. If the device is set to shutdown (EN = GND), undervoltage lockout, or thermal shutdown, an internal resistor pulls the SS/TR pin down to ensure a proper low level. Returning from those states causes a new start-up sequence as set by the SS/TR connection.

A voltage supplied to SS/TR can be used for tracking a master voltage. The output voltage follows this voltage in both directions up and down (see Application and Implementation).

9.3.6 Current Limit And Short Circuit Protection

The TPS6213xA-Q1 is protected against heavy load and short circuit events. If a short circuit is detected ($V_{OUT}$ drops below 0.5 V), the current limit is reduced to 1.6 A, typically. If the output voltage rises above 0.5 V, the device runs in normal operation again. At heavy loads, the current limit determines the maximum output current. If the current limit is reached, the high-side FET turns off. Avoiding shoot through current, the low-side FET switches on to allow the inductor current to decrease. The low-side current limit is typically 3.5 A. The high-side FET turns on again, only if the current in the low-side FET has decreased below the low-side current limit threshold.

The output current of the device is limited by the current limit (see Electrical Characteristics). Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit can be calculated as follows:

$$I_{peak\,(typ)} = I_{LIMF} + \frac{V_L}{L} \cdot t_{PD}$$

where

- $I_{LIMF}$ is the static current limit, specified in the Electrical Characteristics
- $L$ is the inductor value
- $V_L$ is the voltage across the inductor ($V_{IN} - V_{OUT}$)
- $t_{PD}$ is the internal propagation delay

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high-side switch peak current can be calculated as follows:

$$I_{peak\,(typ)} = I_{LIMF} + \frac{(V_{IN} - V_{OUT})}{L} \cdot 30ns$$

9.3.7 Power Good (PG)

The TPS6213xA-Q1 has a built-in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor (to any voltage below 7 V). It can sink 2 mA of current and maintain its specified logic low level. TPS6213xA-Q1 features PG = Low when the device is turned off due to EN, UVLO, or thermal shutdown and can be used to actively discharge $V_{OUT}$ (see Figure 46). $V_{IN}$ must remain present for the PG pin to stay Low. If unused, the PG pin can be left floating.

<table>
<thead>
<tr>
<th>Table 2. Power Good Pin Logic Table</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DEVICE STATE</strong></td>
</tr>
<tr>
<td>Enable (EN = High)</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Shutdown (EN = Low)</td>
</tr>
<tr>
<td>UVLO</td>
</tr>
<tr>
<td>Thermal Shutdown</td>
</tr>
<tr>
<td>Power Supply Removal</td>
</tr>
</tbody>
</table>
9.3.8 Pin-Selectable Output Voltage (DEF)

The output voltage of the TPS6213xA-Q1 can be increased by 5% above the nominal voltage by setting the DEF pin to High \(^{(1)}\). When DEF is Low, the device regulates to the nominal output voltage. Increasing the nominal voltage allows adapting the power supply voltage to the variations of the application hardware. More detailed information on voltage margining using TPS6213xA-Q1 can be found in the Voltage Margining Using the TPS62130 Application Report. A pulldown resistor of about 400 kΩ is internally connected to the pin to ensure a proper logic level if the pin is high impedance or floating after initially set to Low. The resistor is disconnected if the pin is set High.

9.3.9 Frequency Selection (FSW)

To get high power density with very small solution size, a high switching frequency allows the use of small external components for the output filter. However, switching losses increase with the switching frequency. If efficiency is the key parameter, more than solution size, the switching frequency can be set to half (1.25 MHz typ.) by pulling FSW to High. Running with lower frequency, a higher efficiency and a higher output voltage ripple is achieved. Pull FSW to Low for high frequency operation (2.5 MHz typ.). To get low ripple and full output current at the lower switching frequency, it is recommended to use an inductor of at least 2.2 µH. The switching frequency can be changed during operation, if needed. A pulldown resistor of about 400 kΩ is internally connected to the pin, acting the same way as at the DEF Pin (see above).

9.3.10 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents misoperation of the device by switching off both the power FETs. The undervoltage lockout threshold is set typically to 2.7 V. The device is fully operational for voltages above the UVLO threshold and turns off if the input voltage trips the threshold. The converter starts operation again once the input voltage exceeds the threshold by a hysteresis of typically 200 mV.

9.3.11 Thermal Shutdown

The junction temperature \(T_J\) of the device is monitored by an internal temperature sensor. If \(T_J\) exceeds 160°C (typ), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and PG goes Low. When \(T_J\) decreases below the hysteresis amount, the converter resumes normal operation, beginning with soft start. To avoid unstable conditions, a hysteresis of typically 20°C is implemented on the thermal shutdown temperature.

9.4 Device Functional Modes

9.4.1 Operation Above \(T_J = 125°C\)

The operating junction temperature of the device is specified up to 125°C. In power supplying circuits, the self heating effect causes the junction temperature, \(T_J\), to be even higher than the ambient temperature, \(T_A\) (see Figure 43). Depending on \(T_A\) and the load current, the maximum operating \(T_J\) can be exceeded. However, the electrical characteristics are specified up to a \(T_J\) of 125°C only. The device operates as long as thermal shutdown threshold is not triggered.

9.4.2 Operation with \(V_{IN} < 3\) V

The device is functional for supply voltages below 3 V and above the UVLO threshold. Parameters can differ from specified values. The minimum \(V_{IN}\) value of 3 V is not violated by UVLO threshold and hysteresis variations.

9.4.3 Operation with Separate EN Control

The EN pin can be connected to \(V_{IN}\) or be controlled separately. While the EN control voltage level can be lower than the actual \(V_{IN}\) value, it must not exceed \(V_{IN}\) to avoid damage of the device. This might happen at low \(V_{IN}\) during start-up, or power sequencing.

\(^{(1)}\) Maximum allowed voltage is 7V. Therefore it's recommended to connect it to \(V_{OUT}\), not \(V_{IN}\).
10  Application and Implementation

10.1  Application Information

TPS62130xA-Q1 are synchronous switch mode step-down converters, able to convert a 3-V to 17-V input voltage into a lower, 0.9-V to 6-V output voltage, providing up to 3-A load current. The following section gives guidance on choosing external components to complete the power supply design. Application Curves are included for the following typical application.

10.2  Typical Application

10.2.1  TPS62130A-Q1 Point-Of-Load Step Down Converter

![Typical Schematic for 3.3-V Step-Down Converter](image)

Figure 10. Typical Schematic for 3.3-V Step-Down Converter

10.2.1.1  Design Requirements

The step-down converter design can be adapted to different output voltage and load current needs by choosing external components appropriate. The following design procedure is adequate for whole $V_{IN}$, $V_{OUT}$, and load current range of TPS62130A-Q1. Using Table 3, the design procedure needs minimum effort.

10.2.1.2  Detailed Design Procedure

10.2.1.2.1  Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS62130A-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.
Typical Application (continued)

10.2.1.2 Programming The Output Voltage

The TPS6213xA-Q1 can be programmed for output voltages from 0.9 V to 6 V by using a resistive divider from VOUT to AGND. The voltage at the FB pin is regulated to 800 mV. The value of the output voltage is set by the selection of the resistive divider from Equation 6 (see Figure 10). It is recommended to choose resistor values which allow a current of at least 2 µA, meaning the value of R2 should not exceed 400 kΩ. Lower resistor values are recommended for highest accuracy and most robust design. For applications requiring lowest current consumption, the use of fixed output voltage versions is recommended.

\[ R_1 = R_2 \left( \frac{V_{OUT} \text{ (max)}}{0.8V} - 1 \right) \]  

(6)

In case the FB pin gets opened, the device clamps the output voltage at the VOS pin internally to about 7.4 V.

10.2.1.2.3 External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the control loop of the device. The TPS6213xA-Q1 is optimized to work within a range of external components. The inductance and capacitance of the LC output filter must be considered together, creating a double pole, responsible for the corner frequency of the converter (see Output Filter and Loop Stability). Table 3 can be used to simplify the output filter component selection.

Table 3. Recommended LC Output Filter Combinations(1)

<table>
<thead>
<tr>
<th>Inductor (µH)</th>
<th>0.47</th>
<th>1</th>
<th>2.2</th>
<th>3.3</th>
<th>4.7</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.7 µF</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 µF</td>
<td></td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>22 µF</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>47 µF</td>
<td></td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>100 µF</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>200 µF</td>
<td></td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>400 µF</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) The values in the table are nominal values.
(2) This LC combination is the standard value and recommended for most applications.

The TPS6213xA-Q1 can be run with an inductor as low as 1 µH. FSW should be set Low in this case. However, for applications running with the low frequency setting (FSW = High) or with low input voltages, 2.2 µH is recommended.

More detailed information on further LC combinations can be found in Device Behavior Under Slow VBAT Ramp-Down and Ramp-Up Application Report.

10.2.1.2.4 Inductor Selection

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PSM transition point, and efficiency. In addition, the selected inductor has to be rated for appropriate saturation current and DC resistance (DCR). Equation 7 and Equation 8 calculate the maximum inductor current under static load conditions.

\[ I_{L\text{ (max)}} = I_{OUT\ (max)} + \frac{\Delta I_{L\text{ (max)}}}{2} \]  

\[ \Delta I_{L\text{ (max)}} = V_{OUT} \cdot \left( 1 - \frac{V_{OUT}}{V_{IN\ (max)}} \right) \cdot \left( \frac{1}{L_{\text{ (min)}}} \cdot f_{SW} \right) \]  

where

• \( I_{L\ (max)} \) is the maximum inductor current
• \( \Delta I_{L} \) is the peak-to-peak inductor ripple current
• \( L_{\text{ (min)}} \) is the minimum effective inductor value
Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. It is recommended to add a margin of about 20%. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and solution size. The following inductors have been used with the TPS6213xA-Q1 and are recommended for use:

<table>
<thead>
<tr>
<th>TYPE</th>
<th>INDUCTANCE [µH]</th>
<th>CURRENT [A][2]</th>
<th>DIMENSIONS [LxBxH] [mm]</th>
<th>MANUFACTURER</th>
</tr>
</thead>
<tbody>
<tr>
<td>XFL4020-102ME_</td>
<td>1.0 µH, ±20%</td>
<td>4.7</td>
<td>4 x 4 x 2.1</td>
<td>Coilcraft</td>
</tr>
<tr>
<td>XFL4020-152ME_</td>
<td>1.5 µH, ±20%</td>
<td>4.2</td>
<td>4 x 4 x 2.1</td>
<td>Coilcraft</td>
</tr>
<tr>
<td>XFL4020-222ME_</td>
<td>2.2 µH, ±20%</td>
<td>3.8</td>
<td>4 x 4 x 2.1</td>
<td>Coilcraft</td>
</tr>
<tr>
<td>IHLP1212BZ-11</td>
<td>1.0 µH, ±20%</td>
<td>4.5</td>
<td>3 x 3.6 x 2</td>
<td>Vishay</td>
</tr>
<tr>
<td>IHLP1212BZ-11</td>
<td>2.2 µH, ±20%</td>
<td>3.0</td>
<td>3 x 3.6 x 2</td>
<td>Vishay</td>
</tr>
<tr>
<td>SRP4020-3R3M</td>
<td>3.3 µH, ±20%</td>
<td>3.3</td>
<td>4.8 x 4 x 2</td>
<td>Bourns</td>
</tr>
<tr>
<td>VLC5045T-3R3N</td>
<td>3.3 µH, ±30%</td>
<td>4.0</td>
<td>5 x 5 x 4.5</td>
<td>TDK</td>
</tr>
</tbody>
</table>

(1) See Third-Party Products Disclaimer.
(2) Lower of \(I_{RMS}\) at 40°C rise or \(I_{SAT}\) at 30% drop.

The inductor value also determines the load current at which Power Save Mode is entered:

\[
I_{load(PSM)} = \frac{1}{2} \Delta I \text{I}_L
\]

Using Equation 8, this current level can be adjusted by changing the inductor value.

### 10.2.1.2.5 Output Capacitor

The recommended value for the output capacitor is 22 µF. The architecture of the TPS6213xA-Q1 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it is recommended to use an X7R or X5R dielectric. Using a higher value can have some advantages like smaller voltage ripple and a tighter DC output accuracy in Power Save Mode (see the Device Behavior Under Slow VBAT Ramp-Down and Ramp-Up Application Report).

**NOTE**

In power save mode, the output voltage ripple depends on the output capacitance, its ESR, and the peak inductor current. Using ceramic capacitors provides small ESR and low ripple.

### 10.2.1.2.6 Input Capacitor

For most applications, 10µF is sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage during transient events and also decouples the converter from the supply. A low ESR multilayer ceramic capacitor is recommended for best filtering and should be placed between PVIN and PGND as close as possible to those pins. Even though AVIN and PVIN must be supplied from the same input source, it's required to place a capacitance of 0.1µF from AVIN to AGND, to avoid potential noise coupling. An RC, low-pass filter from PVIN to AVIN may be used but is not required.

### 10.2.1.2.7 Soft-start Capacitor

A capacitance connected between SS/TR pin and AGND allows a user-programmable start-up slope of the output voltage. A constant current source supports 2.5 µA to charge the external capacitance. The capacitor required for a given soft-start ramp time for the output voltage is given by:

\[
C_{ss} = \frac{t_{ss} \cdot 2.5 \mu A}{1.25 V}
\]

where
• C_{SS} is the capacitance (F) required at the SS/TR pin
• t_{SS} is the desired soft-start ramp time (s).

\[ \text{(10)} \]

**NOTE**

**DC Bias effect:** High capacitance ceramic capacitors have a DC Bias effect, which have a strong influence on the final effective capacitance, therefore, the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

### 10.2.1.2.8 Tracking Function

If a tracking function is desired, the SS/TR pin can be used for this purpose by connecting it to an external tracking voltage. The output voltage tracks that voltage. If the tracking voltage is between 50 mV and 1.2 V, the FB pin tracks the SS/TR pin voltage as described in Equation 11 and shown in Figure 11.

\[ V_{FB} \approx 0.64 \cdot V_{SS/TR} \]

\[ \text{(11)} \]

![Figure 11. Voltage Tracking Relationship](image)

Once the SS/TR pin voltage reaches about 1.2 V, the internal voltage is clamped to the internal feedback voltage and the device goes to normal regulation. This works for rising and falling tracking voltages with the same behavior, as long as the input voltage is inside the recommended operating conditions. For decreasing SS/TR pin voltage, the device does not sink current from the output, so the resulting decrease of the output voltage can be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin, which is \( V_{IN} + 0.3 \) V.

If the input voltage drops into undervoltage lockout or even down to zero, the output voltage goes to zero, independent of the tracking voltage. Figure 12 shows how to connect devices to get ratiometric and simultaneous sequencing by using the tracking function.
Figure 12. Sequence for Ratiometric and Simultaneous Start-up

The resistive divider of R1 and R2 can be used to change the ramp rate of VOUT2 faster, slower, or the same as VOUT1.

A sequential start-up is achieved by connecting the PG pin of VOUT1 to the EN pin of VOUT2. Ratiometric start-up sequence happens if both supplies are sharing the same soft-start capacitor. Equation 10 calculates the soft-start time, though the SS/TR current has to be doubled. Details about these and other tracking and sequencing circuits are found in the Sequencing and Tracking With the TPS621-Family and TPS821-Family Application Report.

NOTE

If the voltage at the FB pin is below its typical value of 0.8 V, the output voltage accuracy can have a wider tolerance than specified.

10.2.1.2.9 Output Filter and Loop Stability

The devices of the TPS6213xA-Q1 family are internally compensated to be stable with L-C filter combinations corresponding to a corner frequency to be calculated with Equation 12:

\[ f_{LC} = \frac{1}{2\pi \sqrt{L \cdot C}} \]

(12)

Proven nominal values for inductance and ceramic capacitance are given in Table 3 and are recommended for use. Different values can work, but care has to be taken on the loop stability, which is affected. More information, including a detailed LC stability matrix, can be found in the Optimizing the TPS62130/40/50/60 Output Filter Application Report.

The TPS6213xA-Q1 includes an internal 25-pF feedforward capacitor connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, per Equation 13 and Equation 14:

\[ f_{zero} = \frac{1}{2\pi \cdot R_1 \cdot 25pF} \]

(13)
\[ f_{\text{pole}} = \frac{1}{2\pi \cdot 25 \text{pF}} \left( \frac{1}{R_1} + \frac{1}{R_2} \right) \]  

(14)

Though the TPS6213xA-Q1 is stable without the pole and zero being in a particular location, adjusting their location to the specific needs of the application can provide better performance in Power Save mode and improved transient response. An external feedforward capacitor can also be added. A more detailed discussion on the optimization for stability versus transient response can be found in the *Optimizing Transient Response of Internally Compensated DC-DC Converters Application Report* and *Feedforward Capacitor to Improve Stability and Bandwidth of TPS621/821-Family Application Report*. 


10.2.1.3 Application Curves

At $V_{IN} = 12$ V, $V_{OUT} = 3.3$ V and $T_A = 25^\circ$C, FSW = Low, (unless otherwise noted)
Figure 19. Efficiency versus Output Current

Figure 20. Efficiency versus Input Voltage

Figure 21. Efficiency versus Output Current

Figure 22. Efficiency versus Input Voltage

Figure 23. Efficiency versus Output Current

Figure 24. Efficiency versus Input Voltage
Figure 31. Switching Frequency versus Input Voltage

Figure 32. Switching Frequency versus Output Current

Figure 33. Switching Frequency versus Input Voltage

Figure 34. Switching Frequency versus Output Current

Figure 35. Typical Operation in PWM Mode (I_{OUT} = 1 A)

Figure 36. Typical Operation in Power Save Mode (I_{OUT} = 10 mA)
Figure 43. Maximum Ambient Temperature

L = 2.2 µH (XFL4020)  

TPS62130EVM
10.3 System Examples

10.3.1 Regulated Power LED Supply

The TPS62130A-Q1 can be used as a power supply for power LEDs. The FB pin can be easily set down to lower values than nominal by using the SS/TR pin. With that, the voltage drop when the sense resistor is low, avoiding excessive power loss. Since this pin provides 2.5 µA, the feedback pin voltage can be adjusted by an external resistor per Equation 15. This drop, proportional to the LED current, is used to regulate the output voltage (anode voltage) to a proper level to drive the LED. Both analog and PWM dimming are supported with the TPS62130A-Q1. Figure 44 shows an application circuit, tested with analog dimming.

The resistor at SS/TR sets the FB voltage to a level of about 300 mV and is calculated from Equation 15.

\[ V_{FB} = 0.64 \cdot 2.5 \mu A \cdot R_{SS/TR} \]  

(15)

The device now supplies a constant current, set by the resistor at the FB pin, by regulating the output voltage accordingly. The minimum input voltage has to be rated according the forward voltage needed by the LED used. More information is available in the Step-Down LED Driver With Dimming With the TPS61-Family and TPS821-Family Application Report.

10.3.2 Inverting Power Supply

The TPS62130A-Q1 can be used as inverting power supply by rearranging external circuitry as shown in Figure 45.

Since the former GND node now represents a voltage level below system ground, the voltage difference between \( V_{IN} \) and \( V_{OUT} \) has to be limited for operation to the maximum supply voltage of 17 V (see Equation 16).

\[ V_{IN} + |V_{OUT}| \leq V_{INmax} \]  

(16)
System Examples (continued)

The transfer function of the inverting power supply configuration differs from the buck mode transfer function, incorporating a Right Half Plane Zero additionally. The loop stability has to be adapted. An output capacitance of at least 22 µF is recommended. A detailed design example is given in the Using the TPS6215x in an Inverting Buck-Boost Topology Application Report.

10.3.3 Active Output Discharge

The TPS6213xA-Q1 pulls the PG pin low when the device is shut down by EN, UVLO, or thermal shutdown. Connecting PG to VOUT through a resistor can be used to discharge VOUT in those cases (see Figure 46).

The discharge rate can be adjusted by R3, which is also used to pull up the PG pin in normal operation. For reliability, keep the maximum current into the PG pin less than 10 mA.

10.3.4 Various Output Voltages

The transfer function of the inverting power supply configuration differs from the buck mode transfer function, incorporating a Right Half Plane Zero additionally. The loop stability has to be adapted. An output capacitance of at least 22 µF is recommended. A detailed design example is given in the Using the TPS6215x in an Inverting Buck-Boost Topology Application Report.

The TPS6213xA-Q1 pulls the PG pin low when the device is shut down by EN, UVLO, or thermal shutdown. Connecting PG to VOUT through a resistor can be used to discharge VOUT in those cases (see Figure 46).

The discharge rate can be adjusted by R3, which is also used to pull up the PG pin in normal operation. For reliability, keep the maximum current into the PG pin less than 10 mA.

10.3.4 Various Output Voltages

The transfer function of the inverting power supply configuration differs from the buck mode transfer function, incorporating a Right Half Plane Zero additionally. The loop stability has to be adapted. An output capacitance of at least 22 µF is recommended. A detailed design example is given in the Using the TPS6215x in an Inverting Buck-Boost Topology Application Report.

The TPS6213xA-Q1 pulls the PG pin low when the device is shut down by EN, UVLO, or thermal shutdown. Connecting PG to VOUT through a resistor can be used to discharge VOUT in those cases (see Figure 46).

The discharge rate can be adjusted by R3, which is also used to pull up the PG pin in normal operation. For reliability, keep the maximum current into the PG pin less than 10 mA.
System Examples (continued)

Figure 49. 2.5-V/3-A Power Supply

Figure 50. 1.8-V/3-A Power Supply

Figure 51. 1.5-V/3-A Power Supply
11 Power Supply Recommendations

The TPS6213xA-Q1 devices are designed to operate from a 3-V to 17-V input voltage supply. To avoid insufficient supply current due to line drop, ringing due to trace inductance at the VIN terminal, or supply peak current limitations, additional bulk capacitance can be required. If there is ringing that is caused by the interaction with the ceramic input capacitors, an electrolytic or tantalum type capacitor can be needed for damping.
12 Layout

12.1 Layout Guidelines

A proper layout is critical for a switched mode power supply operation, even more so for high switching frequencies, therefore, the PCB layout of the TPS6213x-A-Q1 demands careful attention to ensure operation and to get the specified performance. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation, and noise sensitivity. The layout also influences the thermal performance of the solution by its power dissipation capabilities.

See Figure 55 for the recommended layout of the TPS62130A-Q1, which is designed for common external ground connections, therefore, both AGND and PGND pins are directly connected to the Exposed Thermal Pad. On the PCB, the direct common ground connection of AGND and PGND to the Exposed Thermal Pad and the system ground (ground plane) is mandatory. Also, connect the VOS pin in the shortest way to the VOUT potential at the output capacitor.

Provide low inductive and resistive paths for loops with high di/dt, so paths conducting the switched load current are as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt, so the input and output capacitance are placed as close as possible to the IC pins and parallel wiring over long distances and narrow traces are avoided. Loops that conduct an alternating current must outline an area as small as possible, as this area is proportional to the energy radiated.

Sensitive nodes like FB and VOS need to be connected with short wires and not nearby high dv/dt signals, like SW. Since they carry information about the output voltage, they must be connected as close as possible to the actual output voltage (at the output capacitor). The capacitor on the SS/TR pin and AVIN as well as the FB resistors, R1 and R2, must be kept close to the IC and connect directly to those pins and the AGND pin.

The Exposed Thermal Pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation.

The recommended layout is implemented on the EVM and shown in the TPS62130EVM-505, TPS62140EVM-505, and TPS62150EVM-505 Evaluation Modules User’s Guide. Additionally, the EVM Gerber data are available for download here.

12.2 Layout Example
13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer
TI’S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

13.2 Related Links
The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

<table>
<thead>
<tr>
<th>PARTS</th>
<th>PRODUCT FOLDER</th>
<th>SAMPLE &amp; BUY</th>
<th>TECHNICAL DOCUMENTS</th>
<th>TOOLS &amp; SOFTWARE</th>
<th>SUPPORT &amp; COMMUNITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS62130A-Q1</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
<tr>
<td>TPS62133A-Q1</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
<tr>
<td>TPS6213013A-Q1</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
</tbody>
</table>

13.3 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Support Resources
TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided “AS IS” by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI’s views; see TI’s Terms of Use.

13.5 Trademarks
DCS-Control, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.7 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS6213013AQRGTRQ1</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGT</td>
<td>16</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>13013Q</td>
<td></td>
</tr>
<tr>
<td>TPS6213013AQRGTTQ1</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGT</td>
<td>16</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>13013Q</td>
<td></td>
</tr>
<tr>
<td>TPS62130AQRGTRQ1</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGT</td>
<td>16</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PA6IQ</td>
<td></td>
</tr>
<tr>
<td>TPS62130AQRGTTQ1</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGT</td>
<td>16</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PA6IQ</td>
<td></td>
</tr>
<tr>
<td>TPS62133AQRGTRQ1</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGT</td>
<td>16</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PA6JQ</td>
<td></td>
</tr>
<tr>
<td>TPS62133AQRGTTQ1</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGT</td>
<td>16</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PA6JQ</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE**: Product device recommended for new designs.

**LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines “RoHS” to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, “RoHS” products are suitable for use in specified lead-free processes. TI may reference these types of products as “Pb-Free”.

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines “Green” to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS62130A-Q1:
- Catalog: TPS62130A

NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product
**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**

![Reel Dimensions Diagram]

**TAPE DIMENSIONS**

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

![Quadrant Assignments Diagram]

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS6213013AQRGTRQ1</td>
<td>VQFN</td>
<td>RGT</td>
<td>16</td>
<td>3000</td>
<td>330.0</td>
<td>12.4</td>
<td>3.3</td>
<td>1.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
<td></td>
</tr>
<tr>
<td>TPS6213013AQRGTTQ1</td>
<td>VQFN</td>
<td>RGT</td>
<td>16</td>
<td>250</td>
<td>180.0</td>
<td>12.4</td>
<td>3.3</td>
<td>1.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
<td></td>
</tr>
<tr>
<td>TPS62130AQRGTRQ1</td>
<td>VQFN</td>
<td>RGT</td>
<td>16</td>
<td>3000</td>
<td>330.0</td>
<td>12.4</td>
<td>3.3</td>
<td>1.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
<td></td>
</tr>
<tr>
<td>TPS62130AQRGTTQ1</td>
<td>VQFN</td>
<td>RGT</td>
<td>16</td>
<td>250</td>
<td>180.0</td>
<td>12.4</td>
<td>3.3</td>
<td>1.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
<td></td>
</tr>
<tr>
<td>TPS62133AQRGTRQ1</td>
<td>VQFN</td>
<td>RGT</td>
<td>16</td>
<td>3000</td>
<td>330.0</td>
<td>12.4</td>
<td>3.3</td>
<td>1.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
<td></td>
</tr>
<tr>
<td>TPS62133AQRGTTQ1</td>
<td>VQFN</td>
<td>RGT</td>
<td>16</td>
<td>250</td>
<td>180.0</td>
<td>12.4</td>
<td>3.3</td>
<td>1.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
<td></td>
</tr>
</tbody>
</table>
# TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS6213013AQRGTRQ1</td>
<td>VQFN</td>
<td>RGT</td>
<td>16</td>
<td>3000</td>
<td>552.0</td>
<td>367.0</td>
<td>36.0</td>
</tr>
<tr>
<td>TPS6213013AQRGTTQ1</td>
<td>VQFN</td>
<td>RGT</td>
<td>16</td>
<td>250</td>
<td>552.0</td>
<td>185.0</td>
<td>36.0</td>
</tr>
<tr>
<td>TPS62130AQRGTRQ1</td>
<td>VQFN</td>
<td>RGT</td>
<td>16</td>
<td>3000</td>
<td>552.0</td>
<td>367.0</td>
<td>36.0</td>
</tr>
<tr>
<td>TPS62130AQRGTTQ1</td>
<td>VQFN</td>
<td>RGT</td>
<td>16</td>
<td>250</td>
<td>552.0</td>
<td>185.0</td>
<td>36.0</td>
</tr>
<tr>
<td>TPS62133AQRGTRQ1</td>
<td>VQFN</td>
<td>RGT</td>
<td>16</td>
<td>3000</td>
<td>552.0</td>
<td>367.0</td>
<td>36.0</td>
</tr>
<tr>
<td>TPS62133AQRGTTQ1</td>
<td>VQFN</td>
<td>RGT</td>
<td>16</td>
<td>250</td>
<td>552.0</td>
<td>185.0</td>
<td>36.0</td>
</tr>
</tbody>
</table>
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated