**1 Features**

- **Functional Safety-Capable**
  - Documentation available to aid functional safety system design
- Input voltage range: 2.7 V to 6 V
- Output voltage from 0.6 V to 5.5 V
- 1% feedback voltage accuracy (full temperature range)
- \( T_J = -40^\circ C \) to \(+150^\circ C\)
- Adjustable switching frequency and sync of 1.8 MHz to 4 MHz
- Forced PWM or PWM/PFM operation
- Quiescent current 17 µA typical
- Precise ENABLE input allows:
  - User-defined undervoltage lockout
  - Exact sequencing
- 100% duty cycle mode
- Active output discharge
- Power-good output with window comparator
- For device options with adjustable soft-start, see the TPS628511

**2 Applications**

- Motor drives
- Factory automation and control
- Building automation
- Test and measurement
- General purpose POL

**3 Description**

The TPS62850x is a family of pin-to-pin 1-A and 2-A high efficiency, easy-to-use synchronous step-down DC/DC converters. They are based on a peak current mode control topology. Low resistive switches allow up to 2-A continuous output current at high ambient temperature. The switching frequency is externally adjustable from 1.8 MHz to 4 MHz and can also be synchronized to an external clock in the same frequency range. In PWM/PFM mode, the TPS62850x automatically enters power save mode at light loads to maintain high efficiency across the whole load range. The TPS62850x provides a 1% output voltage accuracy in PWM mode, which helps design a power supply with high output voltage accuracy, fulfilling tight supply voltage requirements of digital processors and FPGA.

The TPS62850x is available in an 8-pin 1.6-mm × 2.1-mm SOT583 package.

**Device Information**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE(1)</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS628501</td>
<td>SOT583</td>
<td>1.6 mm × 2.1 mm (incl pins)</td>
</tr>
<tr>
<td>TPS628502</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

---

**Efficiency versus \( I_{OUT} \), \( V_{OUT} = 3.3 \) V**

---

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>March 2021</td>
<td>*</td>
<td>Initial release</td>
</tr>
</tbody>
</table>
### 5 Device Comparison Table

<table>
<thead>
<tr>
<th>DEVICE NUMBER</th>
<th>OUTPUT CURRENT</th>
<th>(V_{\text{OUT}}) DISCHARGE</th>
<th>FOLDBACK CURRENT LIMIT</th>
<th>SPREAD SPECTRUM CLOCKING (SSC)</th>
<th>SOFT START</th>
<th>OUTPUT VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS628501DRLR</td>
<td>1 A</td>
<td>ON</td>
<td>OFF</td>
<td>by COMP/FSET pin</td>
<td>internal 1 ms</td>
<td>adjustable</td>
</tr>
<tr>
<td>TPS628502DRLR</td>
<td>2 A</td>
<td>ON</td>
<td>OFF</td>
<td>by COMP/FSET pin</td>
<td>internal 1 ms</td>
<td>adjustable</td>
</tr>
</tbody>
</table>
6 Pin Configuration and Functions

![Figure 6-1. 8-Pin SOT583 DRL Package (Top View)](image)

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>I</td>
<td>This is the enable pin of the device. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected.</td>
</tr>
<tr>
<td>FB</td>
<td>I</td>
<td>Voltage feedback input. Connect the resistive output voltage divider to this pin.</td>
</tr>
<tr>
<td>GND</td>
<td></td>
<td>Ground pin</td>
</tr>
<tr>
<td>MODE/SYNC</td>
<td>I</td>
<td>The device runs in PFM/PWM mode when this pin is pulled low. When the pin is pulled high, the device runs in forced PWM mode. Do not leave this pin unconnected. The mode pin can also be used to synchronize the device to an external frequency. See Section 7.5 for the detailed specification for the digital signal applied to this pin for external synchronization.</td>
</tr>
<tr>
<td>COMP/FSET</td>
<td>I</td>
<td>Device compensation and frequency set input. A resistor from this pin to GND defines the compensation of the control loop as well as the switching frequency if not externally synchronized.</td>
</tr>
<tr>
<td>PG</td>
<td>O</td>
<td>Open-drain power-good output</td>
</tr>
<tr>
<td>SW</td>
<td></td>
<td>This is the switch pin of the converter and is connected to the internal Power MOSFETs.</td>
</tr>
<tr>
<td>VIN</td>
<td>I</td>
<td>Power supply input. Make sure the input capacitor is connected as close as possible between pin VIN and GND.</td>
</tr>
</tbody>
</table>

Table 6-1. Pin Functions
7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

<table>
<thead>
<tr>
<th>Pin voltage(2)</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>–0.3</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>SW (DC)</td>
<td>–0.3</td>
<td>V_{IN}+0.3</td>
<td>V</td>
</tr>
<tr>
<td>SW (AC, less than 10 ns)(3)</td>
<td>–3</td>
<td>10</td>
<td>V</td>
</tr>
<tr>
<td>COMP/FSET, PG</td>
<td>–0.3</td>
<td>V_{IN}+0.3</td>
<td>V</td>
</tr>
<tr>
<td>EN, MODE/SYNC, FB</td>
<td>–0.3</td>
<td>6.5</td>
<td>V</td>
</tr>
</tbody>
</table>

_{T_{stg}} Storage temperature | –65   | 150   | °C   |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) All voltage values are with respect to the network ground terminal

(3) While switching

7.2 ESD Ratings

<table>
<thead>
<tr>
<th>V_{(ESD)}</th>
<th>Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)</td>
<td>±2000</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)</td>
<td>±750</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>V_{IN}</th>
<th>Input voltage range</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>2.7</td>
<td>6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_{OUT}</td>
<td>Output voltage range</td>
<td>0.6</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>Effective inductance</td>
<td>0.32</td>
<td>0.47</td>
<td>1.2</td>
<td>μH</td>
</tr>
<tr>
<td>C_{OUT}</td>
<td>Effective output capacitance(1)</td>
<td>8</td>
<td>200</td>
<td>μF</td>
<td></td>
</tr>
<tr>
<td>C_{IN}</td>
<td>Effective input capacitance(1)</td>
<td>5</td>
<td>10</td>
<td>μF</td>
<td></td>
</tr>
<tr>
<td>R_{CF}</td>
<td></td>
<td>4.5</td>
<td>100</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>I_{SINK, PG}</td>
<td>Sink current at PG pin</td>
<td>0</td>
<td>2</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>T_{J}</td>
<td>Junction temperature</td>
<td>–40</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

(1) The values given for all the capacitors in the table are effective capacitance, which includes the DC bias effect. Due to the DC bias effect of ceramic capacitors, the effective capacitance is lower than the nominal value when a voltage is applied. Please check the manufacturer’s DC bias curves for the effective capacitance vs DC voltage applied. Further restrictions may apply. Please see the feature description for COMP/FSET about the output capacitance vs compensation setting and output voltage.
### 7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>TPS62850x</th>
<th>TPS62850x</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DRL (JEDEC)(^{(2)})</td>
<td>DRL (EVM)</td>
</tr>
<tr>
<td></td>
<td>8 PINS</td>
<td>8 PINS</td>
</tr>
<tr>
<td>(R_{\theta JA})</td>
<td>Junction-to-ambient thermal resistance</td>
<td>110</td>
</tr>
<tr>
<td>(R_{\theta JC(top)})</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>41.3</td>
</tr>
<tr>
<td>(R_{\theta JB})</td>
<td>Junction-to-board thermal resistance</td>
<td>20</td>
</tr>
<tr>
<td>(\Psi_{JT})</td>
<td>Junction-to-top characterization parameter</td>
<td>0.8</td>
</tr>
<tr>
<td>(Y_{JB})</td>
<td>Junction-to-board characterization parameter</td>
<td>20</td>
</tr>
<tr>
<td>(R_{\theta JC(bot)})</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>n/a</td>
</tr>
</tbody>
</table>

1. For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

2. JEDEC standard PCB with four layers, no thermal vias

### 7.5 Electrical Characteristics

Over operating junction temperature range \((T_J = –40°C \text{ to } +150°C)\) and \(V_{IN} = 2.7 \text{ V to } 6 \text{ V}\). Typical values at \(V_{IN} = 5 \text{ V}\) and \(T_J = 25°C\). (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SUPPLY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_Q) Quiescent current</td>
<td>(EN = V_{IN}), no load, device not switching, (MODE = GND), (V_{OUT} = 0.6 \text{ V})</td>
<td>17</td>
<td>36</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>(I_{SD,HI}) Shutdown current</td>
<td>(EN = \text{GND}), nominal value at (T_J = 25°C), max value at (T_J = 150°C)</td>
<td>1.5</td>
<td>48</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>(I_{SD}) Shutdown current</td>
<td>(EN = \text{GND}), (T_J = –40°C \text{ to } 85°C), including HSFET leakage</td>
<td>5.5</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>(V_{UVLO}) Undervoltage lockout threshold</td>
<td>(V_{IN}) rising</td>
<td>2.45</td>
<td>2.6</td>
<td>2.7</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(V_{IN}) falling</td>
<td>2.1</td>
<td>2.5</td>
<td>2.6</td>
<td>V</td>
</tr>
<tr>
<td>(T_{JSD}) Thermal shutdown threshold</td>
<td>(T_J) rising</td>
<td>170</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>(T_J) falling</td>
<td>15</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td><strong>CONTROL and INTERFACE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{EN,HI}) Input threshold voltage at (EN), rising edge</td>
<td></td>
<td>1.05</td>
<td>1.1</td>
<td>1.15</td>
<td>V</td>
</tr>
<tr>
<td>(V_{EN,IL}) Input threshold voltage at (EN), falling edge</td>
<td></td>
<td>0.96</td>
<td>1.0</td>
<td>1.05</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IH}) High-level input-threshold voltage at (MODE/SYNC)</td>
<td></td>
<td></td>
<td>1.1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(I_{EN,LKG}) Input leakage current into (EN)</td>
<td>(V_{IH} = V_{IN} \text{ or } V_{IL} = \text{GND})</td>
<td></td>
<td>125</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>(V_{IL}) Low-level input-threshold voltage at (MODE/SYNC)</td>
<td></td>
<td></td>
<td>0.3</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(I_{LKG}) Input leakage current into (MODE/SYNC)</td>
<td></td>
<td></td>
<td>100</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>(t_{\text{Delay}}) Enable delay time</td>
<td>Time from (EN) high to device starts switching; (V_{IN}) applied already</td>
<td>135</td>
<td>200</td>
<td>520</td>
<td>μs</td>
</tr>
<tr>
<td>(t_{\text{Delay}}) Enable delay time</td>
<td>Time from (EN) high to device starts switching; (V_{IN}) applied already, (V_{IN} \geq 3.3 \text{ V})</td>
<td></td>
<td></td>
<td>480</td>
<td>μs</td>
</tr>
<tr>
<td>(t_{\text{Ramp}}) Output voltage ramp time</td>
<td>Time the device starts switching to power good; device not in current limit</td>
<td>0.8</td>
<td>1.3</td>
<td>1.8</td>
<td>ms</td>
</tr>
<tr>
<td>(f_{SYNC}) Frequency range on (MODE/SYNC) pin for synchronization</td>
<td></td>
<td></td>
<td>1.8</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>Duty cycle of synchronization signal at (MODE/SYNC)</td>
<td></td>
<td>20%</td>
<td>80%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time to lock to external frequency</td>
<td></td>
<td></td>
<td>50</td>
<td></td>
</tr>
</tbody>
</table>
7.5 Electrical Characteristics (continued)

Over operating junction temperature range \((T_J = -40^\circ C \text{ to } +150^\circ C)\) and \(V_{IN} = 2.7\) V to 6 V. Typical values at \(V_{IN} = 5\) V and \(T_J = 25^\circ C\). (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistance from COMP/FSET to GND for logic low</td>
<td>Internal frequency setting with (f = 2.25) MHz</td>
<td>0</td>
<td>2.5</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>Voltage on COMP/FSET for logic high</td>
<td>Internal frequency setting with (f = 2.25) MHz</td>
<td>(V_{IN})</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{TH_PG})</td>
<td>UVP power good threshold voltage; DC level</td>
<td>Rising (%(V_{FB}))</td>
<td>92%</td>
<td>95%</td>
<td>98%</td>
</tr>
<tr>
<td>(V_{TH_PG})</td>
<td>OVP power good threshold voltage; DC level</td>
<td>Falling (%(V_{FB}))</td>
<td>97%</td>
<td>100%</td>
<td>103%</td>
</tr>
<tr>
<td>(V_{PG_OL})</td>
<td>Low-level output voltage at PG</td>
<td>(I_{SINK_PG} = 2) mA</td>
<td>0.07</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>(I_{PG_LKG})</td>
<td>Input leakage current into PG</td>
<td>(V_{PG} = 5) V</td>
<td>100</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>(t_{PG})</td>
<td>PG deglitch time</td>
<td>For a high level to low level transition on the power good output</td>
<td>40</td>
<td>µs</td>
<td></td>
</tr>
</tbody>
</table>

### OUTPUT

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{FB})</td>
<td>Feedback voltage, adjustable version</td>
<td>(V_{FB} = 0.6) V</td>
<td>0.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(I_{FB_LKG})</td>
<td>Input leakage current into FB, adjustable version</td>
<td>(V_{FB} = 0.6) V</td>
<td>1</td>
<td>70</td>
<td>nA</td>
</tr>
<tr>
<td>(V_{FB})</td>
<td>Feedback voltage accuracy</td>
<td>PWM, (V_{IN} \geq V_{OUT} + 1) (V)</td>
<td>–1%</td>
<td>1%</td>
<td></td>
</tr>
<tr>
<td>(V_{FB})</td>
<td>Feedback voltage accuracy</td>
<td>PFM, (V_{IN} \geq V_{OUT} + 1) (V), (V_{OUT} \geq 1.0) (V), (C_{o_eff} \geq 10) (\mu F), (L = 0.47) (\mu H)</td>
<td>–1%</td>
<td>2%</td>
<td></td>
</tr>
<tr>
<td>(V_{FB})</td>
<td>Feedback voltage accuracy</td>
<td>PFM, (V_{IN} \geq V_{OUT} + 1) (V), (V_{OUT} &lt; 1.0) (V), (C_{o_eff} \geq 15) (\mu F), (L = 0.47) (\mu H)</td>
<td>–1%</td>
<td>3%</td>
<td></td>
</tr>
<tr>
<td>(R_{DIS})</td>
<td>Output discharge resistance</td>
<td>PWM</td>
<td>0.05</td>
<td>%/A</td>
<td></td>
</tr>
<tr>
<td>(R_{DIS})</td>
<td>Output discharge resistance</td>
<td>PWM, (I_{OUT} = 1) (A), (V_{IN} \geq V_{OUT} + 1) (V)</td>
<td>0.02</td>
<td>%/V</td>
<td></td>
</tr>
<tr>
<td>(f_{SW})</td>
<td>PWM switching frequency range</td>
<td>MODE = high, see the FSET pin functionality about setting the switching frequency</td>
<td>1.8</td>
<td>2.25</td>
<td>4</td>
</tr>
<tr>
<td>(f_{SW})</td>
<td>PWM switching frequency range</td>
<td>MODE = low, see the FSET pin functionality about setting the switching frequency</td>
<td>1.8</td>
<td>3.5</td>
<td></td>
</tr>
<tr>
<td>(f_{SW})</td>
<td>PWM switching frequency</td>
<td>With COMP/FSET tied to GND or (V_{IN})</td>
<td>2.025</td>
<td>2.25</td>
<td>2.475</td>
</tr>
<tr>
<td>(f_{SW})</td>
<td>PWM switching frequency tolerance</td>
<td>Using a resistor from COMP/FSET to GND</td>
<td>–12%</td>
<td>12%</td>
<td></td>
</tr>
<tr>
<td>(t_{on_min})</td>
<td>Minimum on-time of high-side FET</td>
<td>(V_{IN} = 3.3) (V), (T_J = -40^\circ C \text{ to } 125^\circ C)</td>
<td>35</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{on_min})</td>
<td>Minimum on-time of low-side FET</td>
<td></td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>(R_{DS(ON)})</td>
<td>High-side FET on-resistance</td>
<td>(V_{IN} \geq 5) (V)</td>
<td>65</td>
<td>120</td>
<td>mΩ</td>
</tr>
<tr>
<td>(R_{DS(ON)})</td>
<td>Low-side FET on-resistance</td>
<td>(V_{IN} \geq 5) (V)</td>
<td>33</td>
<td>70</td>
<td>mΩ</td>
</tr>
<tr>
<td>(R_{DS(ON)})</td>
<td>High-side MOSFET leakage current</td>
<td>(T_J = -40^\circ C \text{ to } 85^\circ C)</td>
<td>3.5</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>(R_{DS(ON)})</td>
<td>Low-side MOSFET leakage current</td>
<td>(T_J = -40^\circ C \text{ to } 85^\circ C)</td>
<td>0.01</td>
<td>44</td>
<td>µA</td>
</tr>
<tr>
<td>(R_{DS(ON)})</td>
<td>Low-side MOSFET leakage current</td>
<td>(T_J = -40^\circ C \text{ to } 85^\circ C)</td>
<td>0.01</td>
<td>70</td>
<td>µA</td>
</tr>
<tr>
<td>(SW) leakage</td>
<td>(V(SW) = 0.6) (V), current into SW pin</td>
<td>–0.05</td>
<td>11</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>(I_{LIMH})</td>
<td>High-side FET switch current limit</td>
<td>DC value, for TPS628502; (V_{IN} = 3) (V) to 6 (V)</td>
<td>2.85</td>
<td>3.4</td>
<td>3.9</td>
</tr>
</tbody>
</table>
### 7.5 Electrical Characteristics (continued)

Over operating junction temperature range ($T_J = -40^\circ C$ to $+150^\circ C$) and $V_{IN} = 2.7$ V to 6 V. Typical values at $V_{IN} = 5$ V and $T_J = 25^\circ C$. (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{LMH}$</td>
<td>High-side FET switch current limit</td>
<td>2.1</td>
<td>2.6</td>
<td>3.0</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>DC value, for TPS628501; $V_{IN} = 3$ V to 6 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{LMNEG}$</td>
<td>Low-side FET negative current limit</td>
<td></td>
<td></td>
<td>1.8</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>DC value</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
7.6 Typical Characteristics

Figure 7-1. \( R_{DS(ON)} \) of High-side Switch

Figure 7-2. \( R_{DS(ON)} \) of Low-side Switch
8 Parameter Measurement Information

8.1 Schematic

![Schematic Diagram](image)

Figure 8-1. Measurement Setup

Table 8-1. List of Components

<table>
<thead>
<tr>
<th>REFERENCE</th>
<th>DESCRIPTION</th>
<th>MANUFACTURER (1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC</td>
<td>TPS628502</td>
<td>Texas Instruments</td>
</tr>
<tr>
<td>L</td>
<td>0.47-µH inductor DFE252012PD</td>
<td>Murata</td>
</tr>
<tr>
<td>C\textsubscript{IN}</td>
<td>2 × 10 µF / 6.3 V GRM188D70J106MA73</td>
<td>Murata</td>
</tr>
<tr>
<td>C\textsubscript{OUT}</td>
<td>2 × 10 µF / 6.3 V GRM188D70J106MA73 for ( V\text{OUT} \geq 1 \text{V} )</td>
<td>Murata</td>
</tr>
<tr>
<td>C\textsubscript{OUT}</td>
<td>3 × 10 µF / 6.3 V GRM188D70J106MA73 for ( V\text{OUT} &lt; 1 \text{V} )</td>
<td>Murata</td>
</tr>
<tr>
<td>R\textsubscript{CF}</td>
<td>8.06 kΩ</td>
<td>Any</td>
</tr>
<tr>
<td>C\textsubscript{FF}</td>
<td>10 pF</td>
<td>Any</td>
</tr>
<tr>
<td>R\textsubscript{1}</td>
<td>Depending on ( V\text{OUT} )</td>
<td>Any</td>
</tr>
<tr>
<td>R\textsubscript{2}</td>
<td>Depending on ( V\text{OUT} )</td>
<td>Any</td>
</tr>
<tr>
<td>R\textsubscript{3}</td>
<td>100 kΩ</td>
<td>Any</td>
</tr>
</tbody>
</table>

(1) See the Third-party Products Disclaimer.
9 Detailed Description

9.1 Overview

The TPS62850x synchronous switch mode power converters are based on a peak current mode control topology. The control loop is internally compensated.

To optimize the bandwidth of the control loop to the wide range of output capacitance that can be used with TPS62850x, the internal compensation has two settings. See Section 9.3.2. One out of the two compensation settings is chosen either by a resistor from COMP/FSET to GND, or by the logic state of this pin. The regulation network achieves fast and stable operation with small external components and low-ESR ceramic output capacitors. The devices can be operated without a feedforward capacitor on the output voltage divider, however, using a typically 10-pF feedforward capacitor improves transient response.

The devices support forced fixed frequency PWM operation with the MODE pin tied to a logic high level. The frequency is defined as either 2.25 MHz internally fixed when COMP/FSET is tied to GND or VIN, or in a range of 1.8 MHz to 4 MHz defined by a resistor from COMP/FSET to GND. Alternatively, the devices can be synchronized to an external clock signal in a range from 1.8 MHz to 4 MHz, applied to the MODE pin with no need for additional passive components. An internal PLL allows the internal clock to be changed to an external clock during operation. The synchronization to the external clock is done on a falling edge of the clock applied at MODE to the rising edge on the SW pin. This allows a roughly 180° phase shift when the SW pin is used to generate the synchronization signal for a second converter. When the MODE pin is set to a logic low level, the device operates in power save mode (PFM) at low output current and automatically transfers to fixed frequency PWM mode at higher output current. In PFM mode, the switching frequency decreases linearly based on the load to sustain high efficiency down to very low output current.

9.2 Functional Block Diagram

9.3 Feature Description

9.3.1 Precise Enable (EN)

The voltage applied at the enable pin of the TPS62850x is compared to a fixed threshold of 1.1 V for a rising voltage. This allows the user to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a power-up delay.

The Precise Enable input provides a user-programmable undervoltage lockout by adding a resistor divider to the input of the Enable pin.
The enable input threshold for a falling edge is typically 100 mV lower than the rising edge threshold. The TPS62850x starts operation when the rising threshold is exceeded. For proper operation, the enable (EN) pin must be terminated and must not be left floating. Pulling the enable pin low forces the device into shutdown, with a shutdown current of typically 1 μA. In this mode, the internal high-side and low-side MOSFETs are turned off and the entire internal control circuitry is switched off.

9.3.2 COMP/FSET

This pin allows to set three different parameters:

- Internal compensation settings for the control loop (two settings available)
- The switching frequency in PWM mode from 1.8 MHz to 4 MHz
- Enable/disable spread spectrum clocking (SSC)

A resistor from COMP/FSET to GND changes the compensation as well as the switching frequency. The change in compensation allows the user to adopt the device to different values of output capacitance. The resistor must be placed close to the pin to keep the parasitic capacitance on the pin to a minimum. The compensation setting is sampled at start-up of the converter, so a change in the resistor during operation only has an effect on the switching frequency but not on the compensation.

To save external components, the pin can also be directly tied to VIN or GND to set a pre-defined setting. Do not leave the pin floating.

The switching frequency has to be selected based on the input voltage and the output voltage to meet the specifications for the minimum on-time and minimum off-time.

Example: \( V_{\text{IN}} = 5 \, \text{V}, \, V_{\text{OUT}} = 0.6 \, \text{V} \to \text{duty cycle} = 0.6 \, \text{V} / 5 \, \text{V} = 0.12 \)

\[ \rightarrow t_{\text{on,min}} = \frac{1}{f_{\text{sw}}} \times 0.12 \]

\[ \rightarrow f_{\text{sw,max}} = \frac{1}{t_{\text{on,min}}} \times 0.12 = \frac{1}{0.05 \, \mu s} \times 0.12 = 2.4 \, \text{MHz} \]

The compensation range has to be chosen based on the minimum capacitance used. The capacitance can be increased from the minimum value as given in Table 9-1, up to the maximum of 200 μF in both compensation ranges. If the capacitance of an output changes during operation, for example, when load switches are used to connect or disconnect parts of the circuitry, the compensation has to be chosen for the minimum capacitance on the output. With large output capacitance, the compensation must be done based on that large capacitance to get the best load transient response. Compensating for large output capacitance but placing less capacitance on the output can lead to instability.

The switching frequency for the different compensation setting is determined by the following equations.

For compensation (comp) setting 1 with spread spectrum clocking (SSC) disabled:

\[
RCF(k\Omega) = \frac{18 MHz \cdot k\Omega}{f_s(MHz)}
\]  

(1)

For compensation (comp) setting 1 with spread spectrum clocking (SSC) enabled:

\[
RCF(k\Omega) = \frac{60 MHz \cdot k\Omega}{f_s(MHz)}
\]  

(2)

For compensation (comp) setting 2 with spread spectrum clocking (SSC) disabled:
\[ R_{CF}(k\Omega) = \frac{180 MHz \cdot k\Omega}{f_s(MHz)} \]  

(3)

### Table 9-1. Switching Frequency, Compensation and Spread Spectrum Clocking

<table>
<thead>
<tr>
<th>( R_{CF} )</th>
<th>COMPENSATION</th>
<th>SWITCHING FREQUENCY</th>
<th>MINIMUM OUTPUT CAPACITANCE FOR ( V_{OUT} &lt; 1 ) V</th>
<th>MINIMUM OUTPUT CAPACITANCE FOR ( 1 ) V ( \leq V_{OUT} &lt; 3.3 ) V</th>
<th>MINIMUM OUTPUT CAPACITANCE FOR ( V_{OUT} \geq 3.3 ) V</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 kΩ .. 4.5 kΩ</td>
<td>for smallest output capacitance (comp setting 1) SSC disabled</td>
<td>1.8 MHz (10 kΩ) .. 4 MHz (4.5 kΩ) according to Equation 1</td>
<td>15 ( \mu )F</td>
<td>10 ( \mu )F</td>
<td>8 ( \mu )F</td>
</tr>
<tr>
<td>33 kΩ .. 15 kΩ</td>
<td>for smallest output capacitance (comp setting 1) SSC enabled</td>
<td>1.8 MHz (33 kΩ) .. 4 MHz (15 kΩ) according to Equation 2</td>
<td>15 ( \mu )F</td>
<td>10 ( \mu )F</td>
<td>8 ( \mu )F</td>
</tr>
<tr>
<td>100 kΩ .. 45 kΩ</td>
<td>for best transient response (larger output capacitance) (comp setting 2) SSC disabled</td>
<td>1.8 MHz (100 kΩ) .. 4 MHz (45 kΩ) according to Equation 3</td>
<td>30 ( \mu )F</td>
<td>18 ( \mu )F</td>
<td>15 ( \mu )F</td>
</tr>
<tr>
<td>tied to GND</td>
<td>for smallest output capacitance (comp setting 1) SSC disabled</td>
<td>internally fixed 2.25 MHz</td>
<td>15 ( \mu )F</td>
<td>10 ( \mu )F</td>
<td>8 ( \mu )F</td>
</tr>
<tr>
<td>tied to ( V_{IN} )</td>
<td>for best transient response (larger output capacitance) (comp setting 2) SSC enabled</td>
<td>internally fixed 2.25 MHz</td>
<td>30 ( \mu )F</td>
<td>18 ( \mu )F</td>
<td>15 ( \mu )F</td>
</tr>
</tbody>
</table>

Refer to Section 10.1.3.2 for further details on the output capacitance required depending on the output voltage. A resistor value that is too high for \( R_{CF} \) is decoded as "tied to \( V_{IN} \)". A value below the lowest range is decoded as "tied to GND". The minimum output capacitance in Table 9-1 is for capacitors close to the output of the device. If the capacitance is distributed, a lower compensation setting can be required.

### 9.3.3 MODE / SYNC

When MODE/SYNC is set low, the device operates in PWM or PFM mode, depending on the output current. The MODE/SYNC pin allows you to force PWM mode when set high. The pin also allows you to apply an external clock in a frequency range from 1.8 MHz to 4 MHz for external synchronization. The specifications for the minimum on-time and minimum off-time must be observed when setting the external frequency. For use with external synchronization on the MODE/SYNC pin, the internal switching frequency must be set by \( R_{CF} \) to a similar value to the externally applied clock. This ensures that if the external clock fails, the switching frequency stays in the same range and the compensation settings are still valid.

### 9.3.4 Spread Spectrum Clocking (SSC)

The device offers spread spectrum clocking as an option. When SSC is enabled, the switching frequency is randomly changed in PWM mode when the internal clock is used. The frequency variation is typically between the nominal switching frequency and up to 288 kHz above the nominal switching frequency. When the device is externally synchronized by applying a clock signal to the MODE/SYNC pin, the TPS62850x follows the external clock and the internal spread spectrum block is turned off. SSC is also disabled during soft start.

### 9.3.5 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents misoperation of the device by switching off both the power FETs. When enabled, the device is fully operational for input voltages above the rising UVLO threshold and turns off if the input voltage trips below the threshold for a falling supply voltage.

### 9.3.6 Power Good Output (PG)

Power good is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level. It is driven by a window comparator. PG is held low when the device is disabled, in undervoltage lockout in thermal shutdown, and not in soft start. When the output voltage is in regulation hence, within the window defined in the electrical characteristics, the output is high impedance.
\( V_{IN} \) must remain present for the PG pin to stay low. If the power good output is not used, it is recommended to tie it to GND or leave open. The PG indicator features a de-glitch, as specified in the electrical characteristics, for the transition from "high impedance" to "low" of its output.

<table>
<thead>
<tr>
<th>EN</th>
<th>DEVICE STATUS</th>
<th>PG STATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>( V_{IN} &lt; 2 ) V</td>
<td>undefined</td>
</tr>
<tr>
<td>low</td>
<td>( V_{IN} \geq 2 ) V</td>
<td>low</td>
</tr>
<tr>
<td>high</td>
<td>( 2 \leq V_{IN} \leq UVLO ) OR in thermal shutdown OR ( V_{OUT} ) not in regulation OR device in soft start</td>
<td>low</td>
</tr>
<tr>
<td>high</td>
<td>( V_{OUT} ) in regulation</td>
<td>high impedance</td>
</tr>
</tbody>
</table>

### 9.3.7 Thermal Shutdown

The junction temperature \( (T_J) \) of the device is monitored by an internal temperature sensor. If \( T_J \) exceeds 170°C (typ), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and PG goes low. When \( T_J \) decreases below the hysteresis amount of typically 15°C, the converter resumes normal operation, beginning with soft start. During a PFM pause, the thermal shutdown is not active. After a PFM pause, the device needs up to 9 µs to detect a junction temperature that is too high. If the PFM burst is shorter than this delay, the device does not detect a junction temperature that is too high.

### 9.4 Device Functional Modes

#### 9.4.1 Pulse Width Modulation (PWM) Operation

The TPS62850x has two operating modes: forced PWM mode is discussed in this section and PWM/PFM as discussed in Section 9.4.2.

With the MODE/SYNC pin set to high, the TPS62850x operates with pulse width modulation in continuous conduction mode (CCM). The switching frequency is either defined by a resistor from the COMP pin to GND or by an external clock signal applied to the MODE/SYNC pin. With an external clock applied to MODE/SYNC, the TPS62850x follows the frequency applied to the pin. In general, the frequency range in forced PWM mode is 1.8 MHz to 4 MHz. However, the frequency needs to be in a range the TPS62850x can operate at, taking the minimum on-time into account.

#### 9.4.2 Power Save Mode Operation (PWM/PFM)

When the MODE/SYNC pin is low, power save mode is allowed. The device operates in PWM mode as long as the peak inductor current is above the PFM threshold of approximately 0.8 A. When the peak inductor current drops below the PFM threshold, the device starts to skip switching pulses. In power save mode, the switching frequency decreases with the load current maintaining high efficiency. In addition, the frequency set with the resistor on COMP/FSET must be in a range of 1.8 MHz to 3.5 MHz.

#### 9.4.3 100% Duty-Cycle Operation

The duty cycle of a buck converter operated in PWM mode is given as \( D = \frac{V_{OUT}}{V_{IN}} \). The duty cycle increases as the input voltage comes close to the output voltage and the off-time gets smaller. When the minimum off-time of typically 10 ns is reached, the TPS62850x skips switching cycles while it approaches 100% mode. In 100% mode, it keeps the high-side switch on continuously. The high-side switch stays turned on as long as the output voltage is below the target. In 100% mode, the low-side switch is turned off. The maximum dropout voltage in 100% mode is the product of the on-resistance of the high-side switch plus the series resistance of the inductor and the load current.

#### 9.4.4 Current Limit and Short Circuit Protection

The TPS62850x is protected against overload and short circuit events. If the inductor current exceeds the current limit \( I_{LIMH} \), the high-side switch is turned off and the low-side switch is turned on to ramp down the inductor current. The high-side switch turns on again only if the current in the low side-switch has decreased below the low side current limit. Due to internal propagation delay, the actual current can exceed the static current limit. The dynamic current limit is given as:
\[ I_{\text{peak(typ)}} = I_{\text{LIMH}} + \frac{V_I}{L} \cdot t_{\text{PD}} \]  

(4)

where

- \( I_{\text{LIMH}} \) is the static current limit as specified in the *Electrical Characteristics*
- \( L \) is the effective inductance at the peak current
- \( V_L \) is the voltage across the inductor (\( V_{\text{IN}} - V_{\text{OUT}} \))
- \( t_{\text{PD}} \) is the internal propagation delay of typically 50 ns

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high-side switch peak current can be calculated as follows:

\[ I_{\text{peak(typ)}} = I_{\text{LIMH}} + \frac{V_{\text{IN}} - V_{\text{OUT}}}{L} \cdot 50\text{ns} \]  

(5)

### 9.4.5 Foldback Current Limit and Short Circuit Protection

This is valid for devices where foldback current limit is enabled. Contact Texas Instruments for more information on this option.

When the device detects current limit for more than 1024 subsequent switching cycles, it reduces the current limit from its nominal value to typically 1.3 A. Foldback current limit is left when the current limit indication goes away. If device operation continues in current limit, after 3072 switching cycles, it tries for full current limit for 1024 switching cycles.

### 9.4.6 Output Discharge

The purpose of the discharge function is to ensure a defined down-ramp of the output voltage when the device is being disabled and to keep the output voltage close to 0 V when the device is off. The output discharge feature is only active once the TPS62850x has been enabled at least once since the supply voltage was applied. The discharge function is enabled as soon as the device is disabled, in thermal shutdown, or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active is typically 2 V. Output discharge is not activated during a current limit or foldback current limit event.

### 9.4.7 Soft Start

The internal soft-start circuitry controls the output voltage slope during start-up. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high impedance power sources or batteries. When EN is set high to start operation, the device starts switching after a delay of about 200 \( \mu \)s then the internal reference and hence \( V_{\text{OUT}} \) rises with a slope defined by an internally defined slope of 150 \( \mu \)s or 1 ms (OTP option).

### 9.4.8 Input Overvoltage Protection

When the input voltage exceeds the absolute maximum rating, the device is set to PFM mode so it cannot transfer energy from the output to the input.
10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Programming the Output Voltage

The output voltage of the TPS62850x is adjustable. It can be programmed for output voltages from 0.6 V to 5.5 V using a resistor divider from \( V_{OUT} \) to GND. The voltage at the FB pin is regulated to 600 mV. The value of the output voltage is set by the selection of the resistor divider from Equation 6. It is recommended to choose resistor values that allow a current of at least 2 µA, meaning the value of \( R_2 \) must not exceed 400 kΩ. Lower resistor values are recommended for highest accuracy and the most robust design.

\[
R_1 = R_2 \left( \frac{V_{OUT}}{V_{FB}} - 1 \right)
\]  

(6)

10.1.2 Inductor Selection

The TPS62850x family is designed for a nominal 0.47-µH inductor with a switching frequency of typically 2.25 MHz. Larger values can be used to achieve a lower inductor current ripple but they can have a negative impact on efficiency and transient response. Smaller values than 0.47 µH cause a larger inductor current ripple, which causes larger negative inductor current in forced PWM mode at low or no output current. For a higher or lower nominal switching frequency, the inductance must be changed accordingly. See Section 7.3 for details.

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PFM transition point, and efficiency. In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). Equation 7 calculates the maximum inductor current.

\[
I_{L,(max)} = I_{OUT,(max)} + \frac{\Delta I_{L,(max)}}{2}
\]

(7)

\[
\Delta I_{L,(max)} = \frac{V_{OUT} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)}{L_{min}} \cdot \frac{1}{f_{SW}}
\]

(8)

where

- \( I_{L,(max)} \) is the maximum inductor current
- \( \Delta I_{L,(max)} \) is the peak-to-peak inductor ripple current
- \( L_{min} \) is the minimum inductance at the operating point
### Table 10-1. Typical Inductors

<table>
<thead>
<tr>
<th>TYPE</th>
<th>INDUCTANCE [µH]</th>
<th>CURRENT [A] (1)</th>
<th>FOR DEVICE</th>
<th>NOMINAL SWITCHING FREQUENCY</th>
<th>DIMENSIONS [LxBxH] mm</th>
<th>MANUFACTURER(2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>XFL4015-471ME</td>
<td>0.47 µH, ±20%</td>
<td>3.5</td>
<td>TPS628501 / 502</td>
<td>2.25 MHz</td>
<td>4 × 4 × 1.6</td>
<td>Coilcraft</td>
</tr>
<tr>
<td>XFL4015-701ME</td>
<td>0.70 µH, ±20%</td>
<td>3.3</td>
<td>TPS628501 / 502</td>
<td>2.25 MHz</td>
<td>4 × 4 × 1.6</td>
<td>Coilcraft</td>
</tr>
<tr>
<td>XEL3520-801ME</td>
<td>0.80 µH, ±20%</td>
<td>2.0</td>
<td>TPS628501 / 502</td>
<td>2.25 MHz</td>
<td>3.5 × 3.2 × 2.0</td>
<td>Coilcraft</td>
</tr>
<tr>
<td>XEL3515-561ME</td>
<td>0.56 µH, ±20%</td>
<td>4.5</td>
<td>TPS628501 / 502</td>
<td>2.25 MHz</td>
<td>3.5 × 3.2 × 1.5</td>
<td>Coilcraft</td>
</tr>
<tr>
<td>XFL3012-681ME</td>
<td>0.68 µH, ±20%</td>
<td>2.1</td>
<td>TPS628501 / 502</td>
<td>2.25 MHz</td>
<td>3.0 × 3.0 × 1.2</td>
<td>Coilcraft</td>
</tr>
<tr>
<td>XPL2010-681ML</td>
<td>0.68 µH, ±20%</td>
<td>1.5</td>
<td>TPS628501</td>
<td>2.25 MHz</td>
<td>2 × 1.9 × 1</td>
<td>Coilcraft</td>
</tr>
<tr>
<td>DFE252012RD-R68M</td>
<td>0.68 µH, ±20%</td>
<td>see data sheet</td>
<td>TPS628501 / 502</td>
<td>2.25 MHz</td>
<td>2.5 × 2 × 1.2</td>
<td>Murata</td>
</tr>
<tr>
<td>DFE252012RD-R47M</td>
<td>0.47 µH, ±20%</td>
<td>see data sheet</td>
<td>TPS628501 / 502</td>
<td>2.25 MHz</td>
<td>2.5 × 2 × 1.2</td>
<td>Murata</td>
</tr>
<tr>
<td>DFE201612RD-R68M</td>
<td>0.68 µH, ±20%</td>
<td>see data sheet</td>
<td>TPS628501 / 502</td>
<td>2.25 MHz</td>
<td>2 × 1.6 × 1.2</td>
<td>Murata</td>
</tr>
<tr>
<td>DFE201612RD-R47M</td>
<td>0.47 µH, ±20%</td>
<td>see data sheet</td>
<td>TPS628501 / 502</td>
<td>2.25 MHz</td>
<td>2 × 1.6 × 1.2</td>
<td>Murata</td>
</tr>
</tbody>
</table>

(1) Lower of \(I_{\text{RMS}}\) at 20°C rise or \(I_{\text{SAT}}\) at 20% drop.

(2) See the Third-party Products Disclaimer.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. A margin of about 20% is recommended to add. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well.

### 10.1.3 Capacitor Selection

#### 10.1.3.1 Input Capacitor

For most applications, 10-µF nominal is sufficient and is recommended. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low-ESR multilayer ceramic capacitor (MLCC) is recommended for the best filtering and must be placed between \(V_{\text{IN}}\) and GND as close as possible to those pins.

#### 10.1.3.2 Output Capacitor

The architecture of the TPS62850x allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric. Using a higher value has advantages, like smaller voltage ripple and a tighter DC output accuracy in power save mode.

The COMP/FSET pin allows the user to select two different compensation settings based on the minimum capacitance used on the output. The maximum capacitance is 200 µF in any of the compensation settings. The minimum capacitance required on the output depends on the compensation setting and output voltage.

For output voltages below 1 V, the minimum increases linearly from 10 µF at 1 V to 15 µF at 0.6 V with the compensation setting for smallest output capacitance. Other compensation ranges are equivalent. See Table 9-1 for details.
10.2 Typical Application

![Typical Application Diagram]

Figure 10-1. Typical Application

10.2.1 Design Requirements

The design guidelines provide a component selection to operate the device within the recommended operating conditions.

10.2.2 Detailed Design Procedure

\[
R_1 = R_2 \left( \frac{V_{OUT}}{V_{FB}} - 1 \right)
\]  

(9)

With \(V_{FB} = 0.6\) V:

<table>
<thead>
<tr>
<th>NOMINAL OUTPUT VOLTAGE ( V_{OUT} )</th>
<th>( R_1 )</th>
<th>( R_2 )</th>
<th>( C_{FF} )</th>
<th>EXACT OUTPUT VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8 V</td>
<td>16.9 kΩ</td>
<td>51 kΩ</td>
<td>10 pF</td>
<td>0.7988 V</td>
</tr>
<tr>
<td>1.0 V</td>
<td>20 kΩ</td>
<td>30 kΩ</td>
<td>10 pF</td>
<td>1.0 V</td>
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<tr>
<td>1.1 V</td>
<td>39.2 kΩ</td>
<td>47 kΩ</td>
<td>10 pF</td>
<td>1.101 V</td>
</tr>
<tr>
<td>1.2 V</td>
<td>68 kΩ</td>
<td>68 kΩ</td>
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<td>1.2 V</td>
</tr>
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<td>76.8 kΩ</td>
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<td>1.5 V</td>
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<tr>
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<td>40.2 kΩ</td>
<td>10 pF</td>
<td>1.803 V</td>
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<tr>
<td>2.5 V</td>
<td>47.5 kΩ</td>
<td>15 kΩ</td>
<td>10 pF</td>
<td>2.5 V</td>
</tr>
<tr>
<td>3.3 V</td>
<td>88.7 kΩ</td>
<td>19.6 kΩ</td>
<td>10 pF</td>
<td>3.315 V</td>
</tr>
</tbody>
</table>
10.2.3 Application Curves

All plots have been taken with a nominal switching frequency of 2.25 MHz when set to PWM mode, unless otherwise noted. The BOM is according to Table 8-1.

Output Current (A)

Efficiency (%)

50
55
60
65
70
75
80
85
90
95
100

1m 10m 100m 1

D002

V_IN = 4.0 V
V_IN = 5.0 V
V_IN = 6.0 V

V_OUT = 3.3 V

Figure 10-2. Efficiency versus Output Current

PFM

T_A = 25°C

Output Current (A)

Efficiency (%)

75
80
85
90
95
100

1 m 0.5 1.5

D002

V_IN = 2.7 V
V_IN = 3.3 V
V_IN = 4.0 V
V_IN = 5.0 V
V_IN = 6.0 V

V_OUT = 1.8 V

Figure 10-4. Efficiency versus Output Current

PFM

T_A = 25°C

Output Current (A)

Efficiency (%)

75
80
85
90

1 m 0.5 1.5

D002

V_IN = 2.7 V
V_IN = 3.3 V
V_IN = 4.0 V
V_IN = 5.0 V
V_IN = 6.0 V

V_OUT = 1.1 V

Figure 10-6. Efficiency versus Output Current

PFM

T_A = 25°C
Figure 10-8. Efficiency versus Output Current

Figure 10-9. Efficiency versus Output Current

Figure 10-10. Output Voltage versus Output Current

Figure 10-11. Output Voltage versus Output Current

Figure 10-12. Output Voltage versus Output Current

Figure 10-13. Output Voltage versus Output Current
Figure 10-14. Output Voltage versus Output Current

Figure 10-15. Output Voltage versus Output Current

Figure 10-16. Output Voltage versus Output Current

Figure 10-17. Output Voltage versus Output Current

Figure 10-18. Load Transient Response

Figure 10-19. Load Transient Response
Figure 10-20. Load Transient Response

Figure 10-21. Load Transient Response

Figure 10-22. Load Transient Response

Figure 10-23. Load Transient Response

Figure 10-24. Load Transient Response

Figure 10-25. Load Transient Response
Figure 10-26. Load Transient Response

V\text{OUT} = 0.6 \text{ V}  
V\text{IN} = 3.3 \text{ V}  
I\text{OUT} = 0.2 \text{ A} \text{ to } 1.8 \text{ A} \text{ to } 0.2 \text{ A}  
\text{TA} = 25^\circ \text{C}  

Figure 10-27. Load Transient Response

V\text{OUT} = 0.6 \text{ V}  
V\text{IN} = 3.3 \text{ V}  
I\text{OUT} = 0.2 \text{ A} \text{ to } 1.8 \text{ A} \text{ to } 0.2 \text{ A}  
\text{TA} = 25^\circ \text{C}  

Figure 10-28. Line Transient Response

V\text{OUT} = 3.3 \text{ V}  
I\text{OUT} = 0.2 \text{ A}  
V\text{IN} = 4.5 \text{ V} \text{ to } 5.5 \text{ V} \text{ to } 4.5 \text{ V}  
\text{TA} = 25^\circ \text{C}  

Figure 10-29. Line Transient Response

V\text{OUT} = 3.3 \text{ V}  
I\text{OUT} = 2 \text{ A}  
V\text{IN} = 4.5 \text{ V} \text{ to } 5.5 \text{ V} \text{ to } 4.5 \text{ V}  
\text{TA} = 25^\circ \text{C}  

Figure 10-30. Line Transient Response

V\text{OUT} = 1.8 \text{ V}  
I\text{OUT} = 0.2 \text{ A}  
V\text{IN} = 4.5 \text{ V} \text{ to } 5.5 \text{ V} \text{ to } 4.5 \text{ V}  
\text{TA} = 25^\circ \text{C}  

Figure 10-31. Line Transient Response

V\text{OUT} = 1.8 \text{ V}  
I\text{OUT} = 2 \text{ A}  
V\text{IN} = 4.5 \text{ V} \text{ to } 5.5 \text{ V} \text{ to } 4.5 \text{ V}  
\text{TA} = 25^\circ \text{C}
Figure 10-32. Line Transient Response

$V_{\text{OUT}} = 1.2 \text{ V}$
$I_{\text{OUT}} = 0.2 \text{ A}$

$V_{\text{IN}} = 4.5 \text{ V to 5.5 V to 4.5 V}$

$T_A = 25^\circ \text{C}$

Figure 10-33. Line Transient Response

$V_{\text{OUT}} = 1.2 \text{ V}$
$I_{\text{OUT}} = 2 \text{ A}$

$V_{\text{IN}} = 4.5 \text{ V to 5.5 V to 4.5 V}$

$T_A = 25^\circ \text{C}$

Figure 10-34. Line Transient Response

$V_{\text{OUT}} = 1.0 \text{ V}$
$I_{\text{OUT}} = 0.2 \text{ A}$

$V_{\text{IN}} = 4.5 \text{ V to 5.5 V to 4.5 V}$

$T_A = 25^\circ \text{C}$

Figure 10-35. Line Transient Response

$V_{\text{OUT}} = 1.0 \text{ V}$
$I_{\text{OUT}} = 2 \text{ A}$

$V_{\text{IN}} = 4.5 \text{ V to 5.5 V to 4.5 V}$

$T_A = 25^\circ \text{C}$

Figure 10-36. Line Transient Response

$V_{\text{OUT}} = 0.6 \text{ V}$
$I_{\text{OUT}} = 0.2 \text{ A}$

$V_{\text{IN}} = 3.0 \text{ V to 3.6 V to 3.0 V}$

$T_A = 25^\circ \text{C}$

Figure 10-37. Line Transient Response

$V_{\text{OUT}} = 0.6 \text{ V}$
$I_{\text{OUT}} = 2 \text{ A}$

$V_{\text{IN}} = 3.0 \text{ V to 3.6 V to 3.0 V}$

$T_A = 25^\circ \text{C}$
Figure 10-38. Output Voltage Ripple

\[ V_{OUT} = 3.3 \text{ V} \quad \text{PFM} \quad T_A = 25^\circ\text{C} \]
\[ V_{IN} = 5 \text{ V} \quad I_{OUT} = 0.2 \text{ A} \]

Figure 10-39. Output Voltage Ripple

\[ V_{OUT} = 3.3 \text{ V} \quad \text{PWM} \quad T_A = 25^\circ\text{C} \]
\[ V_{IN} = 5 \text{ V} \quad I_{OUT} = 2 \text{ A} \]

Figure 10-40. Output Voltage Ripple

\[ V_{OUT} = 1.8 \text{ V} \quad \text{PFM} \quad T_A = 25^\circ\text{C} \]
\[ V_{IN} = 5 \text{ V} \quad I_{OUT} = 0.2 \text{ A} \]

Figure 10-41. Output Voltage Ripple

\[ V_{OUT} = 1.8 \text{ V} \quad \text{PWM} \quad T_A = 25^\circ\text{C} \]
\[ V_{IN} = 5 \text{ V} \quad I_{OUT} = 2 \text{ A} \]

Figure 10-42. Output Voltage Ripple

\[ V_{OUT} = 1.2 \text{ V} \quad \text{PFM} \quad T_A = 25^\circ\text{C} \]
\[ V_{IN} = 5 \text{ V} \quad I_{OUT} = 0.2 \text{ A} \]

Figure 10-43. Output Voltage Ripple

\[ V_{OUT} = 1.2 \text{ V} \quad \text{PWM} \quad T_A = 25^\circ\text{C} \]
\[ V_{IN} = 5 \text{ V} \quad I_{OUT} = 2 \text{ A} \]
Figure 10-44. Output Voltage Ripple

\[ V_{\text{OUT}} = 1.0 \, \text{V} \]
\[ V_{\text{IN}} = 5 \, \text{V} \]
\[ I_{\text{OUT}} = 0.2 \, \text{A} \]

\[ T_{\text{A}} = 25^\circ \text{C} \]

Figure 10-45. Output Voltage Ripple

\[ V_{\text{OUT}} = 1.0 \, \text{V} \]
\[ V_{\text{IN}} = 5 \, \text{V} \]
\[ I_{\text{OUT}} = 2 \, \text{A} \]

\[ T_{\text{A}} = 25^\circ \text{C} \]

Figure 10-46. Output Voltage Ripple

\[ V_{\text{OUT}} = 0.6 \, \text{V} \]
\[ V_{\text{IN}} = 3.3 \, \text{V} \]
\[ I_{\text{OUT}} = 0.2 \, \text{A} \]

\[ T_{\text{A}} = 25^\circ \text{C} \]

Figure 10-47. Output Voltage Ripple

\[ V_{\text{OUT}} = 0.6 \, \text{V} \]
\[ V_{\text{IN}} = 3.3 \, \text{V} \]
\[ I_{\text{OUT}} = 2 \, \text{A} \]

\[ T_{\text{A}} = 25^\circ \text{C} \]

Figure 10-48. Start-Up Timing

\[ V_{\text{OUT}} = 3.3 \, \text{V} \]
\[ V_{\text{IN}} = 5 \, \text{V} \]
\[ I_{\text{OUT}} = 2 \, \text{A} \]

\[ T_{\text{A}} = 25^\circ \text{C} \]

Figure 10-49. Start-Up Timing

\[ V_{\text{OUT}} = 1.8 \, \text{V} \]
\[ V_{\text{IN}} = 5 \, \text{V} \]
\[ I_{\text{OUT}} = 2 \, \text{A} \]

\[ T_{\text{A}} = 25^\circ \text{C} \]
10.3 System Examples

10.3.1 Synchronizing to an External Clock

The TPS62850x can be externally synchronized by applying an external clock on the MODE/SYNC pin. There is no need for any additional circuitry as long as the input signal meets the requirements given in the electrical specifications. The clock can be applied / removed during operation, allowing an externally defined fixed frequency to be switched to a power-save mode or to internal fixed frequency operation.

The value of the $R_{CF}$ resistor must be chosen such that the internally defined frequency and the externally applied frequency are close to each other. This ensures a smooth transition from internal to external frequency and vice versa.
Figure 10-53. Schematic using External Synchronization

Vin = 5 V  \quad R_{CF} = 8.06 k\Omega  \quad I_{OUT} = 0.1 A

Vout = 1.8 V  \quad f_{EXT} = 2.5 MHz

Figure 10-54. Switching from External Synchronization to Power-Save Mode (PFM)

Vin = 5 V  \quad R_{CF} = 8.06 k\Omega  \quad I_{OUT} = 0.1 A

Vout = 1.8 V  \quad f_{EXT} = 2.5 MHz

Figure 10-55. Switching from External Synchronization to Internal Fixed Frequency
11 Power Supply Recommendations

The TPS62850x device family does not have special requirements for its input power supply. The output current of the input power supply needs to be rated according to the supply voltage, output voltage, and output current of the TPS62850x.

12 Layout

12.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore, the PCB layout of the TPS62850x demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like the following:

- Poor regulation (both in Section 12.2 and load)
- Stability and accuracy weaknesses
- Increased EMI radiation
- Noise sensitivity

See Figure 12-1 for the recommended layout of the TPS62850x, which is designed for common external ground connections. The input capacitor must be placed as close as possible between the VIN and GND pin.

Provide low inductive and resistive paths for loops with high di/dt. Therefore, paths conducting the switched load current must be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt. Therefore, the input and output capacitance must be placed as close as possible to the IC pins and parallel wiring over long distances and narrow traces must be avoided. Loops which conduct an alternating current must outline an area as small as possible since this area is proportional to the energy radiated.

Sensitive nodes like FB need to be connected with short wires and not nearby high dv/dt signals (for example, SW). As they carry information about the output voltage, they must be connected as close as possible to the actual output voltage (at the output capacitor). The FB resistors, R₁ and R₂, must be kept close to the IC and be connected directly to the pin and the system ground plane.

The package uses the pins for power dissipation. Thermal vias on the VIN and GND pins help to spread the heat into the PCB.

The recommended layout is implemented on the EVM and shown in the TPS628502EVM-092 Evaluation Module User's Guide.
12.2 Layout Example

Solution size = 30mm$^2$

Figure 12-1. Example Layout
13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES
OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER
ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

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To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on
Subscribe to updates to register and receive a weekly digest of any product information that has changed. For
change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight
from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do
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13.4 Trademarks

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13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled
with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may
be more susceptible to damage because very small parametric changes could cause the device not to meet its published
specifications.

13.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.
14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
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<tbody>
<tr>
<td>TPS628501DRLR</td>
<td>ACTIVE</td>
<td>SOT-5X3</td>
<td>DRL</td>
<td>8</td>
<td>4000</td>
<td>RoHS &amp; Green</td>
<td>Call TI</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>100</td>
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<tr>
<td>TPS628502DRLR</td>
<td>ACTIVE</td>
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<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>200</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE**: Product device recommended for new designs.

**LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE**: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS628501, TPS628502:

- Automotive: TPS628501-Q1, TPS628502-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
**Tape and Reel Information**

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
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<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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<td>DRL</td>
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<td>8.0</td>
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<td>2.75</td>
<td>1.9</td>
<td>0.8</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
</tbody>
</table>

**Diagram Notes:**
- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers
# TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
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<th>Length (mm)</th>
<th>Width (mm)</th>
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<tr>
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<td>4000</td>
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<td>8</td>
<td>4000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.
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