4.5-V to 18-V Input, High Current, Synchronous Step Down Three DC-DC Converter with Integrated FET and 2 Power Switches

Check for Samples: TPS65288

FEATURES

- **Wide Input Supply Voltage Range: 4.5 V - 18 V**
- **0.8-V, 1% Accuracy Reference**
- **Continuous Loading: 3 A (Buck1), 2 A (Buck2 and 3)**
- **Maximum Current: 3.5 A (Buck 1), 2.5 A (Buck2 and 3)**
- **300-kHz – 2.2-MHz Switching Frequency Set By External Resistor**
- **External Enable Pins With Built-In Current Source for Easy Sequencing**
- **External Soft Start Pins**
- **Adjustable Cycle-by-Cycle Current Limit Set by External Resistor**
- **Current-Mode Control With Simple Compensation Circuit**
- **Pulse Skipping Mode to Achieve High Light Load Efficiency, Allowing for an Output Ripple Better than 2%**
- **Forced PWM Mode**
- **Support Pre-Biased Outputs**
- **Power Good Supervisor and Reset Generator**
- **2 USB Power Switches current limiting at typical 1.2A (0.8/1.0/1.4/1.6/1.8/2.0/2.2A Available with Manufacture Trim Options)**
- **Small, Thermally Efficient 40-Pin 6-mm x 6-mm RHA (QFN) package**
- **-40°C to 125°C Junction Temperature Range**

DESCRIPTION/ORDERING INFORMATION

TPS65288 is a power management IC with three step-down buck converters. Both high-side and low-side MOSFETs are integrated to provide fully synchronous conversion with higher efficiency. The converters are designed to simplify its application while giving the designer the option to optimize their usage according to the target application.

The converters can operate in 5-, 9-, 12- or 15-V systems. The output voltage can be set externally using a resistor divider to any value between 0.8 V and the input supply minus the resistive drops on the converter path. Each converter features enable pin that allows a delayed start-up for sequencing purposes, soft start pin that allows adjustable soft-start time by choosing the soft-start capacitor, and a current limit (RLIM) pin that enables designer to adjust current limit by selecting an external resistor and optimize the choice of inductor. All converters operate in 'hiccup mode': Once an over-current lasting more than 10 ms is sensed in any of the converters, they will shut down for 10 ms and then the start-up sequencing will be tried again. If the overload has been removed, the converter will ramp up and operate normally. If this is not the case the converter will see another over-current event and shuts down again repeating the cycle (hiccup) until the failure is cleared. If an overload condition lasts for less than 10 ms, only the relevant converter affected will shut-down and re-start and no global hiccup mode will occur.

The switching frequency of the converters is set by an external resistor connected to ROSC pin. The switching regulators are designed to operate from 300 kHz to 2.2 MHz. The converters operate with 180° phase between then to minimize the input filter requirements. All converters have peak current mode control which simplifies external frequency compensation.

The device has a built-in slope compensation ramp. The slope compensation can prevent sub harmonic oscillations in peak current mode control. A traditional type II compensation network can stabilize the system and achieve fast transient response. Moreover, an optional capacitor in parallel with the upper resistor of the feedback divider provides one more zero and makes the crossover frequency over 100 kHz.

All converters feature an automatic low power pulse skipping mode (PSM) which improves efficiency during light loads and standby operation, while guaranteeing a very low output ripple, allowing for a value of less than 2% at low output voltages.

The device incorporates an overvoltage transient protection circuit to minimize voltage overshoot. The OVP feature minimizes the output overshoot by implementing a circuit to compare the FB pin voltage to OVP threshold which is 106% of the internal voltage reference. If the FB pin voltage is greater than the OVTP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVP lower threshold which is 104%, the high side MOSFET is allowed to turn on the next clock cycle.

TPS65288 features a supervisor circuit which monitors each buck's output and the PGOOD pin is asserted once sequencing is done. The PGOOD pin is an open drain output. The PGOOD pin is pulled low when any buck converter is pulled below 85% of the nominal output voltage. The PGOOD is pulled up when all converter outputs are more than 90% of its nominal output voltage. The default reset time is 100 ms. The polarity of the PGOOD is active high.

The 2 USB switches provide up to 1.2A of current as required by downstream USB devices. When the output load exceeds the current-limit threshold or a short is present, the PMU limits the output current to a safe level by switching into a constant-current mode and pulling the over current logic output low. When continuous heavy overloads or short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal warning protection circuit shuts off the USB switch and allows the buck converters to carry on operating.

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 160°C. The thermal shutdown forces the device to stop operating when the junction temperature exceeds thermal trip threshold. Once the die temperature decreases below 140°C, the device reinitiates the power up sequence. The thermal shutdown hysteresis is 20°C.

ORDERING INFORMATION(1)

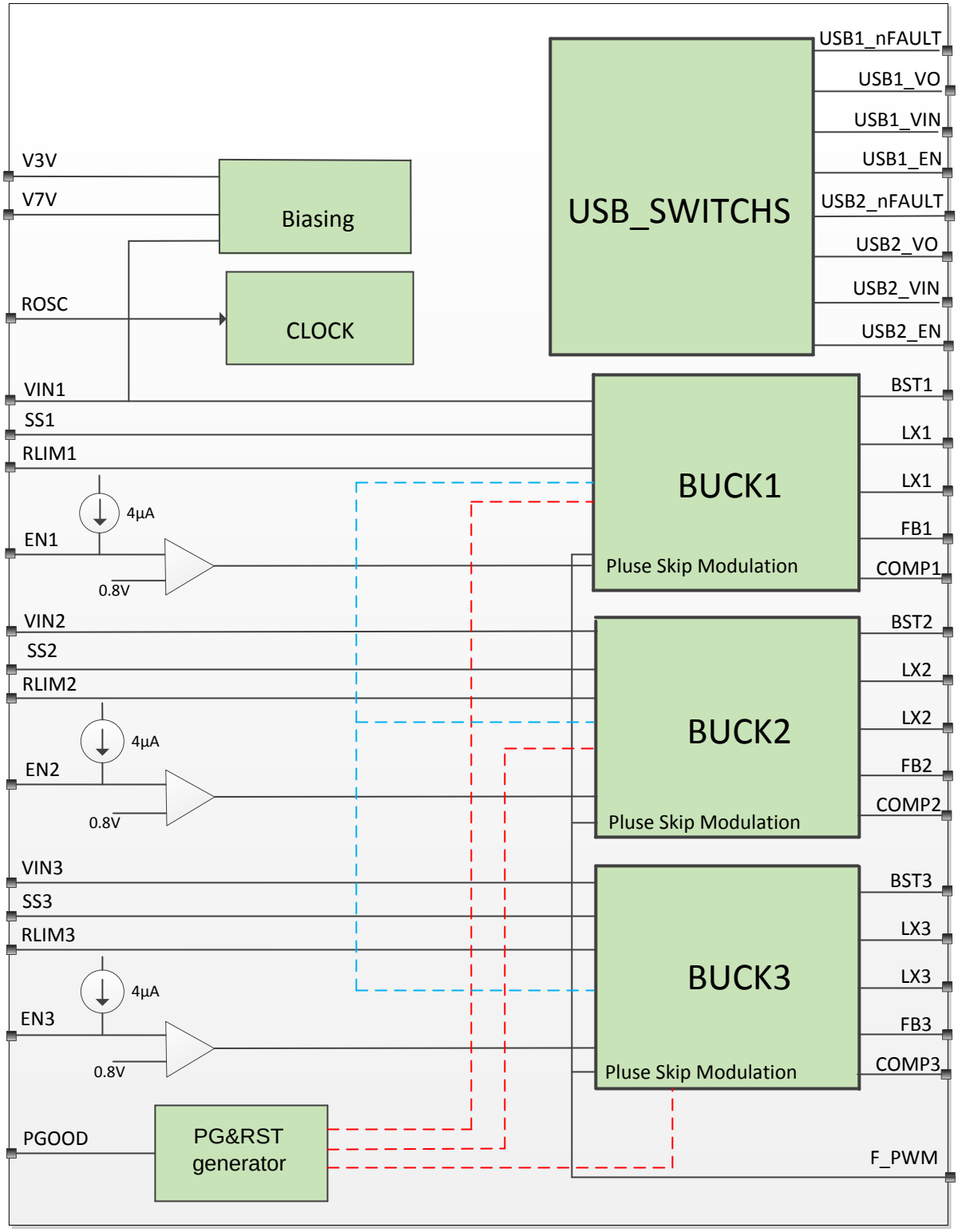
T_A	PACKAGE(2)		PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	40-Pin (QFN) - RHA	Reel of 2500	TPS65288RHAR	TPS65288

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

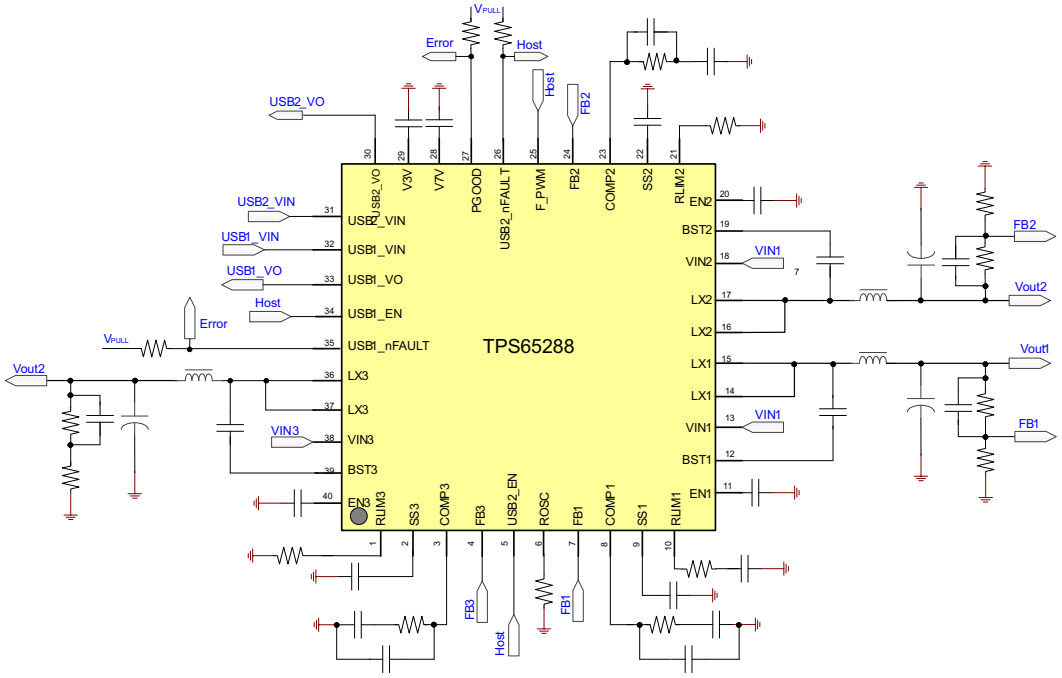
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

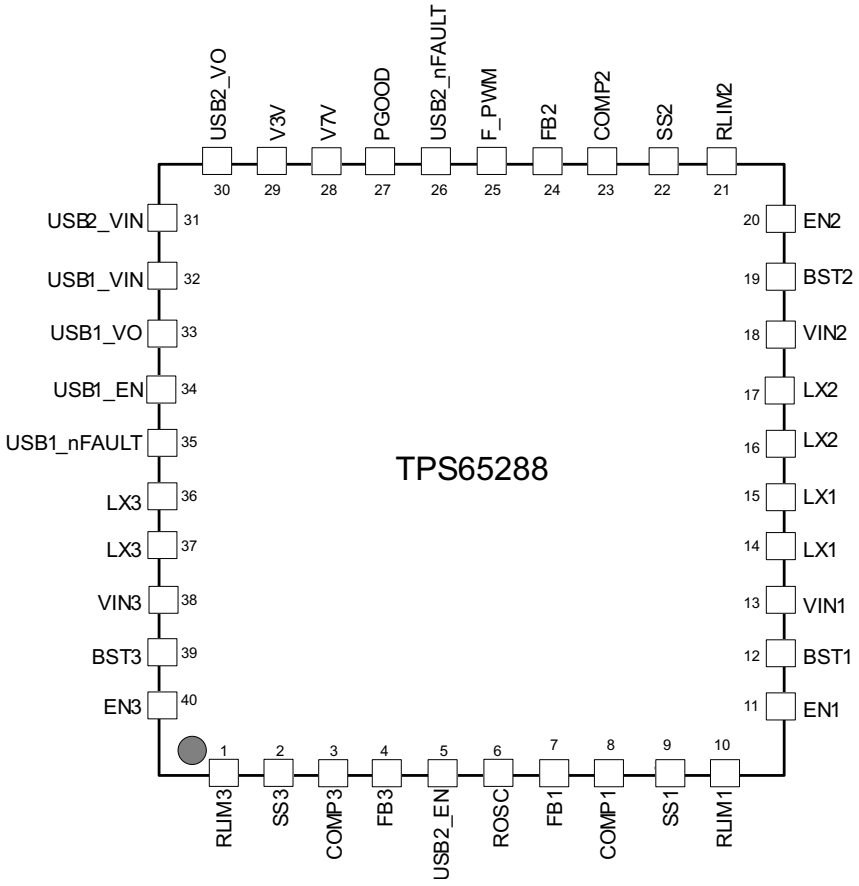
FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION



PIN OUT


TPS65288
1 RLIM3
2 SS3
3 COMP3
4 FB3
5 USB2_EN
6 ROSC
7 FB1
8 COMP1
9 SS1
10 RLIM1
11 EN1
12 BST1
13 VIN1
14 LX1
15 LX1
16 LX2
17 LX2
18 VIN2
19 BST2
20 EN2
21 RLIM2
22 SS2
23 COMP2
24 FB2
25 F_PWM
26 USB2_nFAULT
27 PGOOD
28 V7V
29 V3V
30 USB2_VO
31 USB2_VIN
32 USB1_VIN
33 USB1_VO
34 USB1_EN
35 USB1_nFAULT
36 LX3
37 LX3
38 VIN3
39 BST3
40 EN3

TERMINAL FUNCTIONS

NAME	NO.	I/O	DESCRIPTION
RLIM3	1	I	Current limit setting for Buck3. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
SS3	2	I	Soft start pin for Buck3. Fit a small ceramic capacitor to this pin to set the converter soft start time.
COMP3	3	O	Compensation for Buck3. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
FB3	4	I	Feedback pin for Buck3. Connect a divider set to 0.8 V from the output of the converter to ground.
USB2_EN	5	I	Enable input, high turns on the switch
ROSC	6	I	Oscillator set. This resistor sets the frequency of internal autonomous clock.
FB1	7	I	Feedback pin for Buck1. Connect a divider set to 0.8 V from the output of the converter to ground.
COMP1	8	O	Compensation pin for Buck1. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
SS1	9	I	Soft-start pin for Buck1. Fit a small ceramic capacitor to this pin to set the converter soft-start time.
RLIM1	10	I	Current limit setting pin for Buck1. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
EN1	11	I	Enable pin for Buck1. A high signal on this pin enables the regulator Buck. For a delayed start-up add a small ceramic capacitor from this pin to ground.
BST1	12		Bootstrap capacitor for Buck1. Fit a 47-nF ceramic capacitor from this pin to the switching node.
VIN1	13	I	Input supply for Buck1. Fit a 10-µF ceramic capacitor close to this pin.
LX1	14, 15	O	Switching node for Buck1
LX2	16, 17	O	Switching node for Buck2
VIN2	18	I	Input supply for Buck2. Fit a 10-µF ceramic capacitor close to this pin.
BST2	19		Bootstrap capacitor for Buck2. Fit a 47-nF ceramic capacitor from this pin to the switching node.
EN2	20	I	Enable pin for Buck2. A high signal on this pin enables the regulator. For a delayed start-up add a small ceramic capacitor from this pin to ground.
RLIM2	21	I	Current limit setting pin for Buck2. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
SS2	22	I	Soft-start pin for Buck2. Fit a small ceramic capacitor to this pin to set the converter soft-start time.
COMP2	23	O	Compensation pin for Buck2. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
FB2	24	I	Feedback input for Buck2. Connect a divider set to 0.8 V from the output of the converter to ground.
F_PWM	25	I	Forces PWM operation in all converters when set high. If low converters will operate in automatic PFM/PWM mode.
USB2_nFAULT	26	O	USB2 fault flag output, open drain, active low. Asserted when over current or over temperature condition is detected in the switch.
PGOOD	27	O	Power good. Open drain output asserted low after all converters and sequenced and within regulation. Polarity is factory selectable (active high default).
V7V	28	O	Internal supply. Connect a 4.7-µF to 10-µF ceramic capacitor from this pin to ground.
V3V	29	O	Internal supply. Connect a 3.3-µF to 10-µF ceramic capacitor from this pin to ground.
USB2_VO	30	O	USB switch output
USB2_VIN	31	I	USB switch input supply
USB1_VIN	32	I	USB switch Input supply
USB1_VO	33	O	USB switch output

TERMINAL FUNCTIONS (continued)

NAME	NO.	I/O	DESCRIPTION
USB1_EN	34	I	Enable input, high turns on the switch
USB1_nFAULT	35	O	USB1 fault flag output, open drain, active low. Asserted when overcurrent or overtemperature condition is detected in the switch.
LX3	36, 37	O	Switching node for Buck3
VIN3	38	I	Input supply for Buck3. Fit a 10-µF ceramic capacitor close to this pin.
BST3	39		Bootstrap capacitor for Buck3. Fit a 47-nF ceramic capacitor from this pin to the switching node.
EN3	40	I	Enable pin for Buck3. A high signal on this pin enables the converter. For a delayed start-up add a small ceramic capacitor from this pin to ground.
PowerPAD			PowerPAD. Connect to system ground for electrical and thermal connection.

ABSOLUTE MAXIMUM RATINGS (1)

over operating free-air temperature range (unless otherwise noted, all voltages are with respect to GND)

	Voltage range at VIN1,VIN2, VIN3, LX1, LX2, LX3	–0.3 to 20	V
	Voltage range at LX1, LX2, LX3 (maximum withstand voltage transient < 10 ns)	–3 to 20	V
	Voltage at BST1, BST2, BST3 referenced to LX pin	–0.3 to 7	V
	Voltage at V7V, COMP1, COMP2, COMP3, USB1_VIN, USB1_VO, USB2_VIN, USB2_VO, USB1_EN, USB2_EN, USB1_nFAULT, USB2_nFAULT, PGOOD	–0.3 to 7	V
	Voltage at V3V, RLIM1, RLIM2, RLIM3, SS1, SS2, SS3, FB1, FB2, FB3 , ROSC, EN1, EN2, EN3, F_PWM	–0.3 to 3.6	V
T_J	Operating junction temperature range	–40 to 125	°C
T_{STG}	Storage temperature range	–55 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input operating voltage	4.5		18	V
T_A	Junction temperature	–40		85	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION(1)

	MIN	MAX	UNIT
Human body model (HBM)	2000		V
Charge device model (CDM)	500		V

(1) USB1_Vo, USB2_Vo pins' human body model (HBM) ESD protection rating 4KV, and machine model (MM) rating 200V.

PACKAGE DISSIPATION RATINGS(1)

PACKAGE	θ_{JA} (°C/W)	T_A = 25°C POWER RATING (W)	T_A = 55°C POWER RATING (W)	T_A = 85°C POWER RATING (W)
RHA	30	3.33	2.3	1.3

(1) Based on JEDEC 51.5 HIGH K environment measured on a 76.2 x 114 x 0.6-mm board with the following layer arrangement:
(a) Top layer: 2 Oz Cu, 6.7% coverage
(b) Layer 2: 1 Oz Cu, 90% coverage
(c) Layer 3: 1 Oz Cu, 90% coverage
(d) Bottom layer: 2 Oz Cu, 20% coverage

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 125°C, V_{IN} = 12 V, f_{SW} = 500 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY UVLO AND INTERNAL SUPPLY VOLTAGE						
V_{IN}	Input voltage range		4.5		18	V
IDD_{SDN}	Shutdown	EN pin = low for all converters		180		µA
IDD_Q	Quiescent (push-button pull-up current not included)	Converters enabled, no load Buck1 = 1.2 V Buck2 = 1.8 V Buck3 = 3.3 V T_A = 25°C, F_PWM = Low		700		µA
	Quiescent, forced PWM	Converters enabled, no load F_PWM = High		24		mA
UVLO	V_{IN} under voltage lockout	Rising V_{IN}		4.22		V
		Falling V_{IN}		4.1		
$UVLO_{DEGLITCH}$		Both edges		110		µs
V3p3	Internal biasing supply			3.3		V
V7V	Internal biasing supply			6.25		V
$V7V_{UVLO}$	UVLO for internal V7V rail	Rising V7V		3.8		V
		Falling V7V		3.6		
$V7V_{UVLO\_DEGLITCH}$		Falling edge		120		µs
BUCK CONVERTERS (ENABLE CIRCUIT, CURRENT LIMIT, SOFT-START AND SWITCHING FREQUENCY)						
V_{IH_ENx}	Enable threshold high	V3p3 = 3.2 V - 3.4 V, V_{ENx} rising	0.66 x V3p3			V
V_{IL_ENx}	Enable threshold low	V3p3 = 3.2 V - 3.4 V, V_{ENx} falling			0.33 x V3p3	V
$V_{IH\_F\_PWM}$	Enable threshold high	V3p3 = 3.2 V - 3.4 V, V_{ENx} rising	0.66 x V3p3			V
$V_{IL\_F\_PWM}$	Enable treshold low	V3p3 = 3.2 V - 3.4 V, V_{ENx} falling			0.33 x V3p3	V
ICH_{EN}	Pull up current enable pin			4		µA
t_D	Discharge time enable pins	Power-up		10		ms
I_{SS}	Soft-start pin current source			5		µA
F_{SW_BK}	Converter switching frequency range	Set externally with resistor	0.3		2.2	MHz
f_{SW_TOL}	Internal oscillator accuracy	f_{SW} = 800 kHz	-10		10	%
FEEDBACK, REGULATION, OUTPUT STAGE						
V_{FB}	Feedback voltage	V_{IN} = 12 V , T_A = 25°C	-1%	0.8	1%	V
		V_{IN} = 4.5 V to 18 V	-2%	0.8	2%	
t_{ON_MIN}	Minimum on time (current sense blanking)				135	ns
I_{LIMIT1}	Peak inductor current limit range		0.75		4	A
I_{LIMIT2}	Peak inductor current limit range		0.75		3	A
I_{LIMIT3}	Peak inductor current limit range		0.75		3	A
MOSFET (BUCK 1)						
H.S. Switch	On resistance of high side FET on CH1	25°C, BOOT = 6.5 V		95		mΩ
L.S. Switch	On resistance of low side FET on CH1	25°C, VIN = 12 V		50		mΩ

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 125°C, V_{IN} = 12 V, f_{SW} = 500 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MOSFET (BUCK 2)						
H.S. Switch	On resistance of high side FET on CH2	25°C, BOOT = 6.5 V		120		mΩ
L.S. Switch	On resistance of low side FET on CH2	25°C, VIN = 12 V		80		mΩ
MOSFET (BUCK 3)						
H.S. Switch	On resistance of high side FET on CH3	25°C, BOOT = 6.5 V		120		mΩ
L.S. Switch	On resistance of low side FET on CH3	25°C, VIN = 12 V		80		mΩ
ERROR AMPLIFIER						
g_M	Error amplifier transconductance	-2 µA < ICOMP < 2 µA		130		µS
gm_{PS1}	COMP to ILX gm of Buck1 (1)	I_{LX} = 0.5 A		10		A/V
gm_{PS2}	COMP to ILX gm of Buck2 and 3 (1)	I_{LX} = 0.5 A		8		A/V
POWER GOOD RESET GENERATOR						
VUV_{BUCKX}	Threshold voltage for buck under voltage	Output falling		85		%
		Output rising (PG will be asserted)		90		
$t_{UV\_deglitch}$	Deglitch time (both edges)			11		ms
t_{ON_HICCUP}	Hiccup mode ON time	VUV_{BUCKX} asserted		14		ms
t_{OFF_HICCUP}	Hiccup mode OFF time	All converters disabled. Once t_{OFF_HICCUP} elapses, all converters will go through sequencing again.		20		ms
VOV_{BUCKX}	Threshold voltage for buck over voltage	Output rising (high side FET will be forced off)		106		%
		Output falling (high side FET will be allowed to switch)		104		
t_{RP}	minimum reset period	Measured after the later of Buck1 or Buck3 power-up successfully		100		ms
USB SWITCHES						
VIN_{USB}	USB input voltage range		2.5		6	V
$V_{IH\_USB\_EN}$	USB_EN high level input voltage	V3p3 = 3.2-3.4 V, V_{USB_EN} rising	0.66x V3p3			V
$V_{IL\_USB\_EN}$	USB_EN low level input voltage	V3p3 = 3.2-3.4 V, V_{USB_EN} falling			0.33x V3p3	V
R_{DS_USB}	Static drain-source on-state resistance	USB_VIN = 5 V and Io_USB = 0.5 A, T_J = 2 5°C		135		mΩ
I_{CS_USB}	USB current limit	Increasing USB_Vo current di/dt<1 A/s		1.2		A
V_{USBx_nFAULT}	USBx_nFAULT output voltage low	I_{USB_nFAULT} = 1 mA		150		mV
T_{USB_TRIP}	USB thermal trip point	Rising temperature		130		°C
T_{USB_HYST}	USB thermal trip hysteresis	Hysteresis		20		°C
T_{D_on}	Turn-on delay time	USB_IN = 5 V, C_L = 10 µF, R_L = 100 Ω		1.1		ms
T_{D_off}	Turn-off delay time			1.6		ms
T_{IOS}	Response time to short circuit	USB_IN = 5 V		2		µs
$T_{DEGLITCH(OCP)}$	Switch over current fault deglitch	Fault assertion or de-assertion due to over-current condition		8.8		ms

(1) Specified by design.

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 125°C, V_{IN} = 12 V, f_{SW} = 500 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DIS}	Discharge resistance	USB_IN = 5 V, USB1_EN/USB2_EN = 0 V		130		Ω
THERMAL SHUTDOWN						
T_{TRIP}	Thermal shut down trip point	Rising temperature		160		°C
T_{HYST}	Thermal shut down hysteresis	Device re-starts		20		°C
$T_{TRIP\_DEGLITCH}$	Thermal shut down deglitch			110		µs

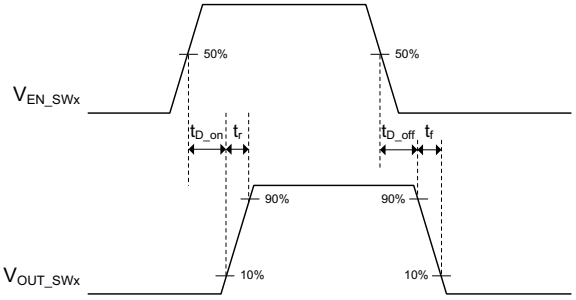


Figure 1. Power Switches Test Circuit and Voltage Waveforms

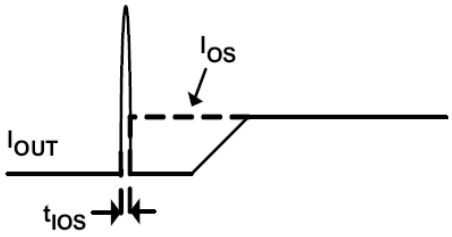


Figure 2. Response Time to Short Circuit Waveform

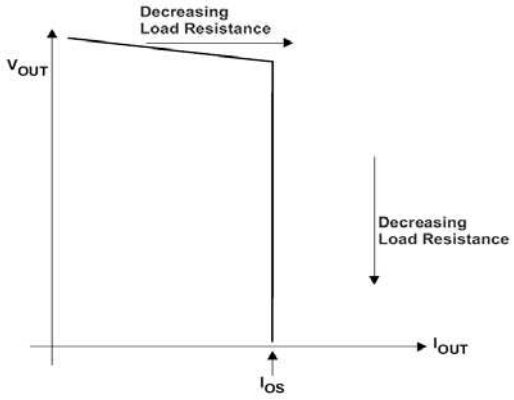


Figure 3. Output Voltage vs Current Limit Threshold

TYPICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 12 V, Buck1 = 1.2 V, Buck2 = 1.8 V, Buck3 = 3.3 V, L = 4.7 µH, f_{SW} = 500 kHz (unless otherwise noted)

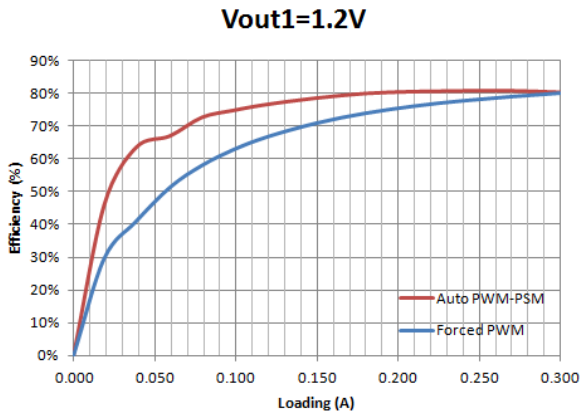


Figure 4. Buck1 1.2V Efficiency, Forced PWM and PSM

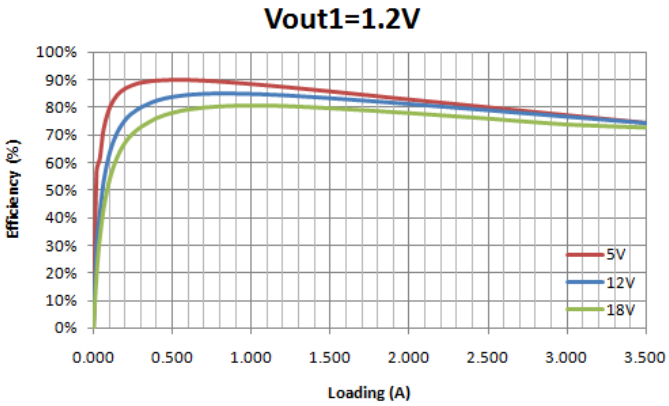


Figure 5. Buck1 1.2V Efficiency, Forced PWM

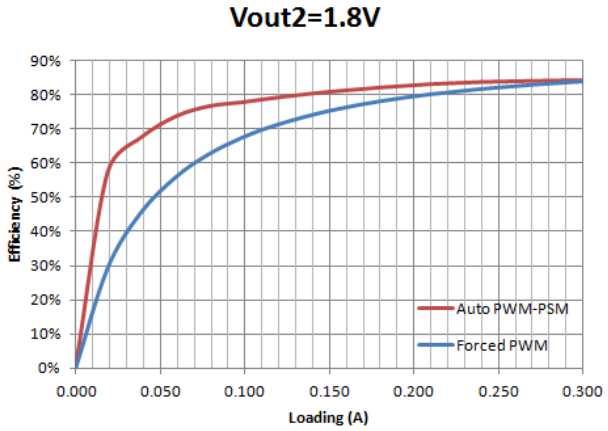


Figure 6. Buck2 1.8V Efficiency, Forced PWN and PSM

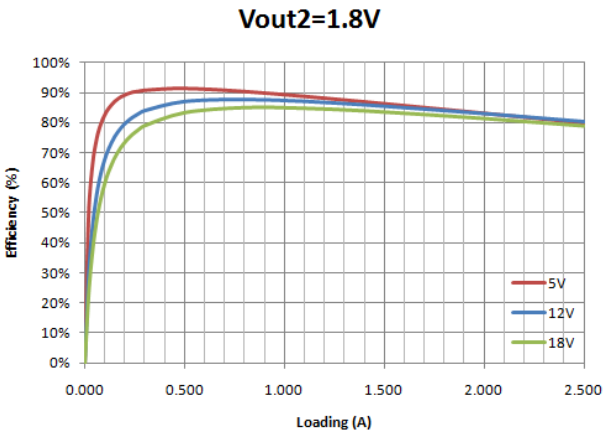


Figure 7. Buck2 1.8V Efficiency, Forced PWM

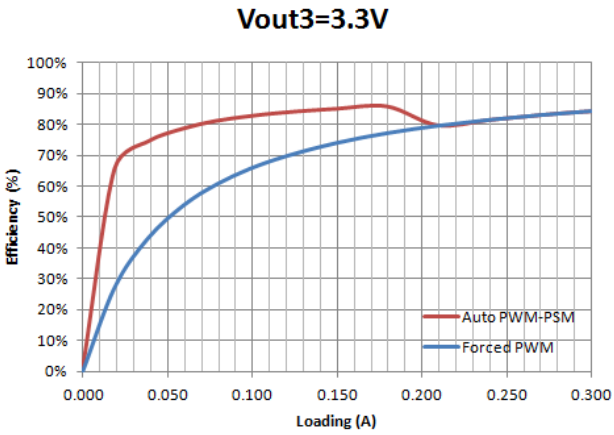


Figure 8. Buck3 3.3 Efficiency, Forced PWM and PSM

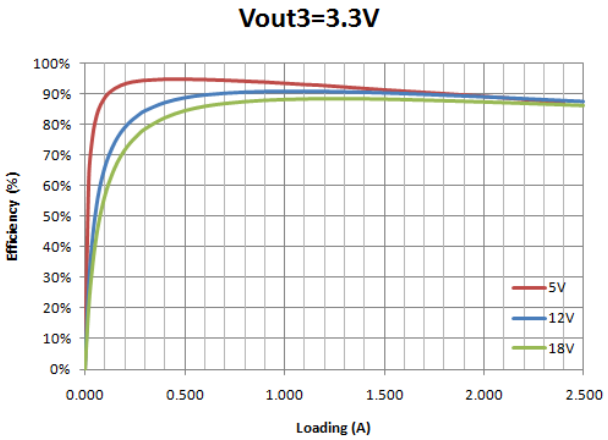


Figure 9. Buck3 3.3V Efficiency, Forced PWM

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{IN} = 12 V, Buck1 = 1.2 V, Buck2 = 1.8 V, Buck3 = 3.3 V, L = 4.7 µH, f_{SW} = 500 kHz (unless otherwise noted)

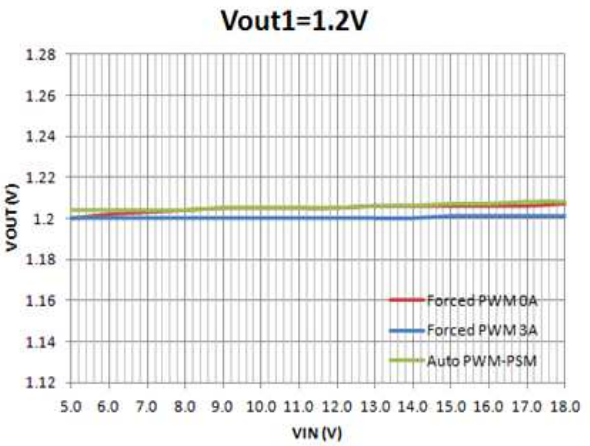


Figure 10. Line Regulation: Buck1 @ 1.2V, 1% Resistor Feedback

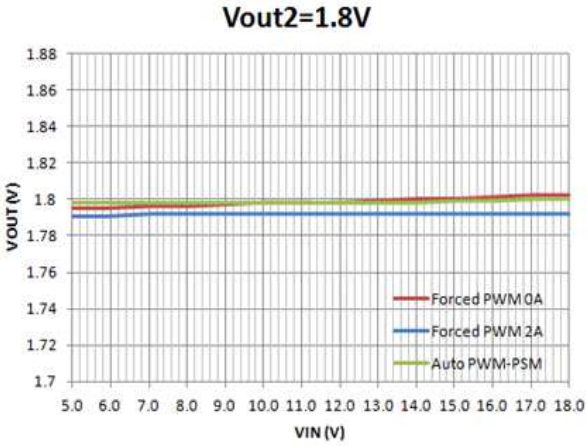


Figure 11. Line Regulation: Buck2 @ 1.8V, 1% Resistor Feedback

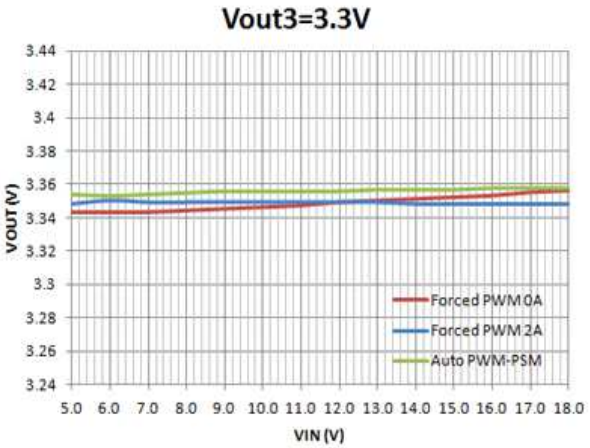


Figure 12. Line Regulation: Buck3 @ 3.3V, 1% Resistor Feedback

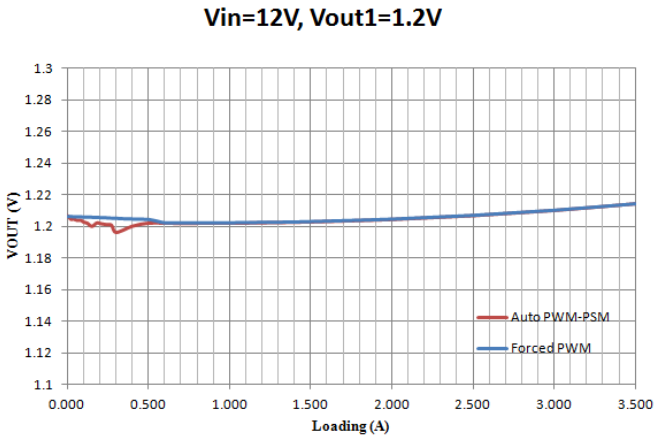


Figure 13. Load Regulation: Buck1 @ 1.2V, 1% Resistor Feedback

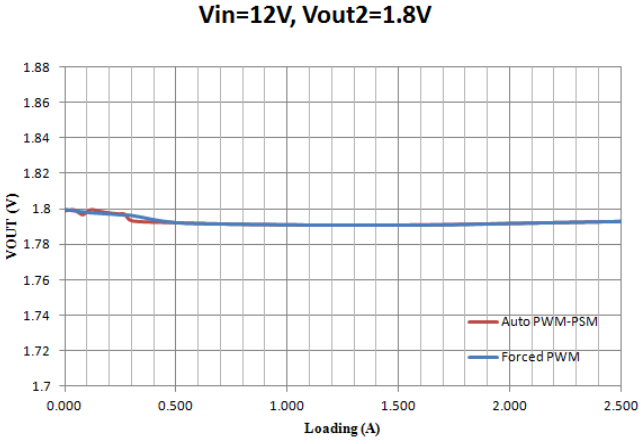


Figure 14. Load Regulation: Buck2 @ 1.8V, 1% Resistor Feedback

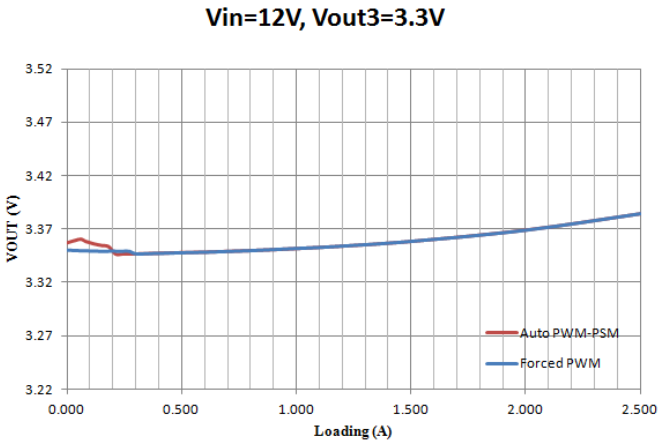


Figure 15. Load Regulation: Buck3 @ 3.3V, 1% Resistor Feedback

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{IN} = 12 V, Buck1 = 1.2 V, Buck2 = 1.8 V, Buck3 = 3.3 V, L = 4.7 µH, f_{SW} = 500 kHz (unless otherwise noted)

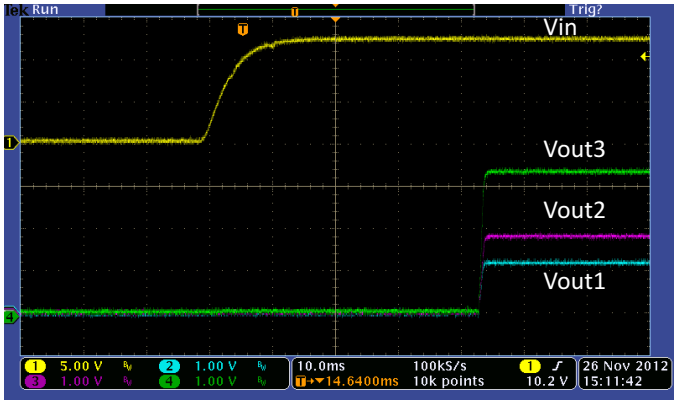


Figure 16. Power-Up All Converters, No Load

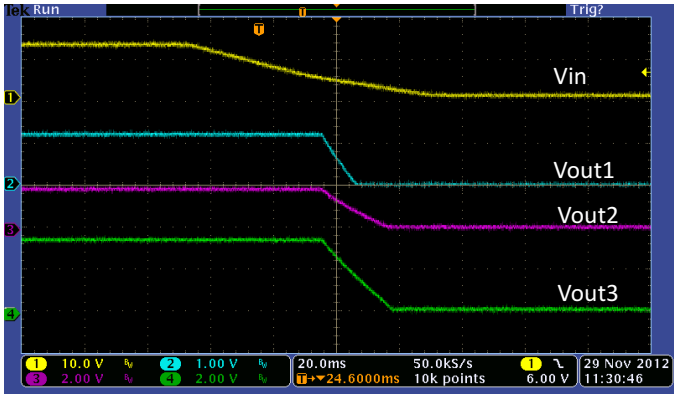


Figure 17. Power-Down All Converters, No Load

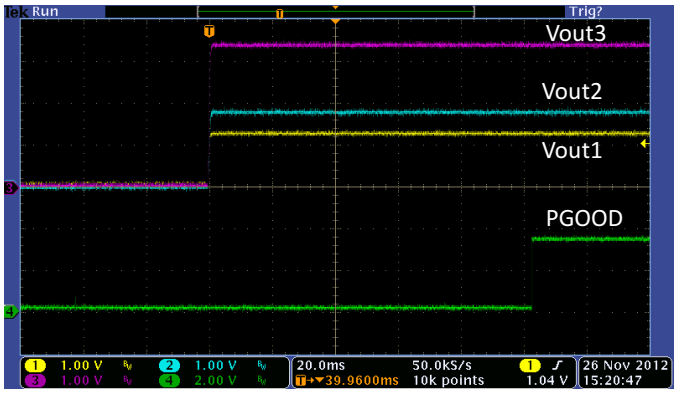


Figure 18. Power-Up All Converters and PGOOD, No Load

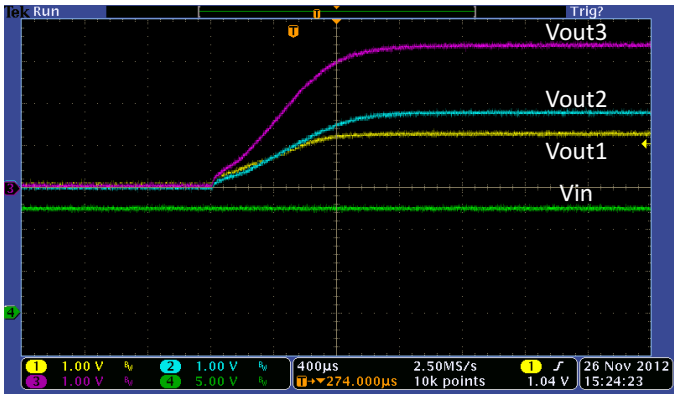


Figure 19. Detail of Start-Up 4.7nF Fitted to All Enable Pins

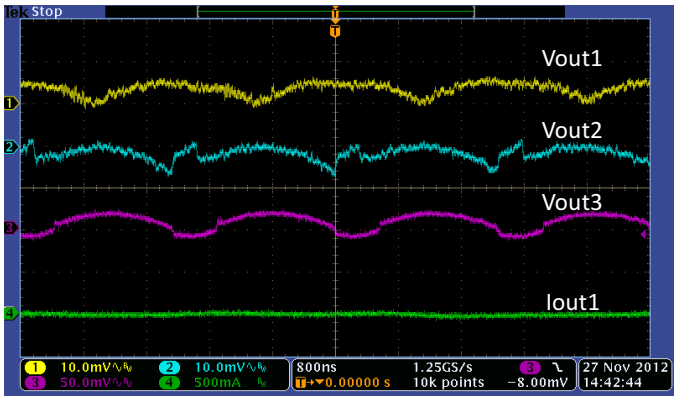


Figure 20. Ripple, Buck1 = 0A, Buck2 = 0A, Buck3 = 0A

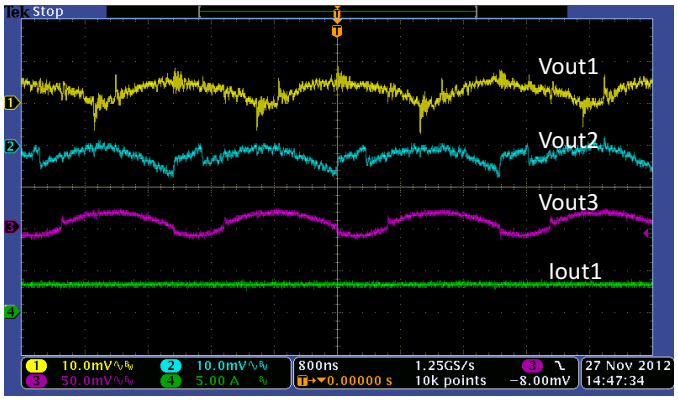


Figure 21. Transient Response Buck1
Ripple, Buck1 = 3A, Buck2 = 2A, Buck3 = 2A

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{IN} = 12 V, Buck1 = 1.2 V, Buck2 = 1.8 V, Buck3 = 3.3 V, L = 4.7 µH, f_{SW} = 500 kHz (unless otherwise noted)

Figure 22. Transient Response Buck1@1.2V, 1-3A Step, Co = 68µF

Figure 23. Transient Response Buck2@1.8V, 1-2A Step, Co = 47µF

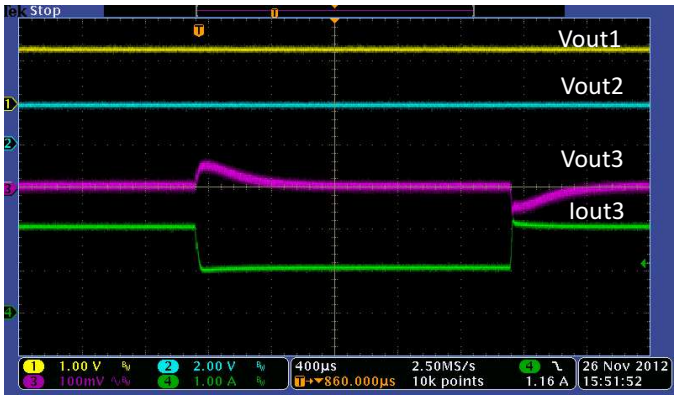


Figure 24. Transient Response Buck3@3.3 V, 1-2A Step, Co = 22µF

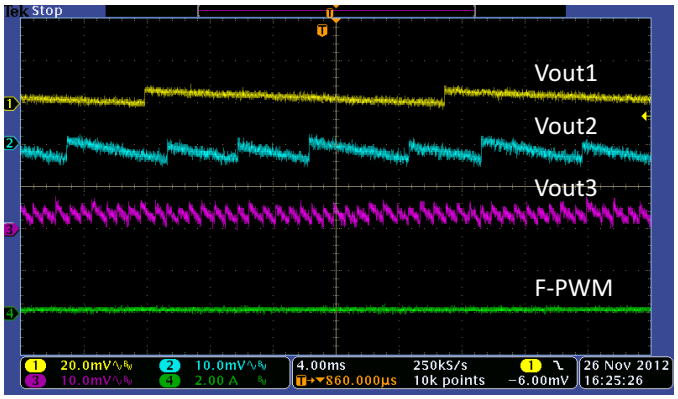


Figure 25. PSM Operation 1.2V, 1.8V, 3.3V

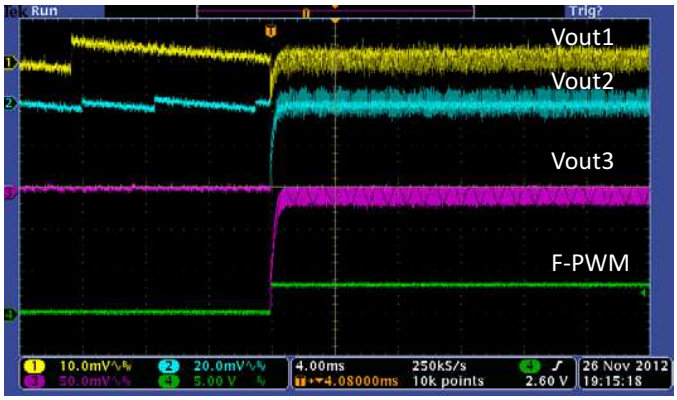


Figure 26. PSM/PWM Transition (Pin 25 Pulled High)

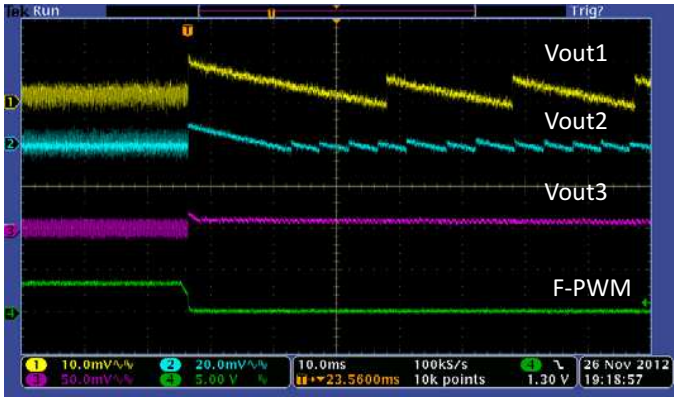


Figure 27. PSM/PWM Transition (Pin 25 Pulled Low)

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{IN} = 12 V, Buck1 = 1.2 V, Buck2 = 1.8 V, Buck3 = 3.3 V, L = 4.7 µH, f_{SW} = 500 kHz (unless otherwise noted)

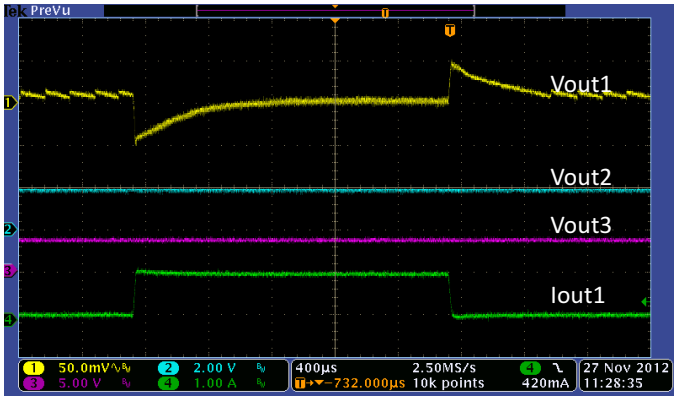


Figure 28. Buck1 Dynamic Transition from PSM to PWM, C=68µF

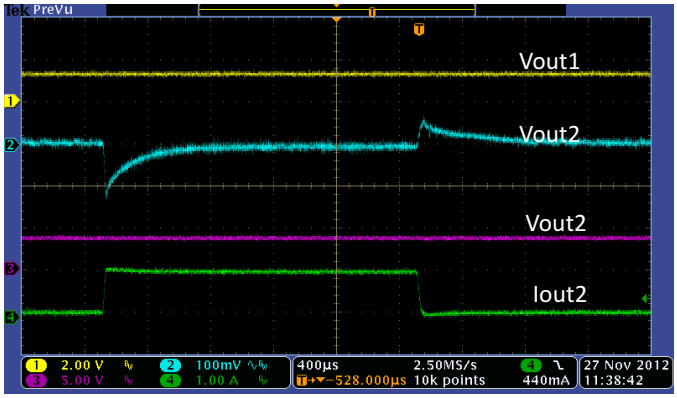


Figure 29. Buck2 Dynamic Transition from PSM to PWM C=47µF

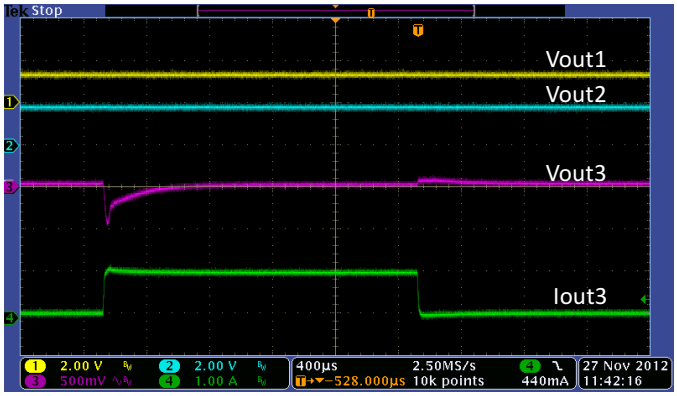


Figure 30. Buck3 Dynamic Transition from PSM to PWM, C=22µF

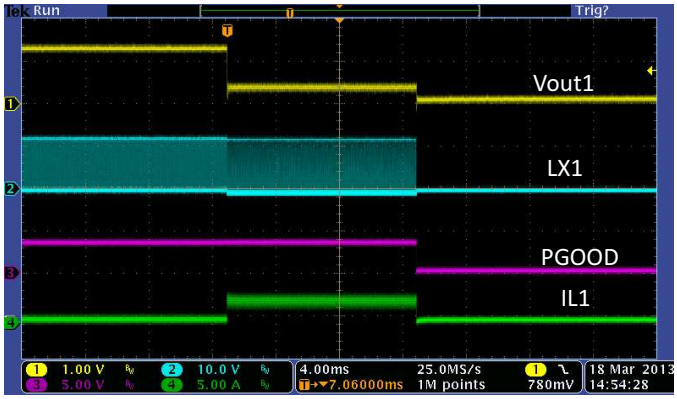


Figure 31. Over Current Protection PGOOD Buck1=1.2V

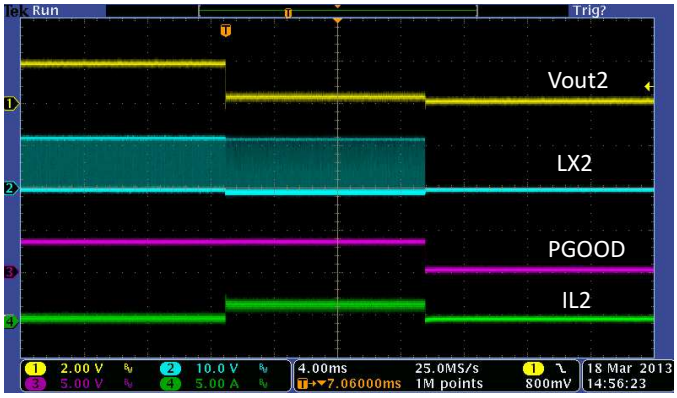


Figure 32. Over Current Protection and PGOOD Buck2=1.8V

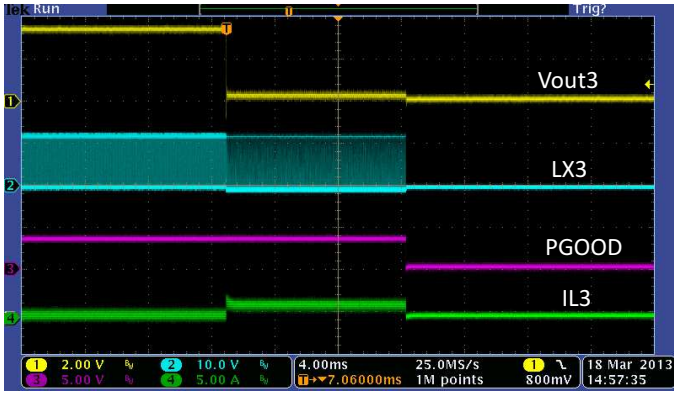


Figure 33. Over Current Protection and PGOOD Buck3=3.3V

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{IN} = 12 V, Buck1 = 1.2 V, Buck2 = 1.8 V, Buck3 = 3.3 V, L = 4.7 µH, f_{SW} = 500 kHz (unless otherwise noted)

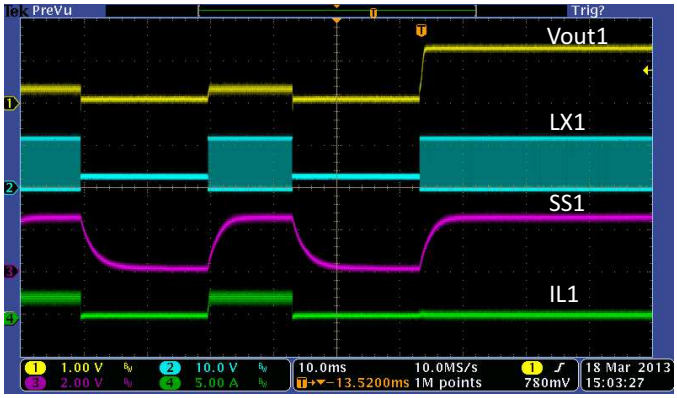


Figure 34. Hiccup Recover, Buck1=1.2V

Figure 35. Hiccup Recover, Buck2=1.8V

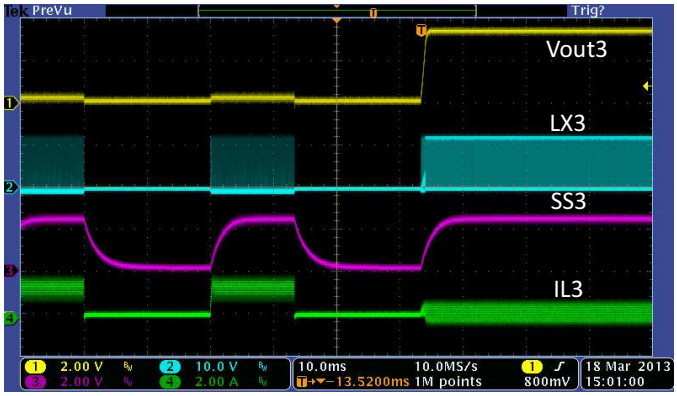


Figure 36. Hiccup Recover, Buck3=3.3V

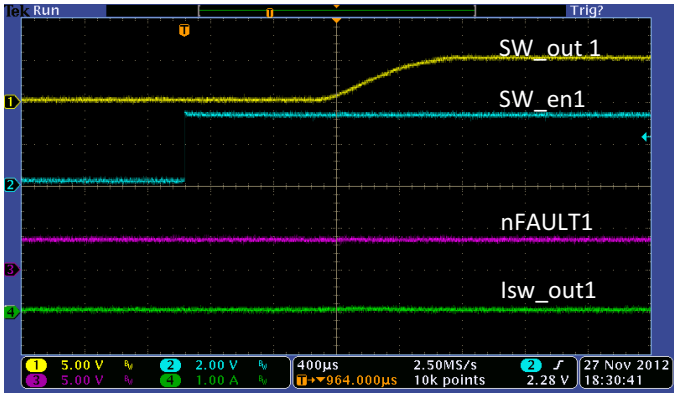


Figure 37. USB Switch1 Start-Up No Load

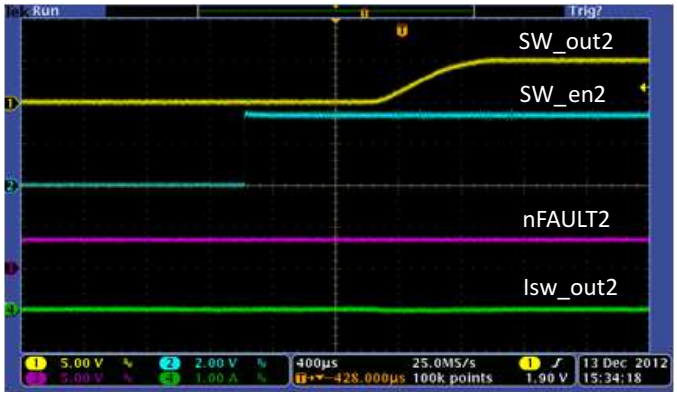


Figure 38. USB Switch2 Start-Up No Load

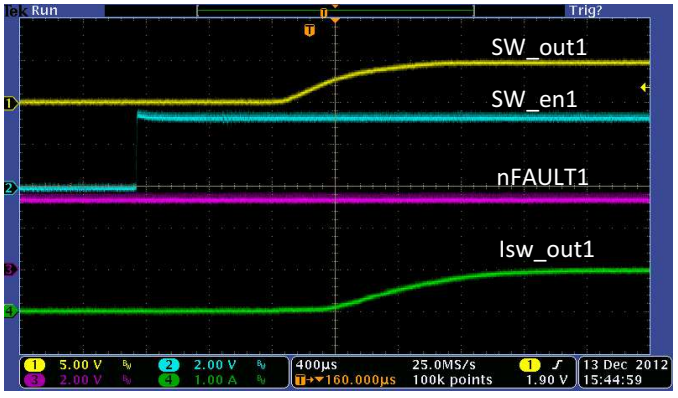


Figure 39. USB Switch1 Start-Up 1A Load

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{IN} = 12 V, Buck1 = 1.2 V, Buck2 = 1.8 V, Buck3 = 3.3 V, L = 4.7 µH, f_{SW} = 500 kHz (unless otherwise noted)

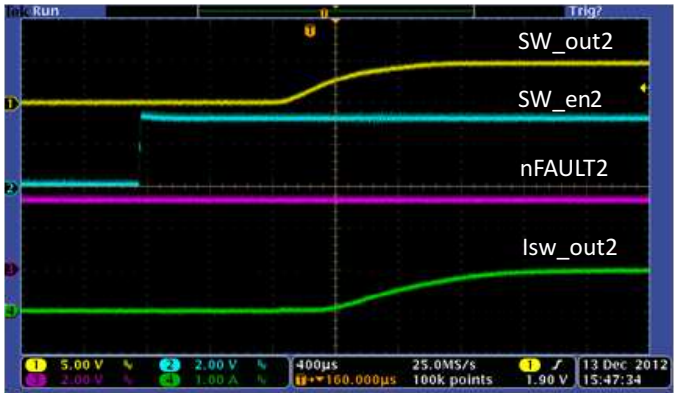


Figure 40. USB Switch2 Start-Up 1A Load

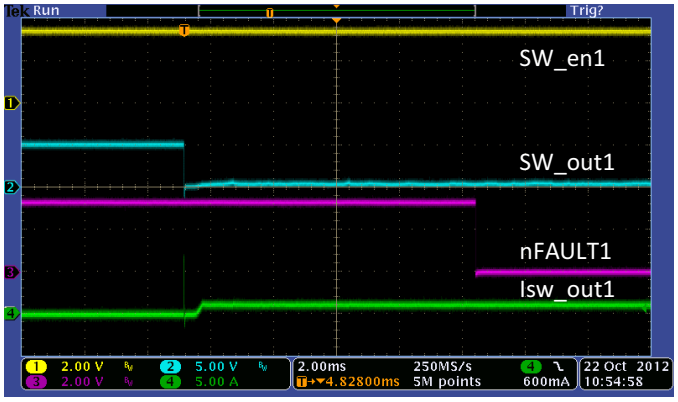


Figure 41. USB Switch1 Current Limit Operation

Figure 42. USB Switch2 Current Limit Operation

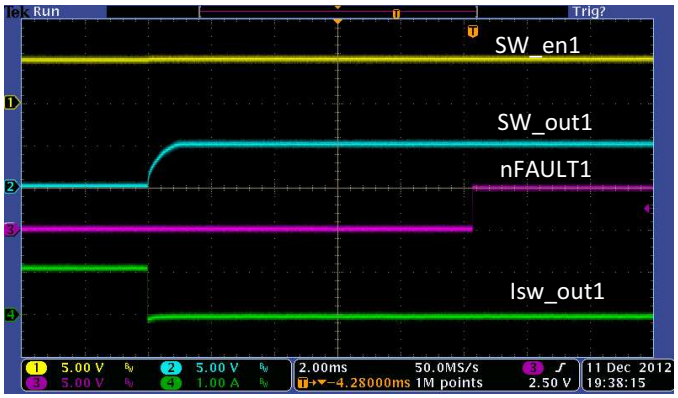


Figure 43. USB Switch1 Current Limit Recovery

Figure 44. USB Switch2 Current Limit Recovery

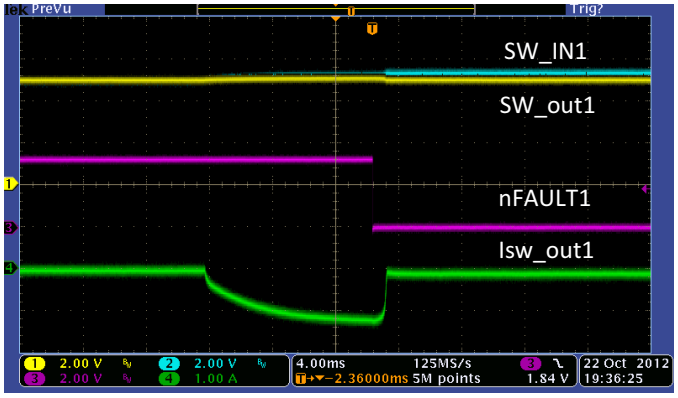


Figure 45. USB Switch1 Output Reverse Protection

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{IN} = 12 V, Buck1 = 1.2 V, Buck2 = 1.8 V, Buck3 = 3.3 V, L = 4.7 µH, f_{SW} = 500 kHz (unless otherwise noted)

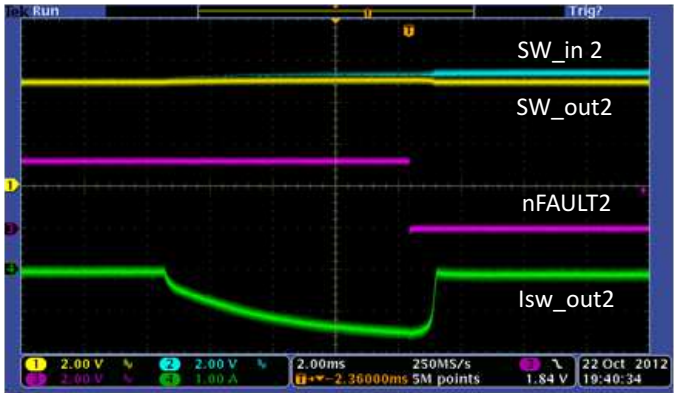


Figure 46. USB Switch2 Output Reverse Protection

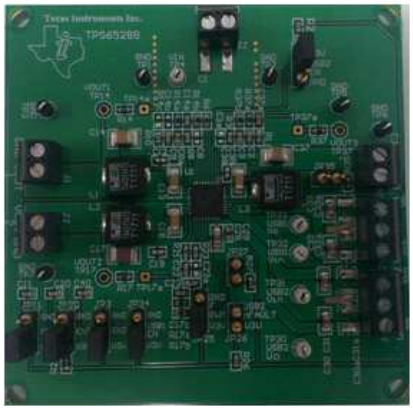


Figure 47. EVM Layout

DETAILED DESCRIPTION

Adjustable Switching Frequency

To select the internal switching frequency, connect a resistor from ROSC to ground. Figure 48 shows the required resistance for a given switching frequency.

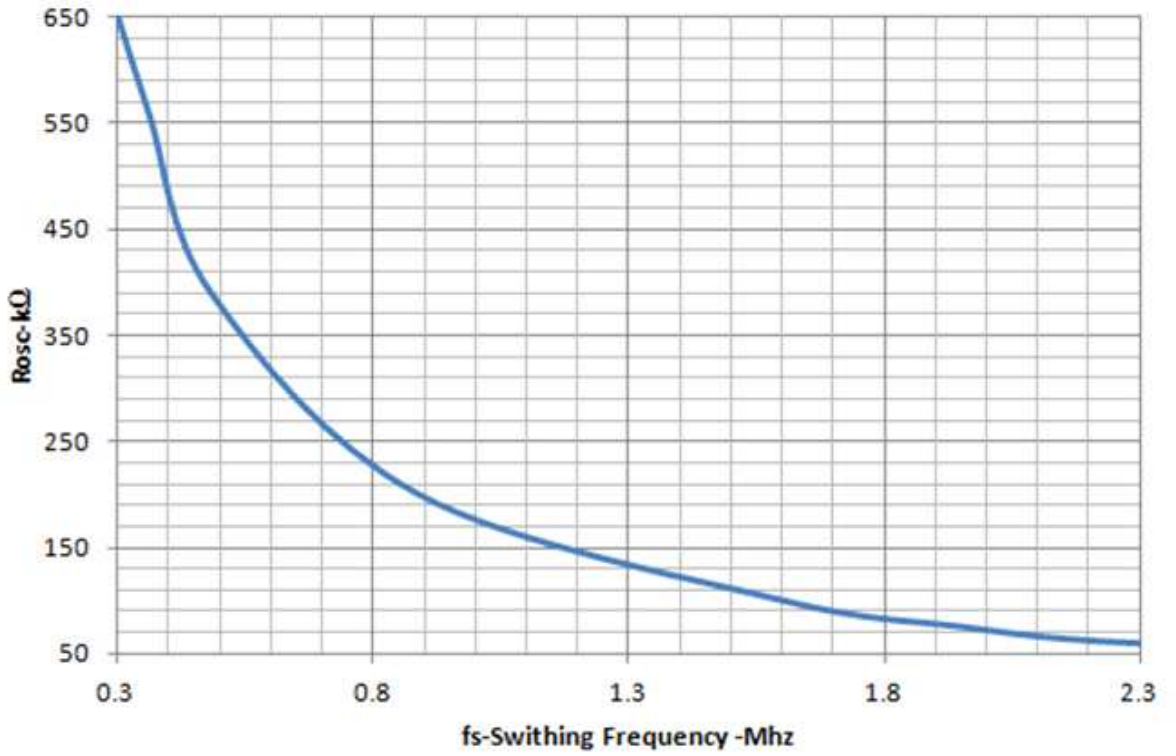


Figure 48. ROSC vs Switching Frequency

$$R_{OSC}(k\Omega) = 169.5 \bullet f_{SW}^{-1.221} \quad (1)$$

Output Inductor Selection

To calculate the value of the output inductor, use Equation 2.

$$Lo = \frac{Vin - Vout}{Io \cdot K_{ind}} \cdot \frac{Vout}{Vin \cdot fsw} \quad (2)$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. In general, K_{IND} is normally from 0.1 to 0.3 for the majority of applications. A value of 0.1 will improve the efficiency at light load, while a value of 0.3 will provide the lowest possible cost solution. The ripple current is:

$$Iripple = \frac{Vin - Vout}{Lo} \cdot \frac{Vout}{Vin \cdot fsw} \quad (3)$$

Output Capacitor

There are two primary considerations for selecting the value of the output capacitor. The output capacitors are selected to meet load transient and output ripple's requirements. If a minimum transient specification is required use the following equation:

$$Co > \frac{\Delta I_{OUT}{}^2 \cdot L_o}{V_{out} \cdot \Delta Vout} \quad (4)$$

The following equation calculates the minimum output capacitance needed to meet the output voltage ripple specification.

$$Co > \frac{1}{8 \cdot fsw} \cdot \frac{1}{\frac{V_{RIPPLE}}{I_{RIPPLE}}} \quad (5)$$

Where f_{SW} is the switching frequency, V_{RIPPLE} is the maximum allowable output voltage ripple, and V_{RIPPLE} is the inductor ripple current.

Input Capacitor

A minimum 10-µF X7R/X5R ceramic input capacitor is recommended to be added between VIN and GND of each converter. The input capacitor must handle the RMS ripple current shown in the following equation.

$$Icirms = Iout \cdot \sqrt{\frac{Vout}{Vin\min} \cdot \frac{(Vin\min - Vout)}{Vin\min}} \quad (6)$$

Bootstrap Capacitor

The device has two integrated boot regulators and requires a small ceramic capacitor between the BST and LX pins to provide the gate drive voltage for the high side MOSFET. The value of the ceramic capacitor should be 0.047 µF. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage.

Delayed Start-Up

If a delayed start-up is required on any of the buck converters fit a ceramic capacitor to the ENx pins. The delay added is ~1.67 ms per nF connected to the pin. Note that the EN pins have a weak 1 MΩ pull-up to the 3V3 rail.

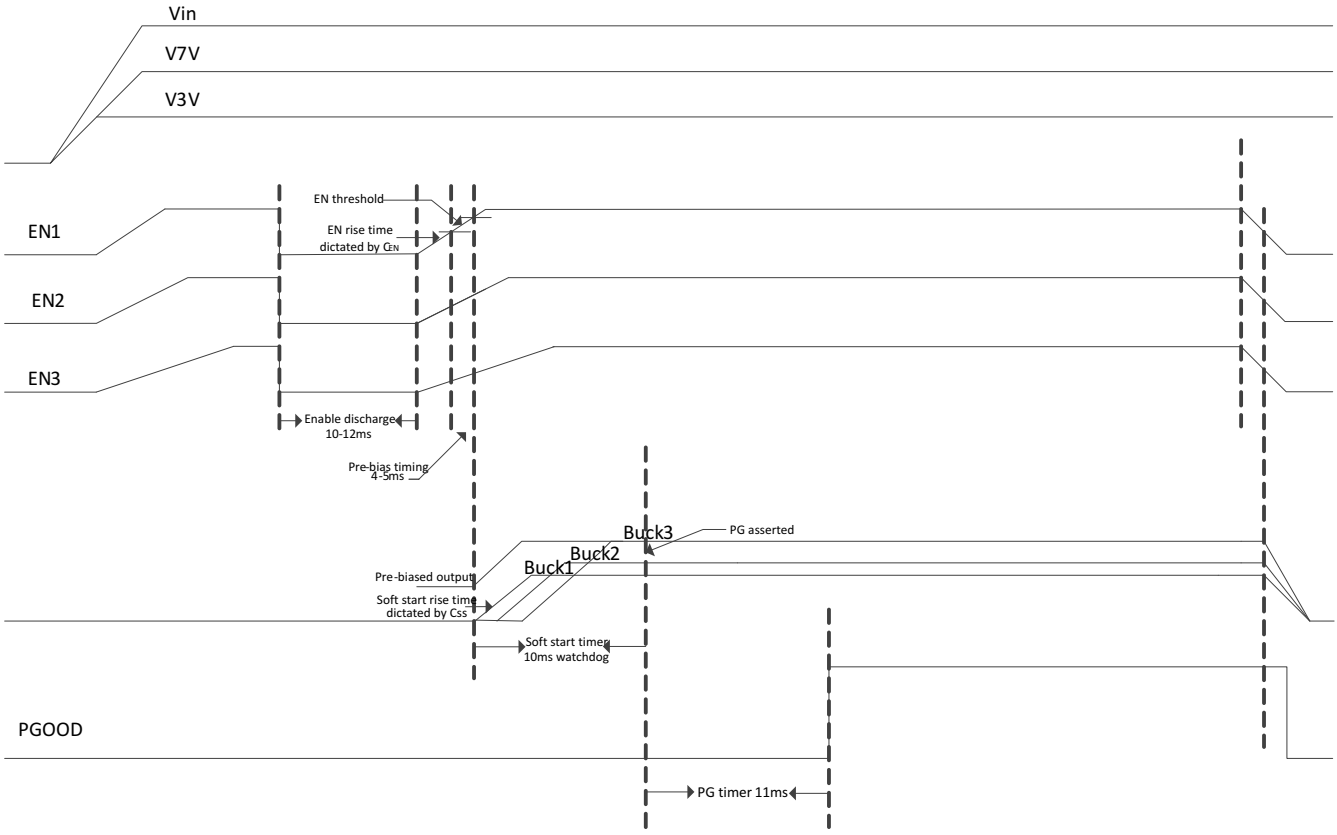


Figure 49. Delayed Start-Up

Out-of-Phase Operation

In order to reduce input ripple current, buck 1 and buck 2 operate 180 degree out-of-phase. This enables the system having less input ripple, then to lower component cost, save board space and reduce EMI.

Soft-Start Time

The device has an internal pull-up current source of 5 µA that charges an external soft-start capacitor to implement a slow start time. Equation 7 shows how to select a soft-start capacitor based on an expected slow start time. The voltage reference (V_{REF}) is 0.8 V and the soft-start charge current (I_{SS}) is 5 µA. The soft-start circuit requires 1 nF per around 167 µs to be connected at the SS pin. A 0.8-ms soft-start time is implemented for all converters fitting 4.7 nF to the relevant SS pin.

$$T_{ss}(ms) = V_{REF}(V) \bullet \left(\frac{C_{ss}(nF)}{I_{ss}(\mu A)} \right) \quad (7)$$

The Power Good circuit for the bucks has a 11-ms watchdog. Therefore the soft-start time should be lower than this value. It is recommended not to exceed 5 ms.

Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better divider resistors. In order to improve efficiency at light load, start with a value close to 40 kΩ for the R1 resistor and use Equation 8 to calculate R2.

$$R2 = R1 \cdot \left(\frac{0.8V}{V_O - 0.8V} \right) \quad (8)$$

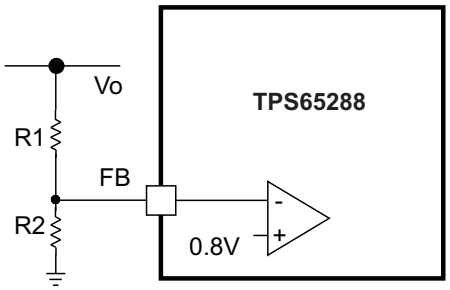


Figure 50. Voltage Divider Circuit

Loop Compensation

TPS65288 is a current mode control DC/DC converter. The error amplifier is a transconductance amplifier with a g_M of 130 µA/V. A typical compensation circuit could be type II (R_c and C_c) to have a phase margin between 60° and 90°, or type III (R_c and C_c and C_{ff} to improve the converter transient response. C_{Roll} adds a high frequency pole to attenuate high-frequency noise when needed. It may also prevent noise coupling from other rails if there is possibility of cross coupling in between rails when layout is very compact.

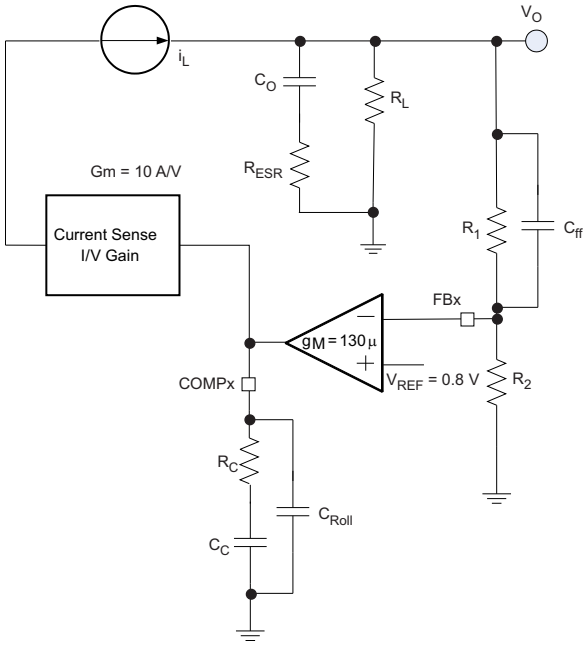


Figure 51. Loop Compensation Scheme

To calculate the external compensation components follow the following steps:

	TYPE II CIRCUIT	TYPE III CIRCUIT
Select switching frequency that is appropriate for application depending on L, C sizes, output ripple, EMI concerns and etc. Switching frequencies around 500 kHz yield best trade off between performance and cost. When using smaller L and C, switching frequency can be increased. To optimize efficiency, switching frequency can be lowered.		Type III circuit recommended for switching frequencies higher than 500 kHz.
Select cross over frequency (f_c) to be at least 1/5 to 1/10 of switching frequency (f_s).	Suggested $f_c = f_s/10$	Suggested $f_c = f_s/10$
Set and calculate R_c.	$R_C = \frac{2\pi \cdot fc \cdot Vo \cdot Co}{g_M \cdot Vref \cdot gm_{ps}}$	$R_C = \frac{2\pi \cdot fc \cdot Vo \cdot Co}{g_M \cdot Vref \cdot gm_{ps}}$
Calculate C_c by placing a compensation zero at or before the converter dominant pole $fp = \frac{1}{C_O \cdot R_L \cdot 2\pi}$	$C_c = \frac{R_L \cdot Co}{R_c}$	$C_c = \frac{R_L \cdot Co}{R_c}$
Add C_{Roll} if needed to remove large signal coupling to high impedance CMP node. Make sure that $fp_{Roll} = \frac{1}{2 \cdot \pi \cdot R_C \cdot C_{Roll}}$ is at least twice the cross over frequency.	$C_{Roll} = \frac{\mathrm{Re}\,sr \cdot Co}{R_C}$	$C_{Roll} = \frac{\mathrm{Re}\,sr \cdot Co}{R_C}$
Calculate C_{ff} compensation zero at low frequency to boost the phase margin at the crossover frequency. Make sure that the zero frequency (fz_{ff}) is smaller than equivalent soft-start frequency ($1/T_{ss}$).	NA	$C_{ff} = \frac{1}{2 \cdot \pi \cdot fz_{ff} \cdot R_1}$

Slope Compensation

The device has a built-in slope compensation ramp. The slope compensation can prevent sub harmonic oscillations in peak current mode control.

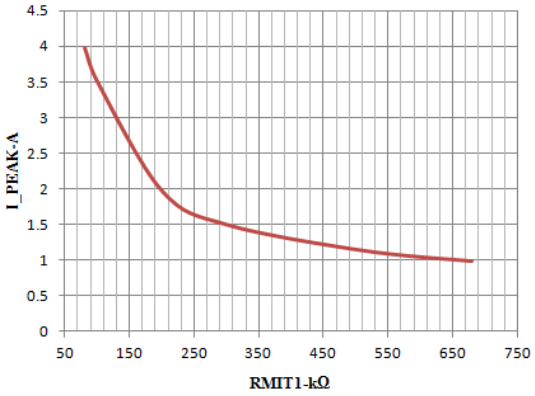
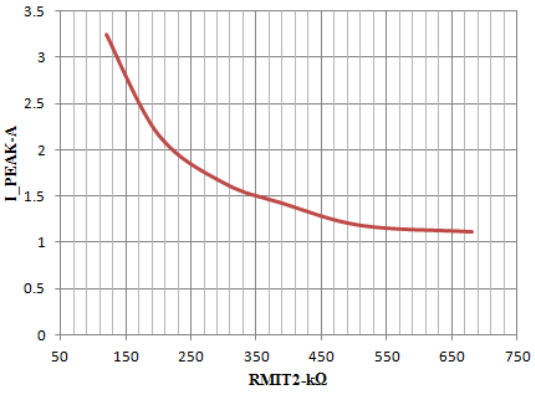
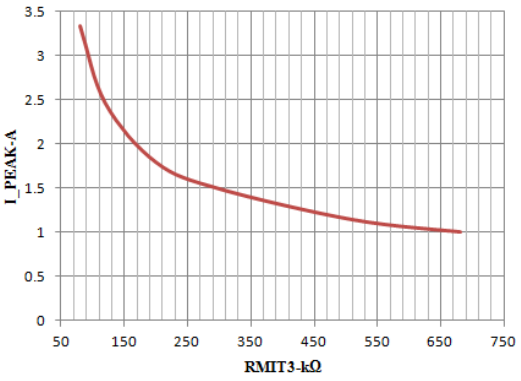
Power Good

The PGOOD pin is an open drain output. The PGOOD pin is pulled low when any buck converter is pulled below 85% of the nominal output voltage. The PGOOD is pulled up when both buck converters' outputs are more than 90% of its nominal output voltage.

The default reset time is 100 ms. The polarity of the PGOOD is active high.

Current Limit Protection

The TPS65288 current limit trip is set by the following formulae:

	TYPE II CIRCUIT
$I_{LIM1}(A) = \frac{268.5}{RLIM1(k\Omega)} + 0.613$ (9)	
$I_{LIM2}(A) = \frac{324.8}{RLIM1(k\Omega)} + 0.543$ (10)	
$I_{LIM3}(A) = \frac{208.7}{RLIM2(k\Omega)} + 0.731$ (11)	

All converters operate in hiccup mode: Once an over-current lasting more than 11 ms is sensed in any of the converters, they will shut down for 11 ms and then the start-up sequencing will be tried again. If the overload has been removed, the converter will ramp up and operate normally. If this is not the case the converter will see another over-current event and shuts-down again repeating the cycle (hiccup) until the failure is cleared.

If an overload condition lasts for less than 11 ms, only the relevant converter affected will shut-down and re-start and no global hiccup mode will occur.

Overvoltage Transient Protection

The device incorporates an overvoltage transient protection (OVP) circuit to minimize voltage overshoot. The OVP feature minimizes the output overshoot by implementing a circuit to compare the FB pin voltage to OVTP threshold which is 106% of the internal voltage reference. If the FB pin voltage is greater than the OVTP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVTP threshold which is 104%, the high side MOSFET is allowed to turn on the next clock cycle.

Low Power/Pulse Skipping Operation

When a buck synchronous converter operates at light load or standby conditions, the switching losses are the dominant source of power losses. Under these load conditions, TPS65288 uses a pulse skipping modulation technique to reduce the switching losses by keeping the power transistors in the off-state for several switching cycles, while maintaining a regulated output voltage. Figure 52 shows the output voltage and load plus the inductor current.

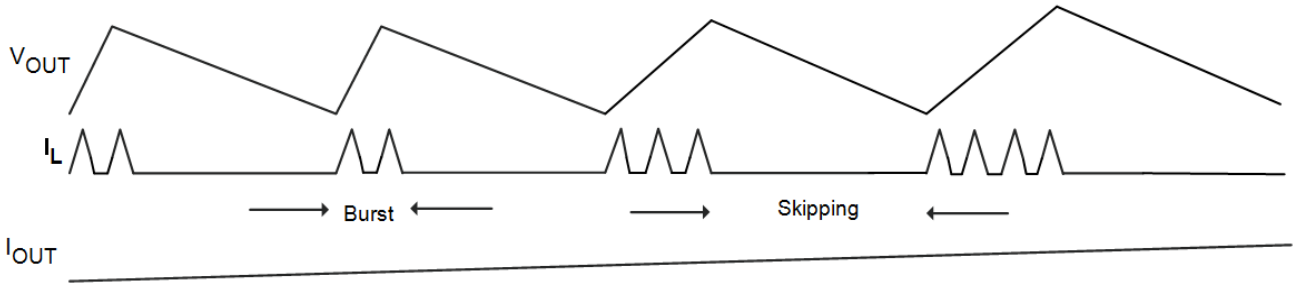


Figure 52. Low Power/Pulse Skipping

During the burst mode, the converter continuously charges up the output capacitor until the output voltage reaches a certain limit threshold. The operation of the converter in this interval is equivalent to the peak inductor current mode control. In each switch period, the main switch is turned on until the inductor current reaches the peak current limit threshold. As the load increases the number of pulses increases to make sure that the output voltage stays within regulation limits. When the load is very light the low power controller has a zero crossing detector to allow the low side mosfet to operate even in light load conditions. The transistor is not disabled at light loads. A zero crossing detection circuit will disable it when inductor current reverses. During the whole process the body diode does not conduct but is used as blocking diode only.

During the skipping interval, the upper and lower transistors are turned off and the converter stays in idle mode. The output capacitors are discharged by the load current until the moment when the output voltage drops to a low threshold.

The choice of output filter will influence the performance of the low power circuit. The maximum ripple during low power mode can be calculated as:

$$V_{OUT\_RIPPLE} = \frac{K_{RIP} T_S}{C_{OUT}} \tag{12}$$

Where K_{RIP} is 1.4 for Buck1 and 0.7 for Buck2 and Buck3. TS can be calculated as:

$$T_S = \frac{0.35}{\left[\left(\frac{V_{IN} - V_{OUT}}{L}\right)\frac{V_{OUT}}{V_{IN}}\right]} \tag{13}$$

USB Switches

The USB switches are enabled (active high) with the USB_ENx pin. The switches have a typical resistance of 135 mΩ. If a continuous short-circuit condition is applied to the USB switch output, the USB switch will shut-down once its temperature reaches 130°C, allowing for the buck converters to operate unaffected. Once the USB switch cools down it will restart automatically.

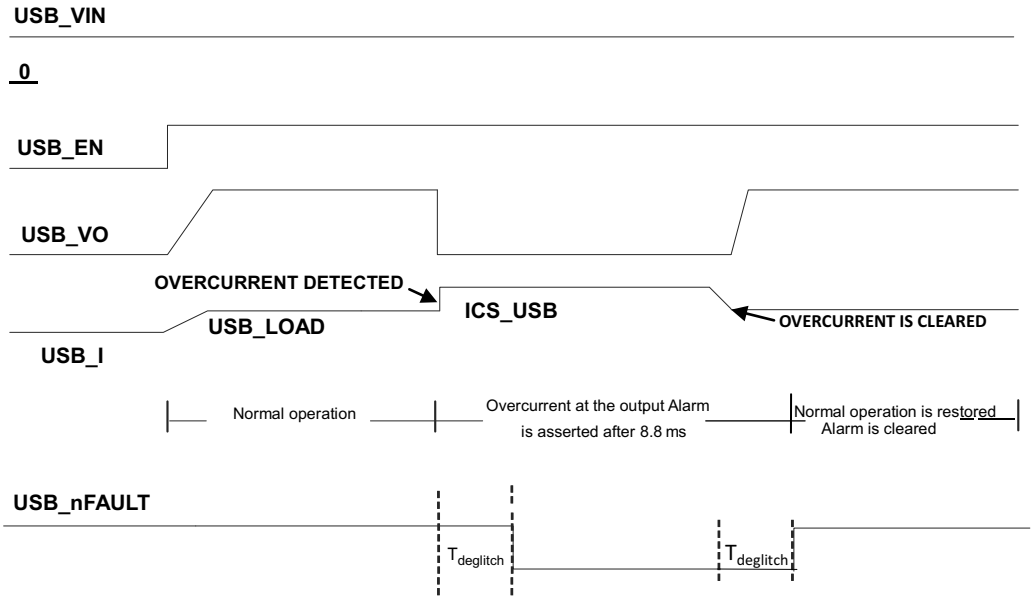


Figure 53. USB Switches

Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 160°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds thermal trip threshold. Once the die temperature decreases below 140°C, the device reinitiates the power up sequence. The thermal shutdown hysteresis is 20°C.

3.3-V and 6.5 LDO Regulators

The following ceramic capacitor (X7R/X5R) should be connected as close as possible to the described pins:

- 4.7 µF to 10 µF for V7V pin 28
- 3.3 µF to 10 µF for V3V pin 29

Layout Recommendation

Layout is a critical portion of PMIC designs.

- Place tracing for output voltage and LX on the top layer and an inner power plane for VIN.
- Fit also on the top layer connections for the remaining pins of the PMIC and a large top side area filled with ground.
- The top layer ground area should be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter capacitor and directly under the TPS65288 device to provide a thermal path from the PowerPad land to ground.
- For operation at full rated load, the top side ground area together with the internal ground plane, must provide adequate heat dissipating area.
- There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the ground connections. Since the LX connection is the switching node, the output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- The output filter capacitor ground should use the same power ground trace as the VIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width.
- The compensation should be as close as possible to the CMPx pins. The CMPx and ROSC pins are sensitive to noise so the components associated to these pins should be located as close as possible to the IC and routed with minimal lengths of trace.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65288RHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65288
TPS65288RHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65288
TPS65288RHARG4	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65288
TPS65288RHARG4.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65288
TPS65288RHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65288
TPS65288RHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65288

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

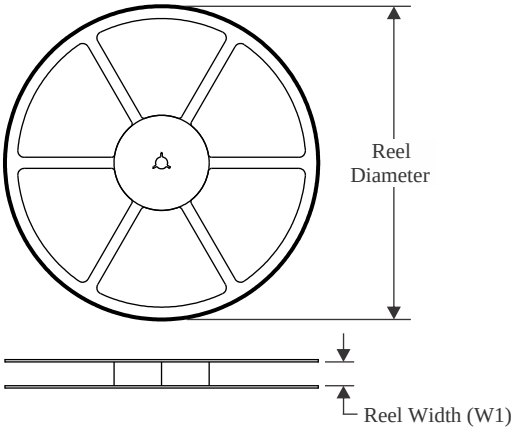
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

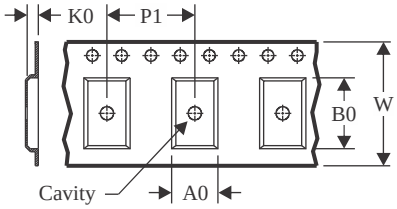
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

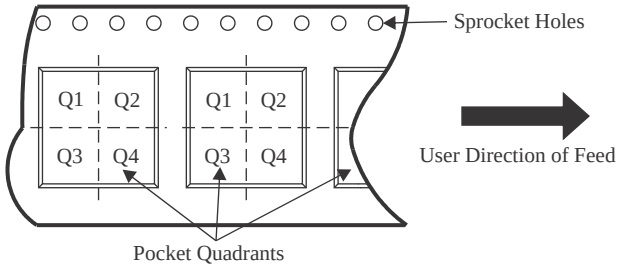


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

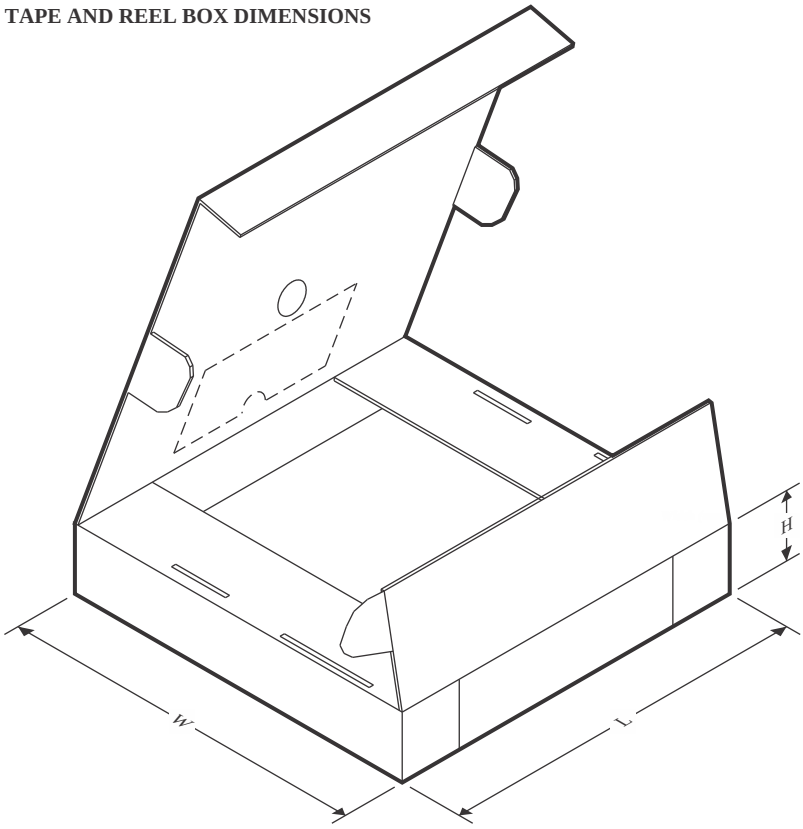
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65288RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65288RHARG4	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65288RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65288RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
TPS65288RHARG4	VQFN	RHA	40	2500	367.0	367.0	38.0
TPS65288RHAT	VQFN	RHA	40	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

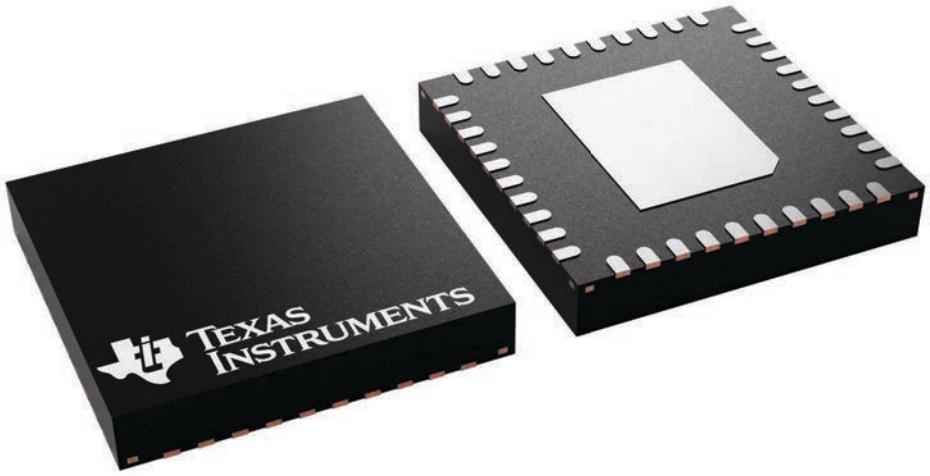
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



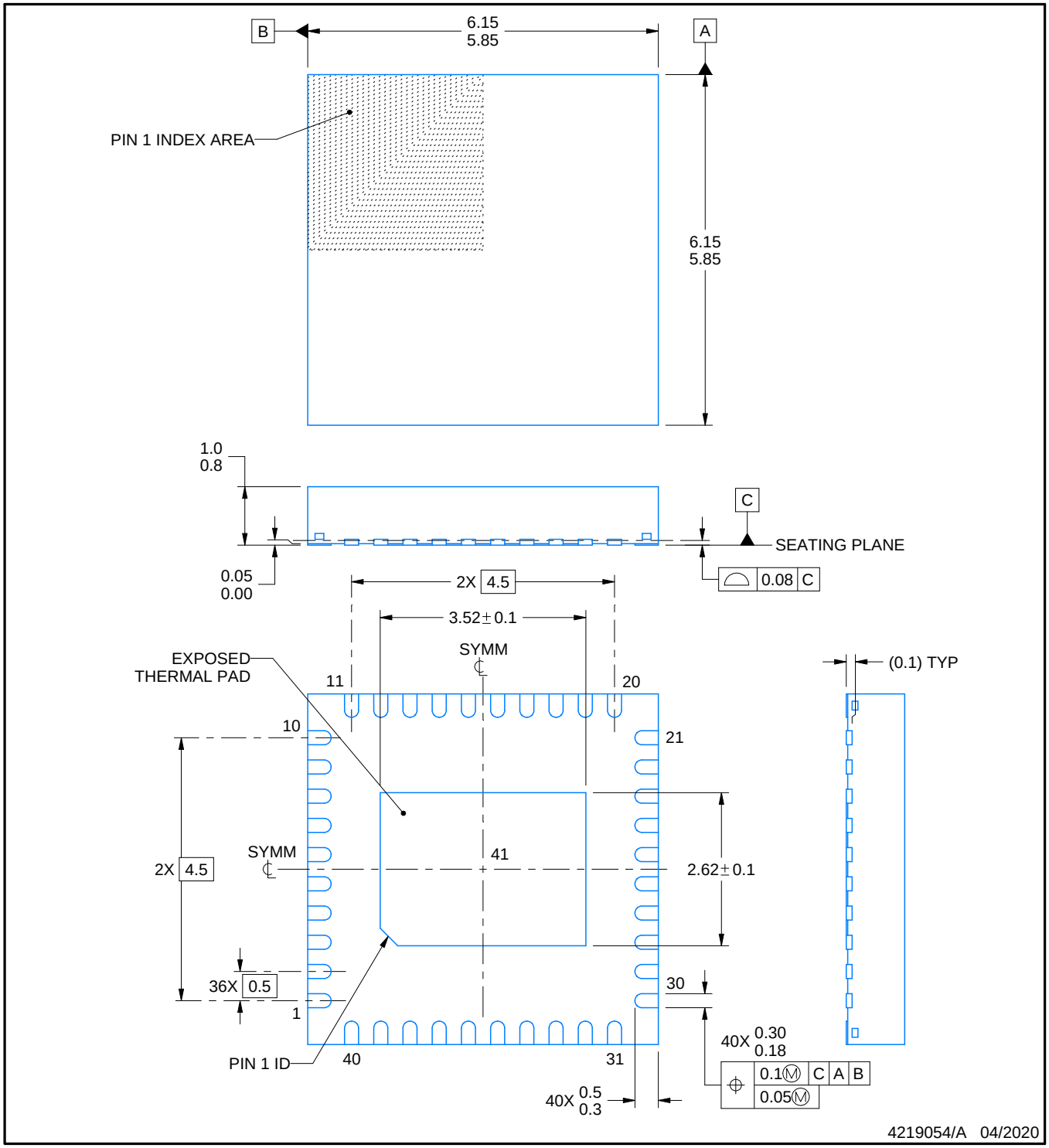
4225870/A

RHA0040E

PACKAGE OUTLINE

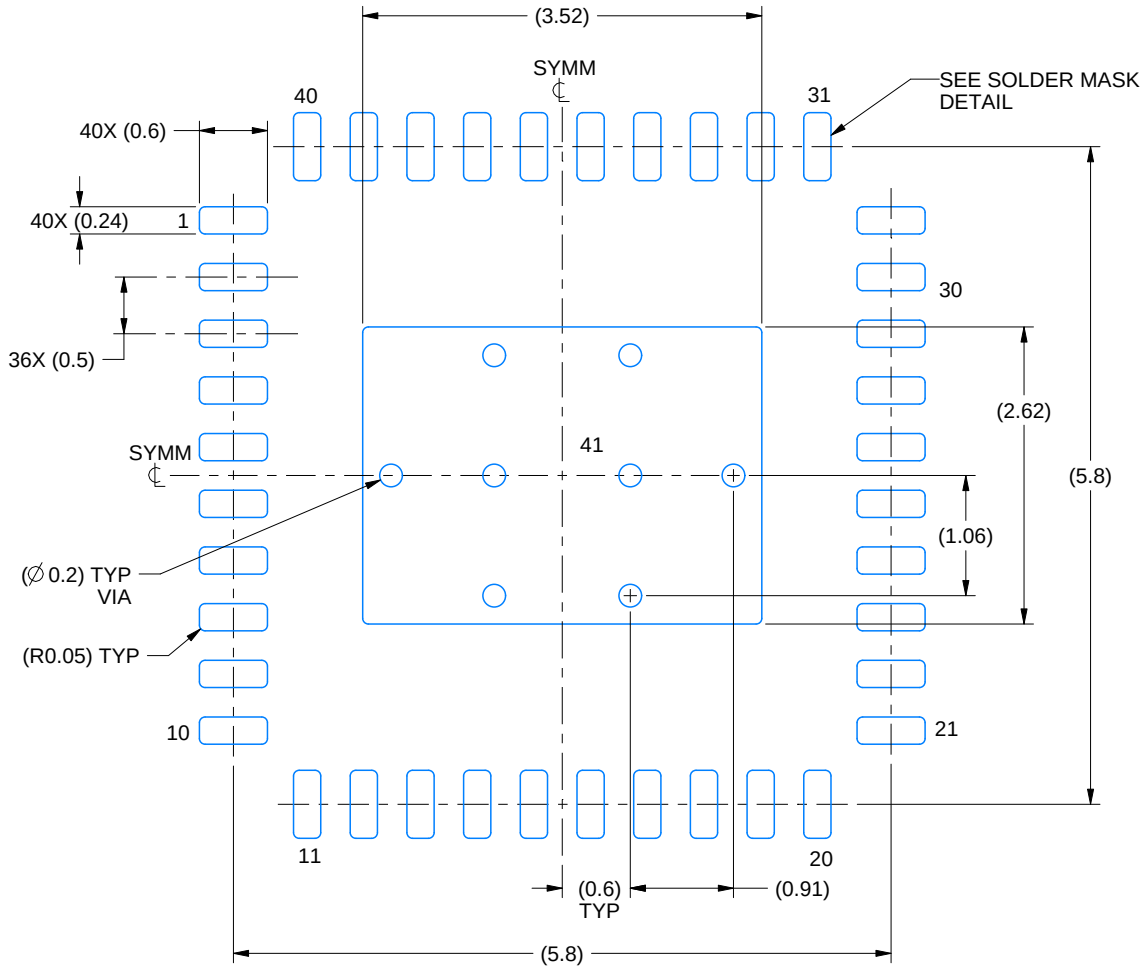
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

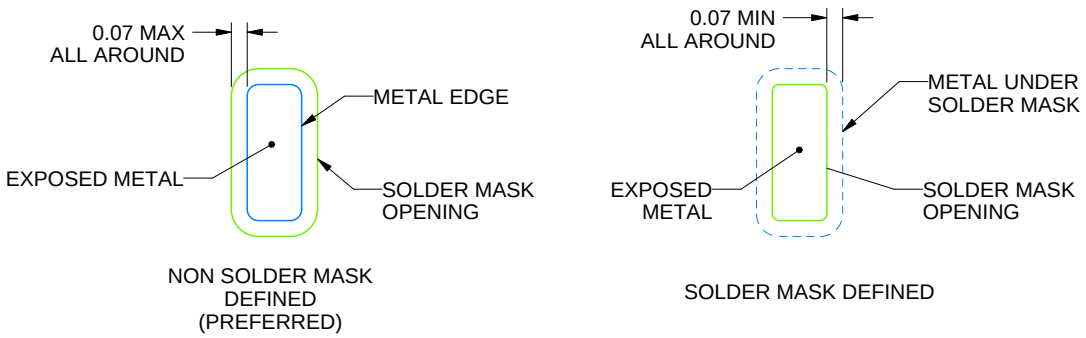


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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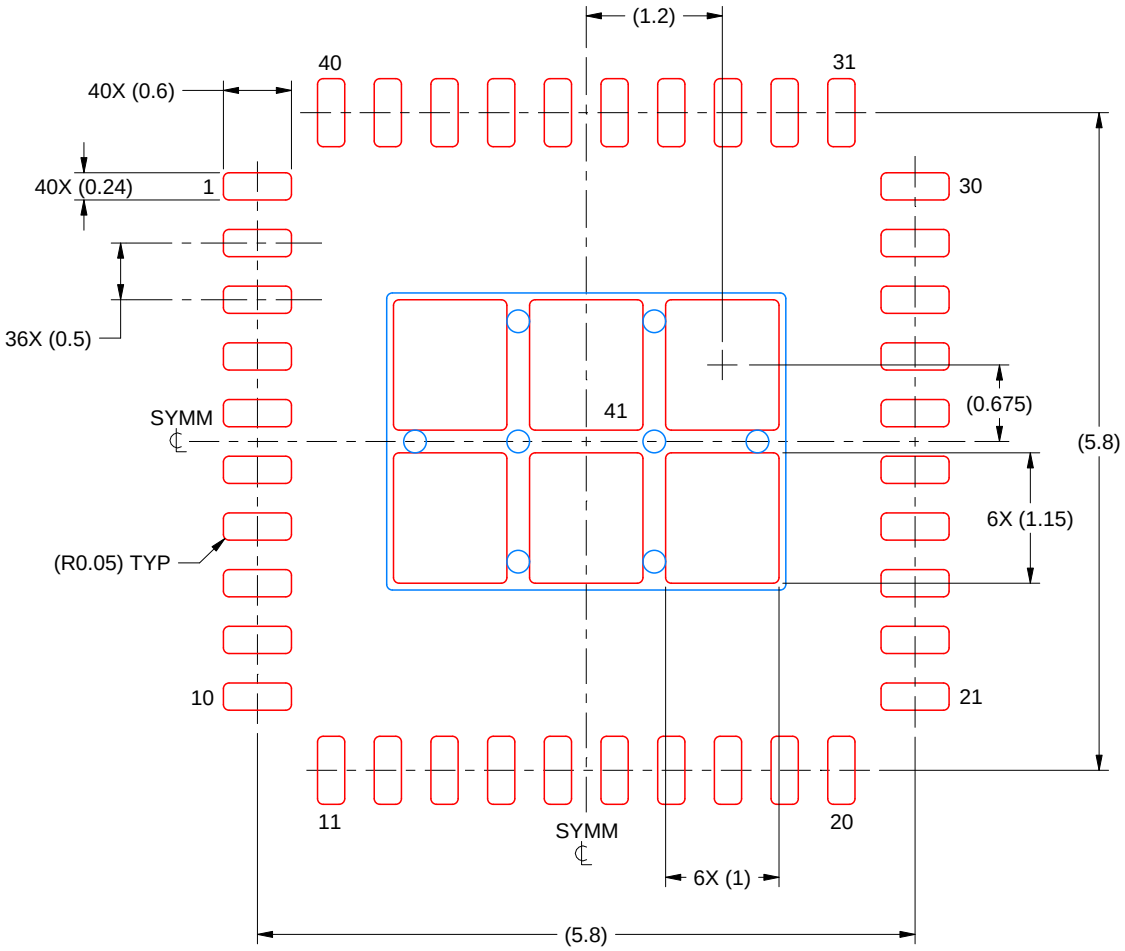
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 41
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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