DUAL-OUTPUT, LOW DROPOUT VOLTAGE REGULATORS
WITH INTEGRATED SVS FOR SPLIT VOLTAGE SYSTEMS

Check for Samples: TPS70445, TPS70448, TPS70451, TPS70458, TPS70402

FEATURES
- Dual Output Voltages for Split-Supply Applications
- Independent Enable Functions (See Part Number TPS703xx for Sequenced Outputs)
- Output Current Range of 1 A on Regulator 1 and 2 A on Regulator 2
- Fast Transient Response
- Voltage Options: 3.3-V/2.5-V, 3.3-V/1.8-V, 3.3-V/1.5-V, 3.3-V/1.2-V, and Dual Adjustable Outputs
- Open Drain Power-On Reset with 120-ms Delay
- Open Drain Power Good for Regulator 1 and Regulator 2
- Ultralow 185μA (typ) Quiescent Current
- 2μA Input Current During Standby
- Low Noise: 78μV RMS Without Bypass Capacitor
- Quick Output Capacitor Discharge Feature
- One Manual Reset Input
- 2% Accuracy Over Load and Temperature
- Undervoltage Lockout (UVLO) Feature
- 24-Pin PowerPAD™ TSSOP Package
- Thermal Shutdown Protection

DESCRIPTION
The TPS704xx family of devices consists of dual-output, low-dropout voltage regulators with integrated SVS (RESET, POR, or power on reset) and power good (PG) functions. These devices are capable of supplying 1 A and 2 A by regulator 1 and regulator 2 respectively. Quiescent current is typically 185 μA at full load. Differentiated features, such as accuracy, fast transient response, SVS supervisory circuit (power on reset), manual reset input, and independent enable functions provide a complete system solution.

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The TPS704xx family of voltage regulators offers very low dropout voltage and dual outputs. These devices have extremely low noise output performance without using any added filter bypass capacitors and are designed to have a fast transient response and be stable with 47-μF low ESR capacitors.

These devices have fixed 3.3-V/2.5-V, 3.3-V/1.8-V, 3.3-V/1.5-V, 3.3-V/1.2-V, and adjustable voltage options. Regulator 1 can support up to 1 A, and regulator 2 can support up to 2 A. Separate voltage inputs allow the designer to configure the source power.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 160 mV on regulator 1) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (maximum of 250 μA over the full range of output current and full range of temperature). This LDO family also features a sleep mode; applying a high signal to EN1 or EN2 (enable) shuts down regulator 1 or regulator 2, respectively. When a high signal is applied to both EN1 and EN2, both regulators enter sleep mode, thereby reducing the input current to 2 μA at TJ = +25°C.

For each regulator, there is an internal discharge transistor to discharge the output capacitor when the regulator is turned off (disabled).

The PG1 pin reports the voltage condition at VOUT1. The PG1 pin can be used to implement a SVS (RESET, POR, or power on reset) for the circuitry supplied by regulator 1. The PG2 pin reports the voltage conditions at VOUT2. The PG2 pin can be used to implement a SVS (power on reset) for the circuitry supplied by regulator 2.

The TPS704xx features a RESET (SVS, POR, or power on reset). RESET is an active low, open drain output and requires a pull-up resistor for normal operation. When pulled up, RESET goes into a high impedance state (that is, logic high) after a 120-ms delay when both of the following conditions are met. First, VIN1 must be above the undervoltage condition. Second, the manual reset (MR) pin must be in a high impedance state. To monitor VOUT1, the PG1 output pin can be connected to MR. To monitor VOUT2, the PG2 output pin can be connected to MR. RESET can be used to drive power on reset or a low-battery indicator. If RESET is not used, it can be left floating.

Internal bias voltages are powered by VIN1 and require 2.7 V for full functionality. Each regulator input has an undervoltage lockout circuit that prevents each output from turning on until the respective input reaches 2.5 V.
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>VOLTAGE (V)</th>
<th>PACKAGE-LEAD (DESIGNATOR)</th>
<th>SPECIFIED TEMPERATURE RANGE (T J)</th>
<th>ORDERING NUMBER</th>
<th>TRANSPORT MEDIA, QUANTITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS70402</td>
<td>Adjustable</td>
<td>Adjustable HTSSOP-24 (PWP)</td>
<td>−40°C to +125°C</td>
<td>TPS70402PWP</td>
<td>Tube, 60</td>
</tr>
<tr>
<td></td>
<td>3.3 V</td>
<td>1.2 V HTSSOP-24 (PWP)</td>
<td>−40°C to +125°C</td>
<td>TPS70402PWPR</td>
<td>Tape and Reel, 2000</td>
</tr>
<tr>
<td>TPS70445</td>
<td>3.3 V</td>
<td>1.5 V HTSSOP-24 (PWP)</td>
<td>−40°C to +125°C</td>
<td>TPS70445PWP</td>
<td>Tube, 60</td>
</tr>
<tr>
<td>TPS70448</td>
<td>3.3 V</td>
<td>1.8 V HTSSOP-24 (PWP)</td>
<td>−40°C to +125°C</td>
<td>TPS70448PWP</td>
<td>Tube, 60</td>
</tr>
<tr>
<td>TPS70451</td>
<td>3.3 V</td>
<td>2.5 V HTSSOP-24 (PWP)</td>
<td>−40°C to +125°C</td>
<td>TPS70451PWP</td>
<td>Tube, 60</td>
</tr>
<tr>
<td>TPS70458</td>
<td>3.3 V</td>
<td>2.5 V HTSSOP-24 (PWP)</td>
<td>−40°C to +125°C</td>
<td>TPS70458PWP</td>
<td>Tube, 60</td>
</tr>
</tbody>
</table>

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at ti.com.

(2) For fixed 1.20 V operation, tie FB to OUT.

**ABSOLUTE MAXIMUM RATING**

Over operating free-air temperature range (unless otherwise noted).

<table>
<thead>
<tr>
<th></th>
<th>TPS704xx</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range: V IN1, V IN2 (2)</td>
<td>−0.3 to +7</td>
<td>V</td>
</tr>
<tr>
<td>Voltage range at EN1, EN2</td>
<td>−0.3 to +7</td>
<td>V</td>
</tr>
<tr>
<td>Output voltage range (V OUT1, V SENSE1)</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Output voltage range (V OUT2, V SENSE2)</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Maximum RESET, PG1, PG2 voltage</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Maximum MR voltage V IN1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Peak output current</td>
<td>Internally limited</td>
<td>—</td>
</tr>
<tr>
<td>Continuous total power dissipation</td>
<td>See Dissipation Ratings Table</td>
<td>—</td>
</tr>
<tr>
<td>Operating virtual junction temperature range, T J</td>
<td>−40 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature range, T STG</td>
<td>−65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>ESD rating, HBM</td>
<td>2</td>
<td>kV</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are tied to network ground.
DISSIPATION RATINGS

<table>
<thead>
<tr>
<th>PACKAGE</th>
<th>AIR FLOW (CFM)</th>
<th>$T_A \leq +25^\circ C$</th>
<th>DERATING FACTOR</th>
<th>$T_A = +70^\circ C$</th>
<th>$T_A = +85^\circ C$</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWP(1)</td>
<td>0</td>
<td>3.067W</td>
<td>30.67mW/°C</td>
<td>1.687W</td>
<td>1.227W</td>
</tr>
<tr>
<td></td>
<td>250</td>
<td>4.115W</td>
<td>41.15mW/°C</td>
<td>2.265W</td>
<td>1.646W</td>
</tr>
</tbody>
</table>

(1) This parameter is measured with the recommended copper heat sink pattern on a 4-layer PCB, 1 oz. copper on a 4-in by 4-in ground layer. For more information, refer to TI technical brief SLMA002.

RECOMMENDED OPERATING CONDITIONS

Over operating temperature range (unless otherwise noted).

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage, $V_T$ (1) (regulator 1 and 2)</td>
<td>2.7</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>Output current, $I_O$ (regulator 1)</td>
<td>0</td>
<td>1</td>
<td>A</td>
</tr>
<tr>
<td>Output current, $I_O$ (regulator 2)</td>
<td>0</td>
<td>2</td>
<td>A</td>
</tr>
<tr>
<td>Output voltage range (for adjustable option)</td>
<td>1.22</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Operating virtual junction temperature, $T_J$</td>
<td>-40</td>
<td>+125</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) To calculate the minimum input voltage for maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max load)}$. 
**ELECTRICAL CHARACTERISTICS**

Over recommended operating junction temperature range ($T_J = -40 \degree C$ to $+125 \degree C$), $V_{IN1}$ or $V_{IN2} = V_{OUT(nom)} + 1 \, V$, $I_O = 1 \, mA$, $EN = 0 \, V$, $C_{OUT1} = 22 \, \mu F$, and $C_{OUT2} = 47 \, \mu F$ (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_O$</td>
<td>Reference voltage</td>
<td>2.7 V $&lt; V_{IN} &lt; 6 , V$, $T_J = +25 \degree C$</td>
<td>FB connected to $V_O$</td>
<td>1.22</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V $&lt; V_{IN} &lt; 6 , V$, $T_J = +25 \degree C$</td>
<td>FB connected to $V_O$</td>
<td>1.196</td>
<td>1.244</td>
</tr>
<tr>
<td>$1.2 , V$</td>
<td>Output (V$_{OUT2}$)</td>
<td>2.7 V $&lt; V_{IN} &lt; 6 , V$, $T_J = +25 \degree C$</td>
<td>1.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V $&lt; V_{IN} &lt; 6 , V$, $T_J = +25 \degree C$</td>
<td>1.176</td>
<td>1.224</td>
<td></td>
</tr>
<tr>
<td>$1.5 , V$</td>
<td>Output (V$_{OUT2}$)</td>
<td>2.7 V $&lt; V_{IN} &lt; 6 , V$, $T_J = +25 \degree C$</td>
<td>1.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.7 V $&lt; V_{IN} &lt; 6 , V$, $T_J = +25 \degree C$</td>
<td>1.47</td>
<td>1.53</td>
<td></td>
</tr>
<tr>
<td>$1.8 , V$</td>
<td>Output (V$_{OUT2}$)</td>
<td>2.8 V $&lt; V_{IN} &lt; 6 , V$, $T_J = +25 \degree C$</td>
<td>1.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.8 V $&lt; V_{IN} &lt; 6 , V$, $T_J = +25 \degree C$</td>
<td>1.764</td>
<td>1.836</td>
<td></td>
</tr>
<tr>
<td>$2.5 , V$</td>
<td>Output (V$_{OUT2}$)</td>
<td>3.5 V $&lt; V_{IN} &lt; 6 , V$, $T_J = +25 \degree C$</td>
<td>2.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.5 V $&lt; V_{IN} &lt; 6 , V$, $T_J = +25 \degree C$</td>
<td>2.45</td>
<td>2.55</td>
<td></td>
</tr>
<tr>
<td>$3.3 , V$</td>
<td>Output (V$_{OUT2}$)</td>
<td>4.3 V $&lt; V_{IN} &lt; 6 , V$, $T_J = +25 \degree C$</td>
<td>3.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.3 V $&lt; V_{IN} &lt; 6 , V$, $T_J = +25 \degree C$</td>
<td>3.234</td>
<td>3.366</td>
<td></td>
</tr>
</tbody>
</table>

- Quiescent current (GND current) for regulator 1 and regulator 2, $ENT = EN2 = 0 \, V$ (1)
  - See (2) $T_J = +25 \degree C$ | 185 | µA |
  - See (2) | 250 | µA |

- Output voltage line regulation ($\Delta V_O/V_O$) for regulator 1 and regulator 2 (3)
  - $V_O + 1 \, V < V_{IN} \leq 6 \, V$, $T_J = +25 \degree C$ (1)
  - $V_O + 1 \, V < V_{IN} \leq 6 \, V$ (3)
  - $0.01$ | %V |
  - $0.1$ | %V |

- Load regulation for $V_{OUT1}$ and $V_{OUT2}$ $T_J = +25 \degree C$
  - $1$ | mV |

- $V_n$ Output noise voltage (TPS70451)
  - Regulator 1
  - BW = 300 Hz to 50 kHz, $C_O = 33 \, \mu F$, $T_J = +25 \degree C$
  - $79$ | µV RMS |
  - Regulator 2
  - $77$ | µV RMS |

- Output current limit
  - Regulator 1
  - $V_{OUT} = 0 \, V$
  - $1.75$ | A |
  - Regulator 2
  - $3.8$ | A |
  - $4.5$ | A |

- Thermal shutdown junction temperature:
  - $+150 \degree C$

- $I_I$ (standby) current
  - Regulator 1
  - $1 \, mA$
  - $2 \, mA$ | µA |
  - Regulator 2
  - $10 \, mA$

- PSRR Power-supply ripple rejection (TPS70451)
  - Regulator 1
  - $f = 1 \, kHz$, $T_J = +25 \degree C$ (1)
  - $65$ | dB |
  - Regulator 2
  - $f = 1 \, kHz$, $T_J = +25 \degree C$ (1)
  - $60$ | dB |

**RESET Terminal**

- Minimum input voltage for valid $RESET$ $I_{RESET} = 300 \, \mu A$, $V_{(RESET)} \leq 0.8 \, V$
  - $1.0$ | V |
  - $1.3$ | V |

- $I_{RESET}$ pulse duration
  - $80$ | ms |
  - $120$ | ms |
  - $160$ | ms |

- Output low voltage $V_{IN} = 3.5 \, V$, $I_{(RESET)} = 1 \, mA$
  - $0.15$ | V |
  - $0.4$ | V |

- Leakage current $V_{(RESET)} = 6 \, V$
  - $1 \, \mu A$

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(1) Minimum input operating voltage is $2.7 \, V$ or $V_{(typ)} + 1 \, V$, whichever is greater. Maximum input voltage = $6 \, V$, minimum output current = $1 \, mA$.

(2) $I_O = 1 \, mA$ to $1 \, A$ for Regulator 1 and $1 \, mA$ to $2 \, A$ for Regulator 2.

(3) If $V_O < 1.8 \, V$ then $V_{max} = 6 \, V$, $V_{min} = 2.7 \, V$, Line regulation (mV) = $\left(\%V\right) \times V_O \times \frac{V_{max} - 2.7}{100} \times 1000$

If $V_O > 2.5 \, V$ then $V_{max} = 6 \, V$, $V_{min} = V_O + 1 \, V$, Line regulation (mV) = $\left(\%V\right) \times V_O \times \frac{V_{max} - \left(V_O + 1\right)}{100} \times 1000$
**ELECTRICAL CHARACTERISTICS (continued)**

Over recommended operating junction temperature range \((T_J = -40°C \text{ to } +125°C)\), \(V_{\text{IN1}}\) or \(V_{\text{IN2}} = V_{\text{OUT(nom)}} + 1\text{ V}\), \(I_O = 1\text{ mA}\), \(EN = 0\text{ V}\), \(C_{\text{OUT1}} = 22\mu\text{F}\), and \(C_{\text{OUT2}} = 47\mu\text{F}\) (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{IN1}}/V_{\text{IN2}}) Terminal</td>
<td>UVLO threshold</td>
<td>2.4</td>
<td>2.65</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>UVLO hysteresis</td>
<td>110</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>(PG1/PG2) Terminal</td>
<td>Minimum input voltage for valid PGx (I_{\text{(PGx)}} = 300\text{ µA}, V_{\text{(PGx)}} \leq 0.8\text{ V})</td>
<td>1.0</td>
<td>1.3</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Trip threshold voltage (V_O) decreasing</td>
<td>92</td>
<td>95</td>
<td>98</td>
<td>%V_{\text{OUT}}</td>
</tr>
<tr>
<td></td>
<td>Hysteresis voltage Measured at (V_O)</td>
<td>0.5</td>
<td></td>
<td></td>
<td>%V_{\text{OUT}}</td>
</tr>
<tr>
<td></td>
<td>(I_{\text{h(PGx)}}) Rising edge deglitch</td>
<td>30</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>Output low voltage (V_{\text{IN}} = 2.7\text{ V}), (I_{\text{(PGx)}} = 1\text{ mA})</td>
<td>0.15</td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Leakage current (V_{\text{(PGx)}} = 6\text{ V})</td>
<td>1</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>(EN1/EN2) Terminal</td>
<td>High-level (ENx) input voltage</td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Low-level (ENx) input voltage</td>
<td></td>
<td>0.7</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Input current ((ENx))</td>
<td></td>
<td>−1</td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td>MR Terminal</td>
<td>High-level input voltage</td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Low-level input voltage</td>
<td></td>
<td>0.7</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Pull-up current source</td>
<td></td>
<td>6</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>(V_{\text{OUT1}}) Terminal</td>
<td>Dropout voltage(^{(4)}) (I_O = 1\text{ A}, V_{\text{IN1}} = 3.2\text{ V}, T_J = +25°C)</td>
<td>160</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>(I_O = 1\text{ A}, V_{\text{IN1}} = 3.2\text{ V})</td>
<td></td>
<td>250</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Peak output current (2\text{ ms pulse width})</td>
<td></td>
<td>1.2</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>Discharge transistor current (V_{\text{OUT1}} = 1.5\text{ V})</td>
<td></td>
<td>7.5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>(V_{\text{OUT2}}) Terminal</td>
<td>Peak output current (2\text{ ms pulse width})</td>
<td></td>
<td>3</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>Discharge transistor current (V_{\text{OUT2}} = 1.5\text{ V})</td>
<td></td>
<td>7.5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>(FB) Terminal</td>
<td>Input current: TPS70402 (FB = 1.8\text{ V})</td>
<td></td>
<td>1</td>
<td></td>
<td>µA</td>
</tr>
</tbody>
</table>

\(^{(4)}\) Input voltage \((V_{\text{IN1}}\) or \(V_{\text{IN2}}\)) = \(V_{\text{O(typ)}} − 100\text{ mV}\). For 1.5-V, 1.8-V, and 2.5-V regulators, the dropout voltage is limited by input voltage range. The 3.3-V regulator input is set to 3.2 V to perform this test.
A. For most applications, V_{SENSE1} and V_{SENSE2} should be externally connected to V_{OUT1} and V_{OUT2}, respectively, as close as possible to the device. For other implementations, refer to SENSE terminal connection discussion in the Application Information section.
Adjustable Voltage Version

A. For most applications, FB1 and FB2 should be externally connected to resistor dividers as close as possible to the device. For other implementations, refer to FB terminals connection discussion in the Application Information section.
**NOTE A:** \( V_{RES} \) is the minimum input voltage for a valid \( \overline{RESET} \). The symbol \( V_{RES} \) is not currently listed within EIA or JEDEC standards for semiconductor symbology.

**NOTES A:** \( V_{PG1} \) is the minimum input voltage for a valid PG. The symbol \( V_{PG1} \) is not currently listed within EIA or JEDEC standards for semiconductor symbology.

**B:** \( V_{IT+} \) trip voltage is typically 5% lower than the output voltage (95%\( V_O \)). \( V_{IT-} \) to \( V_{IT+} \) is the hysteresis voltage.
NOTE A: \( V_{\text{IT}} \) trip voltage is typically 5% lower than the output voltage (95%\(V_O\)). \( V_{\text{IT}} \) to \( V_{\text{IT}} \) is the hysteresis voltage.

### TERMINAL FUNCTIONS

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<th>I/O</th>
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<td>EN1</td>
<td>I</td>
<td>Active low enable for ( V_{\text{OUT}} )</td>
</tr>
<tr>
<td>EN2</td>
<td>I</td>
<td>Active low enable for ( V_{\text{OUT}} )</td>
</tr>
<tr>
<td>GND</td>
<td>—</td>
<td>Ground</td>
</tr>
<tr>
<td>GND/HEATSINK</td>
<td>—</td>
<td>Ground/heatsink</td>
</tr>
<tr>
<td>MR</td>
<td>I</td>
<td>Manual reset input, active low, pulled up internally</td>
</tr>
<tr>
<td>NC</td>
<td>—</td>
<td>No connection</td>
</tr>
<tr>
<td>PG1</td>
<td>O</td>
<td>Open drain output, low when ( V_{\text{OUT}} ) voltage is less than 95% of the nominal regulated voltage</td>
</tr>
<tr>
<td>PG2</td>
<td>O</td>
<td>Open drain output, low when ( V_{\text{OUT}} ) voltage is less than 95% of the nominal regulated voltage</td>
</tr>
<tr>
<td>RESET</td>
<td>O</td>
<td>Open drain output, SVS (power-on reset) signal, active low</td>
</tr>
<tr>
<td>( V_{\text{IN}} )</td>
<td>I</td>
<td>Input voltage of regulator 1</td>
</tr>
<tr>
<td>( V_{\text{IN}} )</td>
<td>I</td>
<td>Input voltage of regulator 2</td>
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<tr>
<td>( V_{\text{OUT}} )</td>
<td>O</td>
<td>Output voltage of regulator 1</td>
</tr>
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<td>( V_{\text{OUT}} )</td>
<td>O</td>
<td>Output voltage of regulator 2</td>
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<tr>
<td>( V_{\text{SENSE}}/\text{FB1} )</td>
<td>I</td>
<td>Regulator 1 output voltage sense/regulator 1 feedback for adjustable</td>
</tr>
<tr>
<td>( V_{\text{SENSE}}/\text{FB2} )</td>
<td>I</td>
<td>Regulator 2 output voltage sense/regulator 2 feedback for adjustable</td>
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</table>
Detailed Description

The TPS704xx low dropout regulator family provides dual regulated output voltages with independent enable functions. These devices provide fast transient response and high accuracy with small output capacitors, while drawing low quiescent current. Other features are integrated SVS (power-on reset, RESET) and power good (PG1, PG2) that monitor output voltages and provide logic output to the system. These differentiated features provide a complete power solution.

The TPS704xx, unlike many other LDOs, features very low quiescent current that remains virtually constant even with varying loads. Conventional LDO regulators use a PNP pass element, the base current of which is directly proportional to the load current through the regulator (I_B = I_O/β). The TPS704xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage-driven, operating current is low and stable over the full load range.

Pin Functions

Enable (EN1, EN2)

The EN terminals are inputs that enable or shut down each respective regulator. If EN is at a voltage high signal, the respective regulator is in shutdown mode. When EN goes to voltage low, the respective regulator is enabled.

Power-Good (PG1, PG2)

The PG terminals are open drain, active high output terminals that indicate the status of each respective regulator. When V_OUT1 reaches 95% of its regulated voltage, PG1 goes to a high impedance state. When V_OUT2 reaches 95% of its regulated voltage, PG2 goes to a high impedance state. Each PG goes to a low impedance state when its respective output voltage is pulled below 95% (that is, goes to an overload condition) of its regulated voltage. The open drain outputs of the PG terminals require a pull-up resistor.

Manual Reset Pin

MR is an active low input terminal used to trigger a reset condition. When MR is pulled to logic low, a POR (RESET) occurs. The terminal has a 6-μA pull-up current to V_IN1; however, it is recommended that the pin be pulled high to V_IN1 when it is not used.

Sense (V_SENSE1, V_SENSE2)

The sense terminals of fixed-output options must be connected to the regulator outputs, and the connection should be as short as possible. Internally, the sense terminal connects to high-impedance, wide-bandwidth amplifiers through a resistor-divider network and noise pickup feeds through to the regulator output. It is essential to route the sense connection in such a way as to minimize or avoid noise pickup. Adding RC networks between sense terminals and V_OUT terminals to filter noise is not recommended because these networks can cause the regulators to oscillate.
FB1 and FB2

FB1 and FB2 are input terminals used for adjustable-output devices and must be connected to the external feedback resistor divider. FB1 and FB2 connections should be as short as possible. It is essential to route them in such a way as to minimize or avoid noise pickup. Adding RC networks between FB terminals and $V_{OUT}$ terminals to filter noise is not recommended because these networks can cause the regulators to oscillate.

RESET Indicator

RESET is an active low, open drain output and requires a pullup resistor for normal operation. When pulled up, RESET goes into a high impedance state (that is, logic high) after a 120-ms delay when both of the following conditions are met. First, $V_{IN1}$ must be above the undervoltage condition. Second, the manual reset (MR) pin must be in a high impedance state. To monitor $V_{OUT1}$, the PG1 output pin can be connected to MR. To monitor $V_{OUT2}$, the PG2 output pin can be connected to MR. If RESET is not used, it can be left floating.

$V_{IN1}$ and $V_{IN2}$

$V_{IN1}$ and $V_{IN2}$ are inputs to each regulator. **Internal bias voltages are powered by $V_{IN1}$.**

$V_{OUT1}$ and $V_{OUT2}$

$V_{OUT1}$ and $V_{OUT2}$ are output terminals of each regulator.
### TYPICAL CHARACTERISTICS

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<td>vs Output current</td>
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<td>PSRR Power-supply rejection ratio</td>
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<td><strong>V&lt;sub&gt;O&lt;/sub&gt;</strong> Output voltage</td>
<td>vs Junction temperature</td>
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<td><strong>V&lt;sub&gt;O&lt;/sub&gt;</strong> Output voltage</td>
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<tr>
<td>Equivalent series resistance (ESR)</td>
<td>vs Output current</td>
<td>Figure 26 and Figure 27</td>
</tr>
</tbody>
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#### Diagrams

**Figure 1.**

TPS70451

OUTPUT VOLTAGE

vs

OUTPUT CURRENT

**Figure 2.**

TPS70451

OUTPUT VOLTAGE

vs

OUTPUT CURRENT

---

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Figure 6.

Figure 7.

Figure 8.

Figure 9.
TYPICAL CHARACTERISTICS (continued)

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

![Graph showing spectral noise density for IN1 and OUT1 with specified parameters.]

- $V_{IN1} = 4.3 \, V$
- $V_{OUT1} = 3.3 \, V$
- $C_{OUT1} = 22 \, \mu F$
- $I_O = 10 \, mA$
- $T_J = 25^\circ C$

Figure 10.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

![Graph showing spectral noise density for IN2 and OUT2 with specified parameters.]

- $V_{IN2} = 2.8 \, V$
- $V_{OUT2} = 1.8 \, V$
- $C_{OUT2} = 47 \, \mu F$
- $I_O = 10 \, mA$
- $T_J = 25^\circ C$

Figure 11.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

![Graph showing spectral noise density for IN2 and OUT2 with specified parameters.]

- $V_{IN1} = 4.3 \, V$
- $V_{OUT1} = 3.3 \, V$
- $C_{OUT1} = 22 \, \mu F$
- $I_O = 1 \, mA$
- $T_J = 25^\circ C$

Figure 12.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

![Graph showing spectral noise density for IN2 and OUT2 with specified parameters.]

- $V_{IN2} = 2.8 \, V$
- $V_{OUT2} = 1.8 \, V$
- $C_{OUT2} = 47 \, \mu F$
- $I_O = 2 \, A$
- $T_J = 25^\circ C$

Figure 13.
TYPICAL CHARACTERISTICS (continued)

OUTPUT IMPEDANCE vs FREQUENCY

Figure 14.

OUTPUT IMPEDANCE vs FREQUENCY

Figure 15.

OUTPUT IMPEDANCE vs FREQUENCY

Figure 16.

OUTPUT IMPEDANCE vs FREQUENCY

Figure 17.
TPS70451
DROPOUT VOLTAGE
vs TEMPERATURE

![Figure 18.](image1)

TPS70451
DROPOUT VOLTAGE
vs TEMPERATURE

![Figure 19.](image2)

TPS70402
DROPOUT VOLTAGE
vs INPUT VOLTAGE

![Figure 20.](image3)

TPS70402
DROPOUT VOLTAGE
vs INPUT VOLTAGE

![Figure 21.](image4)
TYPICAL CHARACTERISTICS (continued)

LOAD TRANSIENT RESPONSE

Figure 22.

V_{IN1} = 4.3 V
V_{OUT1} = 3.3 V
C_{O} = 22 \mu F

I_{O} - Output Current - A

\Delta V_{O} - Change in Output Voltage - mV

0 0.2 0.4 0.6 0.8 1 1.2 1.4 1.6 1.8 2 ms

Figure 23.

V_{OUT2} = 1.8 V
I_{O} = 2 A
C_{O} = 47 \mu F

I_{O} - Output Current - A

\Delta V_{O} - Change in Output Voltage - mV

0 0.2 0.4 0.6 0.8 1 1.2 1.4 1.6 1.8 2 ms

LINE TRANSIENT RESPONSE

Figure 24.

V_{OUT1} = 3.3 V
I_{O} = 1 A
C_{O} = 22 \mu F

V_{I} - Input Voltage - V

\Delta V_{O} - Change in Output Voltage - mV

0 20 40 60 80 100 120 140 160 180 200 \mu s

Figure 25.

V_{OUT2} = 1.8 V
I_{O} = 2 A
C_{O} = 47 \mu F

V_{I} - Input Voltage - V

\Delta V_{O} - Change in Output Voltage - mV

0 20 40 60 80 100 120 140 160 180 200 \mu s
TYPICAL CHARACTERISTICS (continued)

OUTPUT VOLTAGE AND ENABLE VOLTAGE

vs TIME (START-UP)

Figure 26.

OUTPUT VOLTAGE AND ENABLE VOLTAGE

vs TIME (START-UP)

Figure 27.

Figure 28. Test Circuit for Typical Regions of Stability
Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to $C_O$. 
THERMAL INFORMATION

Thermally-Enhanced TSSOP-24 (PWP—PowerPAD™)

The thermally-enhanced PWP package is based on the 24-pin TSSOP, but includes a thermal pad [see Figure 33(c)] to provide an effective thermal contact between the IC and the printed wiring board (PWB).

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, suffer from several shortcomings: they do not address the very low profile requirements (<2 mm) of many of today’s advanced systems, and they do not offer a pin-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PWP package (thermally-enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PWP package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a lead-frame design (patent pending) and manufacturing technique to provide the user with direct connection to the heat-generating IC. When this pad is soldered or otherwise coupled to an external heat dissipator, high power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved.

Because the conduction path has been enhanced, power-dissipation capability is determined by the thermal considerations in the PWB design. For example, simply adding a localized copper plane (heat-sink surface), which is coupled to the thermal pad, enables the PWP package to dissipate 2.5 W in free air (reference Figure 35(a), 8 cm² of copper heat sink and natural convection). Increasing the heat-sink size increases the power dissipation range for the component. The power dissipation limit can be further improved by adding airflow to a PWB/IC assembly (see Figure 34 and Figure 35). The line drawn at 0.3 cm² in Figure 34 and Figure 35 indicates performance at the minimum recommended heat-sink size, illustrated in Figure 36.
The thermal pad is directly connected to the substrate of the IC, which for the TPS704xx series is a secondary electrical connection to device ground. The heat-sink surface that is added to the PWP can be a ground plane or left electrically isolated. In TO220-type surface-mount packages, the thermal connection is also the primary electrical connection for a given terminal which is not always ground. The PWP package provides up to 24 independent leads that can be used as inputs and outputs (Note: leads 1, 12, 13, and 24 are internally connected to the thermal pad and the IC substrate).

![THERMAL RESISTANCE vs COPPER HEATSINK AREA](image)

**Figure 34.**
Figure 35. Power Ratings of the PWP Package at Ambient Temperatures of +25°C, +55°C, and +105°C
Figure 36 is an example of a thermally-enhanced PWB layout for use with the new PWP package. This board configuration was used in the thermal experiments that generated the power ratings shown in Figure 34 and Figure 35. As discussed earlier, copper has been added on the PWB to conduct heat away from the device. $R_{\text{JA}}$ for this assembly is illustrated in Figure 34 as a function of heat-sink area. A family of curves is included to illustrate the effect of airflow introduced into the system.

![Figure 36. PWB Layout (Including Copper Heatsink Area) for Thermally-Enhanced PWP Package](image)

From Figure 34, $R_{\text{JA}}$ for a PWB assembly can be determined and used to calculate the maximum power-dissipation limit for the component/PWB assembly, with the equation:

$$P_{\text{D(max)}} = \frac{T_{\text{J(max)}} - T_{\text{A}}}{R_{\text{JA(system)}}}$$

where:

- $T_{\text{J(max)}}$ is the maximum specified junction temperature (+150°C absolute maximum limit, +125°C recommended operating limit) and $T_{\text{A}}$ is the ambient temperature. (1)

$P_{\text{D(max)}}$ should then be applied to the internal power dissipated by the TPS704xx regulator. The equation for calculating total internal power dissipation of the TPS704xx is:

$$P_{\text{D(total)}} = (V_{\text{IN1}} - V_{\text{OUT1}}) \times I_{\text{OUT1}} + \left(\frac{V_{\text{IN2}} - V_{\text{OUT2}}}{2}\right) \times I_{\text{OUT2}} + V_{\text{IN2}} \times I_{OQ}$$

Since the quiescent current of the TPS704xx is very low, the second term is negligible, further simplifying the equation to:

$$P_{\text{D(total)}} = (V_{\text{IN1}} - V_{\text{OUT1}}) \times I_{\text{OUT1}} + \left(V_{\text{IN2}} - V_{\text{OUT2}}\right) \times I_{\text{OUT2}}$$

(2)

For the case where $T_{\text{A}} = +55^\circ \text{C}$, airflow = 200 ft/min, copper heat-sink area = 4 cm$^2$, the maximum power-dissipation limit can be calculated. First, from Figure 34, we find the system $R_{\text{JA}}$ is +50°C/W; therefore, the maximum power-dissipation limit is:

$$P_{\text{D(max)}} = \frac{T_{\text{J(max)}} - T_{\text{A}}}{R_{\text{JA(system)}}} = \frac{+125^\circ \text{C} - 55^\circ \text{C}}{+50^\circ \text{C/W}} = 1.4 \text{ W}$$

(4)

If the system implements a TPS704xx regulator, where $V_{\text{IN1}} = 5.0 \text{ V}, V_{\text{IN2}} = 2.8 \text{ V}, I_{\text{OUT1}} = 500 \text{ mA},$ and $I_{\text{OUT2}} = 800 \text{ mA},$ the internal power dissipation is:

$$P_{\text{D(total)}} = (V_{\text{IN1}} - V_{\text{OUT1}}) \times I_{\text{OUT1}} + \left(V_{\text{IN2}} - V_{\text{OUT2}}\right) \times I_{\text{OUT2}}$$

$$= (5.0 - 3.3) \times 0.5 + (2.8 - 1.8) \times 0.8 = 1.25 \text{ W}$$

(5)
Comparing $P_{D(total)}$ with $P_{D(max)}$ reveals that the power dissipation in this example does not exceed the calculated limit. When it does, one of two corrective actions should be made: raising the power-dissipation limit by increasing the airflow or the heat-sink area, or lowering the internal power dissipation of the regulator by reducing the input voltage or the load current. In either case, the above calculations should be repeated with the new system parameters. This parameter is measured with the recommended copper heat sink pattern on a 4-layer PWB, 2 oz. copper traces on 4-in × 4-in ground layer. Simultaneous and continuous operation of both regulator outputs at full load may exceed the power dissipation rating of the PWP package.

**Mounting Information**

The primary requirement is to complete the thermal contact between the thermal pad and the PWB metal. The thermal pad is a solderable surface and is fully intended to be soldered at the time the component is mounted. Although voiding in the thermal-pad solder-connection is not desirable, up to 50% voiding is acceptable. The data included in Figure 34 and Figure 36 are for soldered connections with voiding between 20% and 50%. The thermal analysis shows no significant difference resulting from the variation in voiding percentage.

Figure 37 shows the solder-mask land pattern for the PWP package. The minimum recommended heat-sink area is also illustrated. This is simply a copper plane under the body extent of the package, including metal routed under terminals 1, 12, 13, and 24.

![Figure 37. PWP Package Land Pattern](image-url)
Sequencing Timing Diagrams

This section provides a number of timing diagrams showing how this device functions in different configurations.

**Application condition:** \( V_{\text{IN1}} \) and \( V_{\text{IN2}} \) are tied to the same fixed input voltage greater than \( V_{\text{UVLO}} \). PG2 is tied to MR.

\( \text{EN1} \) and \( \text{EN2} \) are initially high; therefore, both regulators are off, and PG1 and PG2 (tied to MR) are at logic low. Since MR is at logic low, RESET is also at logic low. When EN1 is taken to logic low, \( V_{\text{OUT1}} \) turns on. Later, when EN2 is taken to logic low, \( V_{\text{OUT2}} \) turns on. When \( V_{\text{OUT1}} \) reaches 95% of its regulated output voltage, PG1 goes to logic high. When \( V_{\text{OUT2}} \) reaches 95% of its regulated output voltage, PG2 (tied to MR) goes to logic high. When \( V_{\text{IN1}} \) is greater than \( V_{\text{UVLO}} \) and MR (tied to PG2) is at logic high, RESET is pulled to logic high after a 120-ms delay. When \( \text{EN1} \) and \( \text{EN2} \) are returned to logic high, both devices power down and both PG1, PG2 (tied to MR2), and RESET return to logic low.

---

Figure 38. Timing When \( V_{\text{OUT1}} \) Is Enabled Before \( V_{\text{OUT2}} \)

**NOTES:**

A. \( t_1 \): Time at which \( V_{\text{IN}} \) is greater than \( V_{\text{UVLO}} \) and MR is logic high.

B. The timing diagram is not drawn to scale.
Application condition: $V_{IN1}$ and $V_{IN2}$ are tied to the same fixed input voltage greater than $V_{UVLO}$. MR is initially logic high but is eventually toggled.

$EN1$ and $EN2$ are initially high; therefore, both regulators are off, and $PG1$ and $PG2$ are at logic low. Since $V_{INi}$ is greater than $V_{UVLO}$ and $MR$ is at logic high, $RESET$ is also at logic high. When $EN2$ is taken to logic low, $V_{OUT2}$ turns on. Later, when $ENT$ is taken to logic low, $V_{OUT1}$ turns on. When $V_{OUT2}$ reaches 95% of its regulated output voltage, $PG2$ goes to logic high. When $V_{OUT1}$ reaches 95% of its regulated output voltage, $PG1$ goes to logic high. When $MR$ is taken to logic low, $RESET$ is taken low. When $MR$ returns to logic high, $RESET$ returns to logic high after a 120-ms delay.

Figure 39. Timing When $MR$ is Toggled
**Application condition:** $V_{IN1}$ and $V_{IN2}$ are tied to the same fixed input voltage greater than $V_{UVLO}$. PG1 is tied to MR.

EN1 and EN2 are initially high; therefore, both regulators are off, and PG1 (tied to MR) and PG2 are at logic low. Since MR is at logic low, RESET is also at logic low. When EN2 is taken to logic low, $V_{OUT2}$ turns on. Later, when EN1 is taken to logic low, $V_{OUT1}$ turns on. When $V_{OUT2}$ reaches 95% of its regulated output voltage, PG2 goes to logic high. When $V_{OUT1}$ reaches 95% of its regulated output voltage, PG1 goes to logic high. When $V_{IN1}$ is greater than $V_{UVLO}$ and MR (tied to PG2) is at logic high, RESET is pulled to logic high after a 120-ms delay. When a fault on $V_{OUT1}$ causes it to fall below 95% of its regulated output voltage, PG1 (tied to MR) goes to logic low. Since MR is logic low, RESET goes to logic low. $V_{OUT2}$ is unaffected.

**Figure 40. Timing When There is a Fault on $V_{OUT1}$**
APPLICATION INFORMATION

Input Capacitor

For a typical application, a ceramic input bypass capacitor (0.22 μF to 1 μF) is recommended. This capacitor should be as close to the input pins as possible. Due to the impedance of the input supply, large transient currents cause the input voltage to droop. If this droop causes the input voltage to drop below the UVLO threshold, the device turns off. Therefore, it is recommended to place a larger capacitor in parallel with the ceramic bypass capacitor at the regulator input. The size of this capacitor depends on the output current, the response time of the main power supply, and the main power supply distance to the regulator. At a minimum, the capacitor should be sized to ensure that the input voltage does not drop below the minimum UVLO threshold voltage during normal operating conditions.

Output Capacitor

As with most LDO regulators, the TPS704xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value for $V_{OUT1}$ is 22 μF and the ESR (equivalent series resistance) must be between 50 mΩ and 800 mΩ. The minimum recommended capacitance value for $V_{OUT2}$ is 47 μF and the ESR must be between 50 mΩ and 2 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Larger capacitors provide a wider range of stability and better load transient response. Table 1 gives a partial listing of surface-mount capacitors suitable for use with the TPS704xx for fast transient response applications.

This information, along with the ESR graphs, is included to assist in selection of suitable capacitance for user applications. When necessary to achieve low height requirements along with high output current and/or high load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

<table>
<thead>
<tr>
<th>VALUE</th>
<th>MANUFACTURER</th>
<th>MFR PART NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>680 μF</td>
<td>Kemet</td>
<td>T510X6871004AS</td>
</tr>
<tr>
<td>470 μF</td>
<td>Sanyo</td>
<td>4TPB470M</td>
</tr>
<tr>
<td>150 μF</td>
<td>Sanyo</td>
<td>4TPC150M</td>
</tr>
<tr>
<td>220 μF</td>
<td>Sanyo</td>
<td>2R5TPC220M</td>
</tr>
<tr>
<td>100 μF</td>
<td>Sanyo</td>
<td>2R5TPC220M</td>
</tr>
<tr>
<td>68 μF</td>
<td>Sanyo</td>
<td>10TPC68M</td>
</tr>
<tr>
<td>68 μF</td>
<td>Kemet</td>
<td>T495D6861006AS</td>
</tr>
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<td>47 μF</td>
<td>Kemet</td>
<td>T495D4761010AS</td>
</tr>
<tr>
<td>33 μF</td>
<td>Kemet</td>
<td>T495C3361016AS</td>
</tr>
<tr>
<td>22 μF</td>
<td>Kemet</td>
<td>T495C2261010AS</td>
</tr>
</tbody>
</table>
Programming the TPS70402 Adjustable LDO Regulator

The output voltage of the TPS70402 adjustable regulators is programmed using external resistor dividers as shown in Figure 41.

Resistors R1 and R2 should be chosen for approximately a 50-μA divider current. Lower value resistors can be used, but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at the sense terminal increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at approximately 50 μA, and then calculate R1 using Equation 6:

\[ R1 = \left( \frac{V_{OUT}}{V_{REF}} - 1 \right) \times R2 \]

where:

- \( V_{REF} = 1.224 \text{ V typ} \) (the internal reference voltage)

![Figure 41. TPS70402 Adjustable LDO Regulator Programming](image-url)

Output Voltage Programming Guide

<table>
<thead>
<tr>
<th>OUTPUT VOLTAGE</th>
<th>R1</th>
<th>R2</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5 V</td>
<td>31.6</td>
<td>30.1</td>
<td>kΩ</td>
</tr>
<tr>
<td>3.3 V</td>
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<td>30.1</td>
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<td>3.6 V</td>
<td>59.0</td>
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Regulator Protection

Both TPS704xx PMOS-pass transistors have built-in back diodes that conduct reverse currents when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS704xx also features internal current limiting and thermal protection. During normal operation, the TPS704xx regulator 1 limits output current to approximately 1.75 A (typ) and regulator 2 limits output current to approximately 3.8 A (typ). When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds +150°C (typ), thermal-protection circuitry shuts it down. Once the device has cooled below +130°C (typ), regulator operation resumes.
## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision E (February 2010) to Revision F

<table>
<thead>
<tr>
<th>Change Description</th>
<th>Page</th>
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<tr>
<td>Changed Tube transport media, quantity values from 70 to 60 in Ordering Information table</td>
<td>3</td>
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### Changes from Revision D (December, 2007) to Revision E

<table>
<thead>
<tr>
<th>Change Description</th>
<th>Page</th>
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<tbody>
<tr>
<td>Corrected pin description for pin 21 in pinout drawing</td>
<td>1</td>
</tr>
<tr>
<td>Updated Dissipation Ratings table values</td>
<td>4</td>
</tr>
<tr>
<td>Deleted falling edge delay specification</td>
<td>6</td>
</tr>
<tr>
<td>Updated Fixed Voltage Version block diagram</td>
<td>7</td>
</tr>
<tr>
<td>Updated Adjustable Voltage Version block diagram</td>
<td>8</td>
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## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/ Ball material (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
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<tr>
<td>TPS70402PWP</td>
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<td>PWP</td>
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<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
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<td>PT70458</td>
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</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

### REEL DIMENSIONS

- **Reel Diameter**: Dimensions of the reel
- **Reel Width**: Width of the reel

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Sprocket Holes**: Points where the tape can be fed
- **User Direction of Feed**: Direction in which the tape is fed
- **Pocket Quadrants**: Quadrants where the devices are placed

### All dimensions are nominal

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<tr>
<th>Device</th>
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<th>Pins</th>
<th>SPQ</th>
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<th>Reel Width</th>
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<th>B0</th>
<th>K0</th>
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<th>W</th>
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<td>8.0</td>
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### TAPE AND REEL BOX DIMENSIONS

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<td>43.0</td>
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</table>

*All dimensions are nominal*
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Fits within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.
THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments
LAND PATTERN DATA

PWP (R-PDSO-G24)  PowerPAD™ PLASTIC SMALL OUTLINE

Example Board Layout
Via pattern and copper pad size may vary depending on layout constraints

Example Solder Mask Defined Pad
(See Note C, D)

Example Solder Mask Opening
(See Note F)

Example Non Soldermask Defined Pad

Center Power Pad Solder Stencil Opening

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<tr>
<th>Stencil Thickness</th>
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<th>Y</th>
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<tr>
<td>0.127mm</td>
<td>4.68</td>
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<td>0.152mm</td>
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<td>0.178mm</td>
<td>4.2</td>
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Notes:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com (http://www.ti.com). Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

4207609-14/W 09/15

Texas Instruments
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MECHANICAL DATA

PWP (R-PDSO-G24)  PowerPAD™ PLASTIC SMALL OUTLINE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
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E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-153

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The exposed thermal pad dimensions for this package are shown in the following illustration.

![Exposed Thermal Pad Dimensions Diagram]

NOTE:  A. All linear dimensions are in millimeters

Exposed tie strap features may not be present.

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