TPS70751-EP
DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATOR WITH POWER-UP SEQUENCING FOR SPLIT-VOLTAGE DSP SYSTEMS

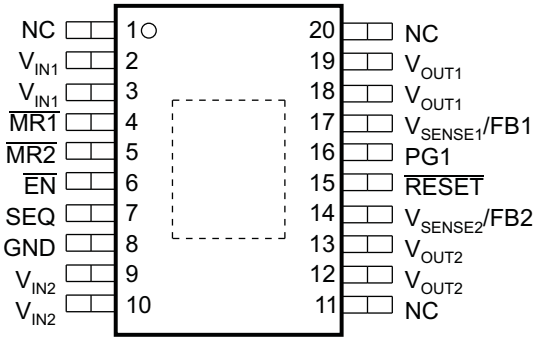
SLVS718 – DECEMBER 2006

FEATURES

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **Dual Output Voltages for Split-Supply Applications**
- **Selectable Power-Up Sequencing for DSP Applications (See Part Number TPS708xx for Independently Enabled Outputs)**
- **Output Current Range of 250 mA on Regulator 1 and 125 mA on Regulator 2**
- **Fast Transient Response**
- **3.3-V/1.8-V Fixed Voltage Outputs**
- **Open-Drain Power-On Reset With 120-ms Delay**
- **Open-Drain Power Good for Regulator 1**
- **Ultralow 190-μA (Typ) Quiescent Current**
- **1-μA Input Current During Standby**
- **Low Noise: 65 μVrms Without Bypass Capacitor**
- **Quick Output Capacitor Discharge Feature**
- **Two Manual Reset Inputs**
- **2% Accuracy Over Load and Temperature**
- **Undervoltage Lockout (UVLO) Feature**
- **20-Pin PowerPAD™ Thin Shrink Small-Outline Package (TSSOP)**
- **Thermal Shutdown Protection**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

PWP PACKAGE
(TOP VIEW)



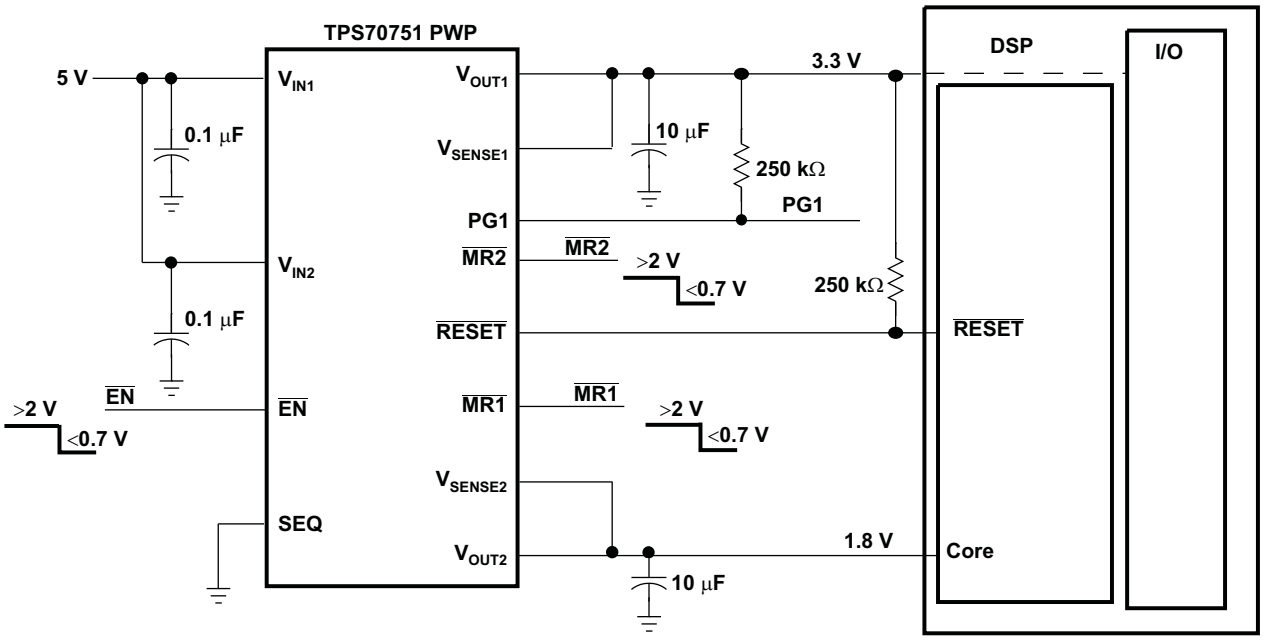
DESCRIPTION

The TPS707xx family devices are designed to provide a complete power-management solution for TI DSP, processor power, ASIC, FPGA, and digital applications where dual-output voltage regulators are required. Easy programmability of the sequencing function makes this family ideal for any TI DSP applications with power-sequencing requirements. Differentiated features, such as accuracy, fast transient response, SVS supervisory circuit (power-on reset), manual reset inputs, and enable function, provide a complete system solution.

The TPS707xx family of voltage regulators offer very low dropout (LDO) voltage and dual outputs with power-up sequence control, which is designed primarily for DSP applications. These devices have extremely low noise output performance without using any added filter bypass capacitors, and are designed to have a fast transient response and be stable with 10-μF low ESR capacitors.

The TPS70751 has a fixed voltage of 3.3 V/1.8 V. Regulator 1 can support up to 250 mA and regulator 2 can support up to 125 mA. Separate voltage inputs allow the designer to configure the source power.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 83 mV on regulator 1) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (maximum of 230 μA over the full range of output current). This LDO family also features a sleep mode; applying a high signal to $\overline{EN}$ (enable) shuts down both regulators, reducing the input current to 1 μA at T_J = 25°C.



The device is enabled when the enable ($\overline{EN}$) pin is connected to a low-level input voltage. The output voltages of the two regulators are sensed at the V_{SENSE1} and V_{SENSE2} pins, respectively.

The input signal at the sequence (SEQ) pin controls the power-up sequence of the two regulators. When the device is enabled and SEQ is pulled high or left open, V_{OUT2} turns on first and V_{OUT1} remains off until V_{OUT2} reaches approximately 83% of its regulated output voltage. At that time, V_{OUT1} is turned on. If V_{OUT2} is pulled below 83% (i.e., overload condition), V_{OUT1} is turned off. Pulling SEQ low reverses the power-up order and V_{OUT1} is turned on first. SEQ is connected to an internal pullup current source.

For each regulator, there is an internal discharge transistor to discharge the output capacitor when the regulator is turned off (disabled).

The power good (PG1) pin reports the voltage conditions at V_{OUT1}. Power good can be used to implement a SVS for the circuitry supplied by regulator 1.

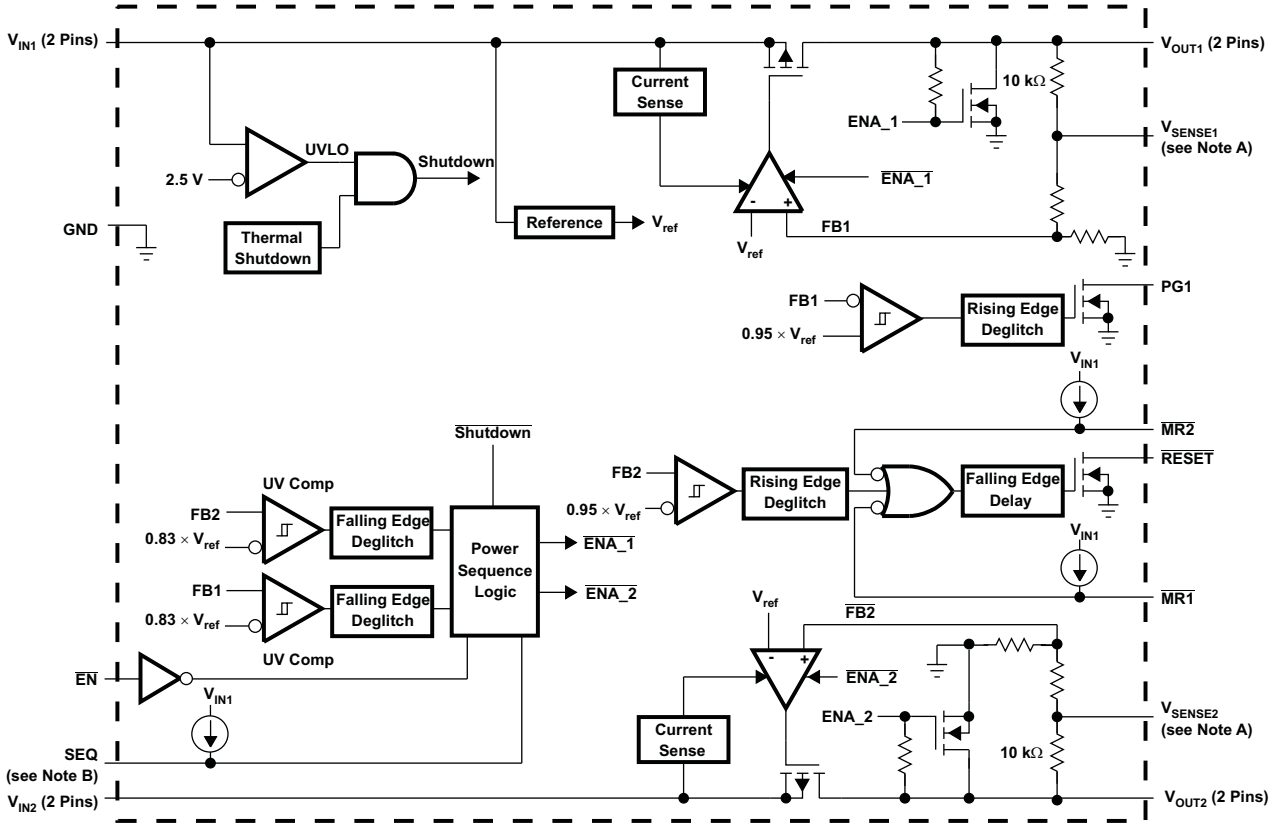
The TPS70751 features a $\overline{RESET}$ (SVS, POR, or power-on reset). The $\overline{RESET}$ output initiates a reset in DSP systems and related digital applications in the event of an undervoltage condition. $\overline{RESET}$ indicates the status of V_{OUT2} and both manual reset ($\overline{MR1}$ and $\overline{MR2}$) pins. When V_{OUT2} reaches 95% of its regulated voltage and $\overline{MR1}$ and $\overline{MR2}$ are in the logic high state, $\overline{RESET}$ goes to a high-impedance state after a 120-ms delay. $\overline{RESET}$ goes to logic low state when V_{OUT2} regulated output voltage is pulled below 95% (i.e., overload condition) of its regulated voltage. To monitor V_{OUT1}, the PG1 output can be connected to $\overline{MR1}$ or $\overline{MR2}$.

The device has an undervoltage lockout (UVLO) circuit that prevents the internal regulators from turning on until V_{IN1} reaches 2.5 V.

AVAILABLE OPTIONS

T_J	REGULATOR 1 V_O (V)	REGULATOR 2 V_O (V)	TSSOP (PWP)
–55°C to 125°C	3.3 V	1.8 V	TPS70751MPWPREP

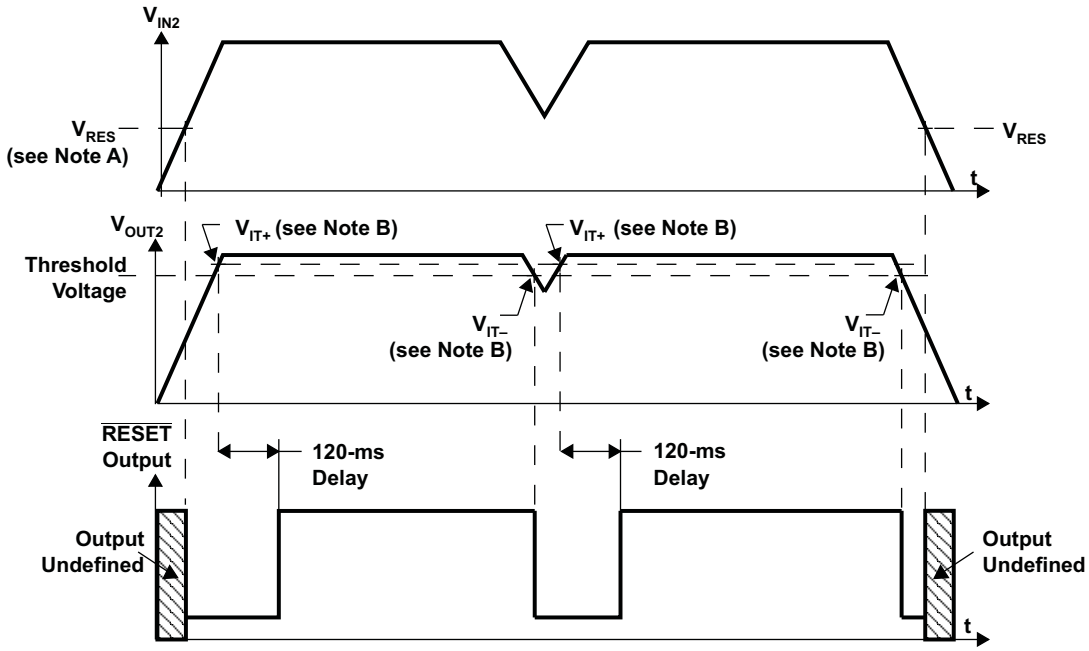
DETAILED BLOCK DIAGRAM – FIXED-VOLTAGE VERSION



NOTES: A. For most applications, V_{SENSE1} and V_{SENSE2} should be externally connected to V_{OUT} as close as possible to the device. For other implementations, refer to the SENSE terminal connection discussion in the Application Information section.

B. If the SEQ terminal is floating at the input, V_{OUT2} powers up first.

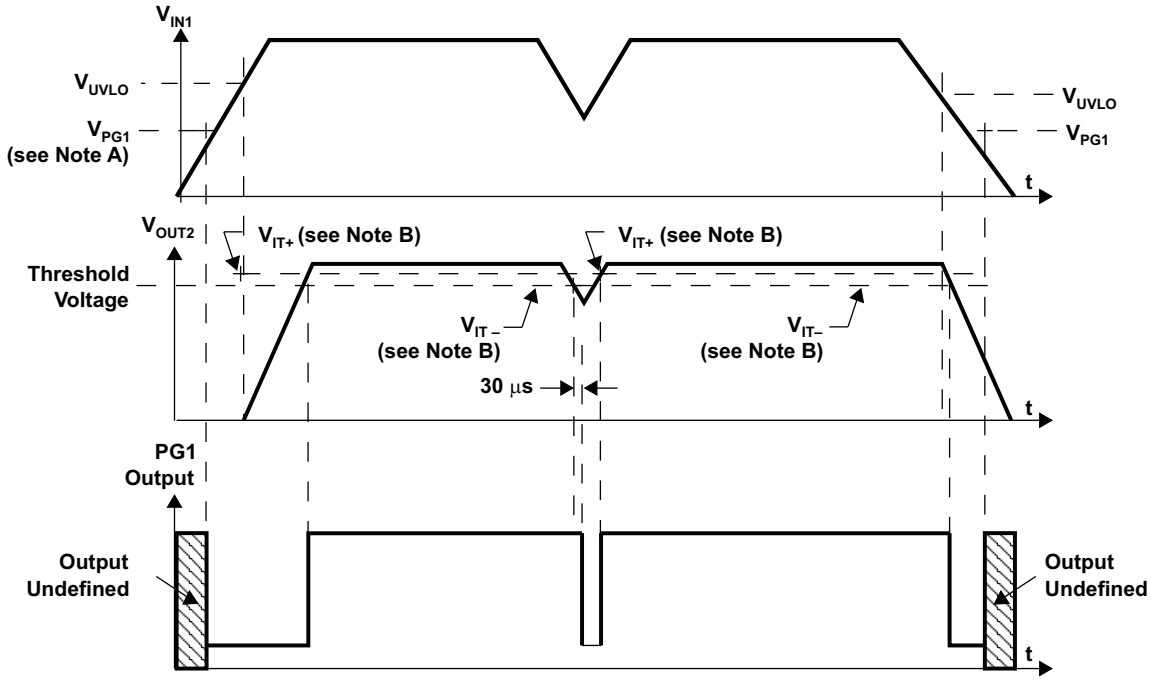
$\overline{\text{RESET}}$ TIMING DIAGRAM (WITH V_{IN1} POWERED UP AND $\overline{\text{MR1}}$ AND $\overline{\text{MR2}}$ AT LOGIC HIGH)



NOTES: A. V_{RES} is the minimum input voltage for a valid $\overline{\text{RESET}}$. The symbol V_{RES} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B. V_{IT} – Trip voltage is typically 5% lower than the output voltage (95% V_O); V_{IT-} to V_{IT+} is the hysteresis voltage.

PG1 TIMING DIAGRAM



NOTES: A. V_{PG1} is the minimum input voltage for a valid PG1. The symbol V_{PG1} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B. V_{IT} – Trip voltage is typically 5% lower than the output voltage (95% V_O); V_{IT-} to V_{IT+} is the hysteresis voltage.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$\overline{EN}$	6	I	Active-low enable
GND	8		Ground
$\overline{MR1}$	4	I	Manual reset 1. Active low, pulled up internally.
$\overline{MR2}$	5	I	Manual reset 2. Active low, pulled up internally.
NC	1, 11, 20		No connection
PG1	16	O	Power good. Open-drain output, low when V_{OUT1} voltage is less than 95% of the nominal regulated voltage.
$\overline{RESET}$	15	O	Reset. Open-drain output, SVS (power-on reset) signal, active low.
SEQ	7	I	Power up sequence control: SEQ = High, V_{OUT2} powers up first; SEQ = Low, V_{OUT1} powers up first, SEQ terminal pulled up internally.
V_{IN1}	2, 3	I	Regulator 1 input voltage
V_{IN2}	9, 10	I	Regulator 2 input voltage
V_{OUT1}	18, 19	O	Regulator 1 output voltage
V_{OUT2}	12, 13	O	Regulator 2 output voltage
V_{SENSE1}/FB1	17	I	Regulator 1 output voltage sense/feedback 1
V_{SENSE2}/FB2	14	I	Regulator 2 output voltage sense/feedback 2

DETAILED DESCRIPTION

The TPS707xx low-dropout regulator family provides dual regulated output voltages for DSP applications that require a high-performance power-management solution. These devices provide fast transient response and high accuracy with small output capacitors, while drawing low quiescent current. Programmable sequencing provides a power solution for DSPs, without any external component requirements. This reduces the component cost and board space while increasing total system reliability. The TPS707xx family has an enable feature that puts the device in sleep mode, reducing the input currents to less than 3 μA. Other features are integrated SVS (power-on reset, $\overline{RESET}$) and power good (PG1) that monitor output voltages and provide logic output to the system. These differentiated features provide a complete DSP power solution.

The TPS70751, unlike many other LDOs, features very low quiescent current that remains virtually constant even with varying loads. Conventional LDO regulators use a PNP pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS70751 uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and stable over the full load range.

Pin Functions

Enable ($\overline{EN}$)

The $\overline{EN}$ terminal is an input that enables or shuts down the device. If $\overline{EN}$ is at a voltage high signal, the device is in shutdown mode. When $\overline{EN}$ goes to voltage low, the device is enabled.

Sequence (SEQ)

The SEQ terminal is an input that programs which output voltage (V_{OUT1} or V_{OUT2}) is turned on first. When the device is enabled and the SEQ terminal is pulled high or left open, V_{OUT2} turns on first and V_{OUT1} remains off until V_{OUT2} reaches approximately 83% of its regulated output voltage. At that time, the V_{OUT1} is turned on. If V_{OUT2} is pulled below 83% (i.e., overload condition), V_{OUT1} is turned off. This terminal has a 6-μA pullup current to V_{IN1}.

Pulling SEQ low reverses the power-up order and V_{OUT1} is turned on first. For detailed timing diagrams, see Figure 33 and Figure 38.

Power Good (PG1)

The PG1 terminal is an open-drain, active-high output terminal that indicates the status of the V_{OUT1} regulator. When the V_{OUT1} reaches 95% of its regulated voltage, PG1 goes into a high-impedance state. PG1 goes into a low-impedance state when V_{OUT1} is pulled below 95% (i.e., overload condition), of its regulated voltage. The open-drain output of the PG1 terminal requires a pullup resistor.

Manual Reset ($\overline{MR1}$ and $\overline{MR2}$)

$\overline{MR1}$ and $\overline{MR2}$ are active-low input terminals used to trigger a reset condition. When either $\overline{MR1}$ or $\overline{MR2}$ is pulled to logic low, a POR ($\overline{RESET}$) occurs. These terminals have a 6-μA pullup current to V_{IN1}.

Sense (V_{SENSE1}, V_{SENSE2})

The sense terminals of fixed-output options must be connected to the regulator output, and the connection should be as short as possible. Internally, sense connects to high-impedance wide-bandwidth amplifiers through a resistor-divider network, and noise pickup feeds through to the regulator output. It is essential to route the sense connection in such a way to minimize/avoid noise pickup. Adding RC networks between the V_{SENSE} terminals and V_{OUT} terminals to filter noise is not recommended because it can cause the regulators to oscillate.

Feedback (FB1 and FB2)

FB1 and FB2 are input terminals used for adjustable-output devices and must be connected to the external feedback resistor divider. FB1 and FB2 connections should be as short as possible. It is essential to route them in such a way as to minimize/avoid noise pickup. Adding RC networks between the FB terminals and V_{OUT} terminals to filter noise is not recommended because it can cause the regulators to oscillate.

$\overline{RESET}$ Indicator

The TPS70751 features a $\overline{RESET}$ (SVS, POR, or power-on reset). $\overline{RESET}$ can be used to drive power-on reset circuitry or a low-battery indicator. $\overline{RESET}$ is an active-low, open-drain output that indicates the status of the V_{OUT2} regulator and both manual reset ($\overline{MR1}$ and $\overline{MR2}$) pins. When V_{OUT2} exceeds 95% of its regulated voltage, and $\overline{MR1}$ and $\overline{MR2}$ are in the high-impedance state, $\overline{RESET}$ goes to a high-impedance state after a 120-ms delay. $\overline{RESET}$ goes to a low-impedance state when V_{OUT2} is pulled below 95% (i.e., overload condition) of its regulated voltage. To monitor V_{OUT1}, the PG1 output can be connected to $\overline{MR1}$ or $\overline{MR2}$. The open-drain output of $\overline{RESET}$ requires a pullup resistor. If $\overline{RESET}$ is not used, it can be left floating.

Input Voltage (V_{IN1} and V_{IN2})

V_{IN1} and V_{IN2} are inputs to the regulators. Internal bias voltages are powered by V_{IN1}.

Output Voltage (V_{OUT1} and V_{OUT2})

V_{OUT1} and V_{OUT2} are output terminals.

Absolute Maximum Ratings(1)

over operating junction temperature (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN1}	Input voltage range(2)		–0.3	7	V
V_{IN2}			–0.3	7	
	Voltage range at $\overline{EN}$		–0.3	7	V
V_{OUT1}, V_{SENSE1}	Output voltage			5.5	V
V_{OUT2}, V_{SENSE2}				5.5	
	Maximum $\overline{RESET}$ and PG1 voltage			7	V
	Maximum $\overline{MR1}$, $\overline{MR2}$, and SEQ voltage			V_{IN1}	V
	Peak output current			Internally Limited	
	Continuous total power dissipation			See Dissipation Rating Tables	
T_J	Operating virtual junction temperature range		–55	150	°C
T_{stg}	Storage temperature range		–65	150	°C
	ESD rating	Human-Body Model (HBM)		2	kV

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are tied to network ground.

Dissipation Ratings

PACKAGE	AIR FLOW (CFM)	$T_A \leq 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP(1)	0	3.067 W	30.67 mW/°C	1.687 W	1.227 W
	250	4.115 W	41.15 mW/°C	2.265 W	4.646 W

(1) This parameter is measured with the recommended copper heatsink pattern on a four-layer PCB, 1-oz copper on 4-in × 4-in ground layer. For more information, refer to TI technical brief SLMA002.

Recommended Operating Conditions

			MIN	MAX	UNIT
V_I	Input voltage(1)		2.7	6	V
I_O	Output current	Regulator 1	0	250	mA
		Regulator 2	0	125	
T_J	Operating virtual junction temperature		–55	125	°C

(1) To calculate the minimum input voltage for maximum output current, use $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$.

Electrical Characteristics

over recommended operating junction temperature (T_J = –55°C to 125°C), V_{IN1} or V_{IN2} = $V_{O(nom)}$ + 1 V, I_O = 1 mA, $\overline{EN}$ = 0, C_O = 33 µF (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage(1)(2)	Reference voltage	2.7 V < V_I < 6 V, FB connected to V_O, T_J = 25°C		1.22		V
		1.8-V output	2.8 V < V_I < 6 V, T_J = 25°C		1.8		
			2.8 V < V_I < 6 V	1.764		1.836	
		3.3-V output	4.3 V < V_I < 6 V, T_J = 25°C		3.3		
			4.3 V < V_I < 6 V	3.234		3.366	
Quiescent current (GND current) for regulator 1 and regulator 2, $\overline{EN}$ = 0 V(1)(2)			T_J = 25°C		190		µA
						230	
Output voltage line regulation ($\Delta V_O/V_O$) for regulator 1 and regulator 2(3)(2)			V_O + 1 V < V_I ≤ 6 V, T_J = 25°C		0.01%		V
			V_O + 1 V < V_I ≤ 6 V			0.1%	
Load regulation for V_{OUT1} and V_{OUT2}(1)			T_J = 25°C		1		mV
V_n	Output noise voltage	Regulator 1	BW = 300 Hz to 50 kHz, C_O = 33 µF, T_J = 25°C		65		µVrms
		Regulator 2			65		
Output current limit		Regulator 1	V_O = 0 V		1.6	2.1	A
		Regulator 2			0.750	1.1	
Thermal shutdown junction temperature					150		°C
$I_{I(standby)}$	Standby current	Regulator 1 and Regulator 2	$\overline{EN}$ = V_I, T_J = 25°C			2	µA
			$\overline{EN}$ = V_I			6	
PSRR	Power-supply ripple rejection		f = 1 kHz, C_O = 33 µF, T_J = 25°C		60		dB

(1) I_O = 1 mA to 250 mA for regulator 1 and 1 mA to 125 mA for regulator 2

(2) Minimum input operating voltage is 2.7 V or VO(typ) + 1 V, whichever is greater. Maximum input voltage = 6 V, minimum output current 1 mA.

(3) If V_O < 1.8 V, then $V_{I(max)}$ = 6 V, $V_{I(min)}$ = 2.7 V:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O(V_{I(max)} - 2.7\ V)}{100} \times 1000$$

If V_O > 2.5 V, then $V_{I(max)}$ = 6 V, $V_{I(min)}$ = Vo + 1 V:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O[V_{I(max)} - (V_O + 1)]}{100} \times 1000$$

Electrical Characteristics (continued)

over recommended operating junction temperature (T_J = –55°C to 125°C), V_{IN1} or V_{IN2} = $V_{O(nom)}$ + 1 V, I_O = 1 mA, $\overline{EN}$ = 0, C_O = 33 µF (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{RESET}$					
Minimum input voltage for valid $\overline{RESET}$	$I_{(RESET)}$ = 300 µA, $V_{(RESET)} \le$ 0.8 V		1	1.3	V
Trip threshold voltage	V_O decreasing	92%	95%	98%	V_O
Hysteresis voltage	Measured at V_O		0.5%		V_O
$t_{(RESET)}$	$\overline{RESET}$ pulse duration	80	120	160	ms
$t_{r(RESET)}$	Rising-edge deglitch		30		µs
Output low voltage	V_I = 3.5 V, $I_{(RESET)}$ = 1 mA		0.15	0.4	V
Leakage current	$V_{(RESET)}$ = 6 V			1	µA
PG1					
Minimum input voltage for valid PG1	$I_{O(PG1)}$ = 300 µA, $V_{(PG1)} \le$ 0.8 V		1	1.3	V
Trip threshold voltage	V_O decreasing	92%	95%	98%	V_O
Hysteresis voltage	Measured at V_O		0.5%		V_O
$t_{f(PG1)}$	Falling-edge deglitch		30		µs
Output low voltage	V_I = 2.7 V, $I_{(PG1)}$ = 1 mA		0.15	0.4	V
Leakage current	$V_{(PG1)}$ = 6 V			1	µA
$\overline{EN}$					
High-level $\overline{EN}$ input voltage		2			V
Low-level $\overline{EN}$ input voltage				0.7	V
Input current ($\overline{EN}$)		–1		1	µA
SEQ					
High-level SEQ input voltage		2			V
Low-level SEQ input voltage				0.7	V
SEQ pullup current source			6		µA
MR1/MR2					
High-level MR1/MR2 input voltage		2			V
Low-level MR1/MR2 input voltage				0.7	V
MR1/MR2 pullup current source			6		µA
V_{OUT2}					
V_{OUT2} UV comparator – positive-going input threshold voltage of V_{OUT1} UV comparator		80% V_O	83% V_O	86% V_O	V
V_{OUT2} UV comparator – falling-edge deglitch	V_{SENSE2} decreasing below threshold		140		µs
Peak output current	2-ms pulse width		375		mA
Discharge transistor current	V_{OUT2} = 1.5 V		7.5		mA
V_{OUT1}					
V_{OUT1} UV comparator – positive-going input threshold voltage of V_{OUT1} UV comparator		80% V_O	83% V_O	86% V_O	V
V_{OUT1} UV comparator – hysteresis			0.5% V_O		mV
V_{OUT1} UV comparator – falling-edge deglitch	V_{SENSE1} decreasing below threshold		140		µs
Dropout voltage(4)	I_O = 250 mA, V_{IN1} = 3.2 V, T_J = 25°C		83		mV
	I_O = 250 mA, V_{IN1} = 3.2 V			140	
Peak output current	2-ms pulse width		750		mA
Discharge transistor current	V_{OUT1} = 1.5 V		7.5		mA
UVLO threshold		2.4		2.65	V

(4) Input voltage (V_{IN1} or V_{IN2}) = $V_{O(typ)}$ – 100 mV. For 1.8-V regulators, the dropout voltage is limited by the input voltage range. The 3.3-V regulator input voltage is to 3.2 V to perform this test.

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Output voltage	vs Output current	1, 2
	vs Junction temperature	3–6
Ground current	vs Junction temperature	7
Power-supply rejection ratio	vs Frequency	8–11
Output spectral noise density	vs Frequency	12–15
Output impedance	vs Frequency	16–19
Dropout voltage	vs Junction temperature	20, 21
Load transient response		22, 23
Line transient response		24, 25
Output voltage	vs Time (start-up)	26, 27
Equivalent series resistance (ESR)	vs Output current	29–32

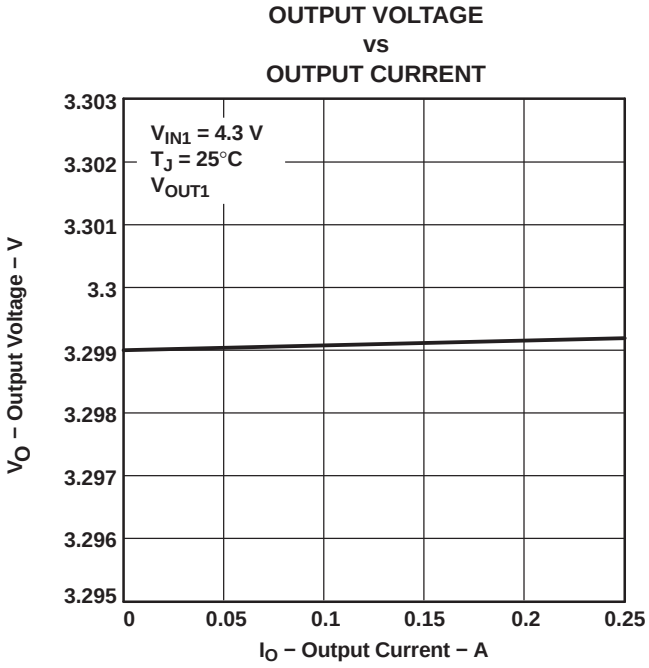


Figure 1.

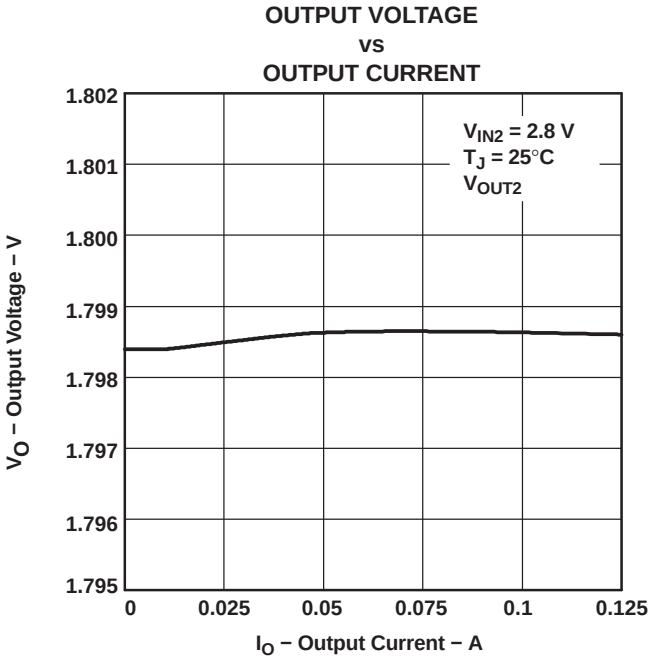


Figure 2.

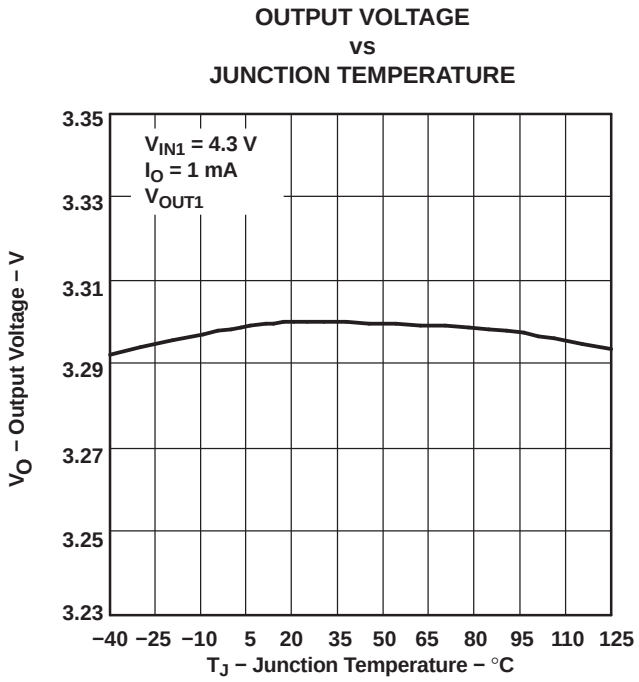


Figure 3.

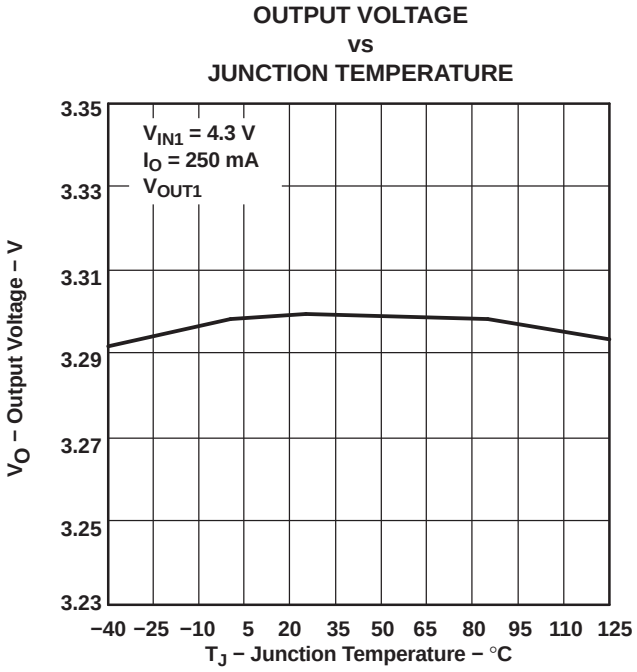


Figure 4.

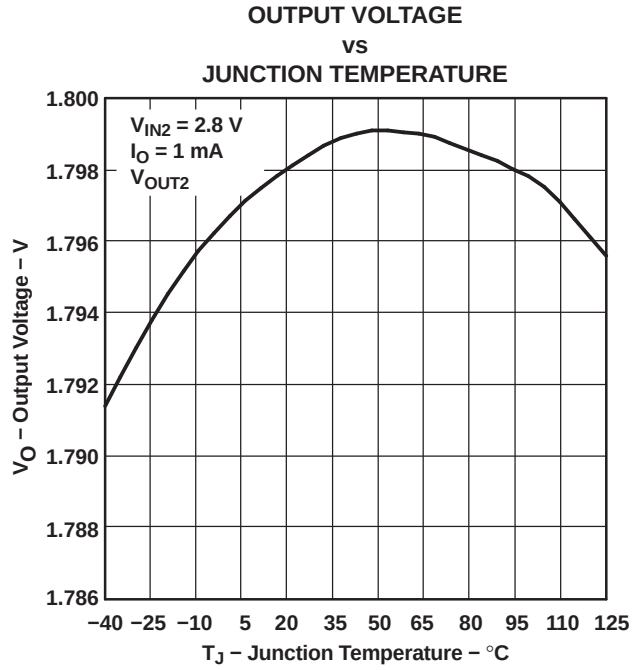


Figure 5.

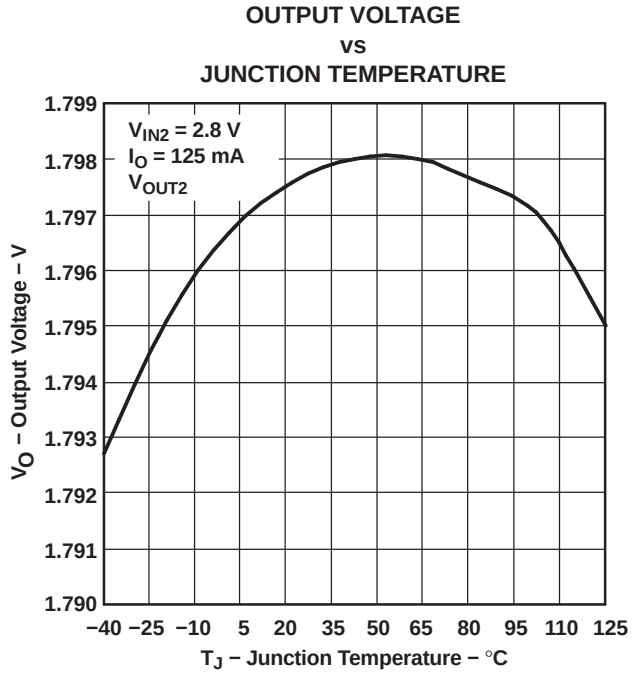


Figure 6.

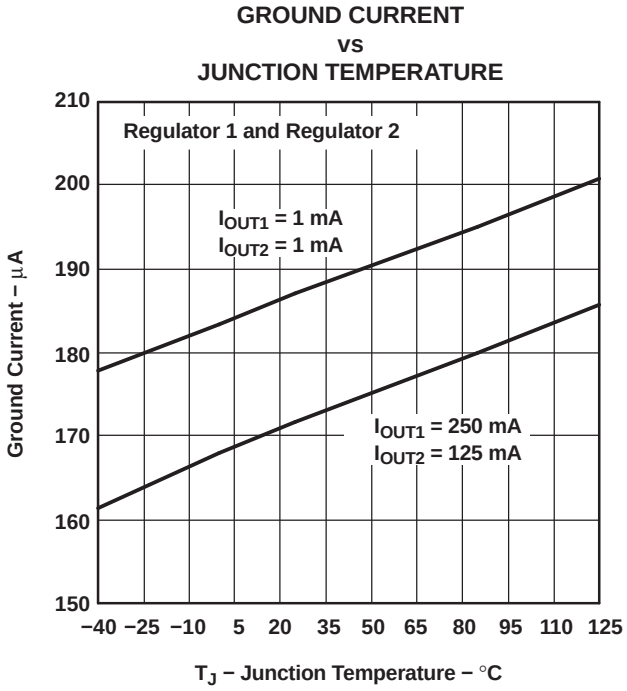


Figure 7.

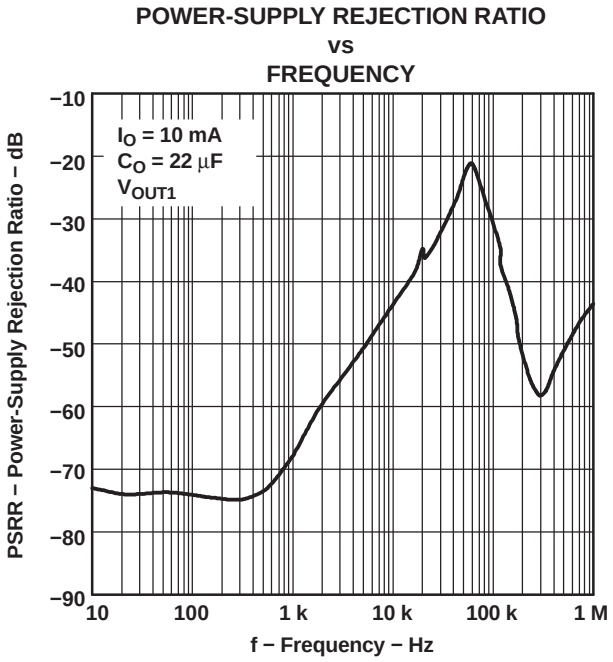


Figure 8.

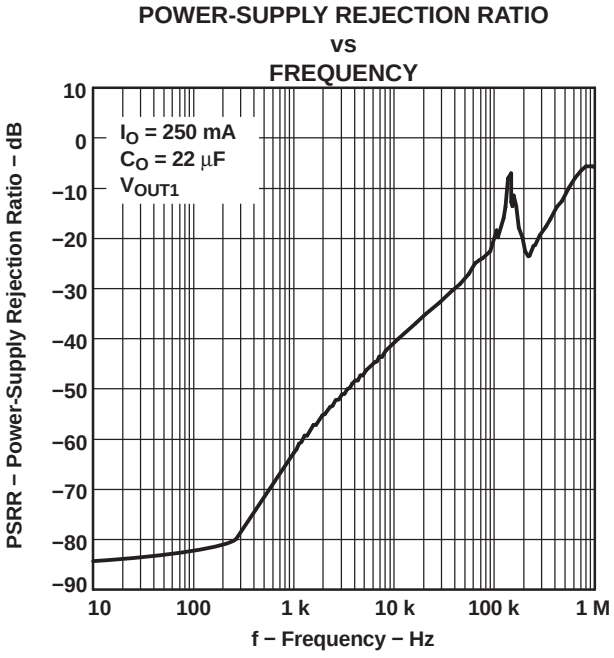


Figure 9.

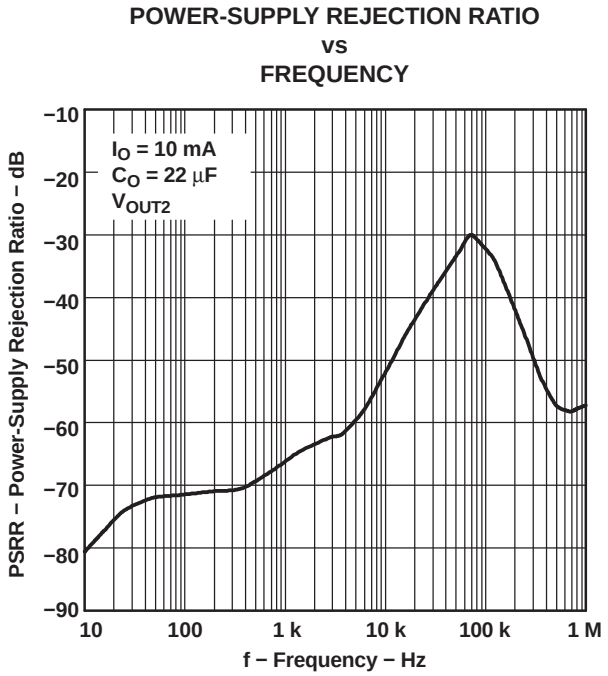


Figure 10.

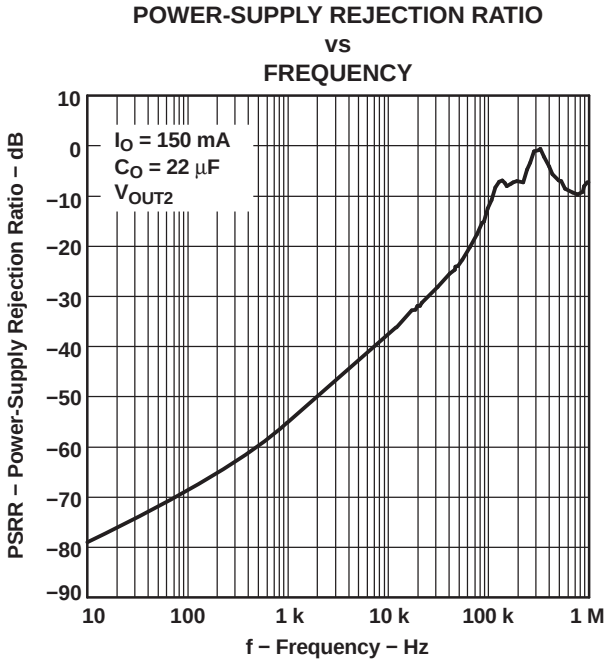


Figure 11.

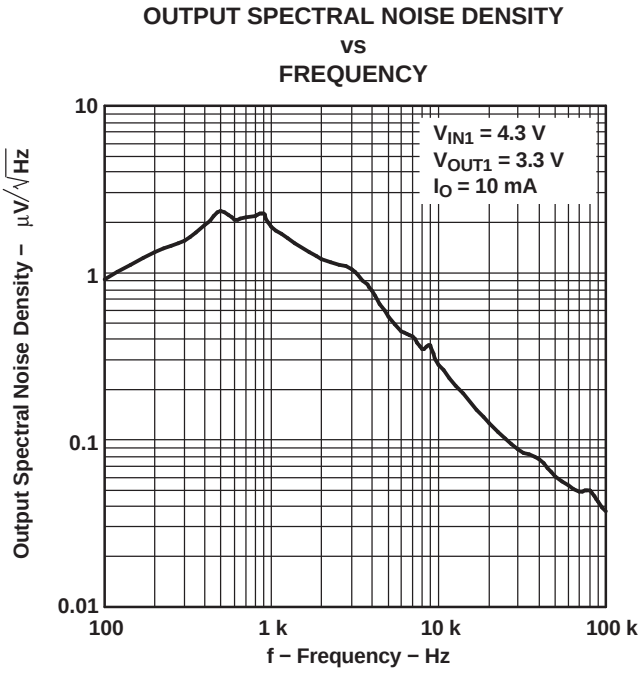


Figure 12.

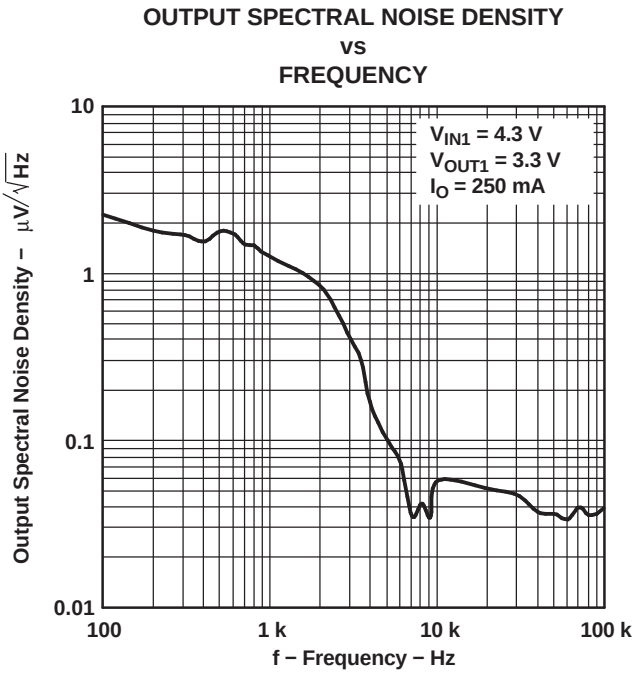


Figure 13.

OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

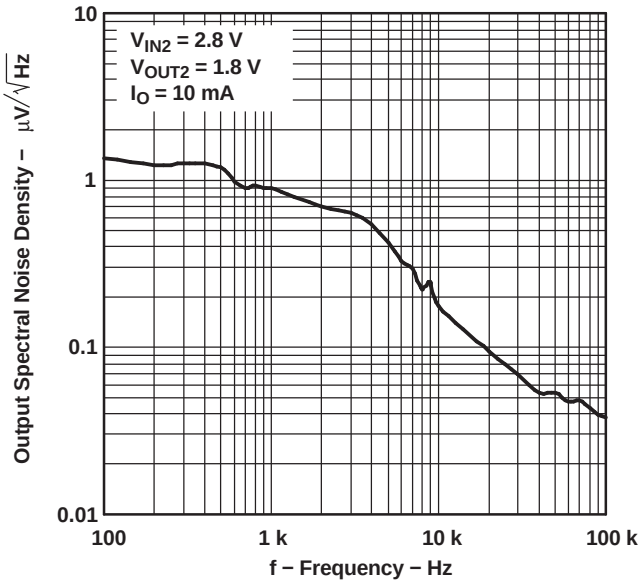


Figure 14.

OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

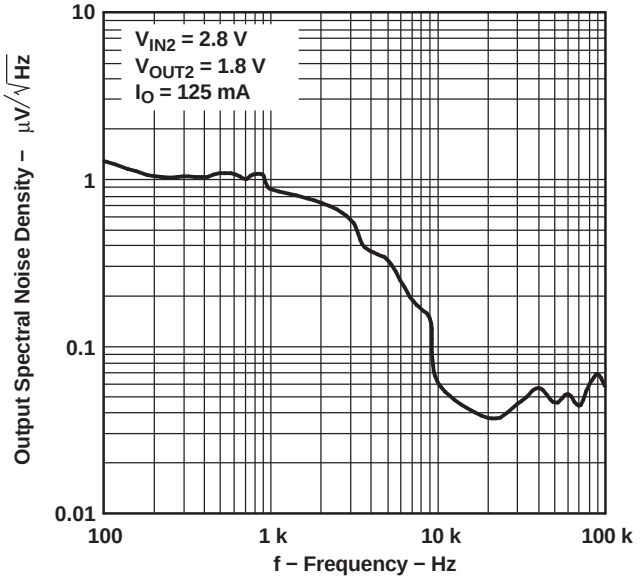


Figure 15.

OUTPUT IMPEDANCE
vs
FREQUENCY

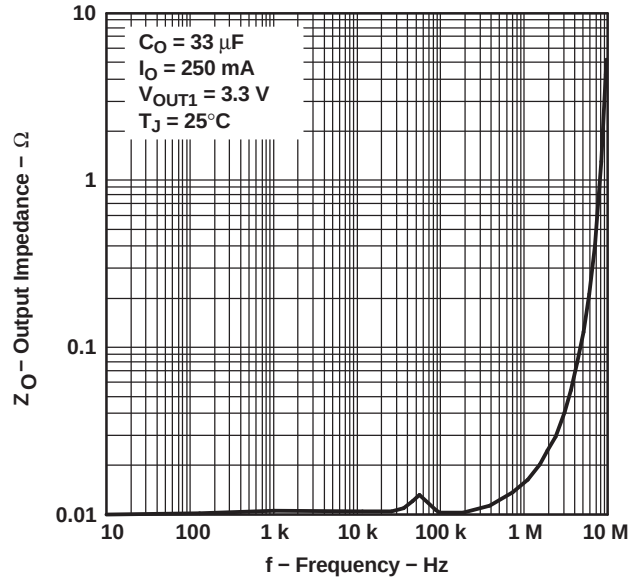


Figure 16.

OUTPUT IMPEDANCE
vs
FREQUENCY

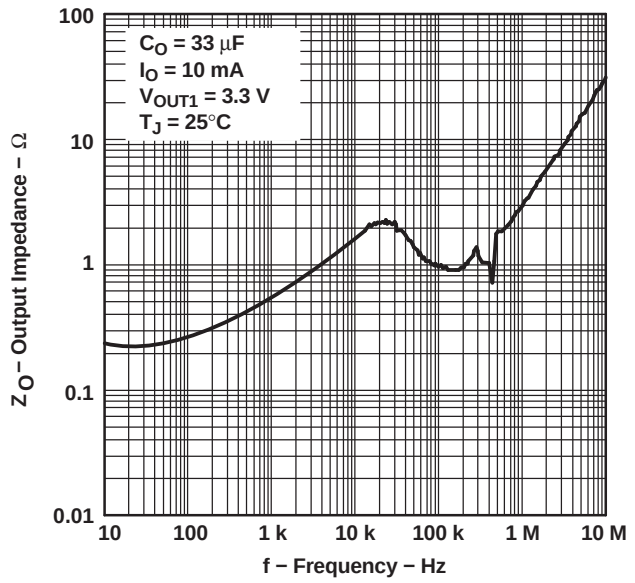


Figure 17.

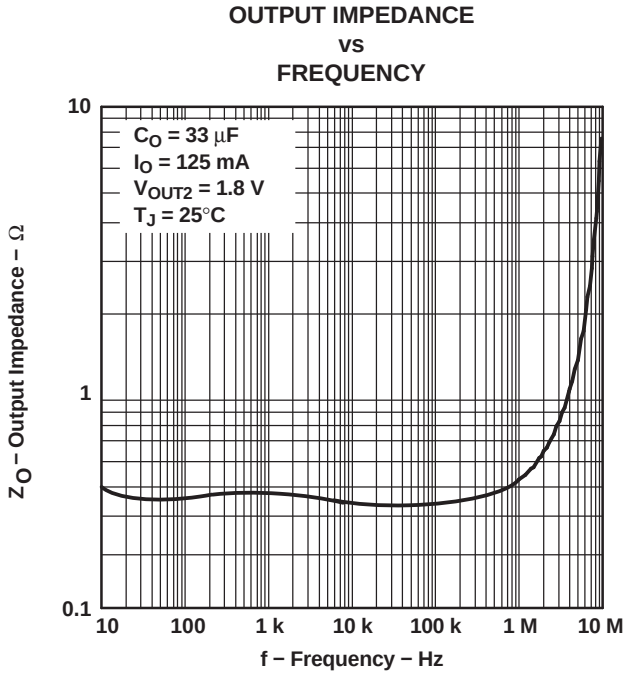


Figure 18.

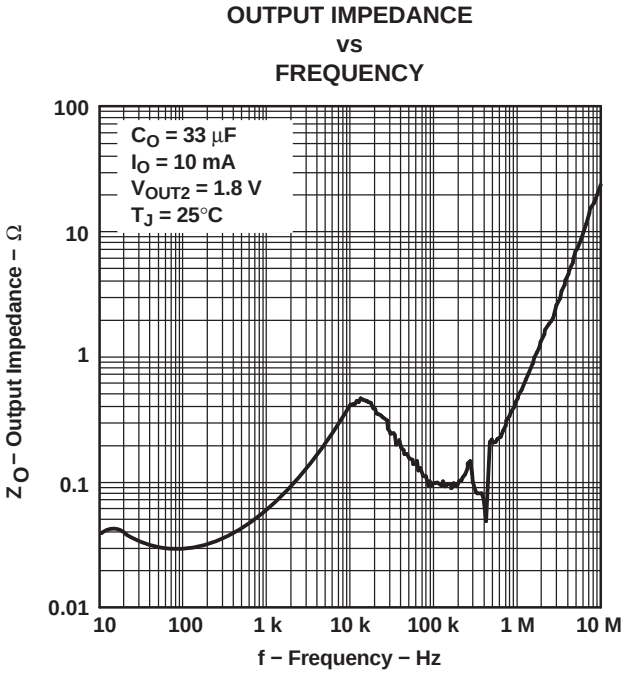


Figure 19.

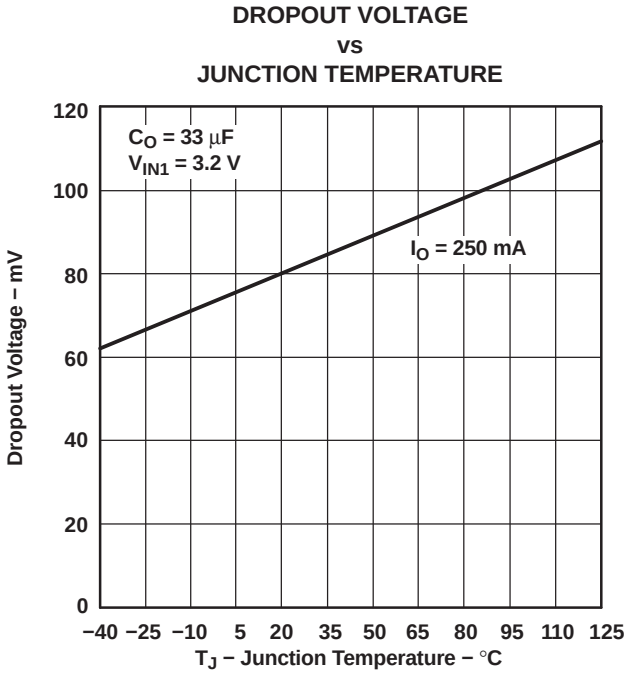


Figure 20.

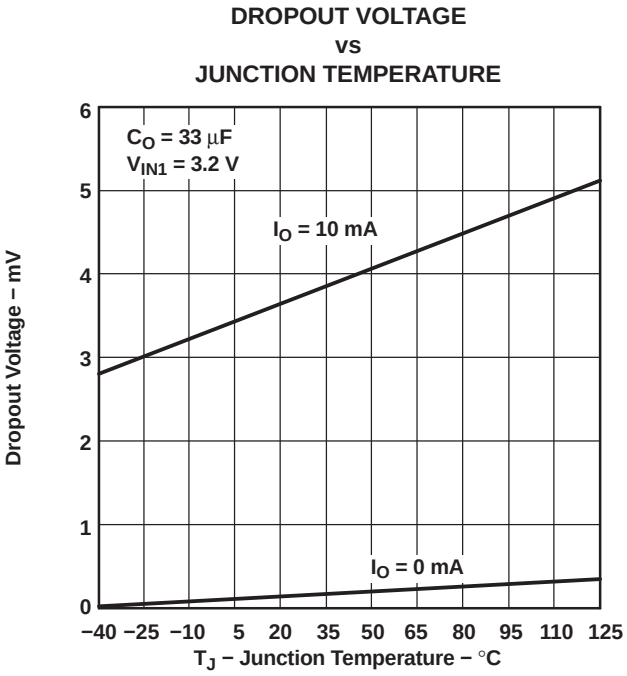


Figure 21.

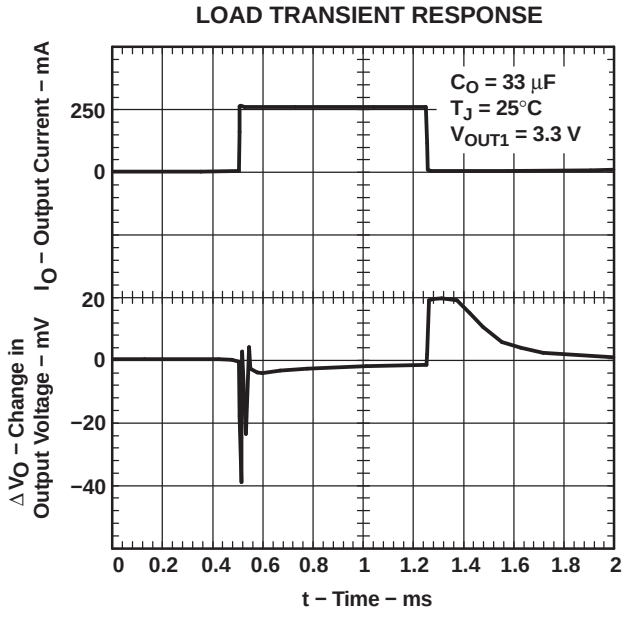


Figure 22.

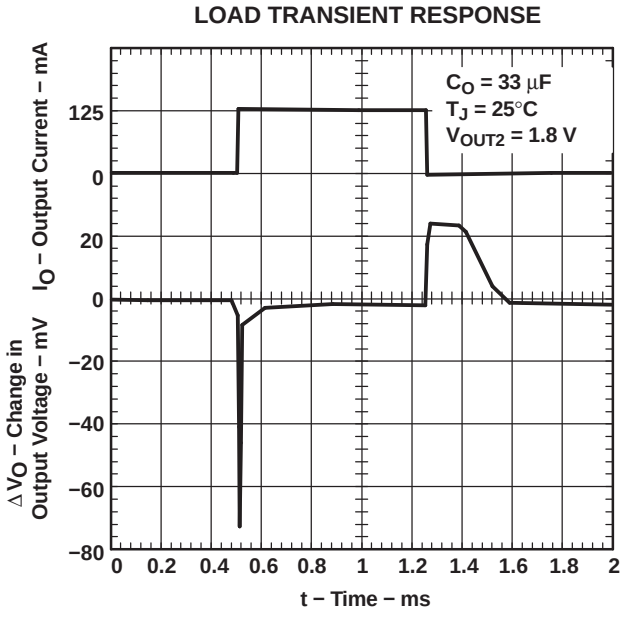


Figure 23.

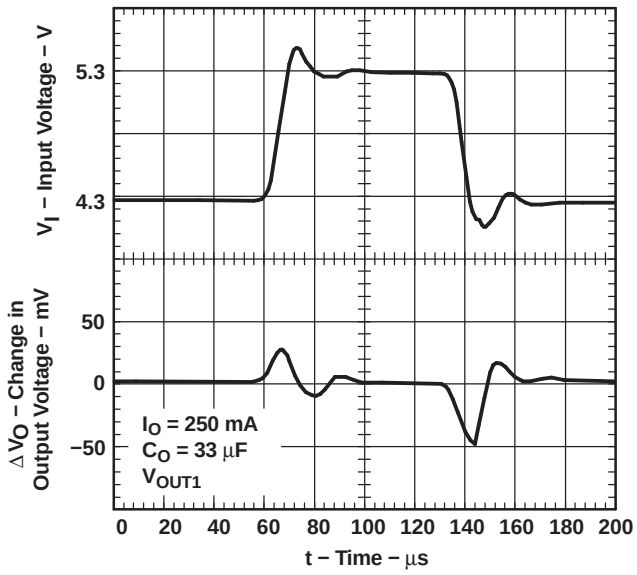


Figure 24.

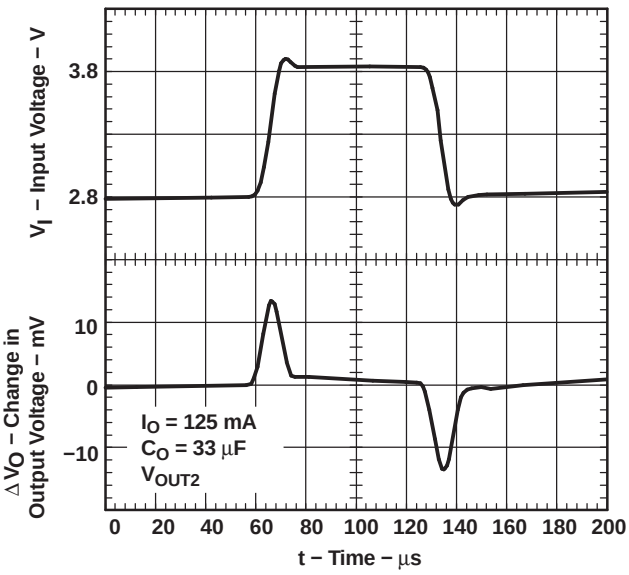


Figure 25.

OUTPUT VOLTAGE
vs
TIME (START-UP)

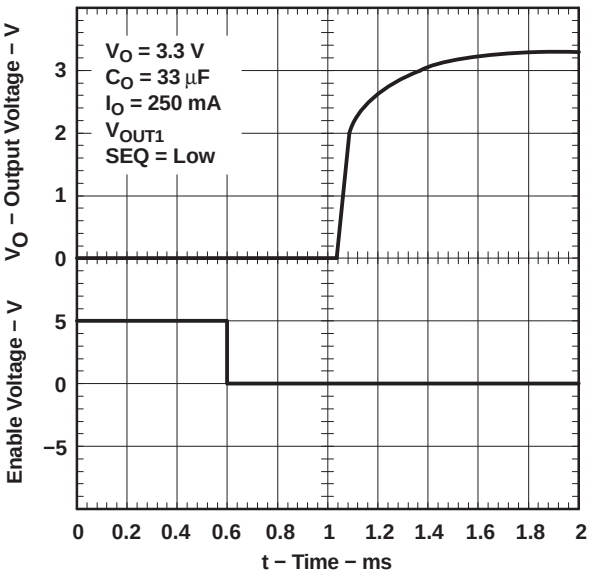


Figure 26.

OUTPUT VOLTAGE
vs
TIME (START-UP)

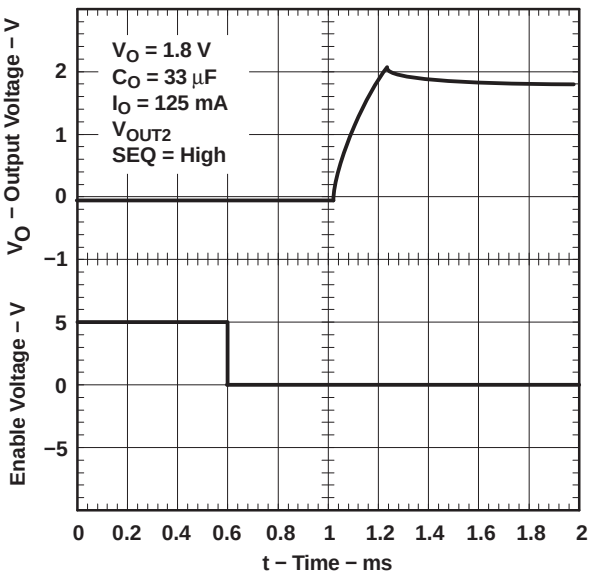


Figure 27.

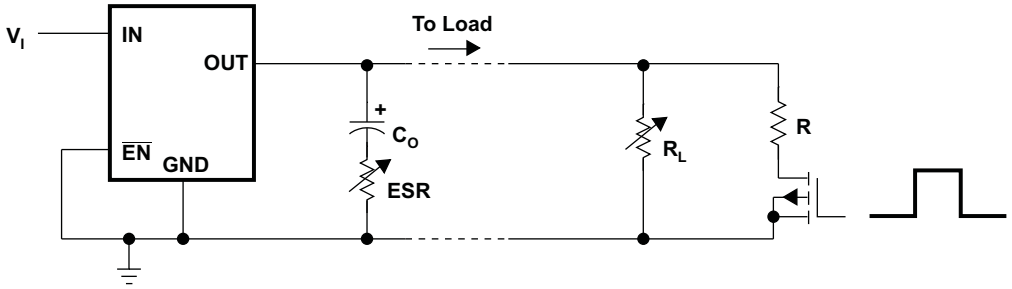


Figure 28. Test Circuit for Typical Regions of Stability

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT

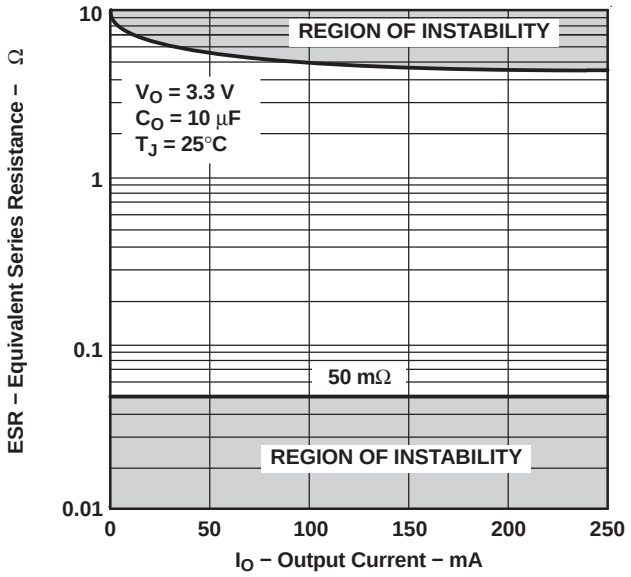


Figure 29.

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT

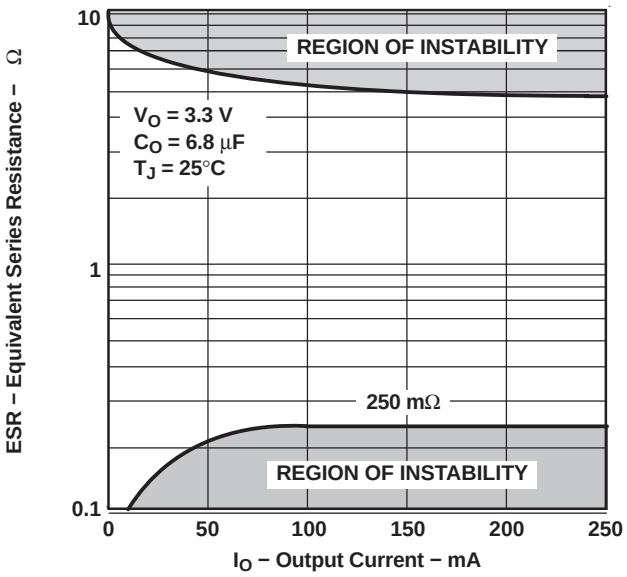
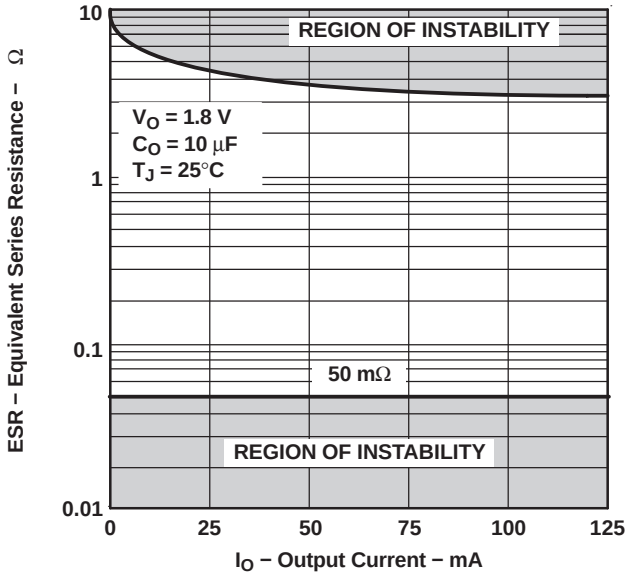


Figure 30.

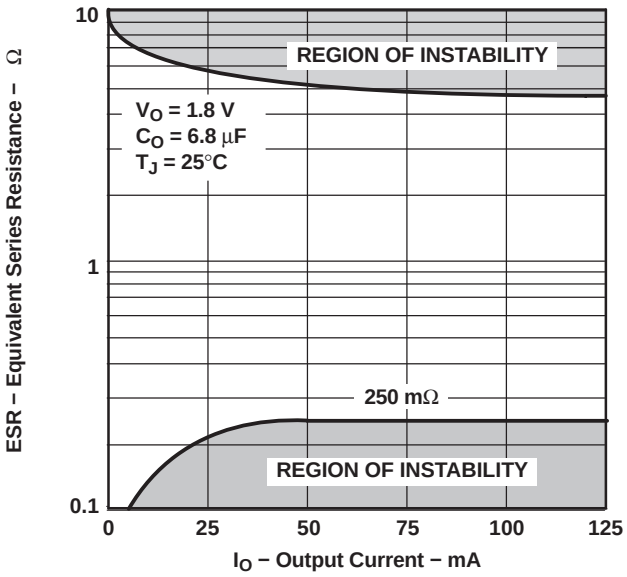
TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE(1)
vs
OUTPUT CURRENT



(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

Figure 31.

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE(1)
vs
OUTPUT CURRENT



(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

Figure 32.

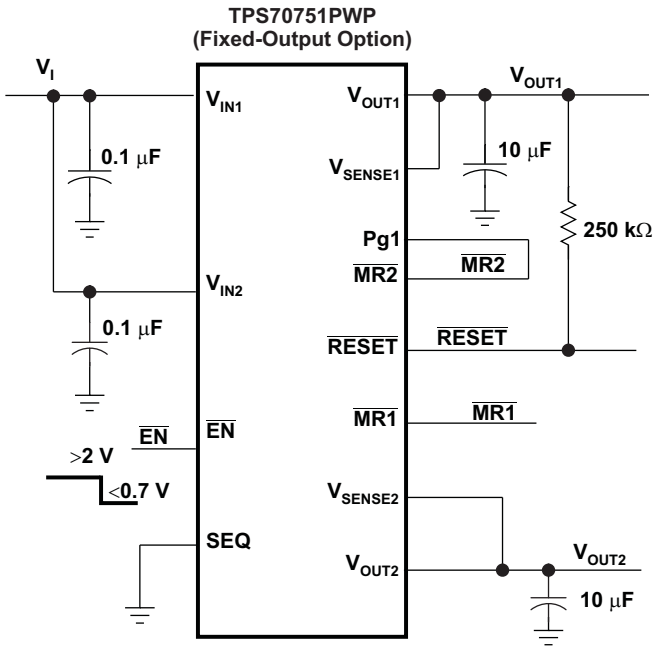
APPLICATION INFORMATION

Sequencing Timing Diagrams

The following figures provide timing diagrams showing how this device functions in different configurations.

Application Conditions Not Shown in Block Diagram

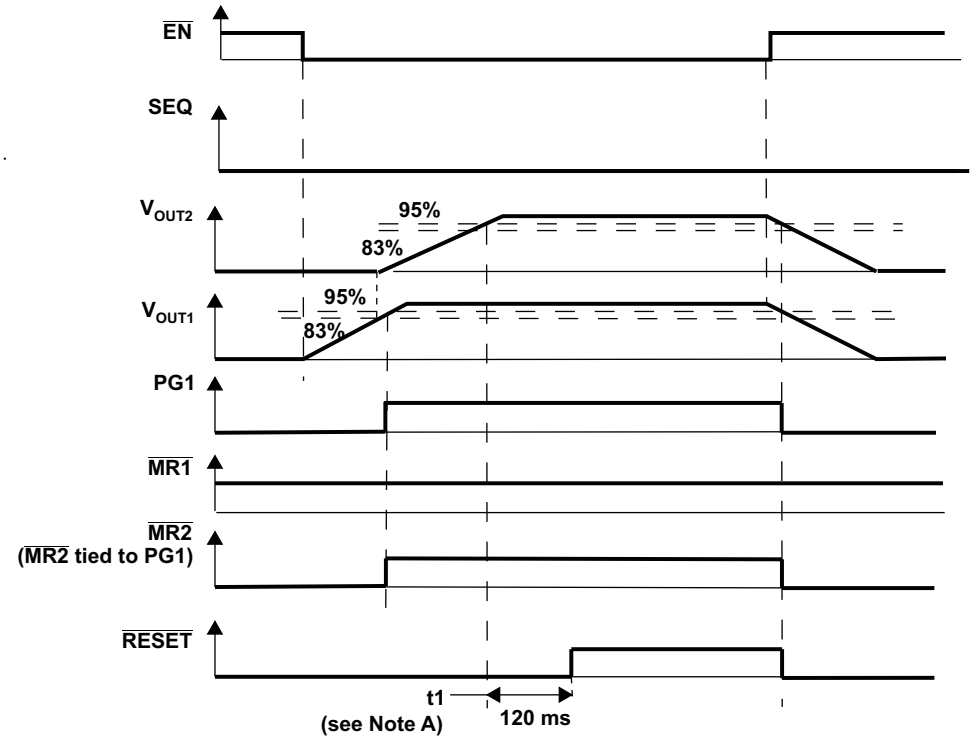
V_{IN1} and V_{IN2} are tied to the same fixed-input voltage greater than the V_{UVLO}, SEQ is tied to logic low, PG1 is tied to $\overline{MR2}$, and $\overline{MR1}$ is left unconnected and is, therefore, at logic high.



Explanation of Timing Diagram

$\overline{EN}$ is initially high; therefore, both regulators are off and PG1 and $\overline{RESET}$ are at logic low. With SEQ at logic low, when $\overline{EN}$ is taken to logic low, V_{OUT1} turns on. V_{OUT2} turns on after V_{OUT1} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both $\overline{MR1}$ and $\overline{MR2}$ (tied to PG1) are at logic high, $\overline{RESET}$ is pulled to logic high after a 120-ms delay. When $\overline{EN}$ is returned to logic high, both devices power down and both PG1 (tied to $\overline{MR2}$) and $\overline{RESET}$ return to logic low.

APPLICATION INFORMATION (continued)



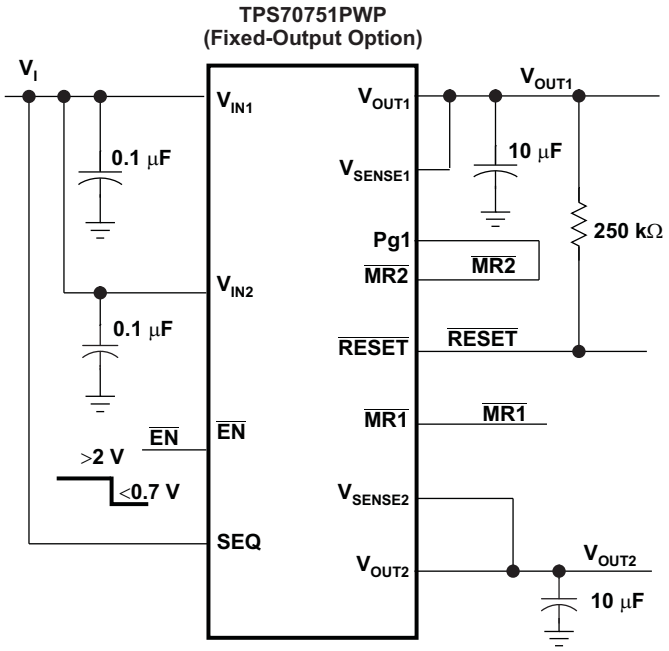
NOTE : A. t1 – Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

Figure 33. Timing When SEQ = Low

APPLICATION INFORMATION (continued)

Application Conditions Not Shown in Block Diagram

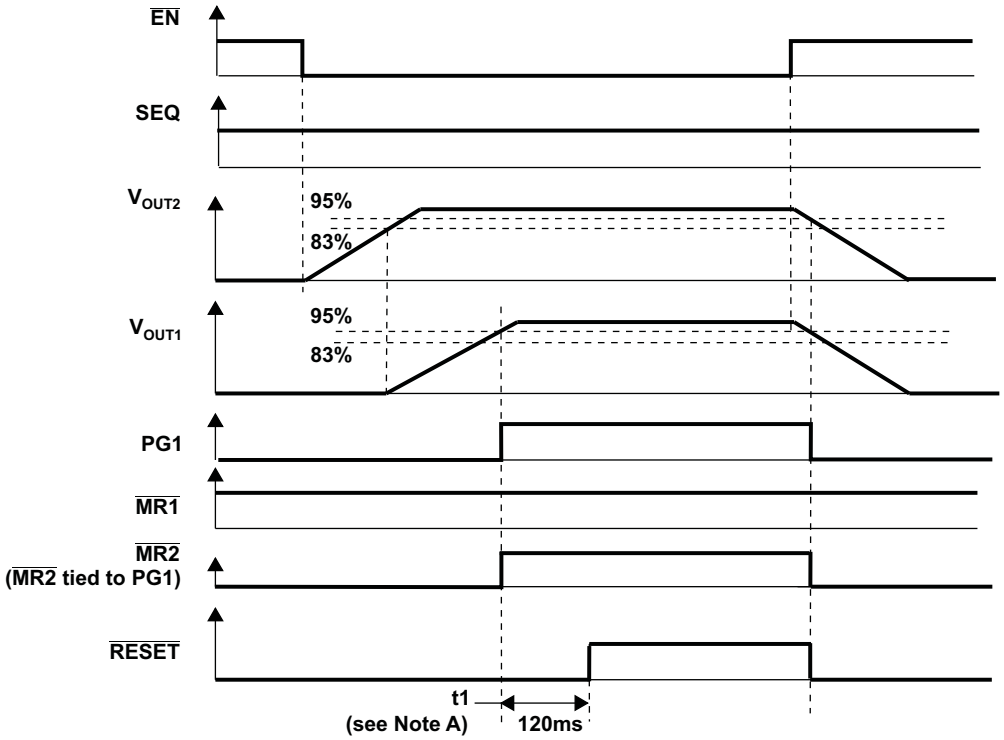
V_{IN1} and V_{IN2} are tied to the same fixed-input voltage greater than the V_{UVLO}, SEQ is tied to logic high, PG1 is tied to $\overline{MR2}$, and $\overline{MR1}$ is left unconnected and is, therefore, at logic high.



Explanation of Timing Diagram

$\overline{EN}$ is initially high; therefore, both regulators are off and PG1 and $\overline{RESET}$ are at logic low. With SEQ at logic high, when $\overline{EN}$ is taken to logic low, V_{OUT2} turns on. V_{OUT1} turns on after V_{OUT2} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both $\overline{MR1}$ and $\overline{MR2}$ (tied to PG1) are at logic high, $\overline{RESET}$ is pulled to logic high after a 120-ms delay. When $\overline{EN}$ is returned to logic high, both devices turn off and both PG1 (tied to $\overline{MR2}$) and $\overline{RESET}$ return to logic low.

APPLICATION INFORMATION (continued)



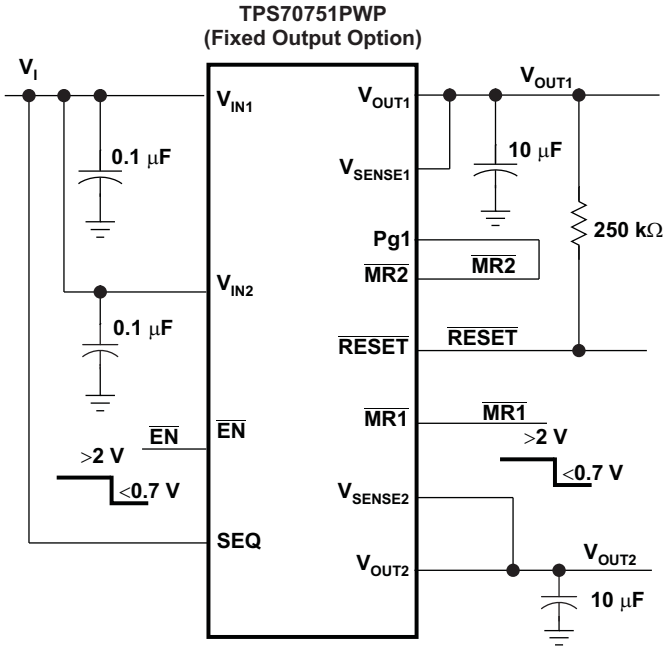
NOTE : A. t1 – Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

Figure 34. Timing When SEQ = High

APPLICATION INFORMATION (continued)

Application Conditions Not Shown in Block Diagram

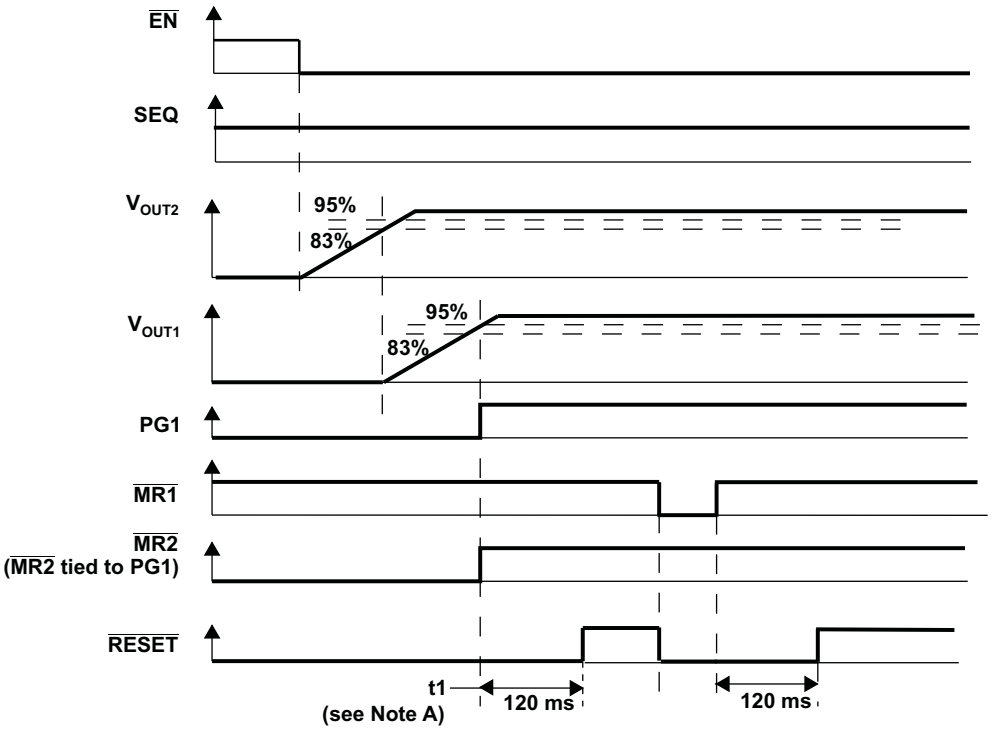
V_{IN1} and V_{IN2} are tied to the same fixed-input voltage greater than the V_{UVLO}, SEQ is tied to logic high, PG1 is tied to $\overline{MR2}$, and $\overline{MR1}$ is initially at logic high but is eventually toggled.



Explanation of Timing Diagram

$\overline{EN}$ is initially high; therefore, both regulators are off and PG1 and $\overline{RESET}$ are at logic low. With SEQ at logic high, when $\overline{EN}$ is taken low, V_{OUT2} turns on. V_{OUT1} turns on after V_{OUT2} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both $\overline{MR1}$ and $\overline{MR2}$ (tied to PG1) are at logic high, $\overline{RESET}$ is pulled to logic high after a 120-ms delay. When $\overline{MR1}$ is taken low, $\overline{RESET}$ returns to logic low but the outputs remain in regulation. When $\overline{MR1}$ is returned to logic high, since both V_{OUT1} and V_{OUT2} remain above 95% of their respective regulated output voltages and $\overline{MR2}$ (tied to PG1) remains at logic high, $\overline{RESET}$ is pulled to logic high after a 120-ms delay.

APPLICATION INFORMATION (continued)



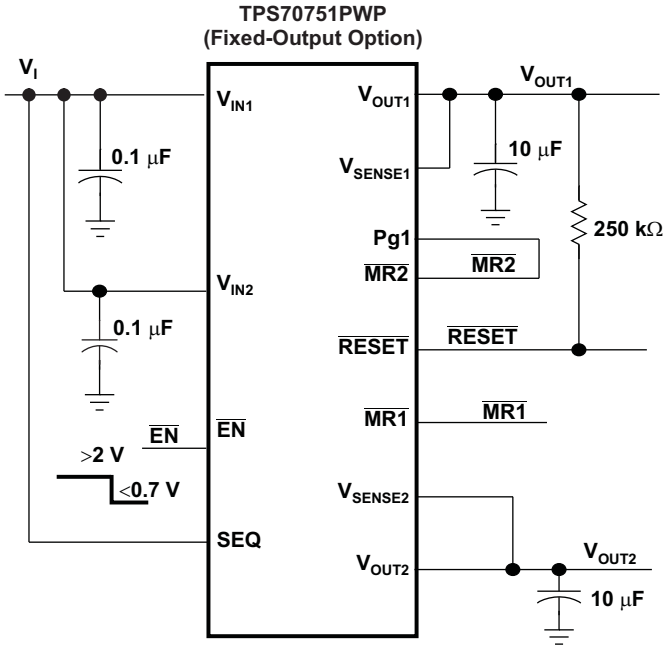
NOTE : A. t1 – Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

Figure 35. Timing When $\overline{MR1}$ Is Toggled

APPLICATION INFORMATION (continued)

Application Conditions Not Shown in Block Diagram

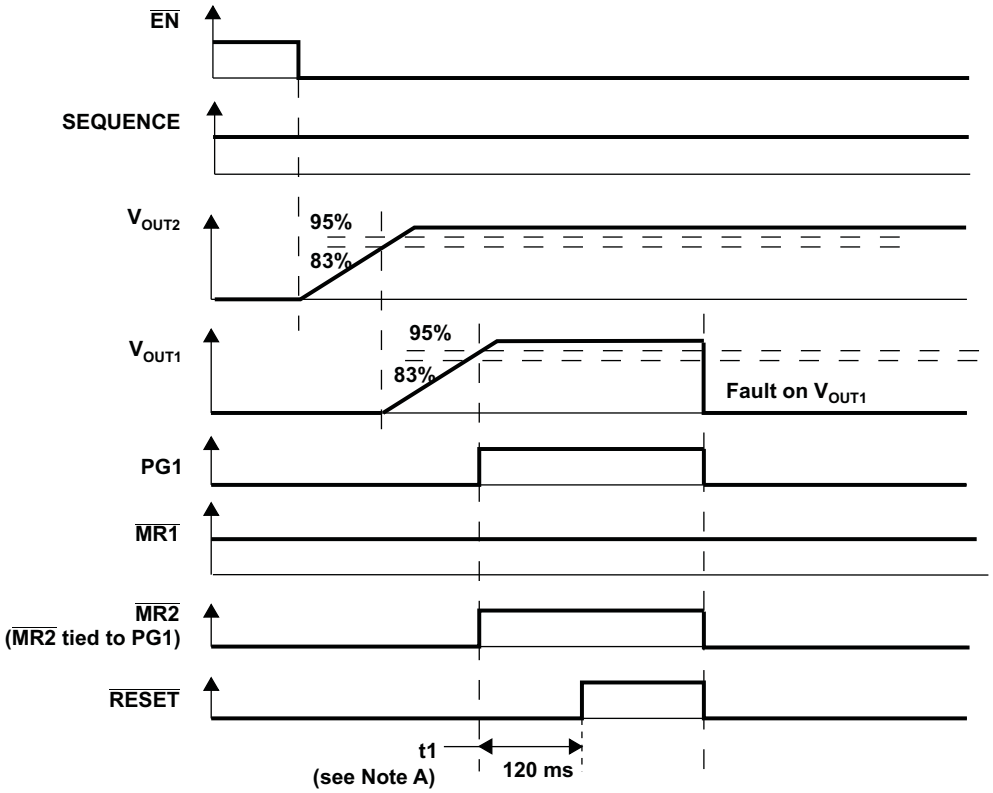
V_{IN1} and V_{IN2} are tied to the same fixed-input voltage greater than the V_{UVLO}, SEQ is tied to logic high, PG1 is tied to $\overline{MR2}$, and $\overline{MR1}$ is left unconnected and is, therefore, at logic high.



Explanation of Timing Diagram

$\overline{EN}$ is initially high; therefore, both regulators are off and PG1 and $\overline{RESET}$ are at logic low. With SEQ at logic high, when $\overline{EN}$ is taken low, V_{OUT2} turns on. V_{OUT1} turns on after V_{OUT2} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both $\overline{MR1}$ and $\overline{MR2}$ (tied to PG1) are at logic high, $\overline{RESET}$ is pulled to logic high after a 120-ms delay. When a fault on V_{OUT1} causes it to fall below 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) goes to logic low, causing $\overline{RESET}$ to return to logic low. V_{OUT2} remains on because SEQ is high.

APPLICATION INFORMATION (continued)



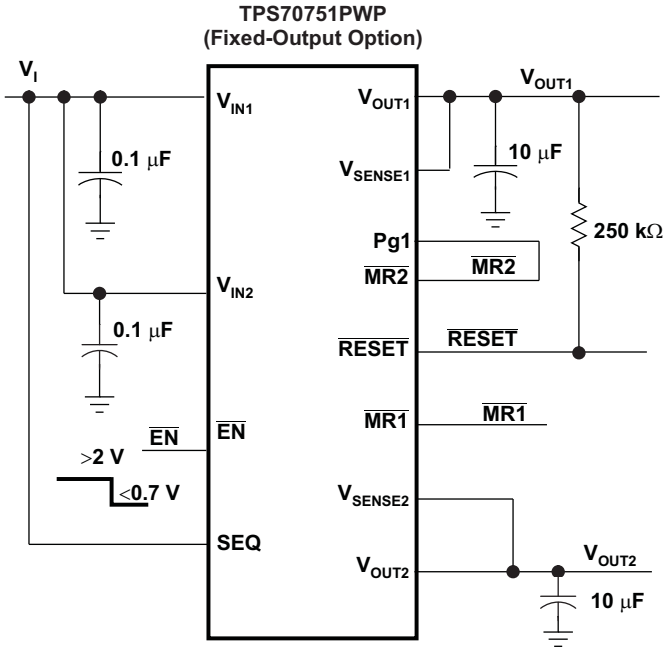
NOTE : A. t1 – Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and MR1 is logic high.

Figure 36. Timing When V_{OUT1} Faults Out

APPLICATION INFORMATION (continued)

Application Conditions Not Shown in Block Diagram

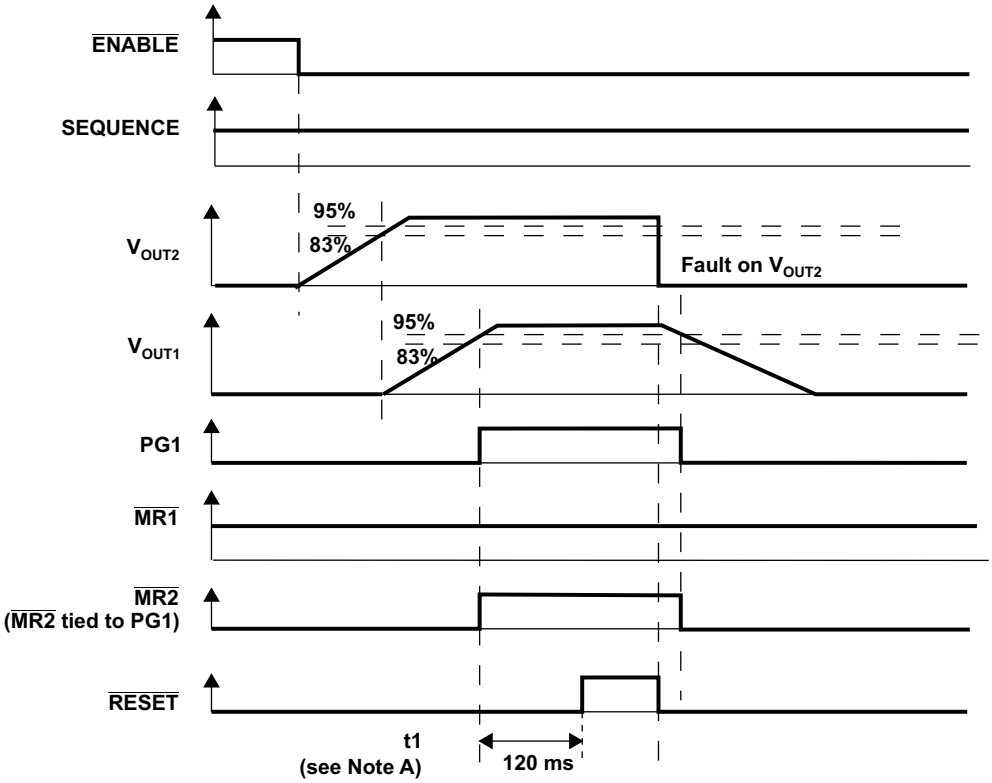
V_{IN1} and V_{IN2} are tied to the same fixed-input voltage greater than the V_{UVLO}, SEQ is tied to logic high, PG1 is tied to $\overline{MR2}$, and $\overline{MR1}$ is left unconnected and is, therefore, at logic high.



Explanation of Timing Diagram

$\overline{EN}$ is initially high; therefore, both regulators are off and PG1 and $\overline{RESET}$ are at logic low. With SEQ at logic high, when $\overline{EN}$ is taken low, V_{OUT2} turns on. V_{OUT1} turns on after V_{OUT2} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both $\overline{MR1}$ and $\overline{MR2}$ (tied to PG1) are at logic high, $\overline{RESET}$ is pulled to logic high after a 120-ms delay. When a fault on V_{OUT2} causes it to fall below 95% of its regulated output voltage, $\overline{RESET}$ returns to logic low and V_{OUT1} begins to power down because SEQ is high. When V_{OUT1} falls below 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) returns to logic low.

APPLICATION INFORMATION (continued)



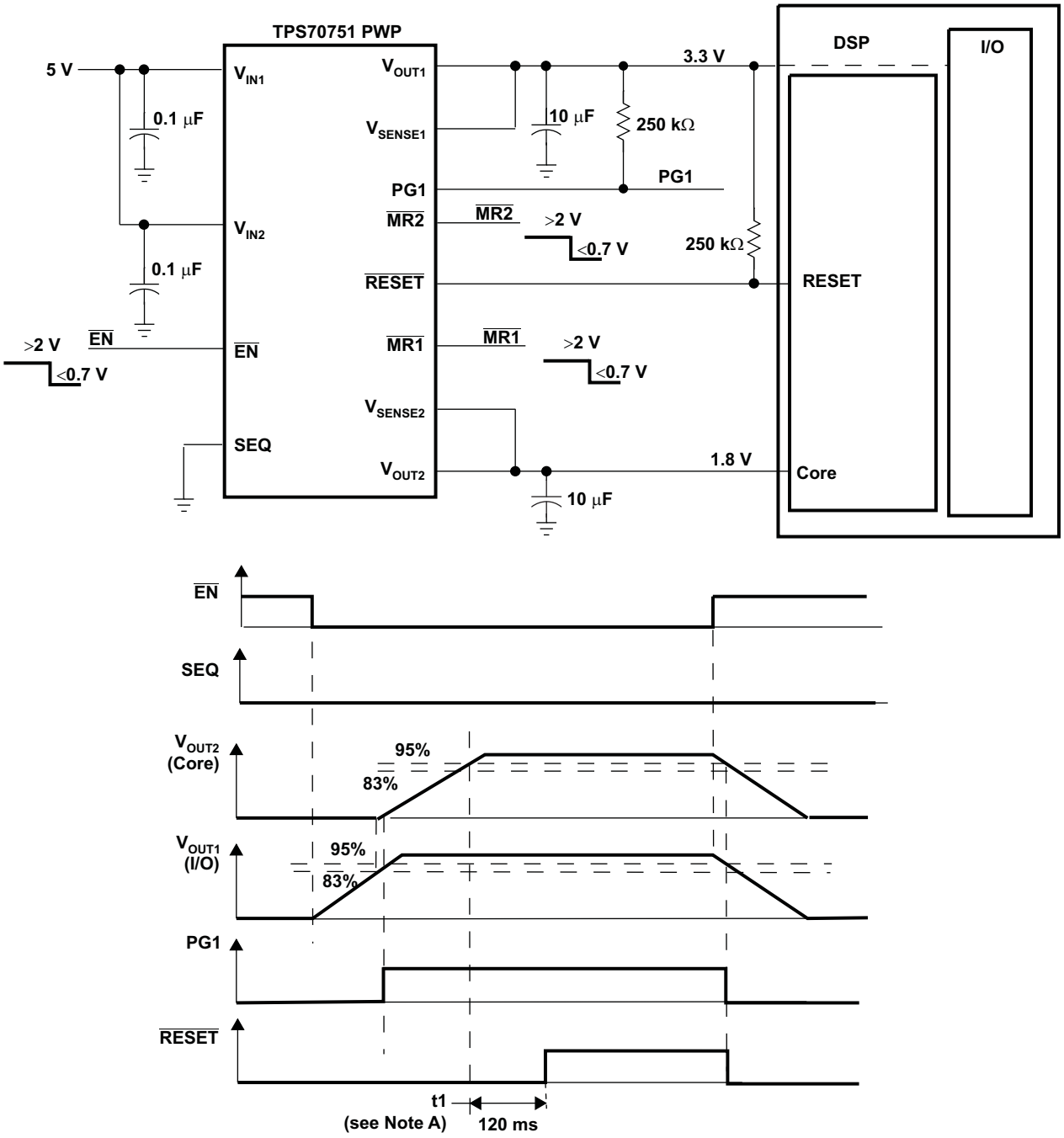
NOTE : A. t1 – Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

Figure 37. Timing When V_{OUT2} Faults Out

APPLICATION INFORMATION (continued)

Split Voltage DSP Application

Figure 38 shows a typical application where the TPS70751 is powering up a DSP. In this application, by grounding the SEQ pin, V_{OUT1}(I/O) is powered up first, and then V_{OUT2}(core) is powered up.

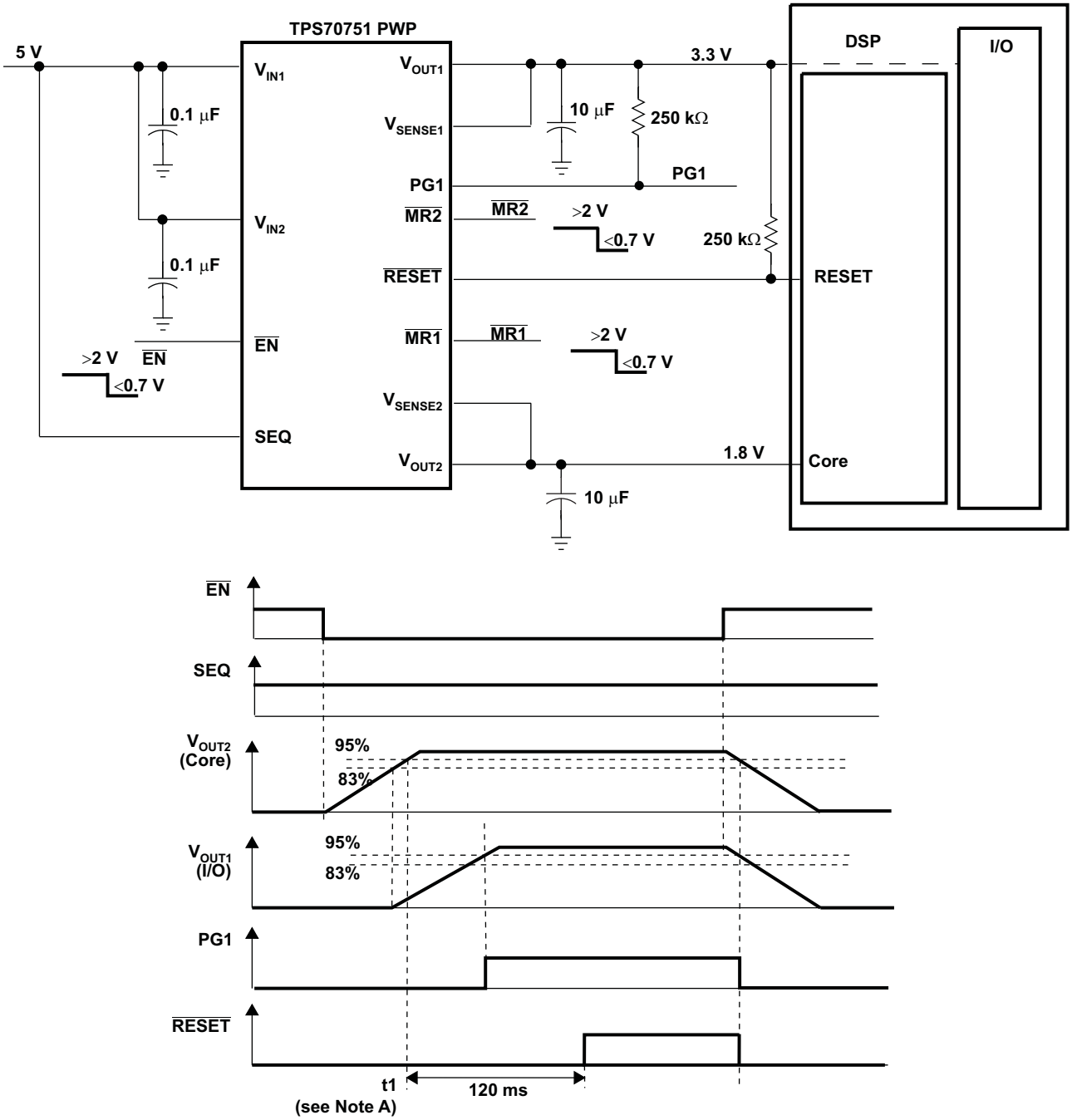


NOTE : A. t1 – Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

Figure 38. Application Timing Diagram (SEQ = Low)

APPLICATION INFORMATION (continued)

Figure 39 shows a typical application where the TPS70751 is powering up a DSP. In this application, by pulling up the SEQ pin, V_{OUT2}(core) is powered up first, and then V_{OUT1}(I/O) is powered up.



NOTE : A. t1 – Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

Figure 39. Application Timing Diagram (SEQ = High)

APPLICATION INFORMATION (continued)

Input Capacitor

For a typical application, an input bypass capacitor (0.1 µF through 1 µF) is recommended. This capacitor filters any high-frequency noise generated in the line. For fast transient condition where droop at the input of the LDO may occur due to high inrush current, it is recommended to place a larger capacitor at the input as well. The size of this capacitor is dependant on the output current and response time of the main power supply, as well as the distance to the V_I pins of the LDO.

Output Capacitor

As with most LDO regulators, the TPS70751 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance values are 10-µF ceramic capacitors with an equivalent series resistance (ESR) between 50 mΩ and 2.5 Ω, or 6.8-µF tantalum capacitors with ESR between 250 mΩ and 4 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors with capacitance values greater than 10 µF are all suitable, provided they meet the requirements previously described. Larger capacitors provide a wider range of stability and better load transient response. The following is a partial listing of surface-mount capacitors usable with the TPS70751 for fast transient response application.

This information, along with the ESR graphs, is included to assist in selection of suitable capacitance for the user's application. When it is necessary to achieve low height requirements along with high output current and/or high load capacitance, several higher ESR capacitors can be used in parallel to meet the previous guidelines.

VALUE	MFR.	MAX ESR	PART NO.
22 µF	Kemet	345 mΩ	7495C226K0010AS
33 µF	Sanyo	100 mΩ	10TPA33M
47 µF	Sanyo	100 mΩ	6TPA47M
68 µF	Sanyo	45 mΩ	10TPC68M

ESR and Transient Response

LDOs typically require an external output capacitor for stability. In fast transient response applications, capacitors are used to support the load current the while the LDO amplifier is responding. In most applications, one capacitor is used to support both functions.

Besides its capacitance, every capacitor also contains parasitic impedances. These parasitic impedances are resistive as well as inductive. The resistive impedance is called ESR, and the inductive impedance is called equivalent series inductance (ESL). The equivalent schematic diagram of any capacitor can, therefore, be drawn as shown in Figure 40.

Figure 40. ESR and ESL

In most cases one can neglect the effect of inductive impedance ESL. Therefore, the following application focuses mainly on the parasitic resistance ESR.

Figure 41 shows the output capacitor and its parasitic impedances in a typical LDO output stage.

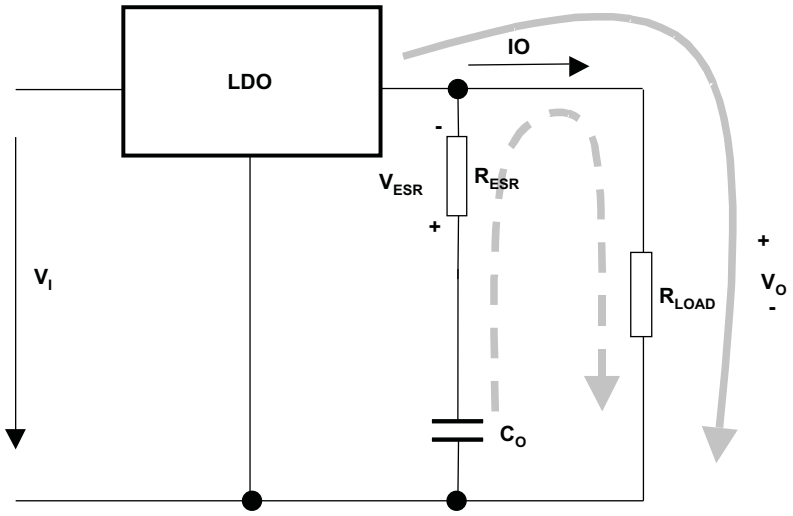


Figure 41. LDO Output Stage With Parasitic Resistances ESR

In steady state (dc state condition), the load current is supplied by the LDO (solid arrow) and the voltage across the capacitor is the same as the output voltage [$V(C_O) = V_O$]. This means no current is flowing into the C_O branch. If I_O suddenly increases (transient condition), the following occurs.

The LDO is not able to supply the sudden current need due to its response time (t_1 in Figure 42). Therefore, capacitor C_O provides the current for the new load condition (dashed arrow). C_O now acts like a battery with an internal resistance, ESR. Depending on the current demand at the output, a voltage drop occurs at R_{ESR}. This voltage is shown as V_{ESR} in Figure 41.

When C_O is conducting current to the load, initial voltage at the load will be $V_O = V(C_O) – V_{ESR}$. Due to the discharge of C_O, the output voltage V_O drops continuously until the response time t_1 of the LDO is reached and the LDO resumes supplying the load. From this point, the output voltage starts rising again until it reaches the regulated voltage. This period is shown as t_2 in Figure 42.

The figure also shows the impact of different ESRs on the output voltage. The left brackets show different levels of ESRs, where number 1 displays the lowest and number 3 displays the highest ESR.

From the previous paragraphs, these conclusions can be drawn:

- The higher the ESR, the larger the droop at the beginning of load transient.
- The smaller the output capacitor, the faster the discharge time and the bigger the voltage droop during the LDO response period.

Conclusion

To minimize the transient output droop, capacitors must have a low ESR and be large enough to support the minimum output voltage requirement.

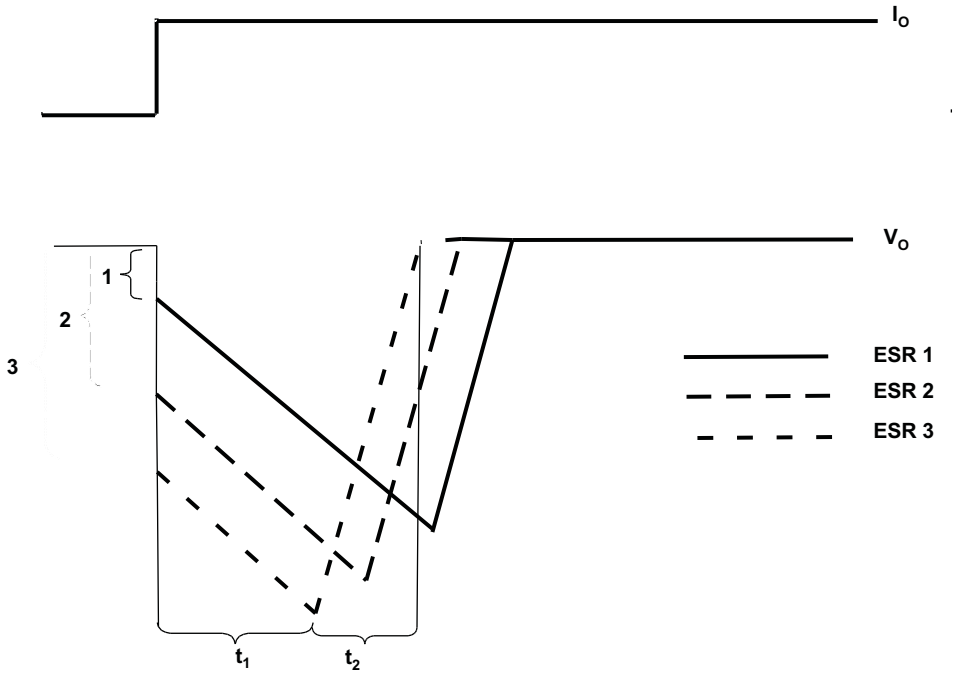


Figure 42. Correlation of Different ESRs and Their Influence to the Regulation of V_O at a Load Step From Low-to-High Output Current

Regulator Protection

Both TPS70751 PMOS-pass transistors have built-in back diodes that conduct reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS70751 also features internal current limiting and thermal protection. During normal operation, the TPS70751 regulator 1 limits output current to approximately 1.6 A (typ) and regulator 2 limits output current to approximately 750 mA (typ). When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C (typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C (typ), regulator operation resumes.

Power Dissipation and Junction Temperature

Specified regulator operation is ensured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where:

$T_J max$ = Maximum allowable junction temperature

$R_{\theta JA}$ = Thermal resistance junction-to-ambient for the package, i.e., 32.6°C/W for the 20-terminal PWP with no airflow

T_A = Ambient temperature

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS70751MPWPREP	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	70751MEP

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

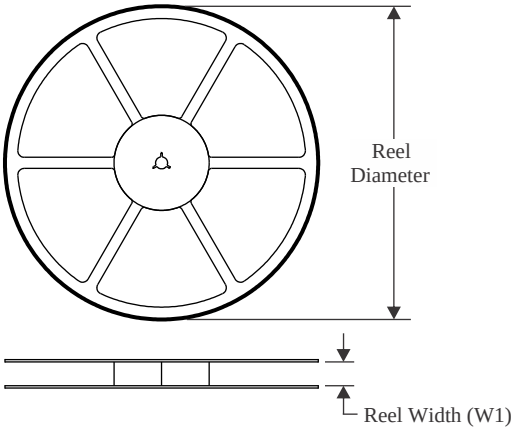
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

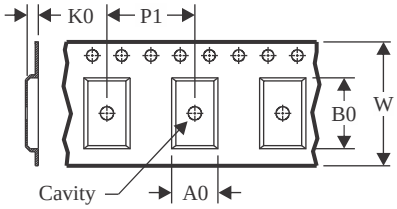
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

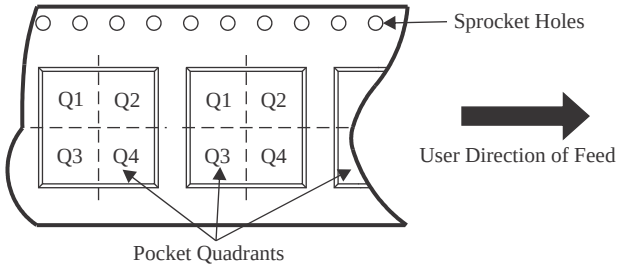


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

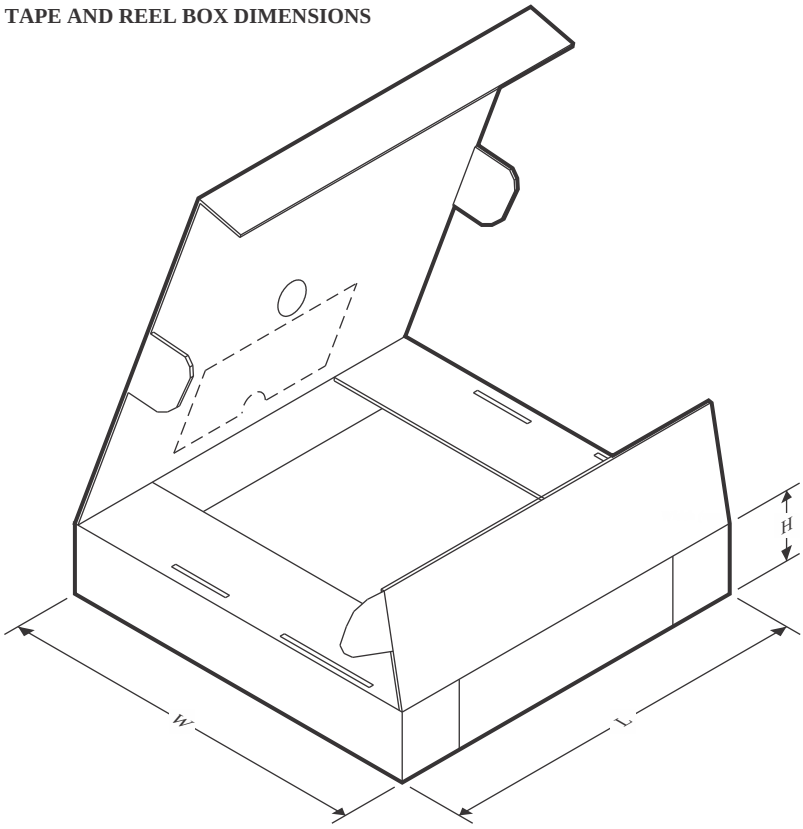
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS70751MPWPREP	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS70751MPWPREP	HTSSOP	PWP	20	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

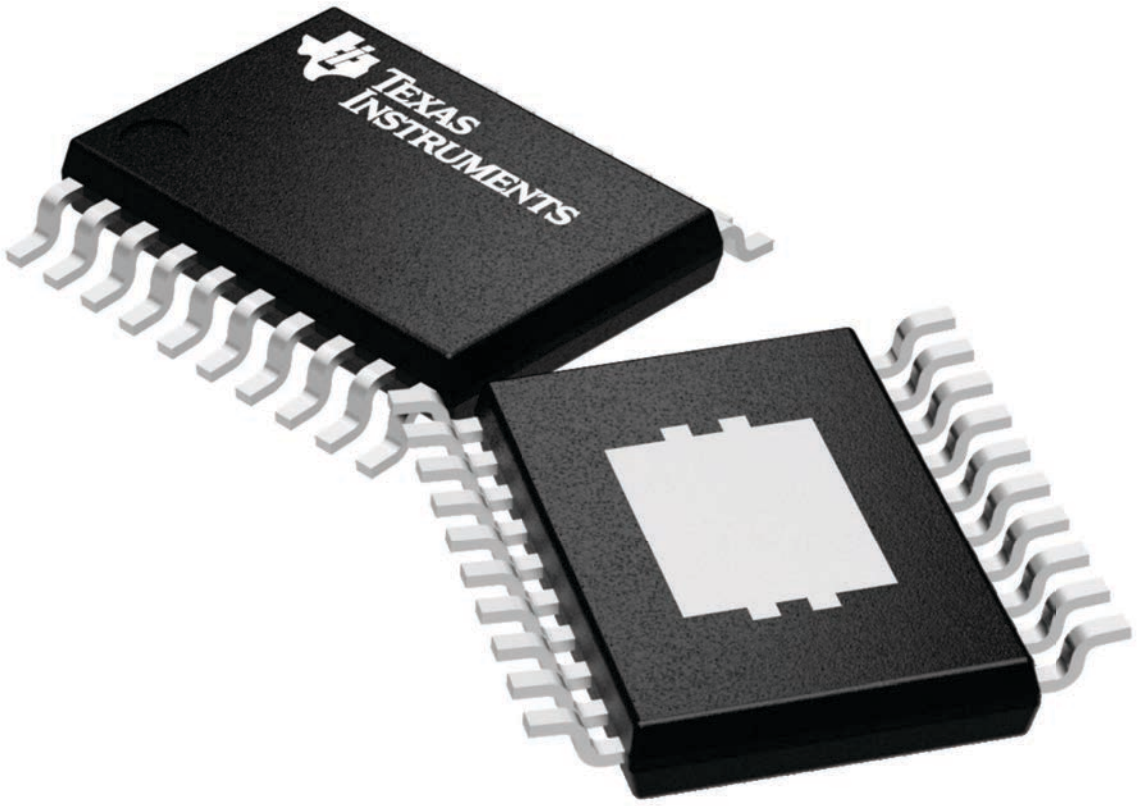
PWP 20

HTSSOP - 1.2 mm max height

6.5 x 4.4, 0.65 mm pitch

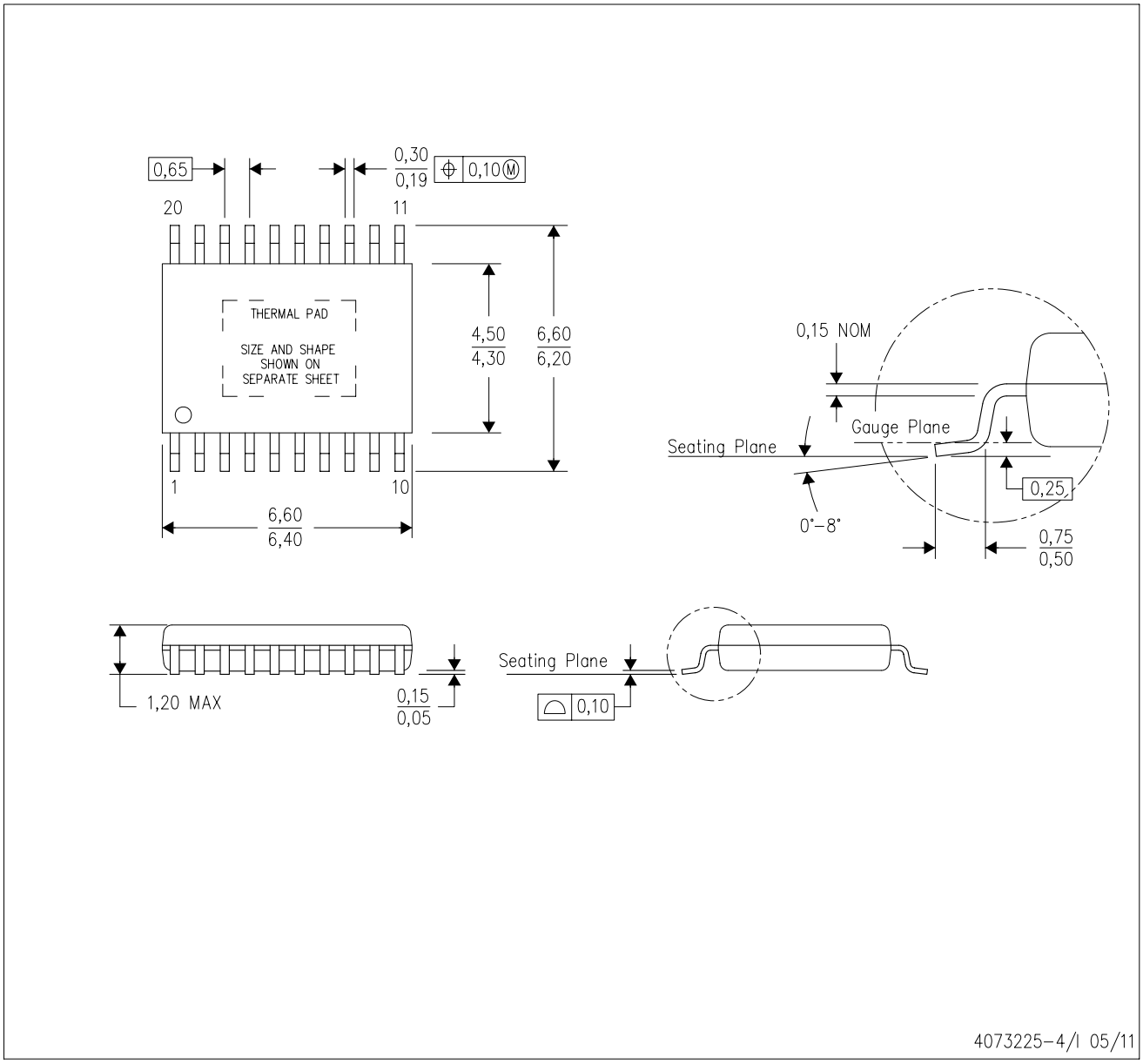
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

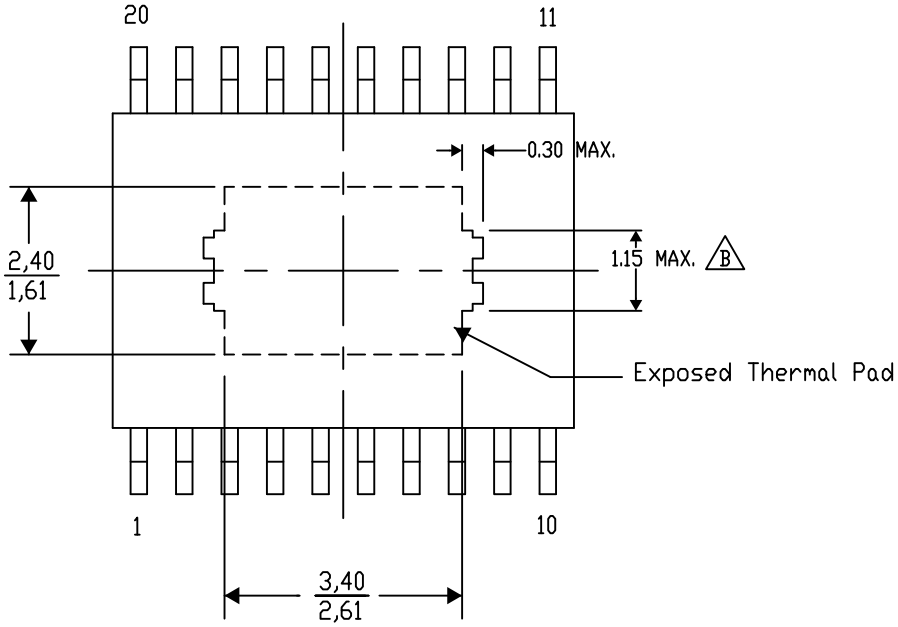
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

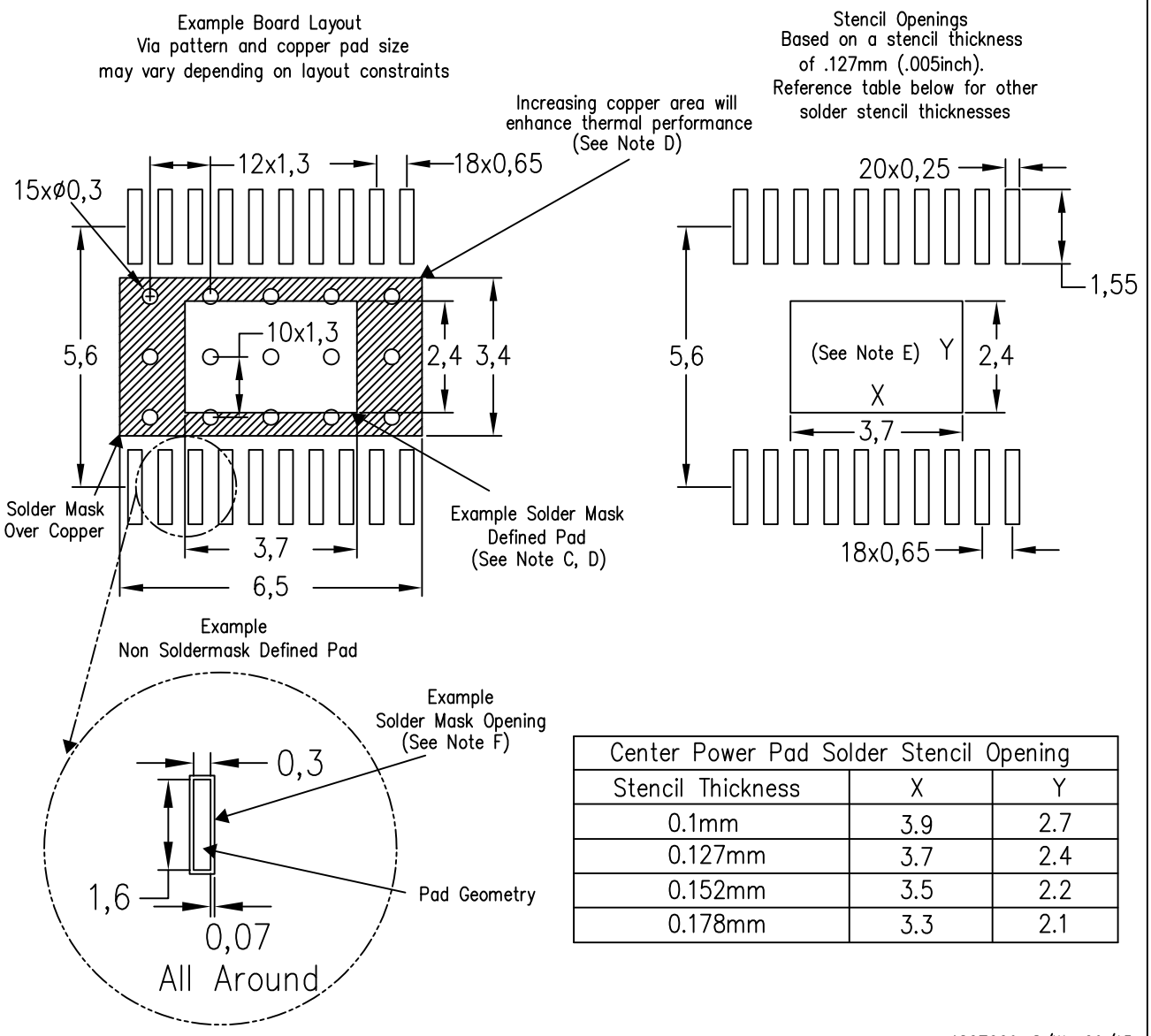
4206332–15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–8/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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