TPS735 500-mA, Low Quiescent Current, Low Noise, High PSRR,
Low-Dropout Linear Regulator

1 Features

• Input Voltage: 2.7 V to 6.5 V
• 500-mA Low-Dropout Regulator With EN
• Low I\text{Q}: 45 \mu A
• Multiple Output Voltage Versions Available:
  – Fixed Outputs of 1.2 V to 4.3 V
  – Adjustable Outputs from 1.25 V to 6 V
• High PSRR: 68 dB at 1 kHz
• Low Noise: 13.2 \mu V\text{RMS}
• Fast Start-Up Time: 45 \mu s
• Stable With a Ceramic, 2.2-\mu F, Low-ESR Output Capacitor
• Excellent Load and Line Transient Response
• 2% Overall Accuracy (Load, Line, and Temperature, V\text{OUT} > 2.2 V)
• Very Low Dropout: 280 mV at 500 mA
• 2-mm x 2-mm WSON-6 and 3-mm x 3-mm SON-8 Packages

2 Applications

• Post DC-DC Converter Ripple Filtering
• IP Network Cameras
• Macro Base Stations
• Thermostats

3 Description

The TPS735 low-dropout (LDO), low-power linear regulator offers excellent AC performance with very low ground current. High power-supply rejection ratio (PSRR), low noise, fast start-up, and excellent line and load transient responses are provided while consuming a very low 45-\mu A (typical) ground current.

The TPS735 device is stable with ceramic capacitors and uses an advanced BiCMOS fabrication process to yield a typical dropout voltage of 280 mV at 500-mA output. The TPS735 device uses a precision voltage reference and feedback loop to achieve overall accuracy of 2% (V\text{OUT} > 2.2 V) over all load, line, process, and temperature variations. This device is fully specified from \( T_J = -40°C \) to +125°C and is offered in a low-profile, 3 mm x 3 mm SON-8 package and a 2 mm x 2 mm WSON-6 package.

Device Information\(^{(1)}\)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS735</td>
<td>WSON (6)</td>
<td>2.00 mm x 2.00 mm</td>
</tr>
<tr>
<td></td>
<td>SON (8)</td>
<td>3.00 mm x 3.00 mm</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application

![Typical Application Diagram]

Optional input capacitor, \( C_{IN} \), to improve source impedance, noise, and PSRR

Optional bypass capacitor, \( C_{NR} \), to reduce output noise and increase PSRR
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   11.1 Device Support .................................................... 20
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision L (January 2015) to Revision M

- Updated data sheet text to latest data sheet and translation standards .................................................. 1
- Changed “Ultra-Low Noise” to “Low Noise” in document title ................................................................. 1
- Changed Low $I_0$ from 46 μA to 45 μA in Features, Description, and Application Information sections ........ 1
- Changed “Standard” to “Ceramic” in Features list ..................................................................................... 1
- Changed 6-pin package from “SON” to “WSON” in Features list .......................................................... 1
- Deleted printers, WiFi®, WiMax Modules, cellular phones, smart phones and microprocessor power from
  Applications section ........................................................................................................................................ 1
- Added post DC/DC ripple filtering, IP network cameras, macro base stations, and thermostats to Applications
  section ................................................................................................................................................................. 1
- Changed $T_A$ to $T_J$ in Description section .................................................................................................. 1
- Changed 6-pin package from “SON” to “WSON” in Description section ................................................. 1
- Changed package in Device Information table from VSON (6) to WSON (6) .............................................. 1
- Changed 6-pin DRB package descriptor from “VSON” to “SON” in Pin Configurations and Functions section .... 4
- Changed 6-pin DRV package descriptor from “VSON” to “WSON” in Pin Configurations and Functions section 4
- Added “feedback resistor” parameter to Recommended Operating Conditions table .................................. 5
- Changed DRV package descriptor from “VSON” to “WSON” in Thermal Information table ..................... 6
- Changed DRB package descriptor from “VSON” to “SON” in Thermal Information table .......................... 6
- Changed TPS735 Ground Pin Current (Disable) vs Temperature in Typical Characteristics section .............. 8
- Changed TPS735 Dropout Voltage vs Output Current in Typical Characteristics section ............................ 8
- Updated Equation 1 ................................................................................................................................. 14
- Changed x-axis scale from “10 ms/div” to “10 μs/div” in Figure 17 ........................................................... 15
- Changed x-axis scale from “10 ms/div” to “10 μs/div” in Figure 18 ........................................................... 15
- Changed $V_{OUT}$ starting value to 0 V in Figure 19 ....................................................................................... 15
- Updated Equation 2 ................................................................................................................................. 17
- Updated Equation 3 ................................................................................................................................. 17
- Changed DRV package descriptor from “SON” to “WSON” in Measuring Points for $T_J$ and $T_B$ ............... 19
Revision History (continued)

• Deleted references to thermal information documents in Related Documentation section ........................................ 20

Changes from Revision K (August, 2013) to Revision L Page

• Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information sections ................................................................. 1
• Added first bullet item in Features list .................................................................................................................. 1
• Changed fourth bullet item in Features list to "fixed outputs of 1.2 V" .................................................................. 1
• Changed eighth bullet item in Features list ........................................................................................................ 1
• Changed last bullet in Features list .................................................................................................................... 1
• Changed last Applications list item .................................................................................................................. 1
• Changed Pin Configuration and Functions section; updated table format and pin descriptions to meet new standards .... 4
• Changed C_{NR} value notation from 0.01 µF to 10 nF throughout Electrical Characteristics.................................. 7
• Changed feedback voltage parameter values and measured test conditions ...................................................... 7
• Changed output current limit maximum specified value ..................................................................................... 7
• Changed power-supply rejection ratio typical specified values for 100 Hz, 10 kHz, and 100 kHz frequency test conditions ................................................................. 7
• Added note (1) to Figure 1 .................................................................................................................................. 8
• Changed y-axis title for Figure 6 ......................................................................................................................... 8
• Changed y-axis title for Figure 7 ......................................................................................................................... 8
• Changed footnote for Figure 13 .......................................................................................................................... 10
• Changed reference to noise-reduction capacitor (C_{NR}) to feed-forward capacitor (C_{FF}) in Transient Response ... 11
• Changed noise-reduction capacitor to feed-forward capacitor in Figure 16 ....................................................... 13
• Changed references to "noise-reduction capacitor" (C_{NR}) to "feed-forward capacitor" (C_{FF}) and section title from "Feedback Capacitor Requirements" to "Feed-forward Capacitor Requirements" in Feed-Forward Capacitor Requirements section .................................................. 14
• Changed C_{NR} value notation from 0.01 µF to 10 nF in Output Noise section .................................................... 14

Changes from Revision J (May, 2011) to Revision K Page

• Added last sentence to first paragraph of Startup and Noise Reduction Capacitor section ..................................... 11

Changes from Revision I (April, 2011) to Revision J Page

• Replaced the Dissipation Ratings with Thermal Information................................................................. 6
• Revised conditions for Typical Characteristics to include statement about TPS73525 device availability ............. 8
• Added Estimating Junction Temperature section ................................................................................................. 18
• Updated Power Dissipation section ................................................................................................................... 19

Changes from Revision H (November, 2009) to Revision I Page

• Corrected typo in Electrical Characteristics table for V_{OUT} specification, DRV package test conditions, V_{OUT} ≤ 2.2V........ 7

Changes from Revision G (March 2009) to Revision H Page

• Revised bullet point in Features list to show very low dropout of 280 mV ................................................................. 1
• Changed dropout voltage typical specification from 250mV to 280mV ................................................................. 7
# 5 Pin Configuration and Functions

## DRB Package
8-Pin SON With Exposed Thermal Pad

### DRV Package
6-Pin WSON With Exposed Thermal Pad

## Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>NAME</th>
<th>NO</th>
<th>DESIGNATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN</td>
<td>I</td>
<td>DRV</td>
<td>6</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DRB</td>
<td>8</td>
<td>I</td>
</tr>
<tr>
<td>GND</td>
<td>—</td>
<td>DRV</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>EN</td>
<td>I</td>
<td>DRV</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>NR</td>
<td>—</td>
<td>DRV</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>FB</td>
<td>I</td>
<td>DRV</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>OUT</td>
<td>O</td>
<td>DRV</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>NC</td>
<td>—</td>
<td>DRV</td>
<td>5</td>
<td>2, 6, 7</td>
</tr>
<tr>
<td>Thermal pad</td>
<td>—</td>
<td>DRV</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

**NC** - No internal connection

Thermal Pad

Not to scale
6 Specifications

6.1 Absolute Maximum Ratings

at –40°C ≤ TJ and TA ≤ +125°C (unless otherwise noted). All voltages are with respect to GND.1

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN Voltage</td>
<td>–0.3</td>
<td>7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VEN</td>
<td>–0.3</td>
<td>V IN + 0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VFB</td>
<td>–0.3</td>
<td>1.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOUT</td>
<td>–0.3</td>
<td>V IN + 0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IOUT Current</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PD(tot) Continuous total power dissipation</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TJ Operating junction temperature</td>
<td>–40</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Tstg Storage temperature</td>
<td>–55</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed as Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated as Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th></th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(ESD) Electrostatic discharge</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Charged device model (CDM), per JEDEC specification JESD22-C101, all pins2</td>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN Input voltage</td>
<td>2.7</td>
<td>6.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOUT Output voltage</td>
<td>VFB</td>
<td>6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IOUT Output current1</td>
<td>0</td>
<td>500</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>TA Operating free-air temperature</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>CIN Input capacitor</td>
<td>1</td>
<td></td>
<td>μF</td>
<td></td>
</tr>
<tr>
<td>Cout Output capacitor</td>
<td>2</td>
<td></td>
<td>μF</td>
<td></td>
</tr>
<tr>
<td>CNR Noise reduction capacitor</td>
<td>10</td>
<td></td>
<td>nF</td>
<td></td>
</tr>
<tr>
<td>CFF Feed-forward capacitor2</td>
<td>3</td>
<td>22</td>
<td>1000</td>
<td>pF</td>
</tr>
<tr>
<td>R2 Feedback resistor2</td>
<td>110</td>
<td></td>
<td>kΩ</td>
<td></td>
</tr>
</tbody>
</table>

(1) When operating at TJ near 125°C, IOUT(min) is 500 μA.
(2) Adjustable version only.
6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TPS735 (2)</th>
<th>DRB (SON)</th>
<th>DRV (WSON)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>8 PINS</td>
<td>6 PINS</td>
<td></td>
</tr>
<tr>
<td>$R_{\text{UA}}$</td>
<td>Junction-to-ambient thermal resistance (3)</td>
<td></td>
<td>52.2</td>
<td>65.1 °C/W</td>
</tr>
<tr>
<td>$R_{\text{UJC(top)}}$</td>
<td>Junction-to-case (top) thermal resistance (4)</td>
<td>59.4</td>
<td>85.6</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{\text{UB}}$</td>
<td>Junction-to-board thermal resistance</td>
<td>19.3</td>
<td>34.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{\text{JT}}$</td>
<td>Junction-to-top characterization parameter (5)</td>
<td>2</td>
<td>1.6</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{\text{JB}}$</td>
<td>Junction-to-board characterization parameter (6)</td>
<td>19.3</td>
<td>35.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{\text{UJC(bot)}}$</td>
<td>Junction-to-case (bottom) thermal resistance (7)</td>
<td>11.8</td>
<td>5.8</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

(2) Thermal data for the DRB, DCQ, and DRV packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:

(a) i. DRB: The exposed pad is connected to the PCB ground layer through a 2 x 2 thermal via array.
   ii. DRV: The exposed pad is connected to the PCB ground layer through a 2 x 2 thermal via array. Due to size limitation of thermal pad, 0.8-mm pitch array is used which is off the JEDEC standard.

(b) i. DRB: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
   ii. DRV: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.

(c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3-in x 3-in copper area. To understand the effects of the copper area on thermal performance, see the Power Dissipation and Estimating Junction Temperature sections.

(3) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(4) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(5) The junction-to-top characterization parameter, $\psi_{\text{JT}}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain $R_{\text{UA}}$ using a procedure described in JESD51-2a (sections 6 and 7).

(6) The junction-to-board characterization parameter, $\psi_{\text{JB}}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain $R_{\text{UB}}$ using a procedure described in JESD51-2a (sections 6 and 7).

(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
6.5 Electrical Characteristics

over operating temperature range \((-40°C ≤ T_J ≤ 125°C)\), \(V_{IN} = V_{OUT(nom)} + 0.5\) V or 2.7 V (whichever is greater), \(I_{OUT} = 1\) mA, \(V_{EN} = V_{IN}\), \(C_{OUT} = 2.2\) μF, and \(C_{NR} = 10\) nF (unless otherwise noted). For the adjustable version (TPS73501), \(V_{OUT} = 3\) V. Typical values are at \(T_A = 25°C\).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{IN})</td>
<td>Input voltage(^{(1)})</td>
<td>2.7</td>
<td>6.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(V_{FB})</td>
<td>Internal reference (adjustable version only)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{OUT})</td>
<td>Output voltage range (adjustable version only)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(\Delta V_{OUT(VIN)})</td>
<td>Line regulation(^{(1)})</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(\Delta V_{OUT(IOUT)})</td>
<td>Load regulation</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{DO})</td>
<td>Dropout voltage(^{(2)})</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{LIM})</td>
<td>Output current limit</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{GND})</td>
<td>Ground pin current</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{FB})</td>
<td>Feedback pin current (adjustable version only)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>Power-supply rejection ratio</td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>(V_{n})</td>
<td>Output noise voltage</td>
<td></td>
<td></td>
<td></td>
<td>μVRMS</td>
</tr>
<tr>
<td>(I_{STR})</td>
<td>Start-up time</td>
<td></td>
<td></td>
<td></td>
<td>μS</td>
</tr>
<tr>
<td>(V_{EN(HI)})</td>
<td>Enable high (enabled)</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(V_{EN(LO)})</td>
<td>Enable low (shutdown)</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(I_{EN(HI)})</td>
<td>Enable pin current, enabled</td>
<td></td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>(T_{sd})</td>
<td>Thermal shutdown temperature</td>
<td></td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>UVLO</td>
<td>Undervoltage lockout</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(V_{IN})</td>
<td>Hysteresis</td>
<td></td>
<td></td>
<td></td>
<td>mV</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Minimum \(V_{IN} = V_{OUT(nom)} + 0.5\) V or 2.7 V, whichever is greater.
\(^{(2)}\) \(V_{DO}\) is not measured for this family of devices with \(V_{OUT(nom)} < 2.8\) V because the minimum \(V_{IN} = 2.7\) V.
6.6 Typical Characteristics

over operating temperature range (T_J = –40°C to +125°C), \( V_{IN} = V_{OUT(nom)} + 0.5 \) V or 2.7 V, whichever is greater; \( I_{OUT} = 1 \) mA, \( V_{EN} = V_{IN}, C_{OUT} = 2.2 \) μF, \( C_{NR} = 10 \) nF. Typical values are at \( T_J = 25°C \), (unless otherwise noted).
Typical Characteristics (continued)

over operating temperature range \((T_J = -40°C \text{ to } +125°C)\), \(V_{EN} = V_{OUT(nom)} + 0.5\) V or 2.7 V, whichever is greater; \(I_{OUT} = 1\) mA, \(V_{EN} = V_{IN}, C_{OUT} = 2.2\ \mu\text{F}, C_{NR} = 10\ n\text{F}\). Typical values are at \(T_J = 25°C\), (unless otherwise noted).

![Figure 7. TPS735 Dropout Voltage vs Output Current](image1)

![Figure 8. Power-Supply Ripple Rejection vs Frequency](image2)

![Figure 9. Power-Supply Ripple Rejection vs Frequency](image3)

![Figure 10. Power-Supply Ripple Rejection vs Frequency](image4)

![Figure 11. TPS73525 RMS Noise vs \(C_{NR}\)](image5)

![Figure 12. TPS735 RMS Noise vs \(C_{OUT}\)](image6)
7 Detailed Description

7.1 Overview
The TPS735 of low dropout (LDO) regulator combines the high performance required by radio frequency (RF) and precision analog applications with ultra-low current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection and very low headroom ($V_{IN} - V_{OUT}$). Fixed voltage versions provide a noise reduction pin to bypass noise that is generated by the band-gap reference and to improve PSRR. A quick-start circuit fast-charges this capacitor at start-up. The combination of high performance and low ground current make the TPS735 device designed for portable applications. All versions have thermal and overcurrent protection and are specified from $-40^\circ C \leq T_J \leq +125^\circ C$.

7.2 Functional Block Diagrams

Figure 13. Fixed Voltage Versions

Figure 14. Adjustable Voltage Versions
7.3 Feature Description

7.3.1 Internal Current Limit

The TPS735 internal current limit protects the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is independent of the output voltage. For reliable operation, do not operate the device in current limit for extended periods of time.

The PMOS pass element in the TPS735 device contains a built-in body diode that conducts current when the voltage at the OUT pin exceeds the voltage at the IN pin. This current is not limited, so if extended reverse voltage operation is expected, external limiting is appropriate.

7.3.2 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage TTL-CMOS levels. When shutdown capability is not required, the EN pin can connect to the IN pin.

7.3.3 Dropout Voltage

The TPS735 device uses a PMOS pass transistor to achieve low dropout. When \( V_{\text{IN}} - V_{\text{OUT}} \) is less than the dropout voltage \( V_{\text{DO}} \), the PMOS pass device is in the linear region of operation and the input-to-output resistance \( R_{\text{IN/OUT}} \) of the PMOS pass element. \( V_{\text{DO}} \) scales with the output current because the PMOS device operates like a resistor in dropout.

As with any linear regulator, PSRR and transient response degrades as \( V_{\text{IN}} - V_{\text{OUT}} \) approaches dropout. Typical Characteristics shows this effect; (see Figure 8 through Figure 10).

7.3.4 Start-Up and Noise Reduction Capacitor

Fixed voltage versions of the TPS735 use a quick-start circuit to charge the noise reduction (NR) capacitor \( C_{\text{NR}} \) if present (see Functional Block Diagrams). This architecture allows the combination of low output noise and fast start-up times. The NR pin is high impedance so a low-leakage \( C_{\text{NR}} \) capacitor must be used. Most ceramic capacitors are appropriate in this configuration. A high-quality, COG-type (NPO) dielectric ceramic capacitor is recommended for \( C_{\text{NR}} \) when used in environments where abrupt changes in temperature can occur.

For the fastest start-up, first apply \( V_{\text{IN}} \), then drive the enable (EN) pin high. If EN is tied to IN, start-up is slower. See Typical Applications. The quick-start switch closes for approximately 135 \( \mu \text{s} \). To ensure that \( C_{\text{NR}} \) is charged during the quick-start time, use a capacitor with a value of no more than 0.01 \( \mu \text{F} \).

7.3.5 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases the transient response duration. In the adjustable version, adding \( C_{\text{FF}} \) between the OUT and FB pins improves stability and transient response performance. The transient response of the TPS735 device is enhanced by an active pulldown that engages when the output overshoots by approximately 5% or more when the device is enabled. The pull-down device operates like a 400-\( \Omega \) resistor to ground when enabled.

7.3.6 Undervoltage Lockout

The TPS735 device uses an undervoltage lockout circuit to disable the output until the internal circuitry is operates properly. The UVLO circuit contains a deglitch feature so that the UVLO ignores undershoot transients on the input if the transients are less than 50 \( \mu \text{s} \) in duration.

7.3.7 Minimum Load

The TPS735 device is stable with no output load. To meet the specified accuracy, a minimum load of 500 \( \mu \text{A} \) is required. If the output is below 500 \( \mu \text{A} \) and if the junction temperature is approximately 125\(^{\circ}\text{C} \), the output can increase enough to turn on the output pulldown. The output pulldown limits voltage drift to 5% (typically) but ground current can increase by approximately 50 \( \mu \text{A} \). In most applications, the junction does not reach high temperatures at light loads because little power is dissipated. As a result, the specified ground current is valid at no load in most applications.
Feature Description (continued)

7.3.8 Thermal Protection
Thermal protection disables the output when the junction temperature increases to approximately 165°C, which allows the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit cycles on and off. This cycling limits the dissipation of the regulator and protects the regulator from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 125°C (maximum). To estimate the thermal margin in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered. Use worst-case loads and signal conditions. For reliable operation, trigger thermal protection at least 40°C above the maximum expected ambient condition of a particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS735 protects against overload conditions. This protection circuitry is not intended to replace proper heat sinking. Continuously running the TPS735 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation
The device regulates to the nominal output voltage under the following conditions:

- The input voltage previously exceeded the UVLO voltage and did not decrease below the UVLO threshold minus \( V_{hys} \).
- The input voltage is greater than the nominal output voltage that is added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is within the specified range.

7.4.2 Dropout Operation
If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is equal to the input voltage minus the dropout voltage. The transient performance of the device degrades because the pass device is in a triode state and the LDO operates like a resistor. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled
The device is disabled under the following conditions:

- The input voltage is less than the UVLO threshold minus \( V_{hys} \), or has not yet exceeded the UVLO threshold.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 lists the conditions that result in different modes of operation.

<table>
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<tr>
<th>OPERATING MODE</th>
<th>PARAMETER</th>
<th>( V_{IN} )</th>
<th>( V_{EN} )</th>
<th>( I_{OUT} )</th>
<th>( T_{J} )</th>
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<td>Normal mode</td>
<td>( V_{IN} &gt; V_{OUTnom} + V_{DO} ) and ( V_{IN} &gt; UVLO )</td>
<td>( V_{EN} &gt; V_{EN(HI)} )</td>
<td>( I_{OUT} &lt; I_{LIM} )</td>
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<tr>
<td>Dropout mode</td>
<td>( UVLO &lt; V_{IN} &lt; V_{OUTnom} + V_{DO} )</td>
<td>( V_{EN} &gt; V_{EN(HI)} )</td>
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<td>( T_{J} &lt; 165°C )</td>
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<tr>
<td>Disabled mode (any true condition disables the device)</td>
<td>( V_{IN} &lt; UVLO - V_{hys} )</td>
<td>( V_{EN} &lt; V_{EN(LO)} )</td>
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<td>( T_{J} &gt; 165°C )</td>
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8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The TPS735 LDO regulator provides a design with an ultra-low noise, high PSRR, low-dropout linear regulation with a very small ground current (5 µA, typical).

The devices are stable with ceramic capacitors and have a dropout voltage of 280 mV at the full output rating of 500 mA. The features of the TPS735 device enables the LDO regulators to be used in a wide variety of applications with minimal design complexity.

8.2 Typical Applications
Figure 15 shows the basic circuit connections for fixed-voltage models. Figure 16 shows the connections for the adjustable output version. R<sub>1</sub> and R<sub>2</sub> can be calculated for any output voltage using the formula in Figure 16.

![Figure 15. Typical Application Circuit for Fixed-Voltage Versions](image)

![Figure 16. Typical Application Circuit for Adjustable-Voltage Versions](image)
Typical Applications (continued)

8.2.1 Design Requirements

8.2.1.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, connecting a 0.1-μF to 1-μF low-equivalent series-resistance (ESR) capacitor across the input supply near the regulator is good analog design practice. This capacitor counteracts reactive input sources and improves transient response and ripple rejection. A higher-value capacitor may be required if large, fast, rise-time load transients are expected, or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-μF input capacitor may be required to ensure stability.

The TPS735 device is designed to be stable with standard ceramic output capacitors of values 2 μF or larger. X5R- and X7R-type capacitors are best because these capacitors feature minimal variation in value and ESR over temperature. Maximum ESR of the output capacitor is < 1 Ω and, therefore, the output capacitor type must be ceramic or conductive polymer electrolytic.

8.2.1.2 Feed-Forward Capacitor Requirements

The feed-forward capacitor (C_{FF}), shown in Figure 16, is required for stability. For a parallel combination of R_1 and R_2 equal to 250 kΩ, any value between 3 pF to 1 nF can be used. Fixed-voltage versions have an internal 30-pF feed-forward capacitor that is quick-charged at start-up. Larger value capacitors improve noise slightly. The TPS735 device is stable in unity-gain configurations (the OUT pin is tied to the FB pin) without C_{FF}.

8.2.2 Detailed Design Procedure

8.2.2.1 Output Noise

In most LDO regulators, the band gap is the dominant noise source. If a noise-reduction capacitor (C_{NR}) is used with the TPS735 device, the band gap does not contribute significantly to noise. Noise is dominated by the output resistor divider and the error-amplifier input. To minimize noise in a given application, use a 10-nF noise reduction capacitor. For the adjustable version, smaller value resistors in the output resistor divider reduce noise. A parallel combination that produces 2 μA of divider current has the same noise performance as a fixed voltage version with a C_{NR}. To further optimize noise, set the ESR of the output capacitor to approximately 0.2 Ω. This configuration maximizes phase margin in the control loop, which reduces the total output noise up to 10%. TI recommends a maximum capacitor value of 10 nF.

Equation 1 calculates the approximate integrated output noise from 10 Hz to 100 kHz with a C_{NR} value of 10 nF.

\[
V_n (\mu V_{\text{RMS}}) = 11(\mu V_{\text{RMS}} / V) \times V_{\text{OUT}} (V)
\]

(1)

The TPS735 adjustable version does not have the noise-reduction pin available, so ultra-low noise operation is not possible. Noise is minimized according to the previously listed recommendations.
Typical Applications (continued)

8.2.3 Application Curves

at $V_{IN} = \min\{V_{OUT\text{nom}} + 0.5\, V, 2.7\, V\}$, whichever is greater; $I_{OUT} = 1\, mA$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\, \mu F$, $C_{NR} = 10\, nF$, and $T_J = 25^\circ C$ (unless otherwise noted)

![Figure 17. TPS735 Turnon Response ($V_{IN} = V_{EN}$)](image1)

![Figure 18. TPS735 Turnon Response Using EN](image2)

![Figure 19. TPS73525 Power-Up and Power-Down ($V_{IN} = V_{EN}$)](image3)

![Figure 20. TPS735 Load Transient Response](image4)

![Figure 21. TPS735 Line Transient Response](image5)
9 Power Supply Recommendations
The device is designed to operate from an input voltage supply range between 2.7 V and 6.5 V. The input voltage range must provide adequate headroom for the device to have a regulated output. This input supply must be well-regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve output noise.

10 Layout

10.1 Layout Guidelines
For best overall performance, place all circuit components on the same side of the circuit board and as near to the respective LDO pin connections as possible. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO component connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and as a result, reduces load-current transients, minimizes noise, and increases circuit stability. TI recommends using a ground reference plane, and is embedded in the printed circuit board (PCB) itself or located on the bottom side of the PCB opposite the components. This reference plane ensures accuracy of the output voltage, shields the LDO from noise, and operates similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the exposed thermal pad. In most applications, this ground plane is required to meet thermal requirements.

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance
To improve AC performance (such as PSRR, output noise, and transient response), TI recommends designing the board with separate ground planes for $V_{IN}$ and $V_{OUT}$, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

10.2 Layout Example

```
Figure 22. TPS735 Fixed Version Layout Reference Diagram
```

(1) $C_{IN}$ and $C_{OUT}$ are 0603 capacitors and $C_{NR}$ is a 0402 capacitor. The footprint is shown to scale with package size.
10.3 Power Dissipation

The ability to remove heat from the die is different for each package type, which presents different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are shown in the Thermal Information section. Heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers improves the heat sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation can be approximated by the product of the output current and the voltage drop across the output pass element, as Equation 2 shows.

\[ P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \]  

NOTE

When the device is used in a condition of high input and low output voltages, \( P_D \) can exceed the junction temperature rating even when the ambient temperature is at room temperature.

Equation 3 is an example calculation for the power dissipation (\( P_D \)) of the DRB package.

\[ P_D = (6.5 \text{ V} - 1.2 \text{ V}) \times 500 \text{ mA} = 2.65 \text{ W} \]  

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output performance.

On the DRB package, the primary conduction path for heat is through the exposed thermal pad to the PCB. The pad can be connected to ground or left floating. The pad must be attached to an appropriate amount of copper PCB area to ensure that the device does not overheat. The maximum allowable junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device. Equation 4 calculates the maximum junction-to-ambient thermal resistance.

\[ R_{JUA} = \frac{(125^\circ \text{C} - T_A)}{P_D} \]
Power Dissipation (continued)

Figure 23 estimates the maximum $R_{\text{JA}}$ and the minimum amount of PCB copper area required to heat sink.

\[
\theta_{\text{JA}} = \theta_{\text{T}} + P
\]

where:
- $P_D$ is the power dissipation calculated with Equation 2,
- $T_T$ is the temperature at the center-top of the device package, and
- $T_B$ is the PCB temperature measured 1 mm away from the device package on the PCB surface (as shown in Figure 25).

\[\text{(5)}\]

Both $T_T$ and $T_B$ can be measured on actual application boards using a thermo-gun (an infrared thermometer).

Estimating Junction Temperature (continued)

According to Figure 24, the new thermal metrics ($\Psi_{JT}$ and $\Psi_{JB}$) do not depend on the copper area. Using $\Psi_{JT}$ or $\Psi_{JB}$ with Equation 5 can estimate $T_J$ by measuring $T_T$ or $T_B$ on an application board.

![Figure 24. $\Psi_{JT}$ and $\Psi_{JB}$ vs Board Size](image)

(1) Power dissipation may limit operating range. See Thermal Information.

![Figure 25. Measuring Points for $T_T$ and $T_B$](image)

10.5 Package Mounting

Solder pad footprint recommendations for the TPS735 device is available from the TI website at www.ti.com.
11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules
Two evaluation modules (EVMs) are available to assist in the initial circuit performance evaluation using the TPS735. The TPS73501EVM-276 evaluation module and the TPS73525EVM-276 Evaluation Module (and related user guide) can be requested at the TI website through the product folders or purchased directly from the TI eStore.

11.1.2 Device Nomenclature

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<th>PRODUCT</th>
<th>$V_{OUT}$</th>
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<td>TPS735xx(x)yyy</td>
<td>xx(x) is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 33 = 3.3 V; 125 = 1.25 V). yyy is the package designator. z is the tape and reel quantity (R = 3000, T = 250). 01 is the adjustable version.</td>
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(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation
For related documentation, see the following:
• Texas Instruments, TPS735EVM-276 User Guide

11.3 Trademarks
All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

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<th>Lead finish/ Ball material</th>
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(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBsolete: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS735:**
- **Automotive:** TPS735-Q1

**NOTE:** Qualified Version Definitions:
- **Automotive** - Q100 devices qualified for high-reliability automotive applications targeting zero defects
### TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

#### REEL DIMENSIONS

- Reel Diameter
- Reel Width (W1)

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- Sprocket Holes
- Pocket Quadrants

*All dimensions are nominal.*

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**TAPE AND REEL BOX DIMENSIONS**

*All dimensions are nominal*

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Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
NOTES:

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5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
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