TPS74901 3-A Low Dropout Linear Regulator With Programmable Soft-Start

1 Features

- $V_{OUT}$ Range: 0.8 V to 3.6 V
- Ultralow $V_{IN}$ Range: 0.8 V to 5.5 V
- $V_{BIAS}$ Range: 2.7 V to 5.5 V
- Low Dropout: 120 mV (Typical) at 3 A
- Power-Good (PG) Output Allows Supply Monitoring or Provides a Sequencing Signal for Other Supplies
- 2% Accuracy Over Line, Load, and Temperature
- Adjustable Start-Up In-Rush Control
- $V_{BIAS}$ Permits Low $V_{IN}$ Operation With Good Transient Response
- Stable with Any Output Capacitor $\geq 2.2 \mu F$
- Packages:
  - Small, 3-mm × 3-mm × 1-mm VSON
  - 5-mm × 5-mm × 1-mm VQFN and DDPAK-7
- Active High Enable

2 Applications

- FPGA Applications
- DSP Core and I/O Voltages
- Servers
- Post-Regulation Applications
- Applications with Special Start-Up Time or Sequencing Requirements

3 Description

The TPS74901 low-dropout (LDO) linear regulator provides an easy-to-use, robust power management solution for a wide variety of applications. User-programmable soft-start minimizes stress on the input power source by reducing capacitive inrush current during start-up. The soft-start is monotonic and well-suited for powering many different types of processors and ASICs. The enable input and power-good output allow easy sequencing with external regulators. This complete flexibility permits the user to configure a solution that meets the sequencing requirements of FPGAs, DSPs, and other applications with special start-up requirements.

A precision reference and error amplifier deliver 2% accuracy over load, line, temperature, and process. The device is stable with any type of capacitor $\geq 2.2 \mu F$, and the device is fully specified from $-40^\circ C$ to $125^\circ C$. The TPS74901 is offered in a small (3 mm × 3 mm) VSON package and a small (5-mm × 5-mm) VQFN package, yielding a highly compact total solution size. The device is also available in a DDPAK-7 package.

Device Information (1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS74901</td>
<td>VQFN (20)</td>
<td>5.00 mm × 5.00 mm</td>
</tr>
<tr>
<td></td>
<td>DDPAK/TO-263 (7)</td>
<td>8.89 mm × 10.10 mm</td>
</tr>
<tr>
<td></td>
<td>VSON (10)</td>
<td>3.00 mm × 3.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Turnon Response

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An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (November 2015) to Revision I  Page

• Added DRC package to document ............................................................. 1
• Changed Packages Features bullet ............................................................. 1
• Added DRC package to Description section .............................................. 1
• Added DRC (VSON) package to Device Information table ............................ 1
• Added DRC package to Pin Configuration and Functions section .................. 3
• Added DRC package to Thermal Information table .................................... 5

Changes from Revision G (November 2010) to Revision H  Page

• Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ............................................................. 1
• Deleted nonimal values from \( V_{\text{IN}}, V_{\text{EN}}, \) and \( V_{\text{BIAS}} \) rows ............................................................. 4
• Changed values in the Thermal Information table ...................................... 5
• Changed values for VBIAS column on Normal mode, Dropout mode, and Disabled mode rows ............................................................. 13
• Changed \( V_{\text{IN(min)}} \) to \( V_{\text{IN(UVLO)}} \) under \( V_{\text{IN}} \) column in Disabled mode row ............................................................. 13

Changes from Revision F (August, 2010) to Revision G  Page

• Corrected equation for and updated values for Table 2 .................................. 16

Changes from Revision E (January, 2010) to Revision F  Page

• Revised Layout Recommendations and Power Dissipation section ................ 20
• Added Estimating Junction Temperature .................................................... 21
5  Pin Configuration and Functions

### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDPAK/TO-263</td>
<td>VQFN</td>
<td>VSON</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>BIAS</td>
<td>I</td>
<td>Bias input voltage for error amplifier, reference, and internal control circuits.</td>
</tr>
<tr>
<td>7</td>
<td>EN</td>
<td>I</td>
<td>Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left floating.</td>
</tr>
<tr>
<td>2</td>
<td>FB</td>
<td>I</td>
<td>This pin is the feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>—</td>
<td>Ground</td>
</tr>
<tr>
<td>5</td>
<td>IN</td>
<td>1, 2</td>
<td>Unregulated input to the device.</td>
</tr>
<tr>
<td>8, 14, 17</td>
<td>NC</td>
<td>—</td>
<td>No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top-side plane.</td>
</tr>
<tr>
<td>1, 18, 19, 20</td>
<td>OUT</td>
<td>9, 10</td>
<td>Regulated output voltage. A small capacitor (total typical capacitance ≥ 2.2 µF, ceramic) is needed from this pin to ground to assure stability.</td>
</tr>
<tr>
<td>9</td>
<td>PG</td>
<td>O</td>
<td>Power-Good (PG) is an open-drain, active-high output that indicates the status of V\textsubscript{OUT}. When V\textsubscript{OUT} exceeds the PG trip threshold, the PG pin goes into a high-impedance state. When V\textsubscript{OUT} is below this threshold the pin is driven to a low-impedance state. A pullup resistor from 10 kΩ to 1 MΩ must be connected from this pin to a supply up to 5.5 V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left floating if output monitoring is not necessary.</td>
</tr>
<tr>
<td>15</td>
<td>SS</td>
<td>—</td>
<td>Soft-Start pin. A capacitor connected on this pin to ground sets the start-up time. If this pin is left floating, the regulator output soft-start ramp time is typically 100 µs.</td>
</tr>
<tr>
<td>Thermal Pad</td>
<td>—</td>
<td>—</td>
<td>Solder to the ground plane for increased thermal performance.</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings
At \( T_J = -40^\circ C \) to 125°C, unless otherwise noted. All voltages are with respect to GND.\(^{(1)}\)

<table>
<thead>
<tr>
<th>( V_{IN}, V_{BIAS} )</th>
<th>Input voltage</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{EN} )</td>
<td>Enable voltage</td>
<td>-0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>( V_{PG} )</td>
<td>Power-good voltage</td>
<td>-0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>( I_{PG} )</td>
<td>PG sink current</td>
<td>0</td>
<td>1.5</td>
<td>mA</td>
</tr>
<tr>
<td>( V_{SS} )</td>
<td>SS pin voltage</td>
<td>-0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>( V_{FB} )</td>
<td>Feedback pin voltage</td>
<td>-0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>( V_{OUT} )</td>
<td>Output voltage</td>
<td>-0.3</td>
<td>( V_{IN} + 0.3 )</td>
<td>V</td>
</tr>
<tr>
<td>( I_{OUT} )</td>
<td>Maximum output current</td>
<td>Internally limited</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output short circuit duration</td>
<td>Indefinite</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( P_{Diss} )</td>
<td>Continuous total power dissipation</td>
<td>See Thermal Information</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_J )</td>
<td>Operating junction temperature</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>( T_{stg} )</td>
<td>Storage junction temperature</td>
<td>-55</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>( V_{(ESD)} )</th>
<th>Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(^{(1)})</td>
<td>±2000</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(^{(2)})</td>
<td>±500</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
\(^{(2)}\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions
over operating junction temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>( V_{IN} )</th>
<th>Input supply voltage</th>
<th>( V_{OUT} + V_{DO} ) (( V_{IN} ))</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{EN} )</td>
<td>Enable supply voltage</td>
<td>0</td>
<td>5.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{BIAS} )</td>
<td>BIAS supply voltage</td>
<td>( V_{OUT} + V_{DO} ) (( V_{BIAS} )) (^{(2)})</td>
<td>5.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{OUT} )</td>
<td>Output voltage</td>
<td>0.8</td>
<td>3.3</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{OUT} )</td>
<td>Output current</td>
<td>0</td>
<td>3</td>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_{OUT} )</td>
<td>Output capacitor</td>
<td>2.2</td>
<td>μF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_{IN} )</td>
<td>Input capacitor(^{(3)})</td>
<td>1</td>
<td>μF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_{BIAS} )</td>
<td>Bias capacitor</td>
<td>0.1</td>
<td>1</td>
<td>μF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_J )</td>
<td>Operating junction temperature</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) BIAS supply is required when \( V_{IN} \) is below \( V_{OUT} + 1.62 \) V.
\(^{(2)}\) \( V_{BIAS} \) has a minimum voltage of 2.7 V or \( V_{OUT} + V_{DO} \) (\( V_{BIAS} \)), whichever is higher.
\(^{(3)}\) If \( V_{IN} \) and \( V_{BIAS} \) are connected to the same supply, the recommended minimum capacitor for the supply is 4.7 μF.
6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TPS74901</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RGW (VQFN)</td>
</tr>
<tr>
<td></td>
<td>20 PINS</td>
</tr>
<tr>
<td>$R_{JA}$ Junction-to-ambient thermal resistance</td>
<td>38.1</td>
</tr>
<tr>
<td>$R_{JUC(top)}$ Junction-to-case (top) thermal resistance</td>
<td>36.3</td>
</tr>
<tr>
<td>$R_{JB}$ Junction-to-board thermal resistance</td>
<td>17.5</td>
</tr>
<tr>
<td>$\psi_{JT}$ Junction-to-top characterization parameter</td>
<td>0.7</td>
</tr>
<tr>
<td>$\psi_{JB}$ Junction-to-board characterization parameter</td>
<td>17.6</td>
</tr>
<tr>
<td>$R_{JUC(bot)}$ Junction-to-case (bottom) thermal resistance</td>
<td>6.2</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
### 6.5 Electrical Characteristics

At \( T_J = -40°C \) to 125°C, \( V_{EN} = 1.1 \) V, \( V_{IN} = V_{OUT} + 0.3 \) V, \( C_{BIAS} = 0.1 \) \( \mu \)F, \( C_{IN} = C_{OUT} = 10 \) \( \mu \)F, \( C_{NR} = 1 \) nF, \( I_{OUT} = 50 \) mA, and \( V_{BIAS} = 5 \) V, unless otherwise noted. Typical values are at \( T_J = 25°C \).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IN} )</td>
<td>Input voltage</td>
<td>( V_{OUT} + V_{DO} )</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{BIAS} )</td>
<td>Bias pin voltage</td>
<td>2.7</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{REF} )</td>
<td>Internal reference (Adj.)</td>
<td>( T_J = 25°C )</td>
<td>0.798</td>
<td>0.802</td>
<td>0.806</td>
</tr>
<tr>
<td>( V_{OUT} )</td>
<td>Output voltage</td>
<td>( V_{IN} = 5 ) V, ( I_{OUT} = 3 ) A</td>
<td>( V_{REF} )</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>( V_{DO} )</td>
<td>( V_{IN} = 5 ) V, ( I_{OUT} = 3 ) A</td>
<td>( V_{OUT} + 2.2 ) V ( \leq ) ( V_{BIAS} \leq 5.5 ) V, ( 50 ) mA ( \leq ) ( I_{OUT} \leq 3 ) A</td>
<td>( -2% )</td>
<td>( \pm 0.5% )</td>
<td>2%</td>
</tr>
<tr>
<td>( I_{OUT} )</td>
<td></td>
<td></td>
<td>( -2% )</td>
<td>( \pm 0.5% )</td>
<td>2%</td>
</tr>
<tr>
<td>( V_{OUT}/V_{IN} )</td>
<td>Line regulation</td>
<td>( V_{OUT} ) ( \leq 0.3 \leq V_{IN} \leq 5.5 ) V</td>
<td>0.03</td>
<td>%/V</td>
<td></td>
</tr>
<tr>
<td>( V_{DO} )</td>
<td>Load regulation</td>
<td>( 50 ) mA ( \leq ) ( I_{OUT} \leq 3 ) A</td>
<td>0.09</td>
<td>%/A</td>
<td></td>
</tr>
<tr>
<td>( V_{DO} )</td>
<td>( V_{DO} )</td>
<td>( V_{IN} = 5 ) V, ( I_{OUT} = 3 ) A, ( V_{BIAS} ) = ( V_{OUT} ) ( +0.3 ) V</td>
<td>120</td>
<td>280</td>
<td>mV</td>
</tr>
<tr>
<td>( V_{BIAS} )</td>
<td>( V_{BIAS} )</td>
<td>( V_{OUT} = 3 ) A, ( V_{IN} ) = ( V_{BIAS} )</td>
<td>1.31</td>
<td>1.75</td>
<td>V</td>
</tr>
<tr>
<td>( I_{CL} )</td>
<td>Current limit</td>
<td>( V_{OUT} ) = ( 80% \times V_{OUT} ) (NOM), RGW Package</td>
<td>3.9</td>
<td>4.6</td>
<td>5.5</td>
</tr>
<tr>
<td>( I_{BIAS} )</td>
<td>Bias pin current</td>
<td></td>
<td></td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>( I_{SHDN} )</td>
<td>Shutdown supply current ( (I_{GND}) )</td>
<td>( V_{EN} ) ( \leq 0.4 ) V</td>
<td>1</td>
<td>50</td>
<td>( \mu )A</td>
</tr>
<tr>
<td>( I_{FB} )</td>
<td>Feedback pin current</td>
<td>( V_{OUT} ) ( \leq 3 ) A</td>
<td>( -1 )</td>
<td>0.150</td>
<td>1</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power-supply rejection ( (V_{IN} ) to ( V_{OUT} ) )</td>
<td>1 kHz, ( I_{OUT} = 1.5 ) A, ( V_{IN} ) = 1.8 V, ( V_{OUT} ) = 1.5 V</td>
<td>60</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>300 kHz, ( I_{OUT} = 1.5 ) A, ( V_{IN} ) = 1.8 V, ( V_{OUT} ) = 1.5 V</td>
<td>30</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Noise</td>
<td>Output noise voltage</td>
<td>100 Hz to 100 kHz, ( I_{OUT} = 3 ) A, ( C_{SS} ) = 0.001 ( \mu )F</td>
<td>( 25 \times V_{OUT} )</td>
<td>( \mu )V_{RMS}</td>
<td></td>
</tr>
<tr>
<td>( I_{STR} )</td>
<td>Minimum start-up time</td>
<td>( R_{LOAD} ) for ( I_{OUT} ) = 1 A, ( C_{SS} ) = open</td>
<td>200</td>
<td>( \mu )s</td>
<td></td>
</tr>
<tr>
<td>( I_{SS} )</td>
<td>Soft-start charging current</td>
<td>( V_{SS} ) = 0.4 V</td>
<td>440</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>( V_{EN, HI} )</td>
<td>Enable input high level</td>
<td></td>
<td>1.1</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>( V_{EN, LO} )</td>
<td>Enable input low level</td>
<td></td>
<td>0</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>( V_{EN, HYS} )</td>
<td>Enable pin hysteresis</td>
<td></td>
<td>50</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( V_{EN, DG} )</td>
<td>Enable pin deglitch time</td>
<td></td>
<td>20</td>
<td>( \mu )s</td>
<td></td>
</tr>
<tr>
<td>( I_{EN} )</td>
<td>Enable pin current</td>
<td>( V_{EN} ) ( = 5 ) V</td>
<td>0.1</td>
<td>1</td>
<td>( \mu )A</td>
</tr>
<tr>
<td>( V_{IT} )</td>
<td>PG trip threshold</td>
<td>( V_{OUT} ) decreasing</td>
<td>85</td>
<td>90</td>
<td>94</td>
</tr>
<tr>
<td>( V_{HYS} )</td>
<td>PG trip hysteresis</td>
<td></td>
<td>3</td>
<td>%( V_{OUT} )</td>
<td></td>
</tr>
<tr>
<td>( V_{PG, LO} )</td>
<td>PG output low voltage</td>
<td>( I_{PG} ) = 1 mA (sinking), ( V_{OUT} &lt; V_{IT} )</td>
<td>0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{PG, LKG} )</td>
<td>PG leakage current</td>
<td>( V_{PG} ) = 5.25 V, ( V_{OUT} &gt; V_{IT} )</td>
<td>0.1</td>
<td>1</td>
<td>( \mu )A</td>
</tr>
<tr>
<td>( T_J )</td>
<td>Operating junction temperature</td>
<td></td>
<td>( -40 )</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>( T_{SD} )</td>
<td>Thermal shutdown temperature</td>
<td>Shutdown, temperature increasing</td>
<td>165</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Reset, temperature decreasing</td>
<td>140</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

(1) Adjustable devices tested at 0.8 V; resistor tolerance is not considered.
(2) Dropout is defined as the voltage from \( V_{IN} \) to \( V_{OUT} \) when \( V_{OUT} \) is 3% below nominal.
(3) 3.25 V is a test condition of this device and can be adjusted by referring to Figure 6.
6.6 Typical Characteristics: \( I_{\text{OUT}} = 50 \text{ mA} \)

At \( T_J = 25^\circ\text{C}, V_{\text{IN}} = V_{\text{OUT(TYP)}} + 0.3 \text{ V}, V_{\text{BIAS}} = 5 \text{ V}, I_{\text{OUT}} = 50 \text{ mA}, V_{\text{EN}} = V_{\text{IN}}, C_{\text{IN}} = 1 \mu\text{F}, C_{\text{BIAS}} = 4.7 \mu\text{F}, \) and \( C_{\text{OUT}} = 10 \mu\text{F}, \) unless otherwise noted.

![Figure 1. \( V_{\text{IN}} \) Line Regulation](image1)

![Figure 2. \( V_{\text{BIAS}} \) Line Regulation](image2)

![Figure 3. Load Regulation](image3)

![Figure 4. Load Regulation](image4)

![Figure 5. \( V_{\text{IN}} \) Dropout Voltage vs \( I_{\text{OUT}} \) and Temperature (\( T_J \))](image5)

![Figure 6. \( V_{\text{IN}} \) Dropout Voltage vs \( V_{\text{IN}} \) Dropout Voltage vs \( I_{\text{OUT}} \) and Temperature (\( T_J \))](image6)
Typical Characteristics: $I_{\text{OUT}} = 50$ mA (continued)

At $T_J = 25^\circ C$, $V_{\text{IN}} = V_{\text{OUT (TYP)}} + 0.3$ V, $V_{\text{BIAS}} = 5$ V, $I_{\text{OUT}} = 50$ mA, $V_{\text{EN}} = V_{\text{IN}}$, $C_{\text{IN}} = 1$ $\mu$F, $C_{\text{BIAS}} = 4.7$ $\mu$F, and $C_{\text{OUT}} = 10$ $\mu$F, unless otherwise noted.
Typical Characteristics: $I_{OUT} = 50 \text{ mA}$ (continued)

At $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(\text{TYP})} + 0.3 \text{ V}$, $V_{BIAS} = 5 \text{ V}$, $I_{OUT} = 50 \text{ mA}$, $V_{EN} = V_{IN}$, $C_{IN} = 1 \mu\text{F}$, $C_{BIAS} = 4.7 \mu\text{F}$, and $C_{OUT} = 10 \mu\text{F}$, unless otherwise noted.

Figure 13. BIAS Pin Current vs $I_{OUT}$ and Temperature ($T_J$)

Figure 14. BIAS Pin Current vs $V_{BIAS}$ and Temperature ($T_J$)

Figure 15. Soft-Start Charging Current ($I_{SS}$) vs Temperature ($T_J$)

Figure 16. Low-Level PG Voltage vs Current

Figure 17. Current Limit vs ($V_{BIAS} - V_{OUT}$)
6.7 Typical Characteristics: $I_{OUT} = 1$ A

At $T_J = 25°C$, $V_{IN} = V_{OUT(TYP)} + 0.3$ V, $V_{BIAS} = 5$ V, $I_{OUT} = 1$ A, $V_{EN} = V_{IN} = 1.8$ V, $V_{OUT} = 1.5$ V, $C_{IN} = 1$ µF, $C_{BIAS} = 4.7$ µF, and $C_{OUT} = 10$ µF, unless otherwise noted.

**Figure 18. $V_{BIAS}$ Line Transient**

**Figure 19. $V_{IN}$ Line Transient**

**Figure 20. Output Load Transient Response**

**Figure 21. Turnon Response**

**Figure 22. Power Up and Power Down**
7 Detailed Description

7.1 Overview
The TPS74901 belongs to a family of low-dropout regulators that feature soft-start capabilities. These regulators use a low-current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very-low input and output voltages.

The use of an NMOS-pass FET offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS74901 to be stable with any capacitor with a value of 2.2 µF or greater. Transient response is also superior to PMOS topologies, particularly for low \( V_{\text{IN}} \) applications.

The TPS74901 features a programmable voltage-controlled soft-start circuit that provides a smooth, monotonic start-up and limits start-up inrush currents that may be caused by large capacitive loads. A power-good (PG) output is available to allow supply monitoring and sequencing of other supplies. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low \( V_{\text{IN}} \) and \( V_{\text{OUT}} \) capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often present in processor-intensive systems.

7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 Enable and Shutdown
The enable (EN) pin is active high and is compatible with standard digital-signaling levels. \( V_{\text{EN}} \) below 0.4 V turns the regulator off and \( V_{\text{EN}} \) above 1.1 V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slowly ramping analog signals. This configuration allows the TPS74901 to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50 mV of hysteresis and a deglitch circuit to help avoid ON-OFF cycling because of small glitches in the \( V_{\text{EN}} \) signal.

The enable threshold is typically 0.8 V and varies with temperature and process variations. Temperature variation is approximately \(-1\) mV/°C; process variation accounts for most of the rest of the variation to the 0.4-V and 1.1-V limits. If precise turnon timing is required, a fast rise-time signal must be used to enable the TPS74901.
Feature Description (continued)

If not used, EN can be connected to either IN or BIAS. If EN is connected to IN, then connect EN as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

7.3.2 Power-Good

The power-good (PG) pin is an open-drain output and can be connected to any 5.5 V or lower rail through an external pullup resistor. This pin requires at least 1.1 V on \( V_{\text{BIAS}} \) to have a valid output. The PG output is high-impedance when \( V_{\text{OUT}} \) is greater than \( V_{\text{IT}} + V_{\text{HYS}} \). If \( V_{\text{OUT}} \) drops below \( V_{\text{IT}} \) or if \( V_{\text{BIAS}} \) drops below 1.9 V, the open-drain output turns on and pulls the PG output low. The PG pin also asserts when the device is disabled. The recommended operating condition of PG pin sink current is up to 1 mA, so the pullup resistor for PG must be in the range of 10 k\( \Omega \) to 1 M\( \Omega \). PG is only provided on the VQFN package. If output voltage monitoring is not needed, the PG pin can be left floating.

7.3.3 Internal Current Limit

The TPS74901 features a factory-trimmed, accurate current limit that is flat over temperature and supply voltage. The current limit allows the device to supply surges of up to 4 A and maintain regulation. The current limit responds in about 10 \( \mu \)s to reduce the current during a short circuit fault.

The internal current limit protection circuitry of the TPS74901 is designed to protect against overload conditions. This circuitry is not intended to allow operation above the rated current of the device. Continuously running the TPS74901 above the rated current degrades device reliability.

7.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature the thermal protection circuit may cycle ON and OFF. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 40°C above the maximum expected ambient condition of the application. This condition produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS74901 is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS74901 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage and bias voltage are both at least at the respective minimum specifications.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.
Device Functional Modes (continued)

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:
• The input or bias voltages are below the respective minimum specifications.
• The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
• The device junction temperature is greater than the thermal shutdown temperature.

Table 1 lists the conditions that lead to the different modes of operation.

<table>
<thead>
<tr>
<th>OPERATING MODE</th>
<th>PARAMETER</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>V_IN</td>
</tr>
<tr>
<td>Normal mode</td>
<td>V_IN &gt; V_OUT(nom) + V_DO(V_IN)</td>
</tr>
<tr>
<td>Dropout mode</td>
<td>V_IN &lt; V_OUT(nom) + V_DO(V_IN)</td>
</tr>
<tr>
<td>Disabled mode (any true condition disables the device)</td>
<td>V_EN &lt; V_EN(low)</td>
</tr>
</tbody>
</table>

Table 1. Device Functional Mode Comparison
8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input, Output, and BIAS Capacitor Requirements

The device is designed to be stable for all available types and values of output capacitors ≥ 2.2 µF. The device is also stable with multiple capacitors in parallel, which can be of any type or value.

The capacitance required on the IN and BIAS pin strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for $V_{IN}$ and $V_{BIAS}$ is 1 µF. If $V_{IN}$ and $V_{BIAS}$ are connected to the same supply, the recommended minimum capacitor for $V_{BIAS}$ is 4.7 µF. Good quality, low-ESR capacitors must be used on the input; ceramic X5R and X7R capacitors are preferred. These capacitors must be placed as close as possible to the pins for optimum performance.

8.1.2 Transient Response

The TPS74901 is designed to have excellent transient response for most applications with a small amount of output capacitance. In some cases, the transient response may be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300 mV. In this case, adding additional input capacitance improves the transient response much more than just adding additional output capacitance would do. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient event; see Figure 20 in the Typical Characteristics: $I_{OUT} = 50 mA$ section. Because the TPS74901 is stable with output capacitors as low as 2.2 µF, many applications may need very little capacitance at the LDO output. For these applications, local bypass capacitance for the powered device may be sufficient to meet the transient requirements of the application. This design reduces the total solution cost by avoiding the need to use expensive high-value capacitors at the LDO output.

8.1.3 Dropout Voltage

The TPS74901 offers very low dropout performance, making the device well-suited for high-current low $V_{IN}$ and low $V_{OUT}$ applications. The low dropout of the TPS74901 allows the device to be used in place of a DC-DC converter and still achieve good efficiencies. This provides designers with the power architecture for their applications to achieve the smallest, simplest, and lowest-cost solution.

There are two different specifications for dropout voltage with the TPS74901. The first specification (see Figure 23) is referred to as $V_{IN}$ Dropout and is used when an external bias voltage is applied to achieve low dropout. This specification assumes that $V_{BIAS}$ is at least 3.25 V above $V_{OUT}$, which is the case for $V_{BIAS}$ when powered by a 5-V rail with 5% tolerance and with $V_{OUT} = 1.5 V$ (3.25 V is a test condition of this device and can be adjusted by referring to Figure 6). If $V_{BIAS}$ is higher than $V_{OUT} + 3.25 V$, $V_{IN}$ dropout is less than specified.
Application Information (continued)

![Simplified Block Diagram](image)

**Figure 23. Typical Application of the TPS74901 Using an Auxiliary Bias Rail**

The second specification (shown in Figure 24) is referred to as $V_{BIAS}$ Dropout and applied to applications where IN and BIAS are tied together. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because $V_{BIAS}$ provides the gate drive to the pass FET; therefore, $V_{BIAS}$ must be 1.75 V above $V_{OUT}$. Dropout is limited by BIAS in these applications because $V_{BIAS}$ provides the gate drive to the pass FET; therefore, $V_{BIAS}$ must be 1.75 V above $V_{OUT}$. Because of this usage, IN and BIAS tied together easily consume huge power. Pay attention not to exceed the power rating of the IC package.

![Simplified Block Diagram](image)

**Figure 24. Typical Application of the TPS74901 Without an Auxiliary Bias**

### 8.1.4 Output Noise

The TPS74901 provides low-output noise when a soft start capacitor is used. When the device reaches the end of the soft start cycle, the soft start capacitor serves as a filter for the internal reference. By using a 0.001-$\mu$F soft start capacitor, the output noise is reduced by half and is typically 30 $\mu$V$_{RMS}$ for a 1.2-V output (10 Hz to 100 kHz). Further increasing $C_{SS}$ has little effect on noise. Because most of the output noise is generated by the internal reference, the noise is a function of the set output voltage. The RMS noise with a 0.001-$\mu$F soft-start capacitor is given in Equation 1.

$$V_{N(\mu V_{RMS})} = 25 \left( \frac{\mu V_{RMS}}{V} \right) \times V_{OUT}(V)$$  \hspace{1cm} (1)

The low-output noise of the TPS74901 makes the device a good choice for powering transceivers, PLLs, or other noise-sensitive circuitry.
Application Information (continued)

8.1.5 Programmable Soft Start

The TPS74901 features a programmable, monotonic, voltage-controlled soft start that is set with an external capacitor (C_SS). This feature is important for many applications because power-up initialization problems are eliminated when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus.

To achieve a linear and monotonic soft start, the TPS74901 error amplifier tracks the voltage ramp of the external soft start capacitor until the voltage exceeds the internal reference. The soft start ramp time is dependent on the soft start charging current (I_SS), soft start capacitance (C_SS), and the internal reference voltage (V_REF), and can be calculated using Equation 2.

\[
t_{SS} = \frac{(V_{REF} \times C_{SS})}{I_{SS}}
\]  

(2)

If large output capacitors are used, the device current limit (I_CL) and the output capacitor may set the start-up time. In this case, the start-up time is given by Equation 3:

\[
t_{SSCL} = \frac{(V_{OUT\,NOM} \times C_{OUT})}{I_{CL\,(MIN)}}
\]

where

- \( V_{OUT\,NOM} \) is the nominal set output voltage.
- \( C_{OUT} \) is the output capacitance.
- \( I_{CL\,(MIN)} \) is the minimum current limit for the device.

(3)

In applications where monotonic start-up is required, the soft start time given by Equation 2 must be set to be greater than Equation 3.

The maximum recommended soft start capacitor is 0.015 µF. Larger soft start capacitors can be used and do not damage the device; however, the soft start capacitor discharge circuit may not be able to fully discharge the soft start capacitor when enabled. Soft start capacitors larger than 0.015 µF could be a problem in applications where the user must rapidly pulse the enable pin and still requires the device to soft start from ground. C_SS must be low-leakage; X7R, X5R, or C0G dielectric materials are preferred. See Table 2 for suggested soft-start capacitor values.

Table 2. Standard Capacitor Values for Programming the Soft-Start Time\(^{(1)}\)

<table>
<thead>
<tr>
<th>C_SS</th>
<th>SOFT START TIME</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open</td>
<td>0.1 ms</td>
</tr>
<tr>
<td>270 pF</td>
<td>0.5 ms</td>
</tr>
<tr>
<td>560 pF</td>
<td>1 ms</td>
</tr>
<tr>
<td>2.7 nF</td>
<td>5 ms</td>
</tr>
<tr>
<td>5.6 nF</td>
<td>10 ms</td>
</tr>
<tr>
<td>0.01 µF</td>
<td>18 ms</td>
</tr>
</tbody>
</table>

\[
t_{SS}(s) = \frac{V_{REF} \times C_{SS}}{I_{SS}} = \frac{0.8V \times C_{SS}(F)}{0.44\mu A}
\]

where \( t_{SS}(s) \) = soft-start time in seconds.

\(^{(1)}\) where \( t_{SS}(s) \) = soft-start time in seconds.
8.1.6 Sequencing Requirements

$V_{IN}$, $V_{BIAS}$, and $V_{EN}$ can be sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Connecting $EN$ to $IN$ is acceptable for most applications as long as $V_{IN}$ is greater than 1.1 V, and the ramp rate of $V_{IN}$ and $V_{BIAS}$ is faster than the set soft start ramp rate. If the ramp rate of the input sources is slower than the set soft start time, the output tracks the slower supply minus the dropout voltage until the set output voltage is reached. If $EN$ is connected to $BIAS$, the device soft-starts as programmed, provided that $V_{IN}$ is present before $V_{BIAS}$. If $V_{BIAS}$ and $V_{EN}$ are present before $V_{IN}$ is applied and the set soft start time has expired, then $V_{OUT}$ tracks $V_{IN}$. If the soft start time has not expired, the output tracks $V_{IN}$ until $V_{OUT}$ reaches the value set by the charging soft start capacitor. Figure 25 shows the use of an RC-delay circuit to hold off $V_{EN}$ until $V_{BIAS}$ has ramped. This technique can also be used to drive $EN$ from $V_{IN}$. An external control signal can also be used to enable the device after $V_{IN}$ and $V_{BIAS}$ are present.

**NOTE**

When $V_{BIAS}$ and $V_{EN}$ are present and $V_{IN}$ is not supplied, this device outputs approximately 50 $\mu$A of current from $OUT$. Although this condition will not cause any damage to the device, the output current may charge up the $OUT$ node if total resistance between $OUT$ and GND (including external feedback resistors) is greater than 10 kΩ.

![Figure 25. Soft-Start Delay Using an RC Circuit on Enable](image-url)
8.2 Typical Application

Figure 26 illustrates the typical application circuit for the TPS74901 adjustable output device. R1 and R2 can be calculated for any output voltage using the formula shown in Figure 26. See Table 3 for sample resistor values of common output voltages. To achieve the maximum accuracy specifications, R2 must be \( \leq 4.99 \text{ k}\Omega \).

\[
V_{\text{OUT}} = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)
\]

Figure 26. Typical Application Circuit for the TPS74901 (Adjustable)

Table 3. Standard 1\% Resistor Values for Programming the Output Voltage\(^{(1)}\)

<table>
<thead>
<tr>
<th>( R_1 (\text{k}\Omega) )</th>
<th>( R_2 (\text{k}\Omega) )</th>
<th>( V_{\text{OUT}} ) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Short</td>
<td>Open</td>
<td>0.8</td>
</tr>
<tr>
<td>0.619</td>
<td>4.99</td>
<td>0.9</td>
</tr>
<tr>
<td>1.13</td>
<td>4.53</td>
<td>1</td>
</tr>
<tr>
<td>1.37</td>
<td>4.42</td>
<td>1.05</td>
</tr>
<tr>
<td>1.87</td>
<td>4.99</td>
<td>1.1</td>
</tr>
<tr>
<td>2.49</td>
<td>4.99</td>
<td>1.2</td>
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<tr>
<td>4.12</td>
<td>4.75</td>
<td>1.5</td>
</tr>
<tr>
<td>3.57</td>
<td>2.87</td>
<td>1.8</td>
</tr>
<tr>
<td>3.57</td>
<td>1.69</td>
<td>2.5</td>
</tr>
<tr>
<td>3.57</td>
<td>1.15</td>
<td>3.3</td>
</tr>
</tbody>
</table>

\(^{(1)}\) \( V_{\text{OUT}} = 0.8 \times \left(1 + \frac{R_1}{R_2}\right) \)

8.2.1 Design Requirements

The goal of this design is to create a 1.2-V rail at 3 A with minimal external components from a 1.5-V rail.

8.2.2 Detailed Design Procedure

First choose the bias, which must be at least 1.75-V above the output voltage. A 3.3-V rail is used to achieve this minimum voltage. For a minimal external component count and size, select the minimum capacitor sizes. \( C_{\text{IN}} = 1 \mu\text{F}, C_{\text{BIAS}} = 1 \mu\text{F}, \) and a \( C_{\text{OUT}} = 10 \mu\text{F} \). The \( C_{\text{OUT}} \) value was chosen to improve transient response. Using Table 3, R1 is set to 2.49 k\Omega and R2 is set to 4.99 k\Omega to create a 1.2-V rail. The pullup resistor for PG is set to 10 k\Omega.
8.2.3 Application Curves

![Figure 27. VIN PSRR vs (VIN - VOUT)](image)

![Figure 28. Noise Spectral Density](image)

9 Power Supply Recommendations

The TPS74901 is designed to operate from an input voltage from 1.1 V to 5.5 V, provided the bias rail is at least 1.75-V higher than the input supply. The bias rail and the input supply must both provide adequate headroom and current for the device to operate normally.

Connect a low-output impedance power supply directly to the IN pin of the TPS74901. This supply must have at least 1 µF of capacitance near the IN pin for stability. A supply with similar requirements must also be connected directly to the bias rail with a separate 1-µF or larger capacitor.

If the IN pin is tied to the bias pin, a minimum 4.7 µF of capacitance is needed for stability.

To increase the overall PSRR of the solution at higher frequencies, use a PI-filter or ferrite bead before the input capacitor.
10 Layout

10.1 Layout Guidelines

An optimal layout can greatly improve transient performance, PSRR, and noise. To minimize the voltage droop on the input of the device during load transients, connect the capacitance on IN and BIAS as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can therefore improve stability. To achieve optimal transient performance and accuracy, connect the top side of R1 in Figure 26 as close as possible to the load. If BIAS is connected to IN, TI recommends connecting BIAS as close to the sense point of the input supply as possible. This connection minimizes the voltage droop on BIAS during transient conditions and can improve the turnon response.

10.2 Layout Example

![Layout Schematic (RGW Package)](image)

Keep the ground planes on the same side of the PCB if possible to improve thermal dissipation.

10.3 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

Power dissipation of the device depends on input voltage and load conditions, and can be calculated using Equation 4:

\[ P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \]
Power Dissipation (continued)

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the VQFN (RGW) package, the primary conduction path for heat is through the exposed pad to the PCB. The pad can be connected to ground or left floating; however, the pad must be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. On the DDPAK (KTW) package, the primary conduction path for heat is through the tab to the PCB. Connect that tab to ground. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be estimated using Equation 5:

\[ R_{\theta JA} = \frac{(+125^\circ C - T_A)}{P_D} \]  

(5)

Knowing the maximum \( R_{\theta JA} \), the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 30.

**Figure 30. \( \theta_{JA} \) versus Board Size**

Figure 30 shows the variation of \( \theta_{JA} \) as a function of ground plane copper area in the board. Figure 30 is intended only as a guideline to demonstrate the affects of heat spreading in the ground plane; do not use Figure 30 to estimate actual thermal performance in real application environments.

**NOTE**

When the device is mounted on an application PCB, TI strongly recommends using \( \Psi_{JT} \) and \( \Psi_{JB} \), as explained in the section.

### 10.4 Thermal Considerations

A better method of estimating the thermal measure comes from using the thermal metrics \( \Psi_{JT} \) and \( \Psi_{JB} \), as shown in Equation 6. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than \( R_{\theta JA} \). The junction temperature can be estimated with the corresponding formulas given in Equation 6.

\[ \Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \cdot P_D \]

\[ \Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \cdot P_D \]

where

- \( P_D \) is the power dissipation shown by Equation 4
- \( T_T \) is the temperature at the center-top of the IC package
- \( T_B \) is the PCB temperature measured 1 mm away from the IC package on the PCB surface (see Figure 31)
Thermal Considerations (continued)

**NOTE**
Both \( T_T \) and \( T_B \) can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring \( T_T \) and \( T_B \), see the application note *Using New Thermal Metrics (SBVA025)*, available for download at www.ti.com.

---

(a) Example RGW (VQFN) Package Measurement
(b) Example KTW (DDPAK) Package Measurement

(1) \( T_T \) is measured at the center of both the X- and Y-dimensional axes.
(2) \( T_B \) is measured below the package lead on the PCB surface.

**Figure 31. Measuring Points for \( T_T \) and \( T_B \)**
Compared with $\theta_{JA}$, the thermal metrics $\Psi_{JT}$ and $\Psi_{JB}$ are less independent of board size but do have a small dependency on board size and layout. Figure 32 shows characteristic performance of $\Psi_{JT}$ and $\Psi_{JB}$ versus board size.

Referring to Figure 32, the RGW package thermal performance has negligible dependency on board size. The KTW package, however, does have a measurable dependency on board size. This dependency exists because the package shape is not point symmetric to an IC center. In the KTW package, for example (see Figure 31), silicon is not beneath the measuring point of $T_T$ which is the center of the X and Y dimension, so that $\Psi_{JT}$ has a dependency. Also, because of that non-point symmetry, device heat distribution on the PCB is not point symmetric either, so that $\Psi_{JB}$ has a greater dependency on board size and layout.

![Figure 32. $\Psi_{JT}$ and $\Psi_{JB}$ versus Board Size](image)

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see the application note Using New Thermal Metrics (SBVA025), available for download at www.ti.com. Also, see the application note IC Package Thermal Metrics (SPRA953) (also available on the TI website) for further information.
11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules
An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS48. The TPS74901EVM-210 evaluation module and related user's guide (SLVU190) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models
Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS748 is available through the product folders under Tools & Software.

11.2 Documentation Support

11.2.1 Related Documentation
For related documentation, see the following:
• Using New Thermal Metrics, SBVA025
• IC Package Thermal Metrics, SPRA953
• Ultimate Regulation of with Fixed Output Versions of the TPS742xx, TPS743xx, and TPS744xx, SBVA024
• Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator, SBVA042
• TPS74901EVM-210 Evaluation Module User Guide, SLVU190

11.3 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks
E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS74901DRCR</td>
<td>ACTIVE</td>
<td>VSON</td>
<td>DRC</td>
<td>10</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>11S</td>
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<td>11S</td>
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<tr>
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<td>KTW</td>
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<td>500</td>
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<td>Call TI</td>
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<td>TPS74901</td>
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</tbody>
</table>

### Notes:

1. The marketing status values are defined as follows:
   - **ACTIVE:** Product device recommended for new designs.
   - **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
   - **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
   - **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
   - **OBSOLETE:** TI has discontinued the production of the device.

2. **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
   - **RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
   - **Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

3. **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

4. There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

5. Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
### TAPE AND REEL INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
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<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*

**TAPE DIMENSIONS**
- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**
- **Q1**: Pocket Quadrant
- **Q2**: Sprocket Holes
- **Q3**: User Direction of Feed
- **Q4**: Reel Diameter

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*Xtended Information*

*Xtended Information*

*All dimensions are nominal.*
<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
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<th>Width (mm)</th>
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<td>35.0</td>
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</table>

*All dimensions are nominal*
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flat pack, No-leads (QFN) package configuration
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-220.
THERMAL PAD MECHANICAL DATA

RGW (S-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

![Exposed Thermal Pad Dimensions](image_url)

NOTE: All linear dimensions are in millimeters
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com (http://www.ti.com).
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
MECHANICAL DATA

KTW (R-PSFM-G7) PLASTIC FLANGE-MOUNT

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead width and height dimensions apply to the plated lead.
D. Leads are not allowed above the Datum B.
E. Stand-off height is measured from lead tip with reference to Datum B.
F. Lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum dimension by more than 0.003”.
G. Cross-hatch indicates exposed metal surface.
H. Falls within JEDEC MO-169 with the exception of the dimensions indicated.
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