TPS75003 Configurable Multirail PMIC

1 Features
- Two 95% Efficient, 3A Buck Controllers and One 300mA LDO
- Tested and Endorsed by Xilinx for Powering the Spartan™-3, Spartan-3E and Spartan-3L FPGAs
- Adjustable (1.2V to 6.5V for Bucks, 1.0V to 6.5V for LDO) Output Voltages on All Channels
- Input Voltage Range: 2.2V to 6.5V
- Independent Soft-Start for Each Supply
- Independent Enable for Each Supply for Flexible Sequencing
- LDO Stable with 2.2μF Ceramic Output Capacitor
- Small, Low-Profile 4.5mm × 3.5mm × 0.9mm VQFN Package

2 Applications
- FPGA, DSP, and ASIC Supplies
- Set-Top Boxes
- DSL Modems
- Plasma TV Display Panels

3 Description
The TPS75003 is a complete power management solution for FPGA, DSP and other multi-supply applications. The device has been tested with and meets all of the Xilinx Spartan-3, Spartan-3E, and Spartan-3L start-up profile requirements, including monotonic voltage ramp and minimum voltage-rail rise time. Independent enables for each output allow sequencing to minimize demand on the power supply at start-up. Soft-start on each supply limits inrush current during start-up. Two integrated buck controllers allow efficient, cost-effective voltage conversion for both low and high current supplies such as core and I/O. A 300-mA LDO is integrated to provide an auxiliary rail such as V_CCAUX on the Xilinx Spartan-3 FPGA. All three output voltages are externally configurable for maximum flexibility.

The TPS75003 is fully specified from –40°C to +85°C and is offered in a VQFN package, yielding a highly compact total solution size with high power dissipation capability.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS75003</td>
<td>VQFN (20)</td>
<td>4.50 mm × 3.50 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
Table of Contents

1 Features ................................................................. 1
2 Applications ........................................................... 1
3 Description ............................................................. 1
4 Revision History ....................................................... 2
5 Pin Configuration and Functions ................................. 3
6 Specifications .......................................................... 4
  6.1 Absolute Maximum Ratings ....................................... 4
  6.2 ESD Ratings .......................................................... 4
  6.3 Recommended Operating Conditions ......................... 4
  6.4 Thermal Information ................................................ 5
  6.5 Electrical Characteristics .......................................... 5
  6.6 Typical Characteristics ............................................ 6
7 Detailed Description .................................................. 10
  7.1 Overview ............................................................. 10
  7.2 Functional Block Diagram ......................................... 11
  7.3 Feature Description ................................................ 11
8 Application and Implementation .................................... 15
  8.1 Application Information ........................................... 15
  8.2 Typical Application ................................................. 16
9 Power Supply Recommendations .................................... 22
10 Layout ................................................................. 23
  10.1 Layout Guidelines .................................................. 23
  10.2 Layout Example .................................................... 24
11 Device and Documentation Support ............................... 25
  11.1 Device Support ..................................................... 25
  11.2 Documentation Support .......................................... 25
  11.3 Receiving Notification of Documentation Updates .......... 25
  11.4 Community Resources ........................................... 25
  11.5 Trademarks ........................................................ 25
  11.6 Electrostatic Discharge Caution ................................. 25
  11.7 Glossary ........................................................... 25
12 Mechanical, Packaging, and Orderable Information ............ 26

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (August 2010) to Revision J

Page

• Changed the title of the data sheet and updated the format to the latest TI data sheet format ........................................... 1
• Moved the ESD rating parameters for HBM and CDM from the Absolute Maximum Ratings table to the ESD Ratings table .................................................. 4
• Added the Recommended Operating Conditions table, Overview section, Feature Description section, Design Requirements section, Power Supply Recommendations section, and Device and Documentation Support section ........ 4
• Updated the symbols for the thermal resistance parameters in the Thermal Information table............................................. 5

Changes from Revision H (August 2008) to Revision I

Page

• Replaced the Dissipation Ratings table with the Thermal Information table ................................................................. 5
## 5 Pin Configuration and Functions

### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>AGND</td>
<td>18</td>
<td>GND Ground connection for LDO.</td>
</tr>
<tr>
<td>DGND</td>
<td>6, 15, PAD</td>
<td>GND Ground connection for BUCK1 and BUCK2 converters. Pins 6 and 15 should be connected to the back side exposed pad by a short metal trace as shown in the PCB Layout Considerations section of this data sheet.</td>
</tr>
<tr>
<td>EN1</td>
<td>17</td>
<td>I Driving the enable pin (ENx) high turns on BUCK1 regulator. Driving this pin low puts it into shutdown mode, reducing operating current. The enable pin does not trigger on fast negative going transients.</td>
</tr>
<tr>
<td>EN2</td>
<td>4</td>
<td>I Same as EN1 but for BUCK2 controller.</td>
</tr>
<tr>
<td>EN3</td>
<td>3</td>
<td>I Same as EN1 but for LDO.</td>
</tr>
<tr>
<td>FB1</td>
<td>11</td>
<td>I (Analog) Feedback pin. Used to set the output voltage of BUCK1 regulator.</td>
</tr>
<tr>
<td>FB2</td>
<td>10</td>
<td>I (Analog) Same as FB1 but for BUCK2 controller.</td>
</tr>
<tr>
<td>FB3</td>
<td>2</td>
<td>I (Analog) Same as FB1 but for LDO.</td>
</tr>
<tr>
<td>IN1</td>
<td>13</td>
<td>I (Analog) Input supply to BUCK1.</td>
</tr>
<tr>
<td>IN2</td>
<td>8</td>
<td>I (Analog) Input supply to BUCK2.</td>
</tr>
<tr>
<td>IN3</td>
<td>20</td>
<td>I (Power) Input supply to LDO.</td>
</tr>
<tr>
<td>IS1</td>
<td>12</td>
<td>I (Analog) Current sense input for BUCK1 regulator. The voltage difference between this pin and IN1 is compared to an internal reference to set current limit. For a robust output start-up ramp, careful layout and bypassing are required. See the Application Information section for details.</td>
</tr>
<tr>
<td>IS2</td>
<td>9</td>
<td>I (Analog) Same as IS1 but compared to IN2 and used for BUCK2 controller.</td>
</tr>
<tr>
<td>OUT3</td>
<td>1</td>
<td>O (Power) Regulated LDO output. A small ceramic capacitor (≥ 2.2 μF) is needed from this pin to ground to ensure stability.</td>
</tr>
<tr>
<td>SS1</td>
<td>16</td>
<td>I (Analog) Connecting a capacitor between this pin and ground increases start-up time of the BUCK1 regulator by slowing the ramp-up of current limit. This high-impedance pin is noise-sensitive; careful layout is important. See the Typical Characteristics, Application Information, and PCB Layout Considerations sections for details.</td>
</tr>
<tr>
<td>SS2</td>
<td>5</td>
<td>I (Analog) Same as SS1 but for BUCK2 regulator.</td>
</tr>
<tr>
<td>SS3</td>
<td>19</td>
<td>I (Analog) Connecting a capacitor from this pin to ground slows the start-up time of the LDO reference, thereby slowing output voltage ramp-up. See the Application Information section for details.</td>
</tr>
<tr>
<td>SW1</td>
<td>14</td>
<td>O (Analog) Gate drive pin for external BUCK1 P-channel MOSFET.</td>
</tr>
<tr>
<td>SW2</td>
<td>7</td>
<td>O (Analog) Same as SW1 but for BUCK2 controller.</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings
Over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{INX}})</td>
<td>(-0.3)</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{ENX}})</td>
<td>(-0.3)</td>
<td>(V_{\text{INX}} + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{SWX}})</td>
<td>(-0.3)</td>
<td>(V_{\text{INX}} + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{ISX}})</td>
<td>(-0.3)</td>
<td>(V_{\text{INX}} + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{OUT3}})</td>
<td>(-0.3)</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{SSX}})</td>
<td>(-0.3)</td>
<td>(V_{\text{INX}} + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{FBX}})</td>
<td>(-0.3)</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td>(I_{\text{OUT3}})</td>
<td>Internally limited</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Junction temperature</td>
<td>(-55)</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under **Recommended Operating Conditions**. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>(V_{\text{ESD}})</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
<td>1000</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(^{(2)})</td>
<td>500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{IN1}})</td>
<td>2.2</td>
<td>6.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{\text{OUT1}})</td>
<td>1.2</td>
<td>(V_{\text{IN1}})</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(I_{\text{OUT1}})</td>
<td>3</td>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{\text{IN2}})</td>
<td>2.2</td>
<td>6.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{\text{OUT2}})</td>
<td>1.2</td>
<td>(V_{\text{IN2}})</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(I_{\text{OUT2}})</td>
<td>3</td>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{\text{IN3}})</td>
<td>2.2</td>
<td>6.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{\text{OUT3}})</td>
<td>1</td>
<td>(V_{\text{IN3}} - V_{\text{DO}})</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(I_{\text{OUT3}})</td>
<td>300</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TPS75003</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{\text{JA}} )</td>
<td>Junction-to-ambient thermal resistance</td>
<td>42.6</td>
</tr>
<tr>
<td>( R_{\text{JUC(top)}} )</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>51.8</td>
</tr>
<tr>
<td>( R_{\text{JUB}} )</td>
<td>Junction-to-board thermal resistance</td>
<td>39.5</td>
</tr>
<tr>
<td>( R_{\text{JT}} )</td>
<td>Junction-to-top characterization parameter</td>
<td>0.6</td>
</tr>
<tr>
<td>( R_{\text{JB}} )</td>
<td>Junction-to-board characterization parameter</td>
<td>14.2</td>
</tr>
<tr>
<td>( R_{\text{JUC(bot)}} )</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>2.8</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

\[ V_{\text{EN1}} = V_{\text{IN1}}, \quad V_{\text{EN2}} = V_{\text{IN2}}, \quad V_{\text{EN3}} = V_{\text{IN3}}, \quad V_{\text{IN1}} = V_{\text{IN2}} = 2.2\,\text{V}, \quad V_{\text{IN3}} = 3.0\,\text{V}, \quad V_{\text{OUT1}} = V_{\text{OUT2}} = 2.5\,\text{V}, \quad C_{\text{OUT1}} = C_{\text{OUT2}} = 47\mu\text{F}, \quad C_{\text{OUT3}} = 2.2\mu\text{F}, \quad T_A = -40°C \text{ to } +85°C, \] unless otherwise noted. Typical values are at \( T_A = +25°C \).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{INX}} )</td>
<td>Input Voltage Range (IN1, IN2, IN3)(1)</td>
<td>2.2</td>
<td>6.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_Q )</td>
<td>Quiescent Current, ( I_Q = I_{\text{DQND}} + I_{\text{DQNG}} )</td>
<td>( I_{\text{OUT1}} = I_{\text{OUT2}} = 0,\text{mA}, \quad I_{\text{OUT3}} = 1,\text{mA} )</td>
<td>75</td>
<td>150</td>
<td>μA</td>
</tr>
<tr>
<td>( I_{\text{ISHDN}} )</td>
<td>Shutdown Supply Current</td>
<td>( V_{\text{EN1}} = V_{\text{EN2}} = V_{\text{EN3}} = 0,\text{V} )</td>
<td>0.05</td>
<td>3</td>
<td>μA</td>
</tr>
<tr>
<td>( V_{\text{IH1}, 2} )</td>
<td>Enable High, enabled (EN1, EN2)</td>
<td>1.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{IH3}} )</td>
<td>Enable High, enabled (EN3)</td>
<td>1.14</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{ILX}} )</td>
<td>Enable Low, shutdown (EN1, EN2, EN3)</td>
<td>0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( I_{\text{ENX}} )</td>
<td>Enable pin current (EN1, EN2, EN3)</td>
<td>0.01</td>
<td>0.5</td>
<td></td>
<td>μA</td>
</tr>
</tbody>
</table>

Buck Controllers 1 and 2

| \( V_{\text{OUT1,2}} \) | Adjustable Output Voltage Range(2) | \( V_{\text{FBX}} \) | \( V_{\text{INX}} \) | V |
| \( V_{\text{FB1,2}} \) | Feedback Voltage (FB1, FB2) | 1.220 | | V |
| \( V_{\text{FB1,2}} \) | Feedback Voltage Accuracy(1) (FB1, FB2) | \(-2\%\) | 2% | |
| \( I_{\text{FB1,2}} \) | Current into FB1, FB2 pins | 0.01 | 0.5 | | μA |
| \( V_{\text{IS1,2}} \) | Reference Voltage for Current Sense | 80 | 100 | 120 | mV |
| \( I_{\text{IS1,2}} \) | Current into IS1, IS2 Pins | 0.01 | 0.5 | | μA |
| \( \Delta V_{\text{OUT}}/\Delta V_{\text{IN}} \) | Line Regulation(1) | Measured with the circuit in Figure 18, \( V_{\text{OUT}} + 0.5\,\text{V} \leq V_{\text{IN}} \leq 6.5\,\text{V} \) | 0.1 | | %/V |
| \( \Delta V_{\text{OUT}}/\Delta I_{\text{OUT}} \) | Load Regulation | Measured with the circuit in Figure 18, \( 30\,\text{mA} \leq I_{\text{OUT}} \leq 2\,\text{A} \) | 0.6 | | %/A |
| \( r_{1,2} \) | Efficiency(3) | Measured with the circuit in Figure 18, \( I_{\text{OUT}} = 1\,\text{A} \) | 94% | | |
| \( t_{\text{STR1,2}} \) | Startup Time(3) | Measured with the circuit in Figure 18, \( R_L = 6\,\Omega, C_{\text{OUT}} = 100\mu\text{F}, C_{\text{SS}} = 2.2\mu\text{F} \) | 5 | | ms |

(1) To be in regulation, minimum \( V_{\text{IN1}} \) (or \( V_{\text{IN2}} \)) must be greater than \( V_{\text{OUT1,NOM}} \) (or \( V_{\text{OUT2,NOM}} \)) by an amount determined by external components. Minimum \( V_{\text{IN3}} = V_{\text{OUT3}} + V_{\text{DO}} \) or 2.2V, whichever is greater.

(2) Maximum \( V_{\text{OUT}} \) depends on external components and will be less than \( V_{\text{IN}} \).

(3) Depends on external components.
Electrical Characteristics (continued)

\[ V_{EN1} = V_{IN1}, V_{EN2} = V_{IN2}, V_{EN3} = V_{IN3}, V_{IN1} = V_{IN2} = 2.2V, V_{IN3} = 3.0V, V_{OUT3} = 2.5V, C_{OUT1} = C_{OUT2} = 47\mu F, C_{OUT3} = 2.2\mu F, T_A = -40^\circ C \text{ to } +85^\circ C, \text{ unless otherwise noted. Typical values are at } T_A = +25^\circ C. \]

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{DS,ON1,2} )</td>
<td>Gate Driver P-Channel and N-Channel MOSFET On-Resistance</td>
<td>( V_{IN1,2} &gt; 2.5V )</td>
<td>4</td>
<td></td>
<td>( \Omega )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{IN1,2} = 2.2V )</td>
<td>6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{SW1,2} )</td>
<td>Gate Driver P-Channel and N-Channel MOSFET Drive Current</td>
<td>100</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_{ON} )</td>
<td>Minimum On Time</td>
<td>1.36</td>
<td>1.55</td>
<td>1.84</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( I_{OFF} )</td>
<td>Minimum Off Time</td>
<td>0.44</td>
<td>0.65</td>
<td>0.86</td>
<td>( \mu s )</td>
</tr>
</tbody>
</table>

**LDO**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OUT3} )</td>
<td>Output Voltage Range</td>
<td>1</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{FB3} )</td>
<td>Feedback Pin Voltage</td>
<td>0.507</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( \Delta V_{OUT}/\Delta V_{IN} )</td>
<td>Feedback Pin Voltage Accuracy(1)</td>
<td>2.95V ≤ ( V_{IN3} ) ≤ 6.5V</td>
<td>-4%</td>
<td>4%</td>
<td></td>
</tr>
<tr>
<td>(1) ( 1mA \leq I_{FB3} \leq 300mA )</td>
<td>Line Regulation(1)</td>
<td>( V_{OUT3} + 0.5V \leq \frac{\Delta V_{OUT}}{\Delta V_{IN}} \leq 6.5V )</td>
<td>0.075</td>
<td></td>
<td>%V</td>
</tr>
<tr>
<td>( \Delta V_{OUT}/\Delta I_{OUT} )</td>
<td>Load Regulation</td>
<td>0mA \leq I_{OUT3} \leq 300mA</td>
<td>0.01</td>
<td></td>
<td>%/mA</td>
</tr>
<tr>
<td>( V_{DO} )</td>
<td>Dropout Voltage ( (V_{IN} = V_{OUT}(NOM) - 0.1) )</td>
<td>( I_{OUT3} = 300mA )</td>
<td>250</td>
<td>350</td>
<td>mV</td>
</tr>
<tr>
<td>( I_{CL3} )</td>
<td>Current Limit</td>
<td>( V_{OUT} = 0.9 \times V_{OUT}(NOM) )</td>
<td>375</td>
<td>600</td>
<td>1000</td>
</tr>
<tr>
<td>( I_{FB3} )</td>
<td>Current into FB3 pin</td>
<td>0.03</td>
<td>0.1</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( V_n )</td>
<td>Output Noise</td>
<td>( BW = 100Hz - 100kHz ), ( I_{OUT3} = 300mA )</td>
<td>400</td>
<td></td>
<td>( \mu V_{RMS} )</td>
</tr>
<tr>
<td>( t_{SD} )</td>
<td>Thermal Shutdown Temperature for LDO</td>
<td>Shutdown, Temp Increasing</td>
<td>175</td>
<td></td>
<td>( ^\circ C )</td>
</tr>
<tr>
<td>(4) ( V_{DO} )</td>
<td>Reset, Temp Decreasing</td>
<td>160</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>UVLO</td>
<td>Under-Voltage Lockout Threshold</td>
<td>( V_{IN} ) Rising</td>
<td>1.80</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>UVLO</td>
<td>Under-Voltage Lockout Hysteresis</td>
<td>( V_{IN} ) Falling</td>
<td>100</td>
<td></td>
<td>mV</td>
</tr>
</tbody>
</table>

(4) \( V_{DO} \) does not apply when \( V_{OUT} + V_{DO} < 2.2V \).

### 6.6 Typical Characteristics

Measured using circuit in **Figure 18**.

#### 6.6.1 Buck Converter

![Figure 1. Buck Load Regulation](image1)

![Figure 2. Buck Load Regulation](image2)
Buck Converter (continued)

Figure 3. Buck Line Regulation

Figure 4. Buck Line Regulation

Figure 5. Buck Switching Frequency vs $I_{OUT}$, $T_A$

Figure 6. Buck Switching Frequency vs $I_{OUT}$

Figure 7. Efficiency vs $I_{OUT}$
6.6.2 LDO Converter

![Graph 1: LDO Load Regulation](image1)

- $V_{IN} = 3.3\, V$
- $V_{OUT} = 2.5\, V$

![Graph 2: LDO Line Regulation](image2)

- $V_{OUT} = 2.5\, V$
- $I_{OUT} = 1\, mA$

![Graph 3: LDO Dropout vs $I_{OUT}$](image3)

- $V_{IN} = 3.3\, V$
- $V_{OUT} = 2.5\, V$

![Graph 4: LDO Dropout vs $T_{A}$](image4)

- $V_{OUT} = 2.5\, V$
- $I_{OUT} = 300\, mA$

![Graph 5: $R_{DS,ON}$ PMOS vs $V_{IN}$](image5)

- $T_{A} = -40\, ^\circ C$
- $T_{A} = +25\, ^\circ C$
- $T_{A} = +85\, ^\circ C$

![Graph 6: $R_{DS,ON}$ NMOS vs $V_{IN}$](image6)

- $T_{A} = -40\, ^\circ C$
- $T_{A} = +25\, ^\circ C$
- $T_{A} = +85\, ^\circ C$
LDO Converter (continued)

Figure 14. LDO $V_{OUT}$ vs $T_A$

$V_{IN} = 3.3$ V
7 Detailed Description

7.1 Overview

The TPS75003 device is a power management IC (PMIC) with two buck controllers and one integrated LDO regulator. The three voltage regulators have independent enable pins for flexible power sequence timing, and all of the output voltages are set by external feedback resistor dividers. The independent power regulators can be wired in parallel, in series, or connected to separate input voltages as needed to meet the requirements of the application.

The two buck controllers are identical and operate over a input voltage range of 2.2 V to 6.5 V to supply a load with an externally configurable output voltage with up to 3-A of current. The buck controllers drive the gate of a single PMOS FET in an asynchronous buck regulator architecture. The use of a PMOS FET lets the buck regulator operate with 100% duty cycle when the input voltage is approximately equal to or less than the desired output voltage. The buck controllers have an externally configurable current sense feature to limit the output current and protect the PMOS FET. The buck controllers have an externally configurable soft-start feature that ramps the voltage and meet the timing requirements of the load.

The LDO regulator integrates the FET and operates over the same input voltage range of 2.2 V to 6.5 V to supply a load with an externally configurable output voltage with up to 300-mA of current. The LDO regulator includes integrated current limiting and thermal protection features. The LDO regulator also has an externally configurable soft-start feature to ramp the voltage to meet desired timing requirements.
7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 Operation (Buck Controllers)
Channels 1 and 2 have two identical non-synchronous buck controllers that use minimum on-time and minimum off-time hysteretic control (see Figure 18. For clarity, BUCK1 is used throughout the discussion of device operation. When \( V_{\text{OUT1}} \) is less than its target, an external PMOS (Q1) is turned on for at least the minimum on-time, increasing current through the inductor (L1) until \( V_{\text{OUT1}} \) reaches its target value or the current limit (set by R1) is reached. When either of these conditions is met, the PMOS is switched off for at least the minimum off-time of the device. After the minimum off-time has passed, the output voltage is monitored and the switch is turned on again when necessary.
Feature Description (continued)

When output current is low, the buck controllers operate in discontinuous mode. In this mode, each switching cycle begins at zero inductor current, rises to a maximum value, then falls back to zero current. When current reaches zero on the falling edge, ringing occurs at the resonant frequency of the inductor and stray switch node capacitance. This operation is normal; it does not affect circuit performance, and can be minimized if desired by using an RC snubber, a resistor in series with the gate of the PMOS, or both as shown in Figure 15.

![Figure 15. RC Snubber and Series Gate Resistor Used to Minimize Ringing](image)

At higher output currents, the TPS75003 device operates in continuous mode. In continuous mode, there is no ringing at the switch node and $V_{OUT}$ is equal to $V_{IN}$ times the duty cycle of the switching waveform.

When $V_{IN}$ approaches or falls to less than $V_{OUT}$, the buck controllers operate in 100% duty cycle mode, fully turning on the external PMOS to let regulation occur at a lower dropout than would otherwise be possible.

7.3.2 Enable (Buck Controllers)

The enable pins (EN1 and EN2) for the buck controllers are active high. When the enable pin is driven low and input voltage is present at IN1 or IN2, an on-chip FET is turned on to discharge the soft-start pin SS1 or SS2, respectively. If the soft-start feature is being used, enable should be driven high at least 10$\mu$s after $V_{IN}$ is applied to make sure that this discharge cycle occurs.

7.3.3 UVLO (Buck Controllers)

The device has an undervoltage lockout circuit to prevent the turn-on of the external PMOS (Q1 or Q2) until a reliable operating voltage is reached on the appropriate regulator (IN1 or IN2). This prevents the buck controllers from misoperation at low input voltages.

7.3.4 Current Limit (Buck Controllers)

An external resistor (R1 or R2) is used to set the current limit for the external PMOS transistor (Q1 or Q2). These resistors are connected between IN1 and IS1 (or IN2 and IS2) to provide a reference voltage across these pins that is proportional to the current flowing through the PMOS transistor. This reference voltage is compared to an internal reference to determine if an overcurrent condition exists. When current limit is exceeded, the external PMOS is turned off for the minimum off-time. Current limit detection is disabled for 10ns any time the PMOS is turned on to avoid triggering on switching noise. In 100% duty cycle mode, current limit is always enabled.

Current limit is calculated using the $V_{IS1}$ or $V_{IS2}$ specification in the Electrical Characteristics section as shown in Equation 1.

$$L_{LIMIT} = \frac{V_{IS1,2}}{R_{1,2}}$$

(1)

The current limit resistor must be appropriately rated for the dissipated power determined by its RMS current calculated by Equation 2.

$$I_{RMS} \approx I_{OUT} \sqrt{D} = I_{OUT} \sqrt{\frac{V_{OUT}}{V_{IN}}}$$

$$P_{DISS} = (I_{RMS})^2 \times R$$

(2)
Feature Description (continued)

For low-cost applications the \( I_{S1,2} \) pin can be connected to the drain of the PMOS, using \( R_{DS,ON} \) instead of \( R1 \) or \( R2 \) to set current limit. Variations in the PMOS \( R_{DS,ON} \) must be considered to make sure that current limit will protect external components such as the inductor, the diode, and the switch itself from damage as a result of overcurrent.

7.3.5 Short-Circuit Protection (Buck Controllers)

In an overload condition, the current rating of the external components (PMOS, diode, and inductor) can be exceeded. To help guard against this, the TPS75003 device increases its minimum off-time when the voltage at the feedback pin is less than the reference voltage. When the output is shorted (\( V_{FB} \) is zero), the minimum off-time is increased to approximately 4\( \mu \)s. The increase in off-time is proportional to the difference between the voltage at the feedback pin and the internal reference.

7.3.6 Soft-Start (Buck Controllers)

The buck controllers each have independent soft-start capability to limit inrush during start-up and to meet timing requirements of the Xilinx Spartan-3 FPGA. Limiting inrush current by using soft-start, or by staggering the turn-on of power rails, also guards against voltage drops at the input source due to its output impedance. Refer to the soft-start circuitry shown in Figure 16 and the soft-start timing diagram shown in Figure 17. The BUCK1 controller is discussed in this section; it is identical to BUCK2. Note that pins SS1 and SS2 are very high-impedance and cannot be probed using a typical oscilloscope setup. When input voltage is applied at IN1 and EN1 is driven low, any charge on the SS pin is discharged by an on-chip pulldown transistor. When EN1 is driven high, an on-chip current source starts charging the external soft-start capacitor \( C_{SS1} \). The voltage on the capacitor is compared to the voltage across the current sense resistor \( R1 \) to determine if an overcurrent condition exists. If the voltage drop across the sense resistor becomes greater than the reference voltage, then the external PMOS is shut off for the minimum off-time. This implementation provides a cycle-by-cycle current limit and lets the user configure the soft-start time over a wide range for most applications. For detailed information on selecting \( C_{SS1} \) and \( C_{SS2} \), see the Soft-Start Capacitor Selection (Buck Controllers) section.

![Figure 16. Soft-Start Circuitry](image)

![Figure 17. Soft-Start Timing Diagram](image)
7.3.7 LDO Operation

The TPS75003 LDO regulator uses a PMOS pass transistor and is offered in an adjustable version to easily configure any output voltage. When used to power $V_{CC,AUX}$, the LDO regulator output voltage is set to 2.5V; the LDO regulator can optionally be set to other output voltages to power other circuitry. The LDO regulator has integrated soft-start, independent enable, and short-circuit and thermal protection. The LDO regulator can be used to power $V_{CC,AUX}$ on the Xilinx Spartan-3 FPGA when 3.3V JTAG signals are used as described in the Using 3.3-V Signals for Spartan-3 Configuration and JTAG Ports application note.

7.3.8 Internal Current Limit (LDO)

The internal current limit of the LDO regulator helps protect the regulator during fault conditions. When an overcurrent condition is detected, the output voltage is decreased until the current falls to a level that will not damage the device. For good device reliability, the LDO regulator should not operate at the current limit.

7.3.9 Enable Pin (LDO)

The active high enable pin (EN3) can be used to put the device into shutdown mode. If shutdown and soft-start capability are not required, EN3 can be tied to IN3.

7.3.10 Dropout Voltage (LDO)

The LDO regulator uses a PMOS transistor to achieve low dropout. When $(V_{IN} - V_{OUT})$ is less than the dropout voltage ($V_{DO}$), the pass transistor is in its linear region of operation, and the input-output resistance is the $R_{DS,ON}$ of the pass transistor. In this region, the LDO regulator is said to be out of regulation; ripple rejection, line regulation, and load regulation degrade as $(V_{IN} - V_{OUT})$ decreases to much lower than 0.5V.

7.3.11 Transient Response (LDO)

The LDO regulator does not have an on-chip pulldown circuit for output overvoltage conditions. This feature lets the device be used in applications that connect higher voltage sources such as an alternate power supply to the output. This design also results in an output overshoot of several percent if the load current quickly drops to zero. The amplitude of overshoot can be reduced by increasing $C_{OUT}$; the duration of overshoot can be decreased by adding a load resistor.

7.3.12 Thermal Protection (LDO)

Thermal protection disables the output when the junction temperature, $T_J$, reaches unsafe levels. When the junction temperature cools, the output is enabled again. The thermal protection circuit may cycle on and off depending on the power dissipation, thermal resistance, and ambient temperature. This cycling limits the dissipation of the regulator, protecting it from damage. For good long term reliability, the device should not be continuously operated at or near thermal shutdown.

7.3.13 Power Dissipation (LDO)

The TPS75003 device is available in a QFN-style package with an exposed lead frame on the package underside. The exposed lead frame is the primary path for removing heat and should be soldered to a PC board that is configured to remove the amount of power dissipated by the LDO regulator, as calculated by Equation 3.

$$P_D = (V_{IN3} - V_{OUT3}) \times I_{OUT3}$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to ensure the required output voltage. The two buck converters do not contribute a significant amount of dissipated power. Using heavier copper will increase the overall effectiveness of removing heat from the device. The addition of plated through-holes to heat-dissipating layers will also improve the heatsink effectiveness.
8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS75003 is an integrated power management IC designed specifically to power DSPs and FPGAs such as the Xilinx Spartan-3, Spartan-3E and Spartan-3L. Two non-synchronous buck controllers can be configured to supply up to 3A for both CORE and I/O rails. A low dropout linear regulator powers auxiliary rails up to 300mA. All channels have independent enable and soft-start, allowing control of inrush current and output voltage ramp time as required by the application.

Table 1 through Table 4 show component values that have been tested for use with up to 3A load currents. Inductors in Table 1 are tested up to the respective saturation currents. Other similar external components can be substituted as desired; however, in all cases the circuits that are used should be tested for compliance to application requirements.

Table 1. Inductors Tested with the TPS75003

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>MANUFACTURER</th>
<th>INDUCTANCE</th>
<th>DC RESISTANCE</th>
<th>SATURATION CURRENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLF7032T-100M1R4</td>
<td>TDK</td>
<td>10μH ±20%</td>
<td>53mΩ ±20%</td>
<td>1.4A</td>
</tr>
<tr>
<td>SLF6025-150MR88</td>
<td>TDK</td>
<td>15μH ±20%</td>
<td>85mΩ ±20%</td>
<td>0.88A</td>
</tr>
<tr>
<td>CDRH6D28-5R0</td>
<td>Sumida</td>
<td>5μH</td>
<td>23mΩ</td>
<td>2.4A</td>
</tr>
<tr>
<td>CDRH6D38-5R0</td>
<td>Sumida</td>
<td>5μH</td>
<td>18mΩ</td>
<td>2.9A</td>
</tr>
<tr>
<td>CDRH103R-100</td>
<td>Sumida</td>
<td>10μH</td>
<td>45mΩ</td>
<td>2.4A</td>
</tr>
<tr>
<td>CDRH4D28-100</td>
<td>Sumida</td>
<td>10μH</td>
<td>96mΩ</td>
<td>1.0A</td>
</tr>
<tr>
<td>CDRH8D43-150</td>
<td>Sumida</td>
<td>15μH</td>
<td>42mΩ</td>
<td>2.9A</td>
</tr>
<tr>
<td>CDRH5D18-6R2</td>
<td>Sumida</td>
<td>6.2μH</td>
<td>71mΩ</td>
<td>1.4A</td>
</tr>
<tr>
<td>DO3316P-472</td>
<td>Coilcraft</td>
<td>4.7μH</td>
<td>18mΩ</td>
<td>5.4A</td>
</tr>
<tr>
<td>MSS7341-153</td>
<td>Coilcraft</td>
<td>15μH</td>
<td>55mΩ</td>
<td>1.6A</td>
</tr>
<tr>
<td>MSS7341-223</td>
<td>Coilcraft</td>
<td>22μH</td>
<td>82mΩ</td>
<td>1.26A</td>
</tr>
<tr>
<td>744052006</td>
<td>Wurth</td>
<td>6.2μH</td>
<td>80mΩ</td>
<td>1.45A</td>
</tr>
<tr>
<td>74451115</td>
<td>Wurth</td>
<td>15μH</td>
<td>90mΩ</td>
<td>0.8A</td>
</tr>
</tbody>
</table>

Table 2. PMOS Transistors Tested with the TPS75003

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>MANUFACTURER</th>
<th>R_DS,ON (TYP)</th>
<th>V_DS</th>
<th>I_D</th>
<th>PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>SI5457DC-T1-GE3</td>
<td>Vishay</td>
<td>0.056Ω at VGS = −2.5V</td>
<td>−20V</td>
<td>−6A at +25°C</td>
<td>1206-8</td>
</tr>
<tr>
<td>SI2301BDS-T1-E3</td>
<td>Vishay</td>
<td>0.15Ω at VGS = −2.5V</td>
<td>−20V</td>
<td>−2.0A at +25°C</td>
<td>SOT-23</td>
</tr>
<tr>
<td>SI2323DS-T1-E3</td>
<td>Vishay</td>
<td>0.052Ω at VGS = −2.5V</td>
<td>−20V</td>
<td>−4.1A at +25°C</td>
<td>SOT-23</td>
</tr>
<tr>
<td>FDG328P</td>
<td>Fairchild</td>
<td>0.12Ω at VGS = −2.5V</td>
<td>−20V</td>
<td>−1.5A</td>
<td>SC70-6</td>
</tr>
</tbody>
</table>

Table 3. Diodes Tested with the TPS75003

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>MANUFACTURER</th>
<th>V_R</th>
<th>I_F</th>
<th>PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSV240AF</td>
<td>ON Semiconductor / Fairchild</td>
<td>40V</td>
<td>2.0A</td>
<td>DO-214-2</td>
</tr>
<tr>
<td>FSV340FP</td>
<td>ON Semiconductor / Fairchild</td>
<td>40V</td>
<td>3.0A</td>
<td>SOD-123-2</td>
</tr>
<tr>
<td>SS32</td>
<td>ON Semiconductor / Fairchild</td>
<td>20V</td>
<td>3.0A</td>
<td>DO-214AB</td>
</tr>
<tr>
<td>ZHC52000QTA</td>
<td>Zetex</td>
<td>40V</td>
<td>2.0A</td>
<td>SOT-23–6</td>
</tr>
<tr>
<td>B320AE-13</td>
<td>Diodes Inc.</td>
<td>20V</td>
<td>3.0A</td>
<td>SMA</td>
</tr>
</tbody>
</table>
### Table 4. Capacitors Tested with the TPS75003

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>MANUFACTURER</th>
<th>CAPACITANCE</th>
<th>ESR</th>
<th>VOLTAGE RATING</th>
</tr>
</thead>
<tbody>
<tr>
<td>10TPB47M (PosCap)</td>
<td>Panasonic</td>
<td>47 μF</td>
<td>0.07Ω</td>
<td>10V</td>
</tr>
<tr>
<td>T491D476M010AT</td>
<td>Kemet</td>
<td>47 μF</td>
<td>0.8Ω</td>
<td>10V</td>
</tr>
<tr>
<td>T495D476K016ATE180</td>
<td>Kemet</td>
<td>47 μF</td>
<td>0.18Ω</td>
<td>16V</td>
</tr>
<tr>
<td>TR3C476K016C0300</td>
<td>Vishay</td>
<td>47 μF</td>
<td>0.3Ω</td>
<td>16V</td>
</tr>
<tr>
<td>T495D107M006ATE050</td>
<td>Kemet</td>
<td>100 μF</td>
<td>0.05Ω</td>
<td>6.3V</td>
</tr>
<tr>
<td>TPSC107M006R0075</td>
<td>AVX</td>
<td>100 μF</td>
<td>0.075Ω</td>
<td>6.3V</td>
</tr>
<tr>
<td>6TPE100MPB (PosCap)</td>
<td>Panasonic</td>
<td>100 μF</td>
<td>0.025Ω</td>
<td>6.3V</td>
</tr>
<tr>
<td>TR3C107K6R3C0125</td>
<td>Vishay</td>
<td>100 μF</td>
<td>0.25Ω</td>
<td>6.3V</td>
</tr>
</tbody>
</table>

### 8.2 Typical Application

Figure 18 shows a typical application circuit for powering the Xilinx Spartan-3 FPGA.

![Typical Application Circuit for Powering the Xilinx Spartan-3 FPGA](image-url)
Typical Application (continued)

8.2.1 Design Requirements

Table 5 lists the design requirements that are met by the application shown in Figure 18

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>DESCRIPTION</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>Input power supply to all regulators: BUCK1 (IN1), BUCK2 (IN2), and LDO (IN3)</td>
<td>3.3 to 6.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OUT1}$</td>
<td>Output of BUCK1 regulator $V_{CCINT}$, core rail power for the FPGA</td>
<td>1.2</td>
<td>V</td>
</tr>
<tr>
<td>$I_{OUT1}$</td>
<td>Load current of FPGA for $V_{CCINT}$ rail</td>
<td>2</td>
<td>A</td>
</tr>
<tr>
<td>$V_{OUT2}$</td>
<td>Output of BUCK2 regulator $V_{CCO}$, I/O rail power for the FPGA</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td>$I_{OUT2}$</td>
<td>Load current of FPGA for $V_{CCO}$ rail</td>
<td>2</td>
<td>A</td>
</tr>
<tr>
<td>$V_{OUT3}$</td>
<td>Output of LDO regulator $V_{CCAUX}$, auxiliary rail power for the FPGA</td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td>$I_{OUT3}$</td>
<td>Load current of FPGA for $V_{CCAUX}$ rail</td>
<td>300</td>
<td>mA</td>
</tr>
</tbody>
</table>

8.2.2 Detailed Design Procedure

8.2.2.1 Input Capacitor $C_{IN1}$, $C_{IN2}$ Selection (Buck Controllers)

It is good analog design practice to place input capacitors near the inputs of the device in order to ensure a low impedance input supply. 10μF to 22μF of capacitance for each buck converter is adequate for most applications, and should be placed within 100mils (0.01in, or 2.54mm) of the IN1 and IN2 pins to minimize the effects of pulsed current switching noise on the soft-start circuitry during the first ~1V of output voltage ramp. Low ESR capacitors also help to minimize noise on the supply line. The minimum value of capacitance can be estimated using Equation 4:

$$C_{IN,MIN} + \frac{(1/2)L \times (\Delta I)^2}{V_{(RIPPLE)} \times V_{IN}} \approx \frac{(1/2)L \times (0.3 \times I_{OUT})^2}{V_{(RIPPLE)} \times V_{IN}}$$

(4)

Note that the capacitors must be able to handle the RMS current in continuous conduction mode, which can be calculated using Equation 5:

$$I_{C,JN,(RMS)} \approx I_{OUT} \sqrt{\frac{V_{OUT}}{V_{IN,MIN}}}$$

(5)

8.2.2.2 Inductor Value Selection (Buck Controllers)

The inductor is chosen based on inductance value and maximum current rating. Larger inductors reduce current ripple (and therefore, output voltage ripple) but are physically larger and more expensive. Inductors with lower DC resistance typically improve efficiency, but also have higher cost and larger physical size. The buck converters work well with inductor values between 4.7μH and 47μH in most applications. When selecting an inductor, the current rating should exceed the current limit set by $R_{IS}$ or $R_{DS,ON}$ (see the Current Limit (Buck Controllers) section). To determine the minimum inductor size, first determine if the device will operate in minimum on-time or minimum off-time mode. The device will operate in minimum on-time mode if Equation 6 is satisfied:

$$V_{IN} - V_{OUT} - I_{OUT} \times R_{DS,ON} - R_L \times I_{OUT} \geq \frac{t_{OFF,MIN} \times (V_{OUT} + V_{SCHOTTKY} + R_L \times I_{OUT})}{t_{ON,MIN}}$$

where

- $R_L$ = the inductor DC resistance

Minimum inductor size needed when operating in minimum on-time mode is given by Equation 7:
Minimum inductor size needed when operating in minimum off-time mode is given by Equation 8:

\[
L_{\text{MIN}} = \frac{(V_{\text{IN}} - V_{\text{OUT}} - I_{\text{OUT}} \times R_{\text{DS,ON}} - R_{L} \times I_{\text{OUT}}) \times t_{\text{ON,MIN}}}{\Delta I_L}
\]

(7)

Minimum inductor size needed when operating in minimum off-time mode is given by Equation 8:

\[
L_{\text{MIN}} = \frac{(V_{\text{OUT}} + V_{\text{SCHOTTKY}} + R_L \times I_{\text{OUT}}) \times t_{\text{OFF,MIN}}}{\Delta I_L}
\]

where

- \(\Delta I_L = (20\% - 30\%) \times I_{\text{OUT-MAX}}\)

(8)

### 8.2.2.3 External PMOS Transistor Selection (Buck Controllers)

The external PMOS transistor is selected based on threshold voltage \(V_T\), on-resistance \(R_{\text{DS,ON}}\), gate capacitance \(C_G\) and voltage rating. The PMOS \(V_T\) magnitude must be much lower than the lowest voltage at IN1 or IN2 that will be used. A \(V_T\) magnitude that is 0.5V less than the lowest input voltage is normally sufficient. The PMOS gate will see voltages from 0V to the maximum input voltage, so gate-to-source breakdown should be a few volts higher than the maximum input supply. The drain-to-source of the device will also see this full voltage swing, and should therefore be a few volts higher than the maximum input supply. The RMS current in the PMOS can be estimated by using Equation 9:

\[
I_{\text{PMOS(RMS)}} \approx I_{\text{OUT}} \sqrt{D} = I_{\text{OUT}} \sqrt{\frac{V_{\text{OUT}}}{V_{\text{IN}}}}
\]

(9)

The power dissipated in the PMOS is comprised of both conduction and switching losses. Switching losses are typically insignificant. The conduction losses are a function of the RMS current and the \(R_{\text{DS,ON}}\) of the PMOS, and are calculated by Equation 10:

\[
P_{\text{(cond)}} = \left(I_{\text{OUT}} \sqrt{D}\right)^2 \times R_{\text{DS,ON}} \times (1 + TC \times \left|T_J - 25^\circ\text{C}\right|) = \left(I_{\text{OUT}} \sqrt{D}\right) \times R_{\text{DS,ON}}
\]

(10)

### 8.2.2.4 Diode Selection (Buck Controllers)

The diode is off when the PMOS is on, and on when the PMOS is off. Since it will be turned on and off at a relatively high frequency, a Schottky diode is recommended for good performance. The peak current rating of the diode should exceed the peak current limit set by the sense resistor \(R_{\text{IS1,2}}\). A diode with low reverse leakage current and low forward voltage at operating current will optimize efficiency. Equation 11 calculates the estimated average power dissipation:

\[
I_{\text{(diode)(RMS)}} \approx I_{\text{OUT}} \left(1 - D\right) = I_{\text{OUT}} \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}\right)
\]

(11)

### 8.2.2.5 Output Capacitor Selection (Buck Controllers)

The output capacitor is selected based on output voltage ripple and transient response requirements. As a result of the nature of the hysteretic control loop, a minimum ESR of a few tens of \(m\Omega\) should be maintained for good operation unless a feed-forward resistor is used. Low ESR bulk tantalum or PosCap capacitors work best in most applications. A 1.0\(\mu\)F ceramic capacitor can be used in parallel with this capacitor to filter higher frequency spikes. The output voltage ripple can be estimated by Equation 12:

\[
\Delta V_{PP} = \Delta I \times \left[\text{ESR} + \left(\frac{1}{8 \times C_{\text{OUT}} \times f}\right)\right] \approx 1.1 \Delta I \times \text{ESR}
\]

(12)

To calculate the capacitance needed to achieve a given voltage ripple as a result of a load transient from zero output to full current, use Equation 13:

\[
C_{\text{OUT}} = \frac{L \times \Delta I_{\text{OUT}}^2}{(V_{\text{IN}} - V_{\text{OUT}}) \times \Delta V}
\]

(13)
If only ceramic or other very low ESR output capacitor configurations are desired, additional voltage ripple must be passed to the feedback pin. For detailed application information, refer to the Using Ceramic Output Capacitors with the TPS6420x and TPS75003 Buck Controllers application report.

8.2.2.6 Output Voltage Ripple Effect on V\textsubscript{OUT} (Buck Controllers)

Output voltage ripple causes V\textsubscript{OUT} to be higher or lower than the target value by half of the peak-to-peak voltage ripple. For minimum on-time, the ripple adds to the voltage; for minimum off-time, it subtracts from the voltage.

8.2.2.7 Soft-Start Capacitor Selection (Buck Controllers)

The soft-start for BUCK1 and BUCK2 is not intended to be a precision function. However, the startup time (from a positive transition on Enable to V\textsubscript{OUT} reaching its final value) has a linear relationship to C\textsubscript{SS} up to approximately 800pF, which results in a startup time of approximately 4ms. Above this value of C\textsubscript{SS}, the variation in start-up time increases rapidly. This variation can occur from unit to unit and even between the two BUCK controllers in one device. Therefore, do not depend on the soft-start feature for sequencing multiple supplies if values of C\textsubscript{SS} greater than 800pF are used.

BUCK1 is discussed in this section; it is identical to BUCK2. Soft-start is implemented on the buck controllers by ramping current limit from 0 to its target value (set by R\textsubscript{1}) over a user-defined time. This time is set by the external soft-start cap connected to pin SS1. If SS1 is left open, a small on-chip capacitor will provide a current limit ramp time of approximately 250μs. Figure 19 shows the effects of R\textsubscript{1} and SS1 on the current limit start-up ramp.

![Figure 19. Effects of C\textsubscript{SS1} and R\textsubscript{1} on Current Ramp Limit](image)

This soft-start current limit ramp can be used to provide inrush current control or output voltage ramp control. While the current limit ramp can be easily understood by looking at Figure 19, the output voltage ramp is a complex function of many variables. The dominant variables in this process are V\textsubscript{OUT1}, C\textsubscript{SS1}, I\textsubscript{OUT1}, and R\textsubscript{1}. Less important variables are V\textsubscript{IN1} and L\textsubscript{1}.

The best way to set a target start-up time is through bench measurement under target conditions, adjusting C\textsubscript{SS1} to get the desired startup profile. To stay above a minimum start-up time, set the nominal start-up time to approximately five times the minimum. To stay below a maximum time, set the nominal start-up time at one-fifth of the maximum. Fastest start-up times occur at maximum V\textsubscript{IN1}, with minimum V\textsubscript{OUT1}, L\textsubscript{1}, C\textsubscript{OUT1}, C\textsubscript{SS1}, and I\textsubscript{OUT1}. Slowest start-up times occur under opposite conditions.

Refer to Figure 21 to Figure 25 for characterization curves showing how the start-up profile is affected by these critical parameters.
8.2.2.8 Output Voltage Setting Selection (Buck Controllers)

Output voltage is set using two resistors as shown for Buck2 in Figure 18. Output voltage is then calculated using Equation 14:

\[ V_{OUT} = V_{FB} \left( \frac{R5}{R6} + 1 \right) \]

where
- \( V_{FB} = 1.22V \) \hspace{1cm} (14)

8.2.2.9 Input Capacitor Selection (LDO)

Although an input capacitor is not required, it is good analog design practice to connect a 0.1\( \mu F \) to 10\( \mu F \) low ESR capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, stability, and ripple rejection. A higher value capacitor may be needed if large, fast rise-time load transients are anticipated, or if the device is located far from its power source.

8.2.2.10 Output Capacitor Selection (LDO)

A 2.2\( \mu F \) or greater capacitor is required near the output of the device to ensure stability. The LDO is stable with any capacitor type, including ceramic. If improved transient response or ripple rejection is required, larger and/or lower ESR output capacitors can be used.

8.2.2.11 Soft-Start Capacitor Selection (LDO)

The LDO uses an external soft-start capacitor, \( C_{SS3} \), to provide an RC-ramped reference voltage to the control loop. See the Functional Block Diagram. This is a voltage-controlled soft-start, as compared to the current-controlled soft-start used by the buck controllers. The start-up waveform can be approximated by Equation 15:

\[ V_{OUT} \left( t \right) = V_{OUT,SET} \left( 1 - e^{-\frac{t}{RC}} \right) \]

where
- \( R = 480 \times 10^3 \)
- \( C = \) capacitance in \( \mu F \) from SS3 to GND \hspace{1cm} (15)

The time taken to reach 90% of final \( V_{OUT} \) can be approximated by Equation 16:

\[ T_{90\%} = 2.3 \times \left( 480 \times 10^3 \right) C_{SS3} \text{ (\( \mu F \))} \]

8.2.2.12 Setting Output Voltage (LDO)

Output voltage is set using two resistors as shown in Figure 18. Output voltage is then calculated using Equation 17:

\[ V_{OUT} = V_{FB} \left( \frac{R3}{R4} + 1 \right) \]

where
- \( V_{FB} = 0.507V \) \hspace{1cm} (17)
8.2.3 Application Curves

**Figure 20. Buck Output Voltage Ripple**

- $V_{IN} = 5\, V$
- $V_{OUT} = 3.3\, V$
- $I_{OUT} = 2\, A$

**Figure 21. Buck Start-Up vs $V_{IN}$ and $I_{OUT}$**

- $V_{OUT} = 1.2\, V$
- $C_{SS} = 0.01\, \mu F$

See the [Soft-Start Capacitor Selection (Buck Controllers)](https://www.ti.com) section.

**Figure 22. Buck Start-Up vs $V_{IN}$ and $C_{OUT}$**

- $V_{OUT} = 1.2\, V$
- $C_{SS} = 0.01\, \mu F$

**Figure 23. Buck Start-Up vs $V_{IN}$ and $C_{SS}$**

- $V_{OUT} = 1.2\, V$
- $I_{OUT} = 1\, A$

See the [Soft-Start Capacitor Selection (Buck Controllers)](https://www.ti.com) section.

**Figure 24. Buck Start-Up vs $I_{OUT}$ and $C_{SS}$**

- $V_{IN} = 5\, V$
- $V_{OUT} = 3.3\, V$
- $I_{OUT} = 2A$
- $C_{SS} = 560\, \mu F$
- $I_{OUT} = 0.5A$
- $C_{SS} = 560\, \mu F$
- $I_{OUT} = 0.5A$
- $C_{SS} = 1500\, \mu F$
- $I_{OUT} = 2A$
- $C_{SS} = 1500\, \mu F$

See the [Soft-Start Capacitor Selection (Buck Controllers)](https://www.ti.com) section.

**Figure 25. Buck Start-Up vs $V_{IN}$ and $R_{SENSE}$**

- $V_{OUT} = 1.2\, V$
- $C_{SS} = 0.01\, \mu F$

See the [Soft-Start Capacitor Selection (Buck Controllers)](https://www.ti.com) section.
9 Power Supply Recommendations

There are three separate blocks internal to the TPS75003 device: two identical buck controllers and one integrated LDO regulator. The input voltage, $V_{\text{IN}X}$, to the IN1 and IN2 pins must be within the range specified in the Electrical Characteristics and must be greater than the nominal output voltage of BUCK1 or BUCK2, respectively. However, the maximum output voltages, $V_{\text{OUT}1}$ and $V_{\text{OUT}2}$, are determined by external component selection and cannot be specified. The input voltage to the LDO regulator, $V_{\text{IN}3}$, must be greater than the dropout voltage ($V_{\text{DO}}$) added to $V_{\text{OUT}3}$ or an absolute value of 2.2 V, whichever is greater. The power supply into the IN1, IN2, and IN3 pins do not need to be equal to each other but all of the design values must adhere to the minimum and maximum specifications of the TPS75003 and external components. Other considerations are based on the relationship of pins used inside the TPS75003 device.

The power supply into IN1 is used as the power supply to drive the gate of the switch connected at SW1. The difference between the voltages at the IN1 pin and IS1 pin is the input to the sensing which controls current limit. The power supply connected at IN1 must be the power supply connected to 33-mΩ sense resistor, and the opposite terminal of the sense resistor must connect directly to IS1 and the source pin(s) of the eternal PMOS FET.

Similarly, the power supply into IN2 is used as the power supply to drive the gate of the switch connected at SW2. The difference between the voltages at the IN2 pin and IS2 pin is the input to the sensing which controls current limit. The power supply connected at IN2 must be the power supply connected to 33-mΩ sense resistor, and the opposite terminal of the sense resistor must connect directly to IS2 and the source pins of the eternal PMOS FET.

The power supply into IN3 is used as the power supply to the LDO regulator and all internal support circuitry. Unlike the BUCK1 and BUCK2 controllers, the power does not bypass the TPS75003 device. Therefore, the output of the LDO is named OUT3 and up to 300-mA of current will go directly from IN3 to OUT3.
10 Layout

10.1 Layout Guidelines

10.1.1 PCB Layout Considerations

As with any switching regulators, careful attention must be paid to board layout. A typical application circuit and corresponding recommended printed circuit board (PCB) layout with emphasis on the most sensitive areas are shown in Figure 26 through Figure 28.

![Typical Application Circuit Diagram]

Note: Most sensitive areas are highlighted by bold lines.

Figure 26. Typical Application Circuit
10.2 Layout Example

Figure 27. Recommended PCB Layout, Component Side, Top View

Figure 28. Recommended PCB Layout, Bottom Side, Top View
11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer
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11.1.2 Development Support
For development support, refer to:
- Design Spreadsheet for the TPS75003
- TPS75003: Gerber Software for TPS75003

11.2 Documentation Support

11.2.1 Related Documentation
For related documentation see the following:
- Texas Instruments, TPS75003EVM User's Guide
- Texas Instruments, Using 3.3-V Signals for Spartan-3 Configuration and JTAG Ports application note
- Texas Instruments, Using Ceramic Output Capacitors with the TPS6420x and TPS75003 Buck Controllers application report

11.3 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.6 Electrostatic Discharge Caution
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
# PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/ Ball material (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
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<tbody>
<tr>
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<td>-40 to 85</td>
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<td>75003</td>
<td>Samples</td>
</tr>
</tbody>
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(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS75003:

- Enhanced Product: TPS75003-EP

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications
### TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

- **Reel Diameter**
- **Reel Width (W1)**

**TAPE DIMENSIONS**

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- **Q1**
- **Q2**
- **Q3**
- **Q4**

**Pocket Quadrants**

**Sprocket Holes**

**User Direction of Feed**

*All dimensions are nominal*

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### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

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Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
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