ULTRALOW-NOISE, HIGH PSRR, FAST RF 100-mA
LOW-DROPOUT LINEAR REGULATORS

FEATURES

- 100-mA Low-Dropout Regulator With EN
- Available in 2.5-V, 2.8-V, 3-V, and Adj.
- High PSRR (75 dB at 10 kHz)
- Ultralow Noise (27 µV)
- Fast Start-Up Time (50 µs)
- Stable With Any 1-µF Ceramic Capacitor
- Excellent Load/Line Transient
- Very Low Dropout Voltage (55 mV at Full Load, TPS79230)
- 5-Pin SOT23 (DBV) Package
- TPS791xx Provides EN Options

APPLICATIONS

- Cellular and Cordless Telephones
- VCOs
- RF
- Bluetooth™, Wireless LAN
- Handheld Organizers, PDA

DESCRIPTION

The TPS792xx family of low-dropout (LDO) low-power linear voltage regulators features high power supply rejection ratio (PSRR), ultralow noise, fast start-up, and excellent line and load transient responses in a small outline, SOT23, package. Each device in the family is stable, with a small 1-µF ceramic capacitor on the output. The family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (e.g., 55 mV at 100 mA, TPS79230). Each device achieves fast start-up times (approximately 50 µs with a 0.001 µF bypass capacitor) while consuming very low quiescent current (170 µA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 µA. The TPS79228 exhibits approximately 27 µV RMS of output voltage noise with a 0.1 µF bypass capacitor. Applications with analog components that are noise sensitive, such as portable RF electronics, benefit from the high PSRR and low noise features as well as the fast response time.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Bluetooth is a trademark owned by the Bluetooth SIG, Inc.
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>T_J</th>
<th>VOLTAGE</th>
<th>PACKAGE</th>
<th>PART NUMBER</th>
<th>SYMBOL</th>
</tr>
</thead>
<tbody>
<tr>
<td>-40°C to 125°C</td>
<td>1.2 to 5.5 V</td>
<td>SOT23 (DBV)</td>
<td>TPS79201DBVT(1)</td>
<td>PEVI</td>
</tr>
<tr>
<td></td>
<td>2.5 V</td>
<td></td>
<td>TPS79225DBVT(1)</td>
<td>PEXI</td>
</tr>
<tr>
<td></td>
<td>2.8 V</td>
<td></td>
<td>TPS79228DBVT(1)</td>
<td>PEWI</td>
</tr>
<tr>
<td></td>
<td>3 V</td>
<td></td>
<td>TPS79230DBVT(1)</td>
<td>PEYI</td>
</tr>
</tbody>
</table>

(1) The DBVT indicates tape and reel of 250 parts.
(2) The DBVR indicates tape and reel of 3000 parts.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

Input voltage range (2) -0.3 V to 6 V
Voltage range at EN -0.3 V to V_I + 0.3 V
Voltage on OUT -0.3 V to 6 V
Peak output current Internally limited
ESD rating, HBM 2 kV
ESD rating, CDM 500 V
Continuous total power dissipation See Dissipation Rating Table
Operating virtual junction temperature range, T_J -40°C to 150°C
Operating ambient temperature range, T_A -40°C to 85°C
Storage temperature range, T_stg -65°C to 150°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

PACKAGE DISSIPATION RATING

<table>
<thead>
<tr>
<th>BOARD</th>
<th>PACKAGE</th>
<th>RθJC</th>
<th>RθJA</th>
<th>DERATING FACTOR ABOVE T_A = 25°C</th>
<th>T_A = 25°C POWER RATING</th>
<th>T_A = 70°C POWER RATING</th>
<th>T_A = 85°C POWER RATING</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low K(1)</td>
<td>DBV</td>
<td>63.75°C/W</td>
<td>256°C/W</td>
<td>3.906 mW/°C</td>
<td>391 mW</td>
<td>215 mW</td>
<td>156 mW</td>
</tr>
<tr>
<td>High K(2)</td>
<td>DBV</td>
<td>63.75°C/W</td>
<td>178.3°C/W</td>
<td>5.609 mW/°C</td>
<td>561 mW</td>
<td>308 mW</td>
<td>224 mW</td>
</tr>
</tbody>
</table>

(1) The JEDEC low K (1s) board design used to derive this data was a 3-inch x 3-inch, two layer board with 2 ounce copper traces on top of the board.
(2) The JEDEC high K (2s2p) board design used to derive this data was a 3-inch x 3-inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage, V_I (1)</td>
<td>2.7</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Continuous output current, I_O (2)</td>
<td>0</td>
<td>100</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Operating junction temperature, T_J</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

(1) To calculate the minimum input voltage for your maximum output current, use the following formula:

V_I(min) = V_O(max) + V_DO (max load)

(2) Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.
ELECTRICAL CHARACTERISTICS
over recommended operating free-air temperature range, (T_J = –40 to 125°C), V_I = V_O(typ) + 1 V, I_O = 1 mA, EN = V_I, C_O = 10 µF, C(byp) = 0.01 µF (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage</td>
<td>T_J = 25°C, 1.22 V ≤ V_O ≤ 5.2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 µA &lt; I_O &lt; 100 mA, 1.22 V ≤ V_O ≤ 5.2 V</td>
<td>0.98</td>
<td>1.02</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>T_J = 25°C, 3.5 V ≤ V_I &lt; 5.5 V</td>
<td>2.45</td>
<td>2.55</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 µA &lt; I_O &lt; 100 mA, 3.8 V ≤ V_I &lt; 5.5 V</td>
<td>2.744</td>
<td>2.856</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>T_J = 25°C, 4 V ≤ V_I &lt; 5.5 V</td>
<td>2.94</td>
<td>3.06</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Quiescent current (GND current)</td>
<td>0 µA &lt; I_O &lt; 100 mA, T_J = 25°C</td>
<td>170</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>0 µA &lt; I_O &lt; 100 mA</td>
<td>250</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Load regulation</td>
<td>V_O + 1 V &lt; V_I ≤ 5.5 V, T_J = 25°C</td>
<td>0.05</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>V_O + 1 V ≤ V_I ≤ 5.5 V, T_J = 25°C</td>
<td>0.12</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output voltage line regulation (ΔV_O/V_O)</td>
<td>BW = 100 Hz to 100 kHz, I_O = 100 mA, T_J = 25°C</td>
<td>50</td>
<td></td>
<td></td>
<td>µVRMS</td>
</tr>
<tr>
<td>Output noise voltage (TPS79228)</td>
<td>C(byp) = 0.001 µF</td>
<td>50</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>C(byp) = 0.0047 µF</td>
<td>33</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>C(byp) = 0.01 µF</td>
<td>31</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Time, start-up (TPS79228)</td>
<td>R_L = 28 Ω, T_J = 25°C</td>
<td>50</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>C_O = 1 µF</td>
<td>70</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>C(byp) = 0.001 µF</td>
<td>90</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output current limit</td>
<td>V_O = 0 V</td>
<td>285</td>
<td>600</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>UVLO threshold</td>
<td>V_CC rising</td>
<td>2.25</td>
<td>2.65</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>UVLO hysteresis</td>
<td>T_J = 25°C</td>
<td>100</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Standby current</td>
<td>EN = 0 V, 2.7 V &lt; V_I ≤ 5.5 V</td>
<td>0.7</td>
<td>1</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>High level enable input voltage</td>
<td>2.7 V &lt; V_I ≤ 5.5 V</td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Low level enable input voltage</td>
<td>2.7 V &lt; V_I ≤ 5.5 V</td>
<td>0.7</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input current (EN)</td>
<td></td>
<td>–1</td>
<td>1</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Power supply ripple rejection</td>
<td>F = 100 Hz, T_J = 25°C, I_O = 10 mA</td>
<td>70</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>F = 100 Hz, T_J = 25°C, I_O = 100 mA</td>
<td>72</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>F = 10 kHz, T_J = 25°C, I_O = 100 mA</td>
<td>75</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>F = 100 kHz, T_J = 25°C, I_O = 100 mA</td>
<td>47</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dropout voltage(3)</td>
<td>I_O = 100 mA, T_J = 25°C</td>
<td>60</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>I_O = 100 mA</td>
<td>110</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>I_O = 100 mA</td>
<td>55</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) The minimum IN operating voltage is 2.7 V or V_O(typ) + 1 V, whichever is greater. The maximum IN voltage is 5.5 V. The maximum output current is 100 mA.
(2) If V_O ≤ 2.5 V then V_Imin = 2.7 V, V_Imax = 5.5 V:
\[
\text{Line regulation (mV)} = \left(\frac{\%}{V}\right) \times \frac{V_O}{V_I} \times 100 \times 1000
\]
If V_O ≥ 2.5 V then V_Imin = V_O + 1 V, V_Imax = 5.5 V:
(3) IN voltage equals V_O(typ) – 100 mV; The TPS79225 dropout voltage is limited by the input voltage range limitations.
FUNCTIONAL BLOCK DIAGRAM—ADJUSTABLE VERSION

FUNCTIONAL BLOCK DIAGRAM—FIXED VERSION

Terminal Functions

<table>
<thead>
<tr>
<th>TERMINAL NAME</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>BYPASS</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>EN</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>FB</td>
<td>5</td>
<td>N/A</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>IN</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>OUT</td>
<td>6</td>
<td>5</td>
</tr>
</tbody>
</table>
TYPICAL CHARACTERISTICS

**Figure 1**

TPS79228

OUTPUT VOLTAGE

VS

OUTPUT CURRENT

\[ V_O = 2.796 \, \text{V} \quad \text{for} \quad I_O = 100 \, \text{mA} \]

\[ V_O = 2.797 \, \text{V} \quad \text{for} \quad I_O = 10 \, \text{mA} \]

\[ V_O = 2.799 \, \text{V} \quad \text{for} \quad I_O = 1 \, \text{mA} \]

**Figure 2**

TPS79228

OUTPUT VOLTAGE

VS

JUNCTION TEMPERATURE

\[ V_I = 3.8 \, \text{V} \]

\[ C_O = 10 \, \mu\text{F} \]

\[ T_J = 25 \, ^\circ\text{C} \]

\[ I_O = 1 \, \text{mA} \]

\[ I_O = 100 \, \text{mA} \]

**Figure 3**

TPS79228

GROUND CURRENT

VS

JUNCTION TEMPERATURE

\[ V_I = 3.8 \, \text{V} \]

\[ C_O = 10 \, \mu\text{F} \]

\[ C_{(byp)} = 0.1 \, \mu\text{F} \]

\[ I_O = 1 \, \text{mA} \]

\[ I_O = 100 \, \text{mA} \]

**Figure 4**

TPS79228

OUTPUT SPECTRAL NOISE DENSITY

VS

FREQUENCY

\[ f = 100 \, \text{Hz} \quad \text{to} \quad 100 \, \text{kHz} \]

\[ f = 1 \, \text{kHz} \quad \text{to} \quad 10 \, \text{kHz} \]

\[ f = 10 \, \text{kHz} \quad \text{to} \quad 100 \, \text{kHz} \]

**Figure 5**

TPS79228

OUTPUT SPECTRAL NOISE DENSITY

VS

FREQUENCY

\[ f = 100 \, \text{Hz} \quad \text{to} \quad 100 \, \text{kHz} \]

\[ f = 1 \, \text{kHz} \quad \text{to} \quad 10 \, \text{kHz} \]

\[ f = 10 \, \text{kHz} \quad \text{to} \quad 100 \, \text{kHz} \]

**Figure 6**

TPS79228

OUTPUT SPECTRAL NOISE DENSITY

VS

FREQUENCY

\[ f = 100 \, \text{Hz} \quad \text{to} \quad 100 \, \text{kHz} \]

\[ f = 1 \, \text{kHz} \quad \text{to} \quad 10 \, \text{kHz} \]

\[ f = 10 \, \text{kHz} \quad \text{to} \quad 100 \, \text{kHz} \]

**Figure 7**

TPS79228

ROOT MEAN SQUARED OUTPUT NOISE

VS

BYPASS CAPACITANCE

\[ C_{(byp)} = 0.1 \, \mu\text{F} \]

\[ C_{(byp)} = 0.001 \, \mu\text{F} \]

\[ C_{(byp)} = 0.01 \, \mu\text{F} \]

**Figure 8**

TPS79228

OUTPUT IMPEDANCE

VS

FREQUENCY

\[ f = 100 \, \text{Hz} \quad \text{to} \quad 100 \, \text{kHz} \]

\[ f = 1 \, \text{kHz} \quad \text{to} \quad 10 \, \text{kHz} \]

\[ f = 10 \, \text{kHz} \quad \text{to} \quad 100 \, \text{kHz} \]

**Figure 9**

TPS79228

DROPOUT VOLTAGE

VS

JUNCTION TEMPERATURE

\[ V_I = 3.8 \, \text{V} \]

\[ C_O = 10 \, \mu\text{F} \]

\[ C_{(byp)} = 0.1 \, \mu\text{F} \]

\[ C_{(byp)} = 0.001 \, \mu\text{F} \]

\[ C_{(byp)} = 0.01 \, \mu\text{F} \]

\[ C_{(byp)} = 0.0047 \, \mu\text{F} \]

\[ C_{(byp)} = 0.01 \, \mu\text{F} \]
TPS79201, TPS79225
TPS79228, TPS79230

TYPICAL CHARACTERISTICS

-- MARCH 2001 – REVISED MAY 2002

TPS79228
DROP OUT VOLTAGE
VS
OUTPUT CURRENT

TPS79201
DROP OUT VOLTAGE
VS
INPUT VOLTAGE

MINIMUM REQUIRED INPUT VOLTAGE
VS
OUTPUT VOLTAGE

TPS79228
RIPPLE REJECTION
VS
FREQUENCY

TPS79228
RIPPLE REJECTION
VS
FREQUENCY

TPS79228
OUTPUT VOLTAGE, ENABLE VOLTAGE
VS
TIME (START-UP)

TPS79228
LINE TRANSIENT RESPONSE

TPS79228
LOAD TRANSIENT RESPONSE

www.ti.com
TPS79228
TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)

vs
OUTPUT CURRENT

Figure 19

TPS79228
TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)

vs
OUTPUT CURRENT

Figure 20

TPS79228
TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)

vs
OUTPUT CURRENT

Figure 21
APPLICATION INFORMATION

The TPS792xx family of low-dropout (LDO) regulators have been optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (170 µA typically), and enable-input to reduce supply currents to less than 1 µA when the regulator is turned off.

A typical application circuit is shown in Figure 22.

EXTERNAL CAPACITOR REQUIREMENTS

A 0.1-µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS792xx, is required for stability and to improve transient response, noise rejection, and ripple rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS792xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 1 µF. Any 1 µF or larger ceramic capacitor is suitable. The device is also stable with a 0.47 µF ceramic capacitor with at least 75 mΩ of ESR.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS792xx has a BYPASS pin which is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the BYPASS pin, creates a low pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the BYPASS pin must be at a minimum because any leakage current creates an IR drop across the internal resistor thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current.

For example, the TPS79228 exhibits only 31 µVRMS of output voltage noise using a 0.1-µF ceramic bypass capacitor and a 1-µF ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases due to the RC time constant at the bypass pin that is created by the internal 250-kΩ resistor and external capacitor.

BOARD LAYOUT RECOMMENDATION TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac measurements like PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for VIN and VOUT, with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the ground pin of the device.
POWER DISSIPATION AND JUNCTION TEMPERATURE

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, \( P_D^{\text{max}} \), and the actual dissipation, \( P_D \), which must be less than or equal to \( P_D^{\text{max}} \).

The maximum-power-dissipation limit is determined using the following equation:

\[
P_D^{\text{max}} = \frac{T_J^{\text{max}} - T_A}{R_{\theta JA}}
\]

Where:
- \( T_J^{\text{max}} \) is the maximum allowable junction temperature.
- \( R_{\theta JA} \) is the thermal resistance junction-to-ambient for the package, see the dissipation rating table.
- \( T_A \) is the ambient temperature.

The regulator dissipation is calculated using:

\[
P_D = (V_I - V_O) \times I_O
\]

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

PROGRAMMING THE TPS79201 ADJUSTABLE LDO REGULATOR

The output voltage of the TPS79201 adjustable regulator is programmed using an external resistor divider as shown in Figure 23. The output voltage is calculated using:

\[
V_O = V_{\text{ref}} \times \left(1 + \frac{R_1}{R_2}\right)
\]

Where:
- \( V_{\text{ref}} = 1.2246 \, \text{V typ} \) (the internal reference voltage)

Resistors \( R_1 \) and \( R_2 \) should be chosen for approximately 50-\( \mu \)A divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across \( R_1/R_2 \) creates an offset voltage that artificially increases/decreases the feedback voltage and thus erroneously decreases/increases \( V_O \). The recommended design procedure is to choose \( R_2 = 30.1 \, \text{k}\Omega \) to set the divider current at 50 \( \mu \)A, \( C_1 = 15 \, \text{pF} \) for stability, and then calculate \( R_1 \) using:

\[
R_1 = \left(\frac{V_O}{V_{\text{ref}}} - 1\right) \times R_2
\]

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between \( \text{OUT} \) and \( \text{FB} \). For voltages <1.8 V, the value of this capacitor should be 100 pF. For voltages >1.8 V, the approximate value of this capacitor can be calculated as:

\[
C_1 = \frac{(3 \times 10^{-7}) \times (R_1 + R_2)}{(R_1 \times R_2)}
\]

The suggested value of this capacitor for several resistor ratios is shown in the table below. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage < 1.8 V is chosen, then the minimum recommended output capacitor is 2.2 \( \mu \)F instead of 1 \( \mu \)F.
REGULATOR PROTECTION

The TPS792xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS792xx features internal current limiting and thermal protection. During normal operation, the TPS792xx limits output current to approximately 400 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package or the absolute maximum voltage ratings of the device. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS79201DBVR</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>6</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>PEVI</td>
<td></td>
</tr>
<tr>
<td>TPS79201DBVT</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>6</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>PEVI</td>
<td></td>
</tr>
<tr>
<td>TPS79201DBVTG4</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>6</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>PEVI</td>
<td></td>
</tr>
<tr>
<td>TPS79225DBVR</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>5</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>PEXI</td>
<td></td>
</tr>
<tr>
<td>TPS79225DBVT</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>5</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>PEXI</td>
<td></td>
</tr>
<tr>
<td>TPS79225DBVTG4</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>5</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>PEXI</td>
<td></td>
</tr>
<tr>
<td>TPS79228DBVR</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>5</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>PEWI</td>
<td></td>
</tr>
<tr>
<td>TPS79228DBVRG4</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>5</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>PEWI</td>
<td></td>
</tr>
<tr>
<td>TPS79228DBVT</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>5</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>PEWI</td>
<td></td>
</tr>
<tr>
<td>TPS79228DBVTG4</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>5</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>PEWI</td>
<td></td>
</tr>
<tr>
<td>TPS79230DBVR</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>5</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>PEYI</td>
<td></td>
</tr>
<tr>
<td>TPS79230DBVRG4</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>5</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>PEYI</td>
<td></td>
</tr>
<tr>
<td>TPS79230DBVT</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>5</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>PEYI</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE**: Product device recommended for new designs.

**LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.

**OBsolete**: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
**TAPE AND REEL INFORMATION**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS79201DBVR</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>3000</td>
<td>178.0</td>
<td>9.0</td>
<td>3.23</td>
<td>3.17</td>
<td>1.37</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>TPS79201DBVT</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>250</td>
<td>178.0</td>
<td>9.0</td>
<td>3.23</td>
<td>3.17</td>
<td>1.37</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>TPS79225DBVR</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>178.0</td>
<td>9.0</td>
<td>3.23</td>
<td>3.17</td>
<td>1.37</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>TPS79225DBVT</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>250</td>
<td>178.0</td>
<td>9.0</td>
<td>3.23</td>
<td>3.17</td>
<td>1.37</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>TPS79228DBVR</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>178.0</td>
<td>9.0</td>
<td>3.23</td>
<td>3.17</td>
<td>1.37</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>TPS79228DBVT</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>250</td>
<td>178.0</td>
<td>9.0</td>
<td>3.23</td>
<td>3.17</td>
<td>1.37</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>TPS79230DBVR</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>178.0</td>
<td>9.0</td>
<td>3.23</td>
<td>3.17</td>
<td>1.37</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>TPS79230DBVT</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>250</td>
<td>178.0</td>
<td>9.0</td>
<td>3.23</td>
<td>3.17</td>
<td>1.37</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS79201DBVR</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>3000</td>
<td>180.0</td>
<td>180.0</td>
<td>18.0</td>
</tr>
<tr>
<td>TPS79201DBVT</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>250</td>
<td>180.0</td>
<td>180.0</td>
<td>18.0</td>
</tr>
<tr>
<td>TPS79225DBVR</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>180.0</td>
<td>180.0</td>
<td>18.0</td>
</tr>
<tr>
<td>TPS79225DBVT</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>250</td>
<td>180.0</td>
<td>180.0</td>
<td>18.0</td>
</tr>
<tr>
<td>TPS79228DBVR</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>180.0</td>
<td>180.0</td>
<td>18.0</td>
</tr>
<tr>
<td>TPS79228DBVT</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>250</td>
<td>180.0</td>
<td>180.0</td>
<td>18.0</td>
</tr>
<tr>
<td>TPS79230DBVR</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>180.0</td>
<td>180.0</td>
<td>18.0</td>
</tr>
<tr>
<td>TPS79230DBVT</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>250</td>
<td>180.0</td>
<td>180.0</td>
<td>18.0</td>
</tr>
</tbody>
</table>
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.
5. Reference JEDEC MO-178.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated