TPS7A16A
60-V, 5-μA $I_Q$, 100-mA, Low-Dropout Voltage Regulator With Enable and Power-Good

1 Features

- Wide input voltage range: 3 V to 60 V
- Ultra-low quiescent current: 5 μA
- Quiescent current at shutdown: 1 μA
- Output current: 100 mA
- Low dropout voltage: 60 mV at 20 mA
- Accuracy: 2%
- Available in:
  - Fixed output voltage: 3.3 V, 5 V
  - Adjustable version: Approximately 1.2 to 18.5 V
- Power-good with programmable delay
- Current-limit and thermal shutdown protections
- Stable with ceramic output capacitors: ≥ 2.2 μF
- Package: High-thermal-performance HVSSOP-8 PowerPAD™

2 Applications

- Emergency call (eCall)
- Battery management systems (BMS)
- Onboard (OBC) and wireless chargers
- DC/DC converters

3 Description

The TPS7A16A ultra-low-power, low-dropout (LDO) voltage regulator offers the benefits of ultra-low quiescent current, high input voltage, and miniaturized, high-thermal-performance packaging.

The TPS7A16A is designed for continuous or sporadic (power backup) battery-powered applications where ultra-low quiescent current is critical to extending system battery life.

The TPS7A16A offers an enable pin (EN) compatible with standard complementary metal oxide semiconductor (CMOS) logic and an integrated open-drain, active-high, power-good output (PG) with a user-programmable delay. These pins are intended for use in microcontroller-based, battery-powered applications where power-rail sequencing is required.

In addition, the TPS7A16A is ideal for generating a low-voltage supply from multicell solutions ranging from high-cell-count, power-tool packs to automotive applications. Not only can this device supply a well-regulated voltage rail, but the TPS7A16A can also withstand and maintain regulation during voltage transients. These features translate to simpler and more cost-effective, electrical surge-protection circuitry.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS7A16A</td>
<td>HVSSOP PowerPAD (8)</td>
<td>3.00 mm × 3.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic
Table of Contents

1 Features ................................................................. 1
2 Applications ......................................................... 1
3 Description ........................................................... 1
4 Revision History ..................................................... 2
5 Pin Configuration and Functions ................................. 3
6 Specifications ......................................................... 4
   6.1 Absolute Maximum Ratings ............................... 4
   6.2 ESD Ratings .................................................... 4
   6.3 Recommended Operating Conditions .................... 4
   6.4 Thermal Information .......................................... 5
   6.5 Electrical Characteristics ................................. 5
   6.6 Typical Characteristics ...................................... 6
7 Detailed Description ................................................ 9
   7.1 Overview ...................................................... 9
   7.2 Functional Block Diagram .................................. 9
   7.3 Feature Description ........................................... 9
   7.4 Device Functional Modes .................................... 10
8 Application and Implementation ............................... 11
   8.1 Application Information ..................................... 11
   8.2 Typical Application .......................................... 11
9 Power Supply Recommendations ............................... 14
10 Layout ............................................................... 14
   10.1 Layout Guidelines .......................................... 14
   10.2 Layout Examples ........................................... 15
11 Device and Documentation Support ........................... 17
   11.1 Device Support ............................................... 17
   11.2 Receiving Notification of Documentation Updates .......... 17
   11.3 Support Resources .......................................... 17
   11.4 Trademarks .................................................. 17
   11.5 Electrostatic Discharge Caution ......................... 17
   11.6 Glossary ..................................................... 17
12 Mechanical, Packaging, and Orderable Information ................. 17
   12.1 Mechanical Data ............................................ 18

4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>May 2022</td>
<td>*</td>
<td>Initial release</td>
</tr>
</tbody>
</table>
5 Pin Configuration and Functions

![Pin Configuration Diagram]

**Figure 5-1.** DGN Package, 8-Pin HVSSOP PowerPAD With Exposed Thermal Pad (Top View)

NC – No internal connection

**Table 5-1. Pin Functions**

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>DELAY</td>
<td>7</td>
<td>O</td>
</tr>
<tr>
<td>EN</td>
<td>5</td>
<td>I</td>
</tr>
<tr>
<td>FB/DNC</td>
<td>2</td>
<td>I</td>
</tr>
<tr>
<td>GND</td>
<td>4</td>
<td>—</td>
</tr>
<tr>
<td>IN</td>
<td>8</td>
<td>I</td>
</tr>
<tr>
<td>NC</td>
<td>6</td>
<td>—</td>
</tr>
<tr>
<td>OUT</td>
<td>1</td>
<td>O</td>
</tr>
<tr>
<td>PG</td>
<td>3</td>
<td>O</td>
</tr>
<tr>
<td>Thermal pad</td>
<td>Pad</td>
<td>—</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Voltage</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN pin to GND pin</td>
<td>–0.3</td>
<td>62</td>
<td>V</td>
</tr>
<tr>
<td>OUT pin to GND pin</td>
<td>–0.3</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>OUT pin to IN pin</td>
<td>–62</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>FB pin to GND pin</td>
<td>–0.3</td>
<td>3</td>
<td>V</td>
</tr>
<tr>
<td>FB pin to IN pin</td>
<td>–62</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>EN pin to IN pin</td>
<td>–62</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>EN pin to GND pin</td>
<td>–62</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>PG pin to GND pin</td>
<td>–0.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>DELAY pin to GND pin</td>
<td>–0.3</td>
<td>5.5</td>
<td>V</td>
</tr>
</tbody>
</table>

Current

- Peak output: Internally limited

Temperature

- Operating virtual junction, \(T_J\), absolute maximum\(^{(2)}\): –40 to 150°C
- Storage, \(T_{STG}\): –65 to 150°C

\(\text{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(\text{(2)}\) Permanent damage does not occur to the part operating within this range, though electrical performance is not specified outside the operating ambient temperature range.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(^{(2)})</td>
<td>±750</td>
<td>V</td>
</tr>
<tr>
<td>Corner pins (OUT, GND, IN, and EN)</td>
<td>±500</td>
<td>V</td>
</tr>
<tr>
<td>Other pins</td>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

\(\text{(1)}\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

\(\text{(2)}\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{IN})</td>
<td>Input voltage</td>
<td>3</td>
<td>60</td>
</tr>
<tr>
<td>(V_{OUT})</td>
<td>Output voltage</td>
<td>1.2</td>
<td>18.5</td>
</tr>
<tr>
<td>(EN)</td>
<td>EN pin voltage</td>
<td>0</td>
<td>(V_{IN})</td>
</tr>
<tr>
<td>EN pin slew-rate, voltage ramp-up</td>
<td>1.5</td>
<td>V/(\mu s)</td>
<td></td>
</tr>
<tr>
<td>(\text{DELAY})</td>
<td>Delay pin voltage</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>(\text{PG})</td>
<td>Power-good pin voltage</td>
<td>0</td>
<td>5</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>DGN (HVSSOP)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\text{JA}}$</td>
<td>52.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{\text{J(top)}}$</td>
<td>72.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{\text{JB}}$</td>
<td>24.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{\text{JT}}$</td>
<td>2.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{\text{JB}}$</td>
<td>24.0</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{\text{J(bottom)}}$</td>
<td>10.1</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at $T_A$ = −40°C to +125°C, $V_{\text{IN}} = V_{\text{OUT(NOM)}} + 500$ mV or $V_{\text{IN}} = 3$ V (whichever is greater), $V_{\text{EN}} = V_{\text{IN}}$, $I_{\text{OUT}} = 10$ μA, $C_{\text{IN}} = 2.2$ μF, $C_{\text{OUT}} = 2.2$ μF, and FB tied to OUT (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{IN}}$</td>
<td>Input voltage range</td>
<td>3</td>
<td>60</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{REF}}$</td>
<td>Internal reference</td>
<td>$T_A = 25°C$, $V_{\text{FB}} = V_{\text{REF}}$, $V_{\text{IN}} = 3$ V, $I_{\text{OUT}} = 10$ μA</td>
<td>1.169</td>
<td>1.193</td>
<td>1.217</td>
</tr>
<tr>
<td>$V_{\text{UVLO}}$</td>
<td>Undervoltage lockout threshold</td>
<td>2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{\text{OUT}}$</td>
<td>Output voltage range</td>
<td>$V_{\text{IN}} \geq V_{\text{OUT(NOM)}} + 0.5$ V</td>
<td>$V_{\text{REF}}$</td>
<td>18.5</td>
<td>V</td>
</tr>
<tr>
<td>Overall $V_{\text{OUT}}$ accuracy</td>
<td>$V_{\text{OUT}} \leq 0.5$ V or $V_{\text{IN}} \leq 60$ V(1), $10$ μA $\leq I_{\text{OUT}} \leq 100$ mA</td>
<td>$-2%$</td>
<td>$2%$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Delta V_{\text{O(\text{L})}}$</td>
<td>Line regulation</td>
<td>3 V $\leq V_{\text{IN}} \leq 60$ V</td>
<td>$\pm 1$</td>
<td>%$V_{\text{OUT}}$</td>
<td></td>
</tr>
<tr>
<td>$\Delta V_{\text{O(\text{D})}}$</td>
<td>Load regulation</td>
<td>$10$ μA $\leq I_{\text{OUT}} \leq 100$ mA</td>
<td>$\pm 1$</td>
<td>%$V_{\text{OUT}}$</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{DO}}$</td>
<td>Dropout voltage</td>
<td>$V_{\text{IN}} = 0.95 V_{\text{OUT(NOM)}}$, $I_{\text{OUT}} = 20$ mA</td>
<td>60</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{IN}} = 0.95 V_{\text{OUT(NOM)}}$, $I_{\text{OUT}} = 100$ mA</td>
<td>265</td>
<td>500</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{\text{LIM}}$</td>
<td>Current limit</td>
<td>$V_{\text{OUT}} = 90% V_{\text{OUT(NOM)}}$, $V_{\text{IN}} = V_{\text{OUT(NOM)}} + 1$ V(3)</td>
<td>101</td>
<td>225</td>
<td>400</td>
</tr>
<tr>
<td>$V_{\text{OUT}} = 90% V_{\text{OUT(NOM)}}$, $V_{\text{IN}} = 3$ V(4)</td>
<td>101</td>
<td>225</td>
<td>400</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{\text{GND}}$</td>
<td>Ground current</td>
<td>$3$ V $\leq V_{\text{IN}} \leq 60$ V, $I_{\text{OUT}} = 10$ μA</td>
<td>5</td>
<td>15</td>
<td>μA</td>
</tr>
<tr>
<td>$I_{\text{OUT}} = 100$ mA, $V_{\text{OUT}} = 1.2$ V</td>
<td>60</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{\text{SHDN}}$</td>
<td>Shutdown supply current</td>
<td>$V_{\text{EN}} = 0.4$ V, $V_{\text{IN}} = 12$ V</td>
<td>0.59</td>
<td>5.0</td>
<td>μA</td>
</tr>
<tr>
<td>$I_{\text{FB}}$</td>
<td>Feedback current(2)</td>
<td>$-1$</td>
<td>$0$</td>
<td>$1$</td>
<td>μA</td>
</tr>
<tr>
<td>$I_{\text{EN}}$</td>
<td>Enable current</td>
<td>$3$ V $\leq V_{\text{IN}} \leq 12$ V, $V_{\text{IN}} = V_{\text{EN}}$</td>
<td>$-1$</td>
<td>0.01</td>
<td>1</td>
</tr>
<tr>
<td>$I_{\text{EN, HI}}$</td>
<td>Enable high-level voltage</td>
<td>1.2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{\text{EN, LO}}$</td>
<td>Enable low-level voltage</td>
<td>0.3</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{\text{VT}}$</td>
<td>PG trip threshold</td>
<td>OUT pin floating, $V_{\text{FB}}$ increasing, $V_{\text{IN}} \geq V_{\text{IN, MIN}}$</td>
<td>85</td>
<td>95</td>
<td>%$V_{\text{OUT}}$</td>
</tr>
<tr>
<td>OUT pin floating, $V_{\text{FB}}$ decreasing, $V_{\text{IN}} \geq V_{\text{IN, MIN}}$</td>
<td>83</td>
<td>93</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{\text{HYS}}$</td>
<td>PG trip hysteresis</td>
<td>2.3</td>
<td>%$V_{\text{OUT}}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{\text{PG, LO}}$</td>
<td>PG output low voltage</td>
<td>OUT pin floating, $V_{\text{FB}} = 80% V_{\text{REF}}$, $I_{\text{IO}} = 100$ μA</td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{\text{PG, LKG}}$</td>
<td>PG leakage current</td>
<td>$V_{\text{PG}} = V_{\text{OUT(NOM)}}$</td>
<td>$-1$</td>
<td>1</td>
<td>μA</td>
</tr>
<tr>
<td>$I_{\text{DELAY}}$</td>
<td>DELAY pin current</td>
<td>1</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$PSRR$</td>
<td>Power-supply rejection ratio</td>
<td>$V_{\text{IN}} = 3$ V, $V_{\text{OUT(NOM)}} = V_{\text{REF}}$, $C_{\text{OUT}} = 10$ μF, $f = 100$ Hz</td>
<td>50</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>$T_{\text{SD}}$</td>
<td>Thermal shutdown temperature</td>
<td>Shutdown, temperature increasing</td>
<td>175</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Reset, temperature decreasing</td>
<td>155</td>
<td>°C</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Maximum input voltage is limited to 24 V because of the package power dissipation limitations at full load ($P = (V_{\text{IN}} - V_{\text{OUT}}) \times I_{\text{OUT}} = (24$ V $- V_{\text{REF}}) \times 50$ mA $= 1.14$ W). The device is capable of sourcing a maximum current of 50 mA at higher input voltages as long as the power dissipated is within the thermal limits of the package plus any external heat sinking.

(2) $I_{\text{FB}} > 0$ μA flows out of the device.

(3) For fixed output voltages only.

(4) For adjustable output only, where $V_{\text{OUT}} = 1.2$ V.
6.6 Typical Characteristics

at $T_A = -40°C$ to $125°C$, $V_{IN} = V_{OUT(NOM)} + 0.5$ V or $V_{IN} = 3$ V (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 10 \mu A$, $C_{IN} = 1 \mu F$, $C_{OUT} = 2.2 \mu F$, and FB tied to OUT (unless otherwise noted)

---

**Figure 6-1. Quiescent Current vs Input Voltage**

**Figure 6-2. Shutdown Current vs Input Voltage**

**Figure 6-3. Ground Current vs Output Current**

**Figure 6-4. Dropout Voltage vs Output Current**

**Figure 6-5. Feedback Voltage vs Input Voltage**

**Figure 6-6. Line Regulation**
6.6 Typical Characteristics (continued)

at $T_A = -40°C$ to $125°C$, $V_{IN} = V_{OUT(NOM)} + 0.5$ V or $V_{IN} = 3$ V (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 10 \mu$A, $C_{IN} = 1 \mu$F, $C_{OUT} = 2.2 \mu$F, and FB tied to OUT (unless otherwise noted)
6.6 Typical Characteristics (continued)

at $T_A = -40^\circ C$ to $125^\circ C$, $V_{IN} = V_{OUT(\text{NOM})} + 0.5$ V or $V_{IN} = 3$ V (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 10$ μA, $C_{IN} = 1$ μF, $C_{OUT} = 2.2$ μF, and FB tied to OUT (unless otherwise noted)

![Figure 6-13. Power-Good Delay](image-url)
7 Detailed Description

7.1 Overview

The TPS7A16A is an ultra-low-power, low-dropout (LDO) voltage regulator that offers the benefits of ultra-low quiescent current, high input voltage, and miniaturized, high thermal-performance packaging. The TPS7A16A also offers an enable pin (EN) and an integrated open-drain, active-high, power-good output (PG) with a user-programmable delay.

7.2 Functional Block Diagram

![Functional Block Diagram](image)

7.3 Feature Description

7.3.1 Enable (EN)

The enable pin is a high-voltage-tolerant pin. A high input on EN actives the device and turns on the regulator. For self-bias applications, connect this input to the IN pin. Ensure that $V_{EN} \leq V_{IN}$ at all times.

When the enable signal is comprised of pulse-width modulation (PWM) pulses, the slew rate of the rising and falling edges must be less than 1.5 V/µs. Adding a 0.1-µF capacitor from the EN pin to GND is recommended.

7.3.2 Regulated Output ($V_{OUT}$)

The OUT pin is the regulated output based on the required voltage. The output has current limitation. During initial power up, the regulator has a soft-start incorporated to control the initial current through the pass element. In the event that the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the undervoltage lockout (UVLO) threshold, the regulator shuts down until the input voltage recovers above the minimum start-up level.

7.3.3 PG Delay Timer (DELAY)

The power-good delay time ($t_{DELAY}$) is defined as the time period from when $V_{OUT}$ exceeds the PG trip threshold voltage ($V_{IT}$) to when the PG output is high. This power-good delay time is set by an external capacitor ($C_{DELAY}$) connected from the DELAY pin to GND; this capacitor is charged from 0 V to approximately 1.8 V by the DELAY pin current ($I_{DELAY}$) when $V_{OUT}$ exceeds the PG trip threshold ($V_{IT}$).
7.4 Device Functional Modes

7.4.1 Power-Good

The power-good (PG) pin is an open-drain output and can be connected to any 5.5-V or lower rail through an external pullup resistor. When no $C_{\text{DELAY}}$ is used, the PG output is high-impedance when $V_{\text{OUT}}$ is greater than the PG trip threshold ($V_{\text{IT}}$). If $V_{\text{OUT}}$ drops below $V_{\text{IT}}$, the open-drain output turns on and pulls the PG output low. If output voltage monitoring is not needed, the PG pin can be left floating or connected to GND.

To ensure proper operation of the power-good feature, maintain $V_{\text{IN}} \geq 3$ V ($V_{\text{IN_MIN}}$).

7.4.1.1 Power-Good Delay and Delay Capacitor

The power-good delay time ($t_{\text{DELAY}}$) is defined as the time period from when $V_{\text{OUT}}$ exceeds the PG trip threshold voltage ($V_{\text{IT}}$) to when the PG output is high. This power-good delay time is set by an external capacitor ($C_{\text{DELAY}}$) connected from the DELAY pin to GND; this capacitor is charged from 0 V to approximately 1.8 V by the DELAY pin current ($I_{\text{DELAY}}$) when $V_{\text{OUT}}$ exceeds the PG trip threshold ($V_{\text{IT}}$).

When $C_{\text{DELAY}}$ is used, the PG output is high-impedance when $V_{\text{OUT}}$ exceeds $V_{\text{IT}}$, and $V_{\text{DELAY}}$ exceeds $V_{\text{REF}}$.

The power-good delay time can be calculated using: $t_{\text{DELAY}} = (C_{\text{DELAY}} \times V_{\text{REF}}) / I_{\text{DELAY}}$. For example, when $C_{\text{DELAY}} = 10$ nF, the PG delay time is approximately 12 ms; that is, $(10 \text{ nF} \times 1.193 \text{ V}) / 1 \mu\text{A} = 11.93$ ms.
8 Application and Implementation

**Note**
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information
The TPS7A16A offers the benefit of ultra-low quiescent current, high input voltage, and miniaturized, high-thermal-performance packaging.

The TPS7A16A is designed for continuous or sporadic (power backup) battery-operated applications where ultra-low quiescent current is critical to extending system battery life.

8.2 Typical Application
8.2.1 TPS7A16A Circuit as an Adjustable Regulator

![Schematic Diagram]

**Figure 8-1. The TPS7A16A Circuit as an Adjustable Regulator Schematic**

8.2.1.1 Design Requirements

Table 8-1 lists the design parameters for this application.

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>5.5 V to 40 V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>5 V</td>
</tr>
<tr>
<td>Output current rating</td>
<td>100 mA</td>
</tr>
<tr>
<td>Output capacitor range</td>
<td>2.2 µF to 100 µF</td>
</tr>
<tr>
<td>Delay capacitor range</td>
<td>100 pF to 100 nF</td>
</tr>
</tbody>
</table>
8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Adjustable Voltage Operation

The TPS7A16A has an output voltage range from 1.194 V to 20 V. As shown in Figure 8-2, the nominal output of the device is set by two external resistors.

![Figure 8-2. Adjustable Operation](image)

Equation 1 can calculate \( R_1 \) and \( R_2 \) for any output voltage range:

\[
R_1 = R_2 \left( \frac{V_{OUT}}{V_{REF}} - 1 \right)
\]

(1)

8.2.1.2.1.1 Resistor Selection

Use resistors in the order of MΩ to keep the overall quiescent current of the system as low as possible (by making the current used by the resistor divider negligible compared to the quiescent current of the device).

If greater voltage accuracy is required, take into account the voltage offset contributions as a result of feedback current and use 0.1% tolerance resistors.

Table 8-2 shows the resistor combination to achieve an output for a few of the most common rails using commercially available 0.1% tolerance resistors to maximize nominal voltage accuracy, while adhering to the formula in Equation 1.

<table>
<thead>
<tr>
<th>( V_{OUT} )</th>
<th>( R_1 )</th>
<th>( R_2 )</th>
<th>( \frac{V_{OUT}}{(R_1 + R_2)} \times I_Q )</th>
<th>NOMINAL ACCURACY</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.194 V</td>
<td>0 Ω</td>
<td>( \infty )</td>
<td>0 μA</td>
<td>±2%</td>
</tr>
<tr>
<td>1.8 V</td>
<td>1.18 MΩ</td>
<td>2.32 MΩ</td>
<td>514 nA</td>
<td>±(2% + 0.14%)</td>
</tr>
<tr>
<td>2.5 V</td>
<td>1.5 MΩ</td>
<td>1.37 MΩ</td>
<td>871 nA</td>
<td>±(2% + 0.16%)</td>
</tr>
<tr>
<td>3.3 V</td>
<td>2 MΩ</td>
<td>1.13 MΩ</td>
<td>1056 nA</td>
<td>±(2% + 0.35%)</td>
</tr>
<tr>
<td>5 V</td>
<td>3.4 MΩ</td>
<td>1.07 MΩ</td>
<td>1115 nA</td>
<td>±(2% + 0.39%)</td>
</tr>
<tr>
<td>10 V</td>
<td>7.87 MΩ</td>
<td>1.07 MΩ</td>
<td>1115 nA</td>
<td>±(2% + 0.42%)</td>
</tr>
<tr>
<td>12 V</td>
<td>14.3 MΩ</td>
<td>1.58 MΩ</td>
<td>755 nA</td>
<td>±(2% + 0.18%)</td>
</tr>
<tr>
<td>15 V</td>
<td>42.2 MΩ</td>
<td>3.65 MΩ</td>
<td>327 nA</td>
<td>±(2% + 0.19%)</td>
</tr>
<tr>
<td>18 V</td>
<td>16.2 MΩ</td>
<td>1.15 MΩ</td>
<td>1038 nA</td>
<td>±(2% + 0.26%)</td>
</tr>
</tbody>
</table>

Close attention must be paid to board contamination when using high-value resistors; board contaminants can significantly impact voltage accuracy. If board cleaning measures cannot be ensured, consider using a fixed-voltage version of the TPS7A16A or using resistors in the order of hundreds or tens of kΩ.
8.2.1.2.2 Capacitor Recommendations

Use low equivalent-series-resistance (ESR) capacitors for the input, output, and feed-forward capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved overtemperature performance, but ceramic X5R capacitors are the most cost-effective and are available in higher values.

However, high-ESR capacitors can degrade PSRR.

8.2.1.2.3 Input and Output Capacitor Requirements

The TPS7A16A ultra-low-power, high-voltage linear regulator achieves stability with a minimum input capacitance of 0.1 µF and output capacitance of 2.2 µF; however, use a 10-µF ceramic capacitor to maximize ac performance.

8.2.1.2.4 Feed-Forward Capacitor (Only for Adjustable Version)

Although a feed-forward capacitor (C_{FF}) from OUT to FB is not needed to achieve stability, using a 0.01-µF feed-forward capacitor helps maximize ac performance.

8.2.1.2.5 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases the duration of the transient response.

8.2.1.3 Application Curves

![Figure 8-3](channel1 is \(V_{OUT}\), channel 2 is PG, channel 4 is \(I_{OUT}\), \(V_{IN}\) is 12 V and Ready Before EN)

![Figure 8-4](channel1 is \(V_{OUT}\), channel 2 is PG, channel 3 is EN, channel 4 is \(I_{OUT}\), and \(V_{IN}\) is 12 V Connected to EN)
9 Power Supply Recommendations

The device is designed for operation from an input voltage supply with a range between 3 V and 60 V. This input supply must be well regulated. The TPS7A16A ultra-low-power, high-voltage linear regulator achieves stability with a minimum input capacitance of 0.1 µF and output capacitance of 2.2 µF; however, use a 10-µF ceramic capacitor to maximize ac performance.

10 Layout

10.1 Layout Guidelines

To improve ac performance such as PSRR, output noise, and transient response, the board is recommended to be designed with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. This grounding scheme is commonly referred to as star grounding. In addition, directly connect the ground connection for the output capacitor to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and ensure stability. Every capacitor must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they can impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance denoted in this document, use the same layout pattern used for the TPS7A16A evaluation board, available at www.ti.com.

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, bypass the IN pin to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric.

Acceptable performance can be obtained with alternative PCB layouts; however, the layout and the schematic have been shown to produce good results and are meant as a guideline.

Figure 10-1 illustrates the schematic for the suggested layout. Figure 10-2 and Figure 10-3 depict the top and bottom printed circuit board (PCB) layers for the suggested layout, respectively.

10.1.1 Additional Layout Considerations

The high impedance of the FB pin makes the regulator sensitive to parasitic capacitances that can couple undesirable signals from nearby components (especially from logic and digital devices, such as microcontrollers and microprocessors). These capacitively-coupled signals can produce undesirable output voltage transients. Thus, use a fixed-voltage version of the TPS7A16A, or isolate the FB node by flooding the local PCB area with ground-plane copper to minimize any undesirable signal coupling.

10.1.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Using heavier copper increases the effectiveness of removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heat sink effectiveness.

Power dissipation depends on input voltage and load conditions. As Equation 2 shows, power dissipation \( P_D \) is equal to the product of the output current times the voltage drop across the output pass transistor:

\[
P_D = (V_{IN} - V_{OUT}) I_{OUT}
\]  

(2)
10.1.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting the regulator from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat-spreading area. For reliable operation, limit junction temperature to a maximum of 125°C at the worst-case ambient temperature for a given application. To estimate the margin of safety in a complete design (including the copper heat-spreading area), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, trigger thermal protection at least 45°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A16A is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS7A16A into thermal shutdown degrades device reliability.

10.2 Layout Examples

![Schematic for Suggested Layout](image-url)

Figure 10-1. Schematic for Suggested Layout
Figure 10-2. Suggested Layout: Top Layer

Figure 10-3. Suggested Layout: Bottom Layer
11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>VOUT, PACKAGE, QUANTITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS7A16xxAyyy</td>
<td>xx is the nominal output voltage. Two digits are used in the ordering number (for example, 33 = 3.3 V; 01 = adjustable). yyy is the package designator. z is the package quantity. R is for reel (2500 pieces for DGN).</td>
</tr>
</tbody>
</table>

1. For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on Subscribe to updates to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
12.1 Mechanical Data

PowerPAD™ VSSOP - 1.1 mm max height

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.
### Example Stencil Design

**DGN0008A**

**PowerPAD™ VSSOP - 1.1 mm max height**

**Small Outline Package**

---

#### Solder Stencil Opening

- **METAL COVERED BY SOLDER MASK**
  - SEE TABLE FOR DIFFERENT OPENINGS FOR OTHER STENCIL THICKNESSES

---

#### Solder Paste Example

**Exposed Pad 9**

100% Printed Solder Coverage by Area

**Scale**: 15X

---

#### Stencil Thickness

<table>
<thead>
<tr>
<th>Stencil Thickness</th>
<th>Solder Stencil Opening</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1</td>
<td>2.10 X 2.24</td>
</tr>
<tr>
<td>0.125</td>
<td>1.88 X 2.00 (SHOWN)</td>
</tr>
<tr>
<td>0.15</td>
<td>1.72 X 1.83</td>
</tr>
<tr>
<td>0.175</td>
<td>1.59 X 1.69</td>
</tr>
</tbody>
</table>

---

#### Notes (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

11. Board assembly site may have different recommendations for stencil design.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PINS</th>
<th>Package Qty</th>
<th>Lead finish/Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS7A1601ADGNR</td>
<td>ACTIVE</td>
<td>HVSSOP</td>
<td>DGN</td>
<td>8</td>
<td>2500</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>-40 to 150</td>
<td>2RDT</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TPS7A16A :**

---

Addendum-Page 1
Automotive: TPS7A16A-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**
- Reel Diameter
- Reel Width (W1)

**TAPE DIMENSIONS**
- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**
- Pocket Quadrants
- Sprocket Holes
- User Direction of Feed

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS7A1601ADGNR</td>
<td>HVSSOP</td>
<td>DGN</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>5.3</td>
<td>3.4</td>
<td>1.4</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS7A1601ADGNR</td>
<td>HVSSOP</td>
<td>DGN</td>
<td>8</td>
<td>2500</td>
<td>366.0</td>
<td>364.0</td>
<td>50.0</td>
</tr>
</tbody>
</table>
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