TPS7A20 300-mA, Ultra-Low-Noise, Low-I_Q, High PSRR LDO

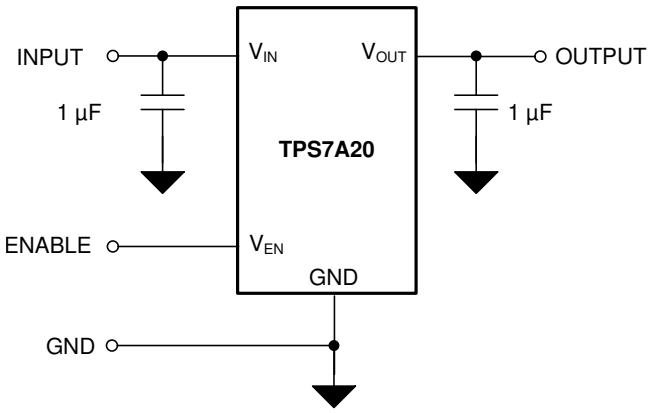
1 Features

- Low output voltage noise: 6 μV_{RMS}
  - No noise-bypass capacitor required
- High PSRR: 85 dB at 1 kHz
- Very low I_Q: 6.5 µA
- Input voltage range: 1.6 V to 6.0 V
- Output voltage range: 0.8 V to 5.5 V
- Output voltage tolerance: ±1.5% (max)
- Very low dropout:
  - 140 mV (max) at 300 mA (V_{OUT} = 3.3 V)
- Low inrush current
- Smart enable pulldown
- Stable with 1-µF minimum ceramic output capacitors
- Packages:
  - 1-mm × 1-mm X2SON
  - 0.603-mm × 0.603-mm DSBGA (preview)
  - 2.90-mm × 1.60-mm SOT23-5 (preview)

2 Applications

- Smartphones and tablets
- IP network cameras
- Portable medical equipment
- Smart meters and field transmitters
- Motor drives
- Wearables

Simplified Schematic



3 Description

The TPS7A20 is an ultra-small, low-dropout (LDO) linear regulator that can source 300 mA of output current. The TPS7A20 is designed to provide low noise, high PSRR, and excellent load line transient performance that can meet the requirements of RF and other sensitive analog circuits. Using innovative design techniques, the TPS7A20 offers an ultra-low noise performance without the addition of a noise bypass capacitor. The TPS7A20 also provides the advantage of low quiescent current, which can be ideal for any battery-powered applications. The TPS7A20 can be used for a wide variety of applications by supporting an input voltage range from 1.6 V to 6.0 V and a wide output range of 0.8 V to 5.5 V. The device uses a precision reference circuit to provide a maximum accuracy of 1.5% over load, line, and temperature variations

The TPS7A20 features an internal soft-start to lower the inrush current, thus minimizing the input voltage drop during start up. The device is stable with small ceramic capacitors, allowing for a small overall solution size.

The TPS7A20 has a smart enable input circuit with an internally controlled pulldown resistor that keeps the LDO disabled even when the EN pin is left floating and helps eliminate the external components used to pulldown the EN pin.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A20	X2SON (4)	1.00 mm × 1.00 mm
	DSBGA (4)(2)	0.603 mm × 0.603 mm
	SOT-23 (5)(2)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Preview package.

ADVANCE INFORMATION

Table of Contents

ADVANCE INFORMATION

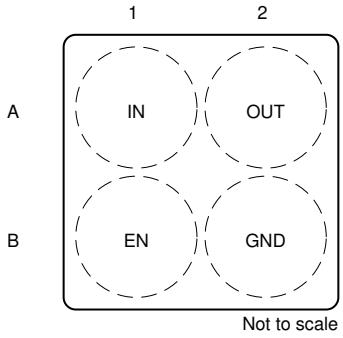
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2020) to Revision A	Page
• Changed *low output voltage noise* from 7 μV_{RMS} to 6 μV_{RMS} in *Features* section	1
• Changed YEN package designator to YWD throughout document	3
• Changed DQN pin out drawing from *Bottom View* to *Top View*	4

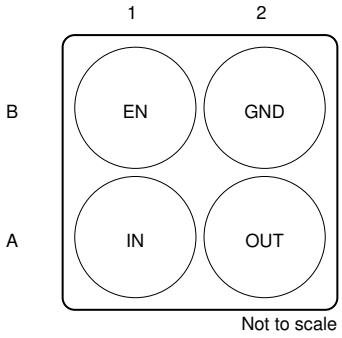
5 Pin Configuration and Functions

YWD Package (Preview)
4-Pin DSBGA
Top View



Not to scale

YWD Package (Preview)
4-Pin DSBGA
Bottom View



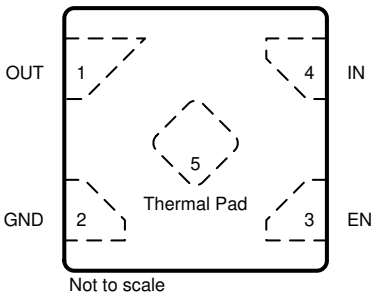
Not to scale

Pin Functions: DSBGA

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	IN	I	Input voltage supply. For best transient response and to minimize input impedance, use the recommended value or larger capacitor from IN to ground as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the IN and GND pins of the device as possible.
A2	OUT	O	Regulated output voltage. A minimum 1-µF low equivalent series resistance (ESR) capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger capacitor from OUT to ground. Follow the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUT and GND pins of the device as possible. An internal 150-Ω (typical) pulldown resistor prevents a charge from remaining on V_{OUT} when the regulator is in shutdown mode ($V_{EN} < V_{IL}$).
B1	EN	I	Enable input. A low voltage ($< V_{IL}$) on this pin turns the regulator off and discharges the output pin to GND. A high voltage ($> V_{IH}$) on this pin enables the regulator output. This pin has an internal 500-kΩ pulldown resistor to hold the regulator off by default.
B2	GND	—	Common ground.

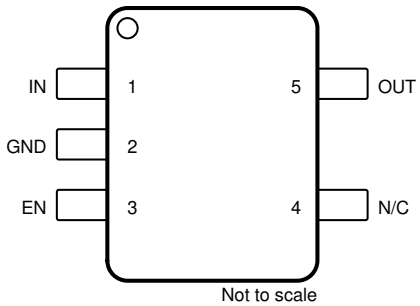
ADVANCE INFORMATION

DQN Package
4-Pin X2SON
Top View



Not to scale

DBV Package (Preview)
5-Pin SOT-23
Top View



Not to scale

Pin Functions: X2SON, SOT-23

PIN			I/O	DESCRIPTION
NAME	X2SON	SOT-23		
IN	4	1	I	Input voltage supply. For best transient response and to minimize input impedance, use the recommended value or larger capacitor from IN to ground as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the IN and GND pins of the device as possible.
OUT	1	5	O	Regulated output voltage. A minimum 1-µF low ESR capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger capacitor from OUT to ground. Follow the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUT and GND pins of the device as possible. An internal 150-Ω (typical) pulldown resistor prevents a charge from remaining on V_{OUT} when the regulator is in shutdown mode ($V_{EN} < V_{IL}$).
EN	3	3	I	Enable input. A low voltage ($< V_{IL}$) on this pin turns the regulator off and discharges the output pin to GND. A high voltage ($> V_{IH}$) on this pin enables the regulator output. This pin has an internal 500-kΩ pulldown resistor to hold the regulator off by default.
GND	2	2	—	Common ground.
N/C	—	4	—	No internal electrical connection.
Thermal Pad	5	—	—	Thermal pad for the X2SON package. Connect this pad to GND or leave floating. Do not connect to any potential other than GND. Connect the thermal pad to a large-area ground plane for best thermal performance.

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	6.5	V
	V_{OUT}	–0.3	V_{IN} + 0.3 or 6.0V(2)	
	V_{EN}	–0.3	6.5	
Current	Maximum output current	Internally limited		A
Temperature	Operating junction temperature, T_J	-40	125	°C
	Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, and functional operation of the device at these or any other conditionsbeyond those indicated under*Recommended Operating Conditions*is not implied. Exposure to absolute-maximum-rated conditions forextended periods may affect device reliability.
(2) Maximum is V_{IN} + 0.3 V, or 6.0 V, whichever is smaller

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	1.6		6.0	V
V_{EN}	Enable input voltage	0		6.0	V
V_{OUT}	Output voltage	0.8		5.5	V
I_{OUT}	Output current	0		300	mA
C_{IN}	Input capacitor		1		µF
C_{OUT}	Output capacitor(1) (2)	1		200	µF
ESR	Output Capacitor			80	mΩ
T_J	Operating junction temperature	–40		125	°C

(1) Effective output capacitance of 0.5 µF minimum is required for stability
(2) 200 µF is the maximum derated capacitance that can be used for stability

ADVANCE INFORMATION

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A20 DBV (2) (SOT-23) 5 PINS	TPS7A20 DQN (X2SON) 4 PINS	TPS7A20 YWD(2) (DSBGA) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	179.1	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	137.6	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	116.3	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	6.1	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	116.3	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	112.3	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Preview Package

6.5 Electrical Characteristics

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6V, whichever is greater, V_{EN} = 1.0 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF (unless otherwise noted); all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔV_{OUT}	Output voltage tolerance	V_{IN} = ($V_{OUT(NOM)}$ + 0.3 V) to 6.0 V, I_{OUT} = 1 mA to 300 mA, V_{OUT} ≥ 1.5 V		–1.5		1.5	%
		V_{IN} = ($V_{OUT(NOM)}$ + 0.5 V) to 6.0 V, I_{OUT} = 1 mA to 300 mA V_{OUT} < 1.5 V		–30		30	mV
ΔV_{OUT} (ΔV_{IN})	Line regulation	V_{IN} = ($V_{OUT(NOM)}$ + 0.3 V) to 6.0 V, I_{OUT} = 1 mA			0.03		%/V
ΔV_{OUT}(ΔI_{OUT})	Load regulation	I_{OUT} = 1 mA to 300 mA			0.003		%/mA
I_{GND}	Ground current	V_{EN} = V_{IN}, V_{IN} = 6.0 V, I_{OUT} = 0 mA	T_J = 25°C		6.5	8	µA
			T_J = –40°C to 85°C			10	
			T_J = –40°C to 125°C			20	
		V_{EN} = V_{IN}, V_{IN} = 6.0 V, I_{OUT} = 300 mA			2000		
I_{SHTDWN}	Shutdown current	V_{EN} = 0 V (disabled), V_{IN} = 6.0 V, T_J = 25°C			0.15	0.5	µA
$I_{GND(DO)}$	Ground current in dropout	V_{IN} ≤ $V_{OUT(NOM)}$, I_{OUT} = 0 mA			6.5	20	µA
V_{DO}	Dropout voltage	I_{OUT} = 300 mA, V_{OUT} = 95% x $V_{OUT(NOM)}$	0.8 V ≤ VOUT < 1.0 V			690	mV
			1.0 V ≤ VOUT < 1.2 V			490	
			1.2 V ≤ VOUT < 1.5 V			355	
			1.5 V ≤ VOUT < 2.5 V			240	
			2.5 V ≤ VOUT < 3.3 V			140	
			3.3 V ≤ VOUT ≤ 5.5 V			140	
I_{CL}	Output current limit	V_{OUT} = 0.9 x $V_{OUT(NOM)}$, V_{IN} = $V_{OUT(NOM)}$ + V_{DO}		360	520	730	mA
I_{SC}	Short-circuit current limit	V_{OUT} = 0 V			160		mA
PSRR	Power-supply rejection ratio	I_{OUT} = 20 mA, V_{IN} = V_{OUT} + 1.0 V	f = 1 kHz		85		dB
			f = 10 kHz		73		dB
			f = 100 kHz		70		dB
			f = 1 MHz		49		dB
PSRR	Power-supply rejection ratio	I_{OUT} = 300 mA, V_{IN} = V_{OUT} + 1.0 V	f = 1 kHz		85		dB
			f = 10 kHz		73		dB
			f = 100 kHz		56		dB
			f = 1 MHz		48		dB
V_N	Output noise voltage	BW = 10 Hz to 100 kHz V_{OUT} = 2.8V	I_{OUT} = 300 mA		6		μV_{RMS}
			I_{OUT} = 1 mA		10		
$R_{PULLDOWN}$	Output automatic discharge pulldown resistance	V_{EN} < $V_{EN(LOW)}$ (output disabled)			150		Ω

ADVANCE INFORMATION

Electrical Characteristics (continued)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6V, whichever is greater, V_{EN} = 1.0 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF (unless otherwise noted); all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD}	Thermal shutdown rising	T_J rising		165		°C
	Thermal shutdown falling	T_J falling		140		
$V_{EN(LOW)}$	EN pin logic low threshold	V_{IN} = 1.6 V to 6.0 V, V_{EN} falling until the output is disabled			0.25	V
$V_{EN(HI)}$	EN pin logic high threshold	V_{IN} = 1.6 V to 6.0 V V_{EN} rising until the output is enabled	0.92			V
V_{UVLO}	UVLO threshold	V_{IN} rising	1.21	1.35	1.55	V
		V_{IN} falling	1.17	1.3	1.5	V
$V_{UVLO(HYST)}$	UVLO hysteresis			50		mV
I_{EN}	EN Pin leakage current	V_{EN} = 6.0 V and V_{IN} = 6.0 V		120	250	nA
$R_{EN(PULL-DOWN)}$	Smart enable pulldown resistor	V_{EN} = 0.25 V		500		KΩ

6.6 Switching Characteristics

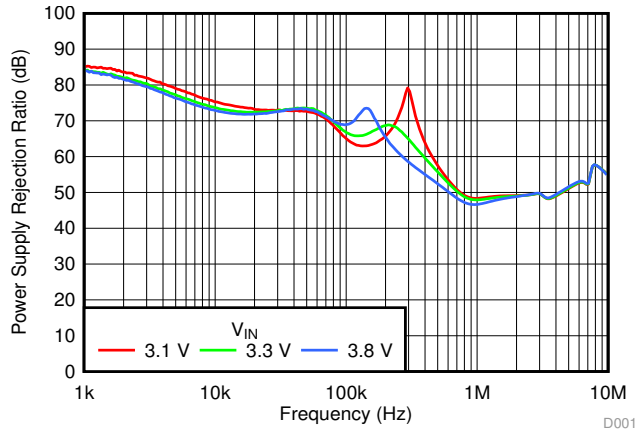
at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6V, whichever is greater, V_{EN} = 1.0 V, I_{OUT} = 1 mA, C_{IN}= 1 µF, C_{OUT} = 1 µF (unless otherwise noted); all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	From V_{EN} > V_{IH} to V_{OUT} = 95% of $V_{OUT(NOM)}$,		750	1500	µs

ADVANCE INFORMATION

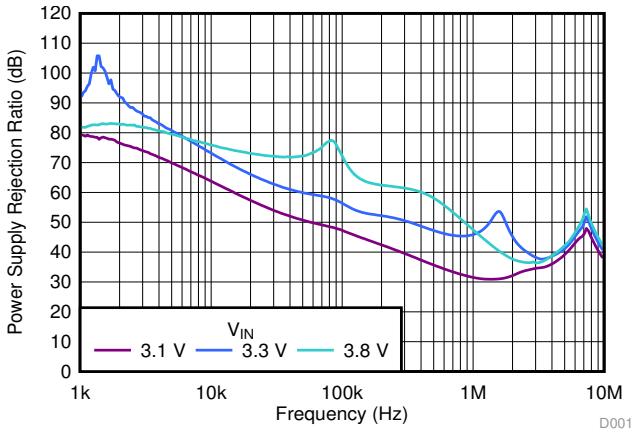
6.7 Typical Characteristics

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



V_{OUT} = 2.8 V, I_{OUT} = 20 mA, C_{OUT} = 1 µF

Figure 1. PSRR at 20-mA Loads



V_{OUT} = 2.8 V, I_{OUT} = 300 mA, C_{OUT} = 1 µF

Figure 2. PSRR at 300-mA Loads

ADVANCE INFORMATION

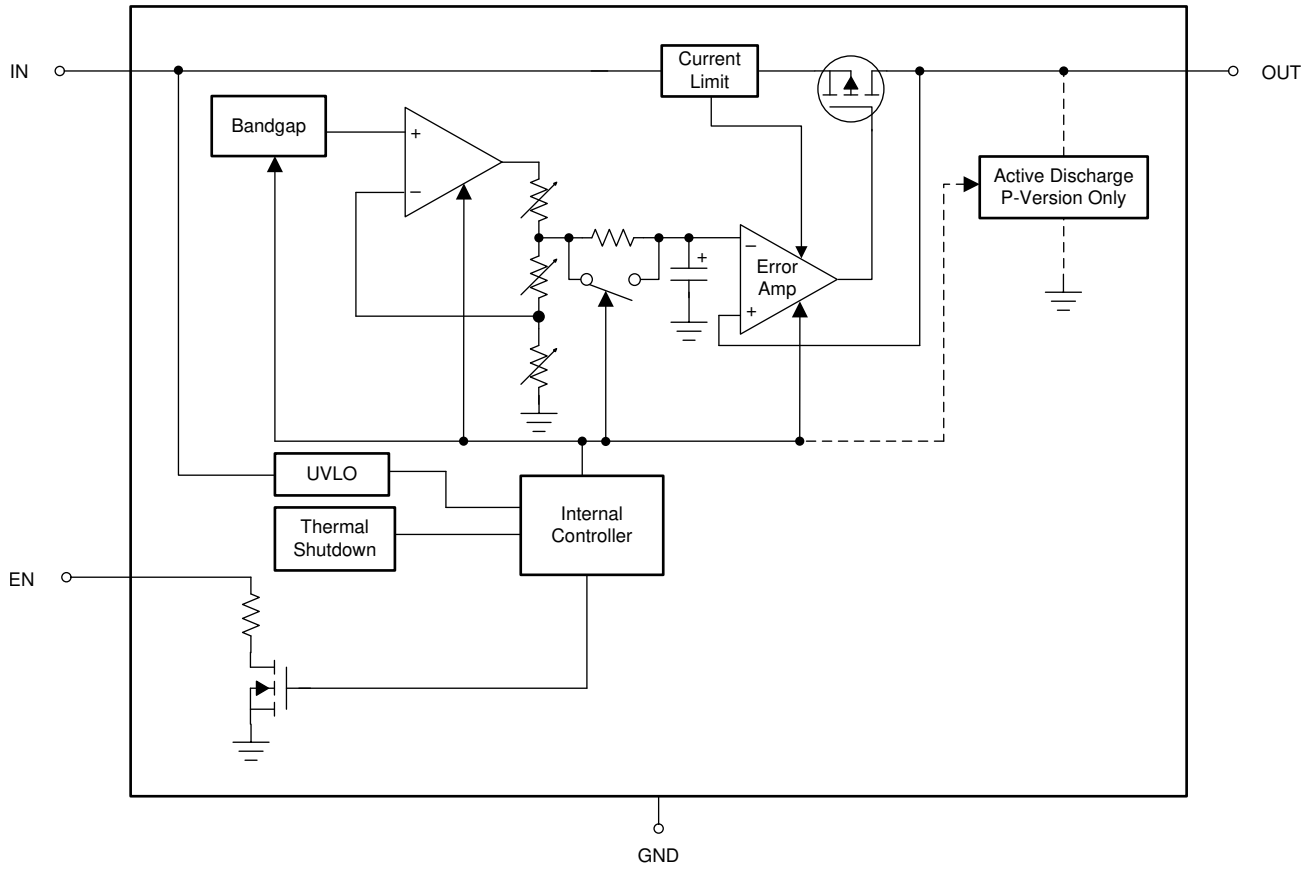
7 Detailed Description

7.1 Overview

Designed to meet the needs of sensitive RF and analog circuits, the TPS7A20 provides low noise, high PSRR, low quiescent current, as well as low line and load transient response figures. Using innovative design techniques, the TPS7A20 offers class-leading noise performance without the need for a separate noise filter capacitor.

The TPS7A20 is designed to perform with a single 1-µF input capacitor and a single 1-µF ceramic output capacitor.

7.2 Functional Block Diagram



ADVANCE INFORMATION

7.3 Feature Description

7.3.1 Low Output Noise

Any internal noise at the TPS7A20 reference voltage is reduced by a first-order, low-pass RC filter before being passed to the output buffer stage. The low-pass RC filter has a –3-dB cut-off frequency of approximately 0.1 Hz.

7.3.2 Smart Enable

The enable pin for the device is an active-high pin. The output voltage is enabled when the voltage of the enable pin is greater than the high-level input voltage of the EN pin and disabled with the enable pin voltage is less than the low-level input voltage of the EN pin. If independent control of the output voltage is not needed, connect the enable pin to the input of the device.

This device has a smart enable circuit to reduce quiescent current. When the voltage on the enable pin is driven above $V_{EN(HI)}$, as listed in the *Electrical Characteristics* table, the device is enabled and the smart enable internal pulldown resistor ($R_{EN(PULLDOWN)}$) is disconnected. When the enable pin is floating, the $R_{EN(PULLDOWN)}$ is connected and pulls the enable pin low to disable the device. The $R_{EN(PULLDOWN)}$ value is listed in the *Electrical Characteristics* table.

This device has an internal pulldown circuit that activates when the device is disabled to actively discharge the output voltage.

7.3.3 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. Use Equation 1 to calculate the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

7.3.4 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{CL}$]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{SC}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.

ADVANCE INFORMATION

Feature Description (continued)

Figure 3 shows a diagram of the foldback current limit.

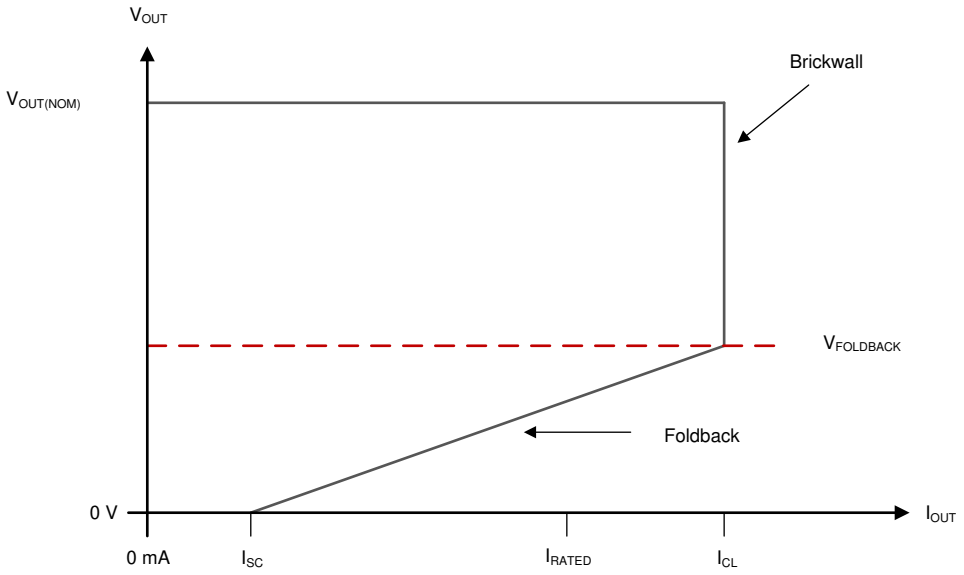


Figure 3. Foldback Current Limit

7.3.5 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

7.3.6 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large $V_{IN} – V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.3.7 Active Discharge

The device has an internal pulldown MOSFET that connects an $R_{PULLDOWN}$ resistor to ground when the device is disabled to actively discharge the output voltage. The active discharge circuit is activated by the enable pin or by the undervoltage lockout (UVLO).

ADVANCE INFORMATION

Feature Description (continued)

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device. Limit reverse current to no more than 5% of the device rated current for a short period of time.

7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

ADVANCE INFORMATION

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.1.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is recommended if the source impedance is more than 0.5 Ω. A higher value capacitor may be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

8.1.3 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: the transition from a light to a heavy load and the transition from a heavy to a light load. The regions shown in Figure 4 are broken down as follows. Regions A, E, and H are where the output voltage is in steady-state.

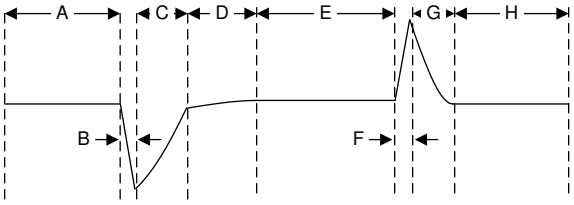


Figure 4. Load Transient Waveform

During transitions from a light load to a heavy load, the:

- Initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing its sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load, the:

- Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)

ADVANCE INFORMATION

Application Information (continued)

- Recovery from the rise results from the LDO decreasing its sourcing current in combination with the load discharging the output capacitor (region G)

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger DC load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

8.1.4 Undervoltage Lockout (UVLO) Operation

The UVLO circuit ensures that the device stays disabled before its input supply reaches the minimum operational voltage range, and ensures that the device shuts down when the input supply collapses. Figure 5 shows the UVLO circuit response to various input voltage events. The diagram can be separated into the following parts:

- Region A: The device does not start until the input reaches the UVLO rising threshold.
- Region B: Normal operation, regulating device.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output may fall out of regulation but the device remains enabled.
- Region D: Normal operation, regulating device.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is reenabled when the UVLO rising threshold is reached by the input voltage and a normal start-up follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0 V. The output falls because of the load and active discharge circuit.

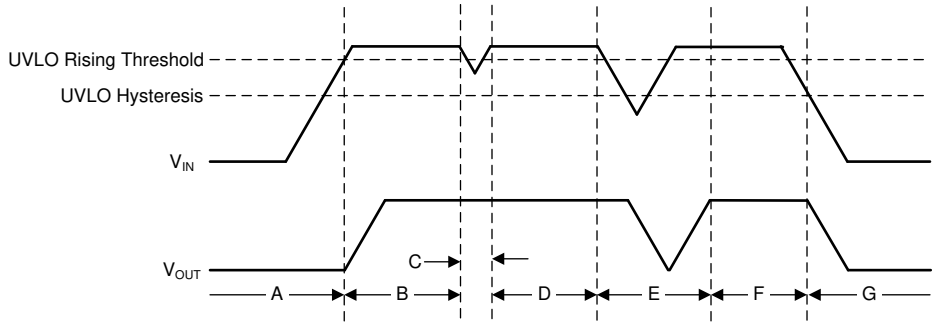


Figure 5. Typical UVLO Operation

8.1.5 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use Equation 2 to approximate P_D:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS7A20 allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

ADVANCE INFORMATION

Application Information (continued)

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. According to Equation 3, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A). Equation 4 rearranges Equation 3 for output current.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \quad (4)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the X2SON package junction-to-case (bottom) thermal resistance ($R_{\theta JC(bot)}$) plus the thermal resistance contribution by the PCB copper.

8.1.5.1 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with Equation 5 and are given in the *Thermal Information* table.

$$\Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D \text{ and } \Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D$$

where:

- P_D is the power dissipated as explained in Equation 2
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge (5)

8.1.5.2 Recommended Area for Continuous Operation

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is given in Figure 6 and can be separated into the following parts:

- Dropout voltage limits the minimum differential voltage between the input and the output ($V_{IN} - V_{OUT}$) at a given output current level. See the *Dropout Operation* section for more details.
- The rated output currents limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
  - The shape of the slope is given by Equation 4. The slope is nonlinear because the maximum-rated junction temperature of the LDO is controlled by the power dissipation across the LDO; thus when $V_{IN} - V_{OUT}$ increases the output current must decrease.
- The rated input voltage range governs both the minimum and maximum of $V_{IN} - V_{OUT}$.

ADVANCE INFORMATION

Application Information (continued)

Figure 6 shows the recommended area of operation for this device on a JEDEC-standard high-K board with a $R_{\theta JA}$ as given in the *Thermal Information* table.

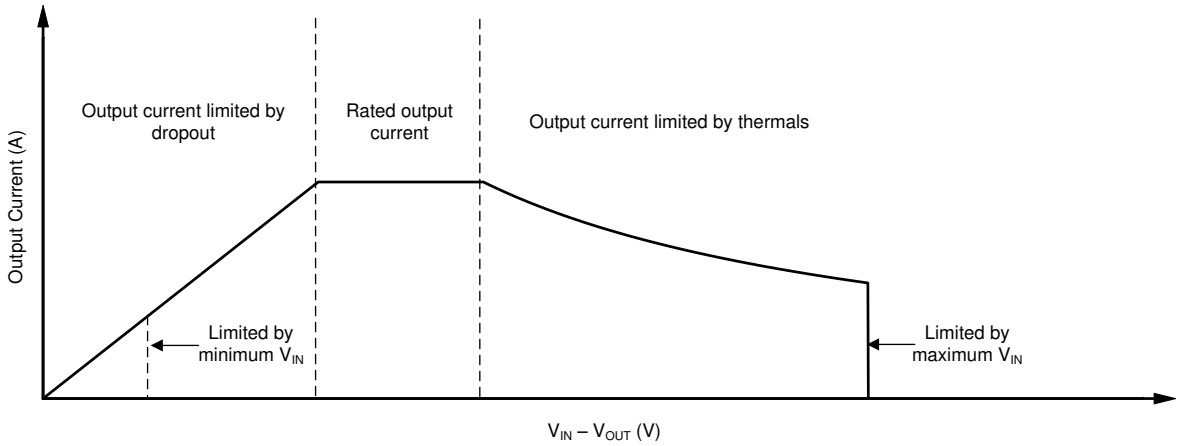


Figure 6. Region Description of Continuous Operation Regime

The TPS7A20 is designed to meet the requirements of RF and analog circuits, by providing low noise, high PSRR, low quiescent current, and low line or load transient response figures. The device offers excellent noise performance without the need for a noise bypass capacitor and is stable with input and output capacitors with a value of 1 µF. The TPS7A20 delivers this performance in industry-standard packages such as DSBGA, X2SON, and SOT-23 which, for this device, are specified with an operating junction temperature (T_J) of –40°C to +125°C.

ADVANCE INFORMATION

8.2 Typical Application

Figure 7 shows the typical application circuit for the TPS7A20. Input and output capacitances may need to be increased above the 1 µF minimum for some applications.

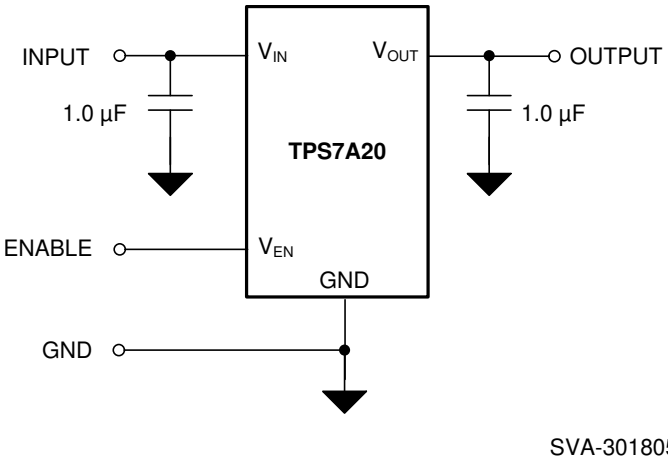


Figure 7. TPS7A20 Typical Application

8.2.1 Design Requirements

Table 2 summaries the design requirements for Figure 7.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	3.1 V to 6.0 V
Output voltage	2.8 V
Output current	200 mA
Output capacitor range	0.7 µF to 10 µF
Output capacitor ESR range	5 mΩ to 80 mΩ

8.2.2 Detailed Design Procedure

The TPS7A20 is designed to meet the requirements of RF and analog circuits, by providing low noise, high PSRR, low quiescent current, and low line or load transient response figures. The device offers excellent noise performance without the need for a noise bypass capacitor and is stable with input and output capacitors with a value of 1 µF. The TPS7A20 delivers this performance in industry standard packages such as DSBGA, X2SON, and SOT-23 which, for this device, are specified with an operating junction temperature (T_J) of –40°C to 125°C.

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.6 V to 6.0 V. The input supply must be well regulated and free of spurious noise. To ensure that the output voltage is well regulated and dynamic performance is optimum, the input supply must be at least $V_{OUT(nom)}$ + 0.3 V or 1.6 V, whichever is greater. TI highly recommends using a 1-µF or greater input capacitor to reduce the impedance of the input supply, especially during transients.

ADVANCE INFORMATION

10 Layout

10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Do not place a thermal via directly beneath the thermal pad of the DQN package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

10.2 Layout Examples

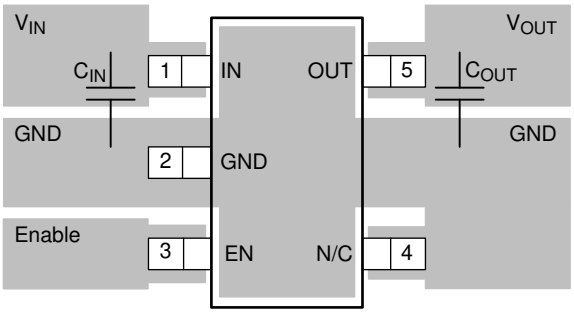


Figure 8. DBV Package (SOT-23) Typical Layout

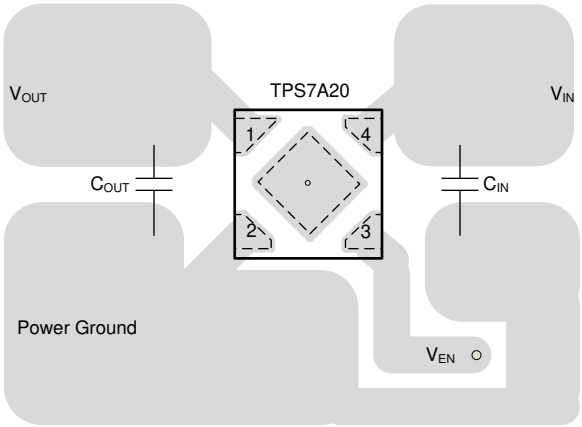


Figure 9. DQN Package (X2SON) Typical Layout

Layout Examples (continued)

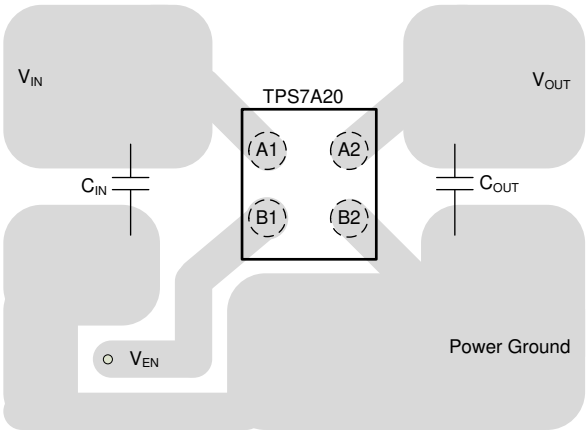


Figure 10. YWD Package (DSBGA) Typical Layout

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Table 3. Device Nomenclature(1)(2)

PRODUCT	V_{OUT}
TPS7A20**xx(x)Pyyyz**	**XX(X)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). **P** indicates an active output discharge feature. All members of the TPS7A20 family actively discharge the output when the device is disabled. **YYY** is the package designator. **Z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 0.8 V to 5.5 V in 25-mV increments are available. Contact the factory for details and availability.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS7A2012PDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS7A2012PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS7A2015PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS7A20185PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS7A2018PDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS7A2018PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS7A2025PDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS7A2025PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS7A2028PDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS7A2028PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS7A2029PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS7A2030PDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS7A2030PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS7A2033PDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS7A2033PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS7A2045PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS7A2050PDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TPS7A2012PDQNR	PREVIEW	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		
TPS7A2015PDQNR	PREVIEW	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		
TPS7A20185PDBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		
TPS7A20185PDQNR	PREVIEW	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A2018PDBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		
TPS7A2024PDBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		
TPS7A2025PDBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		
TPS7A2025PDQNR	PREVIEW	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		
TPS7A2028PDBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		
TPS7A2028PDQNR	PREVIEW	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		
TPS7A2029PDQNR	PREVIEW	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		
TPS7A2030PDBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		
TPS7A2030PDQNR	PREVIEW	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		
TPS7A2033PDBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		
TPS7A2033PDQNR	PREVIEW	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		
TPS7A2045PDQNR	PREVIEW	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		
TPS7A2050PDBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

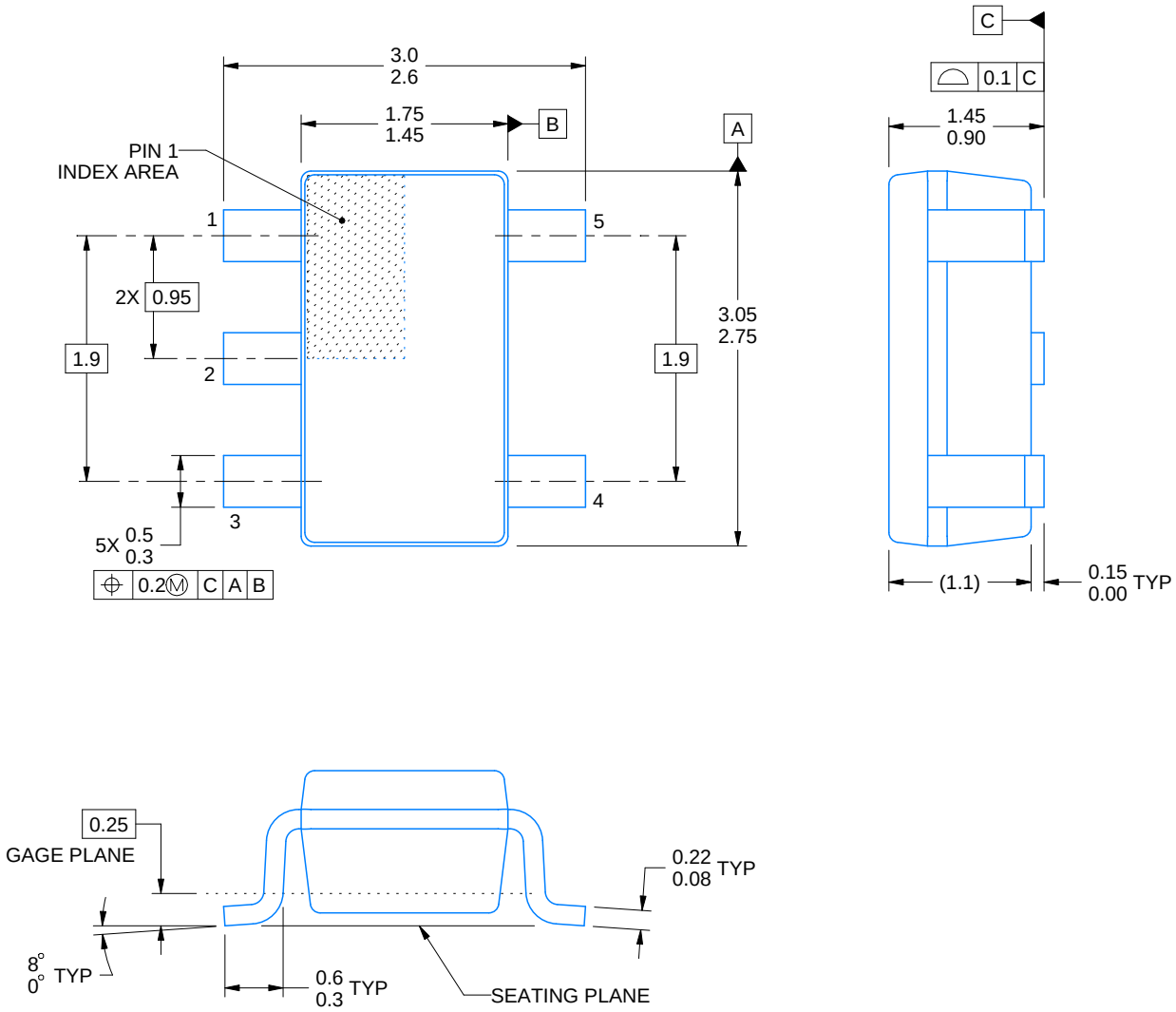
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

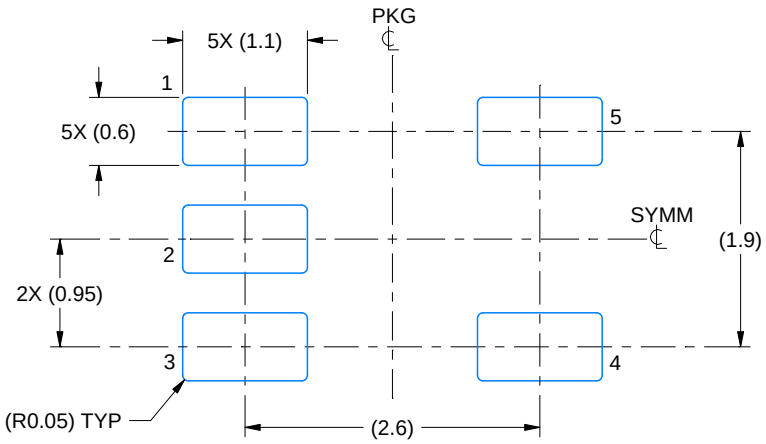
SMALL OUTLINE TRANSISTOR



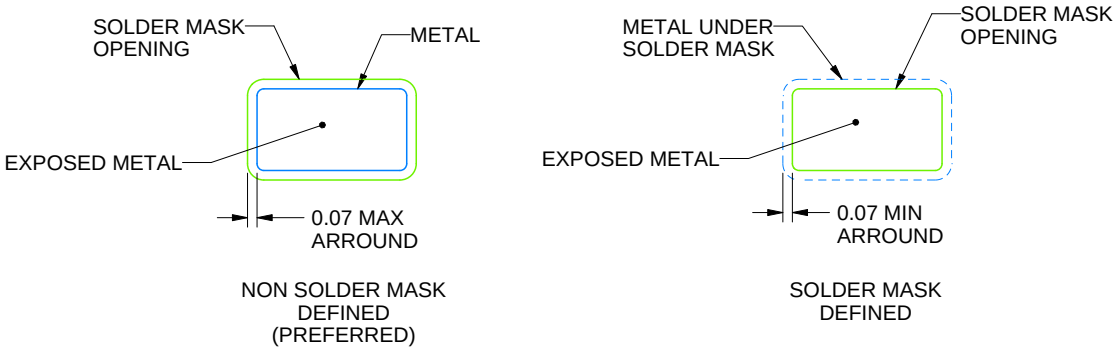
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

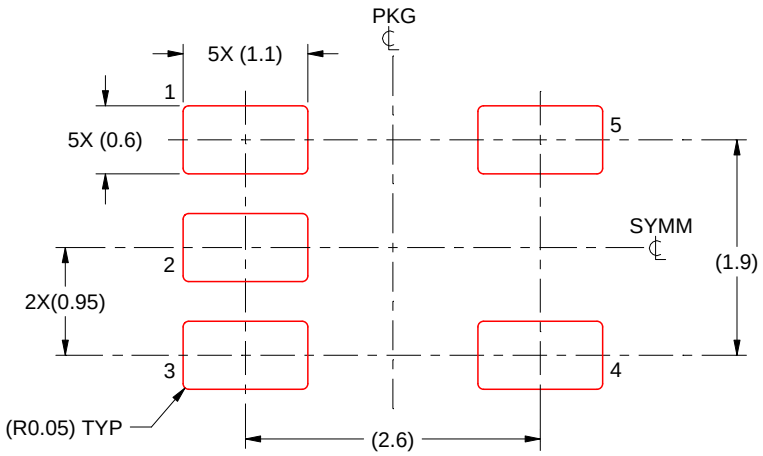


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DQN 4 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4210367/F

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265