1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C
  - Junction temperature: –40°C to +150°C
- Very low $I_Q$: 6.5μA
- Input voltage range: 2.0V to 6.0V
- Output voltage range: 0.8V to 5.5V (50mV steps)
- High PSRR: 91dB at 1kHz
- Low output voltage noise: 7.7μVRMS
- Low dropout:
  - 265mV (maximum) at 500mA (2.5V $V_{OUT}$)
- Smart EN pulldown
- Output voltage tolerance: ±1% at 1mA $I_{OUT}$
- Supports a wide range of ceramic capacitors:
  - 1μF to 200μF
- Package:
  - 3mm × 3mm wettable flank VSON
  - 2mm × 2mm wettable flank WSON (Advance Information)
  - 2mm × 2mm WSON (Advance Information)

2 Applications

- DAS cameras and radar
- Automotive infotainment
- Telematics systems
- Navigation systems

3 Description

The TPS7A21-Q1 is a small, low-dropout (LDO) linear voltage regulator that sources 500mA of output current. The device provides low noise, high PSRR, and excellent load and line transient performance to meet the requirements of RF and other sensitive analog circuits in automotive applications. Innovative design techniques result in low-noise performance without the addition of an external noise bypass capacitor. The TPS7A21-Q1 low quiescent current is a good choice for low-power systems. The 2.0V to 6.0V input voltage range and 0.8V to 5.5V output voltage range support a variety of system requirements. The maximum output voltage tolerance is 1.5%, –2.25% over load, line, and temperature variations.

An internal soft-start circuit helps control inrush current, thus minimizing the input voltage drop during start-up. The LDO is stable with small ceramic capacitors, allowing for a small overall solution size.

A smart enable input circuit with an internally controlled pulldown resistor keeps the LDO disabled even when the EN pin is unconnected. This circuit also helps eliminate external components that are otherwise required to pull down the EN input.

Package Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE(1)</th>
<th>PACKAGE SIZE(2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS7A21-Q1</td>
<td>DRB (Wettable flank VSON, 8)</td>
<td>3mm × 3mm</td>
</tr>
<tr>
<td></td>
<td>DSG (Wettable flank WSON, 8)(3)</td>
<td>2mm × 2mm</td>
</tr>
<tr>
<td></td>
<td>DSG (WSON, 8)(3)</td>
<td>2mm × 2mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Advance Information (not Production Data).
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4 Pin Configuration and Functions

Table 4-1. Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>DRB</th>
<th>DSG0008B</th>
<th>DSG0008A (C Version)</th>
<th>TYPE(1)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>EN</td>
<td>5</td>
<td>5</td>
<td>2</td>
<td>I</td>
<td>Enable pin. Drive EN greater than $V_{EN(HI)}$ to turn on the regulator. Drive EN less than $V_{EN(LO)}$ to put the low-dropout regulator (LDO) into shutdown mode.</td>
</tr>
<tr>
<td></td>
<td>GND</td>
<td>4</td>
<td>4</td>
<td>1</td>
<td>—</td>
<td>Ground pin.</td>
</tr>
<tr>
<td></td>
<td>IN</td>
<td>8</td>
<td>7, 8</td>
<td>3, 4</td>
<td>I</td>
<td>Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the Recommended Operating Conditions table and the Input and Output Capacitor Requirements section. Place the input capacitor as close to the output of the device as possible.</td>
</tr>
<tr>
<td></td>
<td>NC</td>
<td>2, 3, 6, 7</td>
<td>3, 6</td>
<td>7, 8</td>
<td>—</td>
<td>No internal connection. Ground this pin for better thermal performance.</td>
</tr>
<tr>
<td></td>
<td>OUT</td>
<td>1</td>
<td>1, 2</td>
<td>5, 6</td>
<td>O</td>
<td>Regulated output voltage pin. Connect a low-equivalent series resistance (ESR) capacitor to this pin. For best transient response, use the nominal recommended value or larger capacitor from OUT to GND. An internal pulldown resistor prevents a charge from remaining on OUT when the regulator is in shutdown mode ($V_{EN} &lt; V_{EN(LOW)}$).</td>
</tr>
<tr>
<td></td>
<td>Thermal Pad</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.</td>
</tr>
</tbody>
</table>

(1) I = input, O = output, NC = no connect.
5 Specifications

5.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)[(1) (3)]

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$ Input voltage</td>
<td>$-0.3$</td>
<td>$6.5$</td>
</tr>
<tr>
<td>$V_{OUT}$ Output voltage</td>
<td>$-0.3$</td>
<td>Lesser of $V_{IN} + 0.3$, or $6.5$</td>
</tr>
<tr>
<td>$V_{EN}$ Enable input voltage</td>
<td>$-0.3$</td>
<td>$6.5$</td>
</tr>
<tr>
<td>Maximum output current[(3)]</td>
<td>Internally limited</td>
<td>A</td>
</tr>
<tr>
<td>$T_J$ Operating junction temperature</td>
<td>$-40$</td>
<td>$150$</td>
</tr>
<tr>
<td>$T_{stg}$ Storage temperature</td>
<td>$-65$</td>
<td>$150$</td>
</tr>
</tbody>
</table>

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) All voltages are with respect to the GND pin.

(3) Internal thermal shutdown circuitry helps protect the device from permanent damage.

5.2 ESD Ratings

<table>
<thead>
<tr>
<th>$V_{(ESD)}$ Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]</td>
<td>±750</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions
over the operating free-air temperature range (unless otherwise noted)[(1)]

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$ Input supply voltage</td>
<td>$2.0$</td>
<td>$6.0$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{EN}$ Enable input voltage</td>
<td>$0$</td>
<td>$6.0$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OUT}$ Nominal output voltage range</td>
<td>$0.8$</td>
<td>$5.5$</td>
<td>V</td>
</tr>
<tr>
<td>$I_{OUT}$ Output current</td>
<td>$0$</td>
<td>$500$</td>
<td>mA</td>
</tr>
<tr>
<td>$C_{IN}$ Input capacitor[(2)]</td>
<td>$1$</td>
<td></td>
<td>µF</td>
</tr>
<tr>
<td>$C_{OUT}$ Output capacitor[(3)]</td>
<td>$1$</td>
<td>$200$</td>
<td>µF</td>
</tr>
<tr>
<td>ESR Output capacitor effective series resistance</td>
<td></td>
<td></td>
<td>nΩ</td>
</tr>
<tr>
<td>$T_J$ Operating junction temperature</td>
<td>$-40$</td>
<td>$150$</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) All voltages are with respect to the GND pin.

(2) An input capacitor is not required for LDO stability. However, an input capacitor with an effective value of 0.47µF minimum is recommended to counteract the effect of source resistance and inductance, which in some cases causes symptoms of system-level instability such as ringing or oscillation, especially in the presence of load transients.

(3) Effective output capacitance of 0.4µF minimum and 200µF maximum over all temperature and voltage conditions is required for stability with ESR values as high as 100mΩ. If the ESR is reduced to 20mΩ or lower, stable operation is achieved with effective output capacitance as low as 0.3µF.
5.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TPS7A21-Q1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DRB (VSON)</td>
</tr>
<tr>
<td>$R_{JA}$: Junction-to-ambient thermal resistance</td>
<td>58.9</td>
</tr>
<tr>
<td>$R_{JC(top)}$: Junction-to-case (top) thermal resistance</td>
<td>76.3</td>
</tr>
<tr>
<td>$R_{JU}$: Junction-to-board thermal resistance</td>
<td>31.8</td>
</tr>
<tr>
<td>$R_{JC(bot)}$: Junction-to-case (bottom) thermal resistance</td>
<td>13.3</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics and An empirical analysis of the impact of board layout on LDO thermal performance application notes.

5.5 Electrical Characteristics

specified over operating temperature range ($T_J = -40^\circ C$ to $+150^\circ C$), $V_{IN} = V_{OUT(NOM)} + 0.3$V or 2V, whichever is greater, $V_{EN} = 1.0V$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$ (unless otherwise noted); all typical values are at $T_J = 25^\circ C$

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Delta V_{OUT}$: Output voltage tolerance</td>
<td>$V_{IN} = (V_{OUT(NOM)} + 0.3V)$ to 6.0V, $I_{OUT} = 1mA$ to 500mA, $V_{OUT} = 3.3V$</td>
<td>-2.25</td>
<td>1.5</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{IN} = (V_{OUT(NOM)} + 0.3V)$ to 6.0V, $I_{OUT} = 1mA$ to 500mA, $V_{OUT} &lt; 3.3V$</td>
<td>-2.5</td>
<td>1.5</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{IN} = (V_{OUT(NOM)} + 0.3V)$ to 6.0V, $I_{OUT} = 1mA$ $V_{OUT} = 2.8V$</td>
<td>-1</td>
<td>1</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{IN} = (V_{OUT(NOM)} + 0.3V)$ to 6.0V, $I_{OUT} = 1mA$ $V_{OUT} &lt; 2.8V$</td>
<td>-70</td>
<td>50</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{IN} = (V_{OUT(NOM)} + 0.3V)$ to 6.0V, $I_{OUT} = 1mA$ $V_{OUT} &lt; 2.8V$</td>
<td>-50</td>
<td>50</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$\Delta V_{OUT}$: Line regulation</td>
<td>$V_{IN} = (V_{OUT(NOM)} + 0.3V)$ to 6.0V, $I_{OUT} = 1mA$</td>
<td>0.03</td>
<td>%/V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Delta V_{OUT}$: Load regulation</td>
<td>$I_{OUT} = 1mA$ to 500mA</td>
<td>0.003</td>
<td>%/mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{QND}$: Quiescent current</td>
<td>$V_{EN} = V_{IN}$, $V_{IN} = 6.0V$, $I_{OUT} = 0mA$</td>
<td>6.5</td>
<td>9</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_J = -40^\circ C$ to 85$^\circ C$</td>
<td>11</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_J = -40^\circ C$ to 125$^\circ C$</td>
<td>15</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_J = -40^\circ C$ to 150$^\circ C$</td>
<td>18</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{EN} = V_{IN}$, $V_{IN} = 6.0V$, $I_{OUT} = 500mA$</td>
<td>2300</td>
<td>3500</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{SHUTDOWN}$: Shutdown current</td>
<td>$V_{EN} = 0V$ (disabled), $V_{IN} = 6.0V$, $T_J = 25^\circ C$</td>
<td>0.15</td>
<td>1</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{EN} = 0V$ (disabled), $V_{IN} = 6.0V$, $T_J = -40^\circ C$ to 150$^\circ C$</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{QDDO}$: Quiescent current in dropout</td>
<td>$V_{IN} = V_{OUT(NOM)}$, $I_{OUT} = 0mA$</td>
<td>7</td>
<td>15</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$V_{DO}$: Dropout voltage</td>
<td>$I_{OUT} = 500mA$, $V_{OUT} = 95% \times V_{OUT(NOM)}$</td>
<td>825</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$0.8V \leq V_{OUT} &lt; 1.0V$ (1)</td>
<td>605</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$1.0V \leq V_{OUT} &lt; 1.2V$ (1)</td>
<td>470</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$1.2V \leq V_{OUT} &lt; 1.5V$ (1)</td>
<td>355</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$1.5V \leq V_{OUT} &lt; 2.5V$</td>
<td>265</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$2.5V \leq V_{OUT} \leq 5.5V$</td>
<td>265</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{CL}$: Output current limit</td>
<td>$V_{OUT} = 0.9 \times V_{OUT(NOM)}$</td>
<td>650</td>
<td>1060</td>
<td>1500</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{SC}$: Short-circuit current limit</td>
<td>$V_{OUT} = 0V$</td>
<td>325</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>
TPS7A21-Q1
SBVS437B – DECEMBER 2022 – REVISED FEBRUARY 2024

5.5 Electrical Characteristics (continued)

specified over operating temperature range (T<sub>J</sub> = –40°C to +150°C), V<sub>IN</sub> = V<sub>OUT</sub>(NOM) + 0.3V or 2V, whichever is greater, V<sub>EN</sub> = 1.0V, I<sub>OUT</sub> = 1mA, C<sub>IN</sub> = 1µF, C<sub>OUT</sub> = 1µF (unless otherwise noted); all typical values are at T<sub>J</sub> = 25°C

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSRR</td>
<td>Power-supply rejection ratio</td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>I&lt;sub&gt;OUT&lt;/sub&gt; = 20mA, V&lt;sub&gt;IN&lt;/sub&gt; = V&lt;sub&gt;OUT&lt;/sub&gt; + 1.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>f = 100Hz</td>
<td>90</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>f = 1kHz</td>
<td>91</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>f = 10kHz</td>
<td>71</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>f = 100kHz</td>
<td>61</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>f = 1MHz</td>
<td>50</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>I&lt;sub&gt;OUT&lt;/sub&gt; = 500mA, V&lt;sub&gt;IN&lt;/sub&gt; = V&lt;sub&gt;OUT&lt;/sub&gt; + 1.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>f = 100Hz</td>
<td>65</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>f = 1kHz</td>
<td>85</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>f = 10kHz</td>
<td>79</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>f = 100kHz</td>
<td>44</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>f = 1MHz</td>
<td>50</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;N&lt;/sub&gt;</td>
<td>Output noise voltage</td>
<td></td>
<td></td>
<td></td>
<td>µV&lt;sub&gt;RMS&lt;/sub&gt;</td>
</tr>
<tr>
<td></td>
<td>BW = 10Hz to 100kHz, V&lt;sub&gt;OUT&lt;/sub&gt; = 2.8V</td>
<td></td>
<td>7.7</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>I&lt;sub&gt;OUT&lt;/sub&gt; = 500mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>I&lt;sub&gt;OUT&lt;/sub&gt; = 1mA</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R&lt;sub&gt;PULLDOWN&lt;/sub&gt;</td>
<td>Output automatic discharge pulldown resistance</td>
<td></td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = 2V, V&lt;sub&gt;EN&lt;/sub&gt; &lt; V&lt;sub&gt;IL&lt;/sub&gt; (output disabled)</td>
<td>150</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T&lt;sub&gt;SD&lt;/sub&gt;</td>
<td>Thermal shutdown rising</td>
<td></td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>T&lt;sub&gt;J&lt;/sub&gt; rising</td>
<td>165</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Thermal shutdown falling</td>
<td>140</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;EN&lt;/sub&gt;(LOW)</td>
<td>Low input threshold</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = 2.0V to 6.0V, V&lt;sub&gt;EN&lt;/sub&gt; falling until the output is disabled</td>
<td></td>
<td></td>
<td>0.3</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;EN&lt;/sub&gt;(HIGH)</td>
<td>High input threshold</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = 2.0V to 6.0V, V&lt;sub&gt;EN&lt;/sub&gt; rising until the output is enabled</td>
<td></td>
<td></td>
<td>0.9</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;UVLO&lt;/sub&gt;</td>
<td>UVLO threshold</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; rising</td>
<td>1.11</td>
<td>1.32</td>
<td>1.63</td>
<td></td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; falling</td>
<td>1.05</td>
<td>1.27</td>
<td>1.57</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;UVLO&lt;/sub&gt;(HYST)</td>
<td>UVLO hysteresis</td>
<td></td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;EN&lt;/sub&gt;</td>
<td>EN pin leakage current</td>
<td></td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;EN&lt;/sub&gt; = 6.0V and V&lt;sub&gt;N&lt;/sub&gt; = 6.0V</td>
<td></td>
<td></td>
<td>100</td>
<td>250</td>
</tr>
<tr>
<td>R&lt;sub&gt;EN&lt;/sub&gt;(PULL-DOWN)</td>
<td>Smart enable pulldown resistor</td>
<td></td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>440</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;ON&lt;/sub&gt;</td>
<td>Turnon time</td>
<td></td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>From V&lt;sub&gt;EN&lt;/sub&gt; &gt; V&lt;sub&gt;SH&lt;/sub&gt; to V&lt;sub&gt;OUT&lt;/sub&gt; = 95% of V&lt;sub&gt;OUT&lt;/sub&gt;(NOM)</td>
<td>120</td>
<td>200</td>
<td>280</td>
<td></td>
</tr>
</tbody>
</table>

(1) Dropout voltages for V<sub>OUT</sub> values below or very near the UVLO threshold are not measured directly. Values shown are verified by simulation.
5.6 Typical Characteristics

at $V_{IN} = 3.6V$, $V_{OUT} = 3.3V$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$, and $T_A = 25^\circ C$ (unless otherwise noted)

Figure 5-1. Output Voltage Accuracy vs $I_{OUT}$

Figure 5-2. Output Voltage Accuracy vs $I_{OUT}$

Figure 5-3. Output Voltage Accuracy vs $V_{IN}$

Figure 5-4. Line Regulation vs $V_{IN}$

Figure 5-5. Load Regulation vs $I_{OUT}$

Figure 5-6. Dropout Voltage vs $I_{OUT}$
5.6 Typical Characteristics (continued)

at $V_{\text{IN}} = 3.6\,\text{V}$, $V_{\text{OUT}} = 3.3\,\text{V}$, $I_{\text{OUT}} = 1\,\text{mA}$, $C_{\text{IN}} = 1\,\mu\text{F}$, $C_{\text{OUT}} = 1\,\mu\text{F}$, and $T_{\text{A}} = 25^\circ\text{C}$ (unless otherwise noted)

![Diagram of Dropout Voltage vs $I_{\text{OUT}}$](image1)

![Diagram of $I_{\text{Q}}$ vs $V_{\text{IN}}$](image2)

![Diagram of $I_{\text{Q}}$ vs $V_{\text{IN}}$](image3)

![Diagram of $I_{\text{GND}}$ vs $I_{\text{OUT}}$](image4)

![Diagram of Shutdown Current vs $V_{\text{IN}}$](image5)
5.6 Typical Characteristics (continued)

at $V_{IN} = 3.6V$, $V_{OUT} = 3.3V$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$, and $T_A = 25°C$ (unless otherwise noted)

![Graph showing shutdown current vs $V_{IN}$](image1)

$V_{EN} = 0V$, $I_{OUT} = 0mA$

![Graph showing foldback current limit](image2)

$V_{EN} = 1V$

![Graph showing enable logic threshold vs temperature](image3)

$V_{EN} = 6V$, $I_{OUT} = 0mA$

![Graph showing smart enable pulldown resistor vs temperature and $V_{IN}$](image4)

$V_{EN} = 0.3V$

![Graph showing output pulldown resistance vs temperature and $V_{IN}$](image5)

$V_{EN} = 0.3V$
5.6 Typical Characteristics (continued)

at $V_{IN} = 3.6V$, $V_{OUT} = 3.3V$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$, and $T_A = 25^\circ C$ (unless otherwise noted)

![Graph](image1)

$V_{EN} = 1V$

$V_{IN} = 0V$ to $4.3V$, slew rate $= 1V/\mu s$, $I_{OUT} = 500mA$

![Graph](image2)

$V_{IN} = 0V$ to $4.3V$, slew rate $= 1V/\mu s$, $I_{OUT} = 500mA$

![Graph](image3)

$V_{IN} = 0V$ to $4.3V$, slew rate $= 1V/\mu s$, $I_{OUT} = 500mA$

![Graph](image4)

$V_{IN} = 0V$ to $4.3V$, slew rate $= 1V/\mu s$, $I_{OUT} = 500mA$

![Graph](image5)

$V_{IN} = 0V$ to $4.3V$, slew rate $= 1V/\mu s$, $I_{OUT} = 500mA$

![Graph](image6)

$V_{IN} = 0V$ to $4.3V$, slew rate $= 1V/\mu s$, $I_{OUT} = 500mA$

![Graph](image7)

$V_{IN} = 0V$ to $4.3V$, slew rate $= 1V/\mu s$, $I_{OUT} = 500mA$

![Graph](image8)

$V_{IN} = 0V$ to $4.3V$, slew rate $= 1V/\mu s$, $I_{OUT} = 500mA$

![Graph](image9)

$V_{IN} = 0V$ to $4.3V$, slew rate $= 1V/\mu s$, $I_{OUT} = 500mA$
5.6 Typical Characteristics (continued)

at $V_{IN} = 3.6V$, $V_{OUT} = 3.3V$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$, and $T_A = 25^\circ C$ (unless otherwise noted)

$V_{IN} = 4.3V$, $V_{EN} = 0V$ to 4.3V, slew rate = $1V/\mu s$, $I_{OUT} = 0mA$, $C_{OUT} = 10\mu F$

Figure 5-25. Start-Up Inrush Current

$V_{EN} = V_{EN(HI)}$ to $V_{OUT} = 95\%$ of $V_{OUT(NOM)}$, $I_{OUT} = 0mA$

Figure 5-26. Start-Up Turn-On Time vs Temperature

$V_{EN} = V_{IN}$, $t_r = t_f = 5\mu s$, $I_{OUT} = 500mA$

Figure 5-27. Line Transient From 3.6V to 4.6V

$V_{EN} = V_{IN}$, $t_r = t_f = 5\mu s$, $I_{OUT} = 1mA$

Figure 5-28. Line Transient From 3.6V to 4.6V

$V_{EN} = V_{IN}$, $t_r = t_f = 1\mu s$

Figure 5-29. Load Transient From 1mA to 500mA

$V_{EN} = V_{IN}$, $t_r = t_f = 200\text{ns}$

Figure 5-30. Load Transient From 1mA to 500mA
5.6 Typical Characteristics (continued)

at $V_{IN} = 3.6V$, $V_{OUT} = 3.3V$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$, and $T_{A} = 25^\circ C$ (unless otherwise noted)

Figure 5-31. Load Transient From 0mA to 500mA

$V_{EN} = V_{IN}$, $t_{r} = t_{f} = 1\mu s$

Figure 5-32. Load Transient From 0mA to 500mA

$V_{EN} = V_{IN}$, $t_{r} = t_{f} = 200\text{ns}$

Figure 5-33. PSRR vs Frequency and $I_{OUT}$

Figure 5-34. PSRR vs Frequency and $V_{IN}$

Figure 5-35. PSRR vs Frequency and $V_{IN}$

Figure 5-36. PSRR vs Frequency and $C_{OUT}$
5.6 Typical Characteristics (continued)

at \( V_{IN} = 3.6\text{V}, V_{OUT} = 3.3\text{V}, I_{OUT} = 1\text{mA}, C_{IN} = 1\mu\text{F}, C_{OUT} = 1\mu\text{F}, \) and \( T_A = 25^\circ\text{C} \) (unless otherwise noted)

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>Output Voltage Noise (V/\text{Hz})</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.001</td>
<td>0.002</td>
</tr>
<tr>
<td>0.005</td>
<td>0.01</td>
</tr>
<tr>
<td>0.02</td>
<td>0.05</td>
</tr>
<tr>
<td>0.1</td>
<td>0.2</td>
</tr>
<tr>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
</tr>
</tbody>
</table>

\( V_{EN} = V_{IN}, I_{OUT} = 500\text{mA} \)

\( V_{EN} = V_{IN}, I_{OUT} = 20\text{mA} \)

\( V_{EN} = V_{IN}, I_{OUT} = 500\text{mA} \)

\( V_{EN} = V_{IN}, I_{OUT} = 20\text{mA} \)

\( V_{EN} = V_{IN}, I_{OUT} = 500\text{mA} \)

\( V_{EN} = V_{IN}, I_{OUT} = 20\text{mA} \)

\( V_{EN} = V_{IN}, I_{OUT} = 500\text{mA} \)

\( V_{EN} = V_{IN}, I_{OUT} = 20\text{mA} \)

\( V_{EN} = V_{IN}, I_{OUT} = 500\text{mA} \)
6 Detailed Description

6.1 Overview

Designed to meet the needs of sensitive RF and analog circuits, the TPS7A21-Q1 provides low noise, high PSRR, low quiescent current, and excellent line and load transient response. The TPS7A21-Q1 achieves excellent noise performance without the need for a separate noise filter capacitor.

The TPS7A21-Q1 is designed to operate properly with a single 1µF input capacitor and a single 1µF ceramic output capacitor. Make sure the effective output capacitance is at least 0.4µF across all operating voltage and temperature conditions.

6.2 Functional Block Diagram
6.3 Feature Description

6.3.1 Smart Enable (EN)

The enable pin (EN) is active high. The output is enabled when the voltage applied to EN is greater than \( V_{EN(HI)} \) and disabled when the applied voltage is less than \( V_{EN(LOW)} \). If external control of the output voltage is not needed, connect EN to IN. This device has a smart enable circuit to reduce quiescent current. When the voltage on the enable pin is driven above \( V_{EN(HI)} \), the output is enabled and the smart enable internal pulldown resistor \( R_{EN(PULLDOWN)} \) is disconnected. When the enable pin is floating, the \( R_{EN(PULLDOWN)} \) is connected and pulls the enable pin low to disable the output. In addition to reducing quiescent current, the smart pulldown helps make sure that the logic level is correct even when EN is driven from a source that has limited current drive capability. The \( R_{EN(PULLDOWN)} \) value is listed in the Electrical Characteristics table.

6.3.2 Low Output Noise

Any internal noise at the TPS7A21-Q1 reference voltage is reduced by a first-order, low-pass RC filter before being passed to the output buffer stage. The low-pass RC filter has a –3dB cutoff frequency of approximately 0.1Hz. During start-up, the filter resistor is bypassed to reduce output rise time. The filter begins normal operation after the output voltage reaches the nominal value.

6.3.3 Active Discharge

The regulator has an internal metal-oxide-semiconductor field-effect transistor (MOSFET) that connects a pulldown resistor between the output and ground pins when the device is disabled to actively discharge the output voltage. Make sure the voltage on IN is high enough to turn on the pulldown MOSFET. When \( V_{IN} \) is too low to provide sufficient \( V_{GS} \) on the pulldown MOSFET, the pulldown circuit is not active. The active discharge circuit is activated by the enable pin, or by the voltage on IN falling below the undervoltage lockout (UVLO) threshold.

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply collapses. Reverse current potentially flows from the output to the input. This reverse current flow potentially causes damage to the device. Limit any such transient reverse current to no more than 5% of the device rated current.

6.3.4 Dropout Voltage

Dropout voltage \( V_{DO} \) is defined as the input voltage minus the output voltage \( (V_{IN} - V_{OUT}) \) at the rated output current \( I_{RATED} \), when the pass transistor is fully on. \( I_{RATED} \) is the maximum \( I_{OUT} \) listed in the Recommended Operating Conditions table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the value required to support output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance \( R_{DS(ON)} \) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. Equation 1 calculates the \( R_{DS(ON)} \) of the device.

\[
R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)
\]

6.3.5 Foldback Current Limit

The TPS7A21-Q1 has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage \( V_{FOLDBACK} \).

In a high-load current fault with the output voltage above \( V_{FOLDBACK} \), the brick-wall scheme limits the output current to the current limit \( I_{CL} \). When the output voltage drops below \( V_{FOLDBACK} \), a foldback current limit activates that scales back the current when the output voltage approaches GND. When the output is shorted, the...
device supplies a typical current called the short-circuit current limit \((I_{SC})\). \(I_{CL}\) and \(I_{SC}\) are listed in the Electrical Characteristics table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the regulator begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power \([(V_{IN} - V_{OUT}) \times I_{CL}]\). When the output is shorted and the output voltage is less than \(V_{FOLDBACK}\), the pass transistor dissipates power \([(V_{IN} - V_{OUT}) \times I_{SC}]\). If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition persists, the device cycles between current limit and thermal shutdown. For more information on current limits, see the Know Your Limits application note.

Figure 6-1 shows a diagram of the foldback current limit.

![Figure 6-1. Foldback Current Limit](image)

**6.3.6 Undervoltage Lockout**

An independent undervoltage lockout (UVLO) circuit monitors the input voltage, allowing a controlled and consistent turn on and turn off of the output voltage. If the input voltage drops during load transients (when the device output is enabled), the UVLO has built-in hysteresis to prevent unwanted turn off.

**6.3.7 Thermal Overload Protection (T_{SD})**

Thermal shutdown disables the output when the junction temperature \(T_J\) rises to the shutdown temperature threshold \(T_{SD}\). The thermal shutdown circuit hysteresis requires the temperature to fall to a lower temperature before turning on again. The thermal time constant of the semiconductor die is fairly short. Thus, the device cycles on and off when thermal shutdown is reached until power dissipation is reduced.

High power dissipation occurs during start up from large \(V_{IN} - V_{OUT}\) voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes.

For reliable operation, limit the junction temperature to the maximum listed in the Recommended Operating Conditions table. Operation above this maximum temperature causes the regulator to exceed operational specifications.
Although the thermal shutdown circuitry is designed to protect against temporary thermal overload conditions, this circuitry is not intended to replace proper thermal design. Continuously running the regulator into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

6.4.1 Device Functional Mode Comparison

Table 6-1 shows the conditions that lead to the different modes of operation. See the Electrical Characteristics table for parameter values.

<table>
<thead>
<tr>
<th>OPERATING MODE</th>
<th>PARAMETER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal operation</td>
<td>V$<em>{IN}$ &gt; V$</em>{OUT(nom)}$ + V$<em>{DO}$ and V$</em>{IN}$ &gt; V$_{IN(min)}$</td>
</tr>
<tr>
<td>Dropout operation</td>
<td>V$<em>{IN(min)}$ ≤ V$</em>{IN}$ &lt; V$<em>{OUT(nom)}$ + V$</em>{DO}$</td>
</tr>
<tr>
<td>Disabled (any true condition disables the device)</td>
<td>V$<em>{IN}$ &lt; V$</em>{UVLO}$</td>
</tr>
</tbody>
</table>

6.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:
- The input voltage is greater than the nominal output voltage plus the dropout voltage (V$_{OUT(nom)}$ + V$_{DO}$)
- The output current is less than the current limit (I$_{OUT}$ < I$_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature (T$_{J}$ < T$_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

6.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, V$_{IN}$ < V$_{OUT(NOM)}$ + V$_{DO}$, directly after being in a normal regulation state, but not during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage (V$_{OUT(NOM)}$ + V$_{DO}$), the output voltage overshoots for a short period of time while the device pulls the pass transistor back into the linear region.

For output currents less than approximately 200mA, the slope of the dropout voltage curve is lower than for higher currents. This slope helps maintain better performance when the LDO is in dropout.

6.4.4 Disabled

Shut down the output of the device by forcing the enable pin voltage to less than V$_{EN(LOW)}$. When disabled, the pass transistor is turned off, internal circuits are shut down, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.
7 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for many types of applications and are recommended, but use good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Consult the manufacturer data sheet to verify performance. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the Recommended Operating Conditions table account for an effective capacitance of approximately 50% of the nominal value.

7.1.2 Input and Output Capacitor Requirements

Although the LDO is stable without an input capacitor, good design practice is to connect a capacitor from IN to GND, with a value at least equal to the nominal value specified in the Recommended Operating Conditions table. The input capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR, and is recommended if the source impedance is greater than 0.5Ω. When the source resistance and inductance are sufficiently high, the overall system is susceptible to instability (including ringing and sustained oscillation) and other performance degradation if there is insufficient capacitance between IN and GND. A capacitor with a value greater than the minimum is necessary if there are large fast-rise-time load or line transients or if the LDO is located more than a few centimeters from the input power source.

An output capacitor of an appropriate value helps provide stability and improve dynamic performance. Use an output capacitor within the range specified in the Recommended Operating Conditions table.

7.1.3 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: the transition from a light to a heavy load and the transition from a heavy to a light load. The regions shown in Figure 7-1 are broken down as follows. Regions A, E, and H are where the output voltage is in a steady state.

![Figure 7-1. Load Transient Waveform](image-url)
During transitions from a light load to a heavy load, the:

- Initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing the sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load, the:

- Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing the sourcing current in combination with the load discharging the output capacitor (region G)

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger DC load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

7.1.4 Undervoltage Lockout (UVLO) Operation

The UVLO circuit makes sure that the device remains disabled before the input supply reaches the minimum operational voltage range, and makes sure that the device shuts down when the input supply collapses. Figure 7-2 shows the UVLO circuit response to various input voltage events. The diagram is separated into the following parts:

- Region A: The device does not start until the input reaches the UVLO rising threshold.
- Region B: Normal operation, regulating device.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output falls out of regulation but the device remains enabled.
- Region D: Normal operation, regulating device.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is re-enabled when the UVLO rising threshold is reached by the input voltage and a normal start-up follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0V. The output falls because of the load and active discharge circuit.

![Figure 7-2. Typical UVLO Operation](image-url)

7.1.5 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. Make sure the PCB area around the regulator is as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use Equation 2 to approximate P_D:

$$P_D = \frac{(V_{IN} - V_{OUT}) \times I_{LOAD}}{R_{THermal}}$$
\[ P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \]  

(2)

Power dissipation is minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS7A21-Q1 allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum allowable junction temperature (\( T_J \)) determines the maximum power dissipation for the device. According to Equation 3, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance (\( R_{\theta JA} \)) of the combined PCB and device package and the temperature of the ambient air (\( T_A \)).

\[ T_J = T_A + (R_{\theta JA} \times P_D) \]  

(3)

Equation 4 rearranges Equation 3 for output current.

\[ I_{OUT} = (T_J - T_A) / (R_{\theta JA} \times (V_{IN} - V_{OUT})) \]  

(4)

Unfortunately, this thermal resistance (\( R_{\theta JA} \)) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The \( R_{\theta JA} \) recorded in the Thermal Information table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, \( R_{\theta JA} \) is actually the sum of the package junction-to-case (bottom) thermal resistance (\( R_{\theta JC(bot)} \)) plus the thermal resistance contribution by the PCB copper.

### 7.1.6 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (\( \Psi \)) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (\( \Psi_{JT} \) and \( \Psi_{JB} \)) are used in accordance with Equation 5 and are given in the Thermal Information table.

\[ \Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D \text{ and } \Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D \]  

(5)

where:

- \( P_D \) is the power dissipated as explained in the Power Dissipation (\( P_D \)) section
- \( T_T \) is the temperature at the center-top of the device package
- \( T_B \) is the PCB surface temperature measured 1mm from the device package and centered on the package edge

### 7.1.7 Recommended Area For Continuous Operation

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is given in Figure 7-3 and is separated into the following parts:

- Dropout voltage limits the minimum differential voltage between the input and the output (\( V_{IN} - V_{OUT} \)) at a given output current level. See the Dropout Operation section for more details.
- The rated output currents limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
The shape of the slope is depicted in the third region of Figure 7-3. The slope is nonlinear because the maximum-rated junction temperature of the LDO is controlled by the power dissipation across the LDO. Thus, when $V_{IN} - V_{OUT}$ increases the output current decreases.

- The rated input voltage range governs both the minimum and maximum of $V_{IN} - V_{OUT}$.

Figure 7-3 shows the recommended area of operation for this device on a JEDEC-standard high-K board with a $R_{0JA}$, as given in the Thermal Information table.

![Figure 7-3. Region Description of Continuous Operation Regime](image)

7.2 Typical Application

Figure 7-4 shows the typical application circuit for the TPS7A21-Q1. If necessary for some applications, increase the input and output capacitances above the 1µF minimum value.

![Figure 7-4. TPS7A21-Q1 Typical Application](image)
7.2.1 Design Requirements

Table 7-1 summarizes the design requirements for the typical application circuit.

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>3.6V to 4.2V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>3.3V</td>
</tr>
<tr>
<td>Output current</td>
<td>350mA</td>
</tr>
<tr>
<td>Maximum ambient temperature</td>
<td>125°C</td>
</tr>
</tbody>
</table>

7.2.2 Detailed Design Procedure

For this design example, the 3.3V output version (TPS7A2133PQWDRBRQ1) is selected. A nominal 3.6V input supply is assumed. Use a minimum 1.0μF input capacitor to minimize the effect of resistance and inductance between the source and the LDO input. Use a minimum 1.0μF output capacitor for stability and good load transient response. The dropout voltage ($V_{DO}$) is less than 150mV maximum at a 3.3V output voltage and 500mA output current, so there are no dropout issues with an input voltage of 3.6V and a maximum output current of 350mA.

7.2.2.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source (the junctions of the device) to the ultimate heat sink of the ambient environment. Thus, power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

Equation 6 calculates the maximum allowable power dissipation for the device in a given package:

$$P_{D-MAX} = \frac{(T_{J-MAX} - T_A)}{R_{\theta JA}}$$  \hspace{1cm} (6)

Equation 7 represents the actual power being dissipated in the device:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$  \hspace{1cm} (7)

These two equations establish the relationship between the maximum power dissipation allowed resulting from thermal consideration, the voltage drop across the device, and the continuous current capability of the device. Use these two equations to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation ($P_D$) or excellent package thermal resistance ($R_{\theta JA}$) is present, increase the maximum ambient temperature ($T_{A-MAX}$).

In applications where high power dissipation or poor package thermal resistance is present, derate the maximum ambient temperature ($T_{A-MAX}$) if necessary. As given by Equation 8, $T_{A-MAX}$ is dependent on the maximum operating junction temperature ($T_{J-MAX-OP} = 150°C$), the maximum allowable power dissipation in the device package in the application ($P_{D-MAX}$), and the junction-to ambient thermal resistance of the device or package in the application ($R_{\theta JA}$):

$$T_{A-MAX} = (T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX}))$$  \hspace{1cm} (8)

Alternately, if $T_{A-MAX}$ is unable to be derated, do not reduce the $P_D$ value. This reduction is accomplished by reducing $V_{IN}$ in the $V_{IN} - V_{OUT}$ term as long as the minimum $V_{IN}$ is met, or by reducing the $I_{OUT}$ term, or by some combination of the two.
7.2.3 Application Curves

![Application Curves](image)

**Figure 7-5. Start-Up With \(V_{\text{EN}}\) After \(V_{\text{IN}}\)**

**Figure 7-6. PSRR vs Frequency and \(V_{\text{IN}}\)**

7.3 Power Supply Recommendations

This LDO is designed to operate from an input supply voltage range of 2.0V to 5.5V. Make sure the input supply is well regulated and free of spurious noise. To make sure that the TPS7A21-Q1 output voltage is well regulated and dynamic performance is optimum, set the input supply to be at least \(V_{\text{OUT}} + 0.3\) V. A minimum capacitor value of 1\(\mu\)F is required to be within 1cm of the IN pin.

7.4 Layout

7.4.1 Layout Guidelines

The dynamic performance of the TPS7A21-Q1 is dependent on the layout of the PCB. PCB layout practices that are adequate for typical LDOs potentially degrade the PSRR, noise, or transient performance of the TPS7A21-Q1.

Best performance is achieved by placing \(C_{\text{IN}}\) and \(C_{\text{OUT}}\) on the same side of the PCB as the TPS7A21-Q1, and as close to the package as practical. Route the ground connections for \(C_{\text{IN}}\) and \(C_{\text{OUT}}\) back to the TPS7A21-Q1 ground pin using as wide and short a copper trace as practical.

Avoid connections using long trace lengths, narrow trace widths, or connections through vias. These connections add parasitic inductances and resistance that results in inferior performance, especially during transient conditions.
7.4.2 Layout Example

Figure 7-7. Typical DRB Layout
8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

<table>
<thead>
<tr>
<th>PRODUCT(1) (2)</th>
<th>V_OUT</th>
</tr>
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</table>
| TPS7A21xx(x)(C)PQ(W)yyyQ1 | xx(x) is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8V; 125 = 1.25V).
|                  | C (when present) indicates an alternate pin configuration. |
|                  | P indicates an active output discharge feature. All variants of the TPS7A21 actively discharge the output when the device is disabled. |
|                  | Q indicates that this device is a Grade-1 device in accordance with the AEC-Q100 standard. |
|                  | W (when present) indicates the package has wettable flanks. |
|                  | yyy is the package designator. |
|                  | z is the package quantity. R is for a 3,000 piece reel. |
|                  | Q1 indicates that this is an automotive grade (AEC-Q100) device. |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

(2) Output voltages from 0.8V to 5.5V in 50mV increments are available. Contact the factory for details and availability.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

• Texas Instruments, QFN/SON PCB Attachment application report

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on Notifications to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer’s go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.
9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2023) to Revision B (February 2024)

- Added DGS package information to document as Advance Information .................................................. 1
- Added AEC-Q100 bullets and deleted Operating junction temperature bullet in Features section .......... 1
- Updated voltage tolerance for output voltage < 3.3V .................................................................................. 5
- Added high-temperature quiescent current specification ............................................................................. 5
- Deleted extraneous \( T \) from Equation 1 .............................................................................................................. 15
- Added \( C \) information to Device Nomenclature .......................................................................................... 25

Changes from Revision * (December 2022) to Revision A (August 2023)

- Changed document status from Advance Information to Production Data .................................................. 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
10.1 Mechanical Data

**PACKAGE OUTLINE**

**DSG0008A**

**WSON - 0.8 mm max height**

**PLASTIC SMALLOUTLINE - NO LEAD**

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
EXAMPLE BOARD LAYOUT

**DSG0008A**

**WSON - 0.8 mm max height**

**PLASTIC SMALL OUTLINE - NO LEAD**

---

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
EXAMPLE STENCIL DESIGN

DSG0008A  WSON - 0.8 mm max height
PLASTIC SMALL OUTLINE - NO LEAD

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.
NOTES:
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
EXAMPLE BOARD LAYOUT

DSG0008B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
EXAMPLE STENCIL DESIGN

DSG0008B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.
### PACKAGING INFORMATION

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<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
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(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet J5709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS7A21-Q1:**

- Catalog: TPS7A21

**NOTE:** Qualified Version Definitions:

- Catalog - TI's standard catalog product
### TAPE AND REEL INFORMATION

#### REEL DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

#### TAPE DIMENSIONS

- **K0**: Dimension designed to accommodate the component width
- **P1**: Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Q1**: Pocket Quadrants
- **Q2**: Cavity
- **Q3**: Sprocket Holes
- **Q4**: User Direction of Feed

*All dimensions are nominal*

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<tr>
<th>Device</th>
<th>Package Type</th>
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### TAPE AND REEL BOX DIMENSIONS

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</tbody>
</table>

*All dimensions are nominal*
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
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