TPS7B4250-Q1 50-mA 40-V Voltage-Tracking LDO With 5-mV Tracking Tolerance

1 Features

• Qualified for Automotive Applications
• AEC-Q100 Qualified With the Following Results
  – Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  – Device HBM ESD Classification Level 3A
  – Device CDM ESD Classification Level C6
• –20-V to 45-V Wide, Maximum Input Voltage Range
• Output Current, 50 mA
• Very-Low Output-Tracking Tolerance, 5 mV (max)
• 150-mV Low Dropout Voltage When $I_{\text{OUT}} = 10 \text{ mA}$
• Combined Reference and Enable Input
• 40-µA Low Quiescent Current at Light Load
• Extreme, Wide ESR Range.
  – Stable with 1-µF to 50-µF Ceramic Output Capacitor, ESR 1 mΩ to 20 Ω
• Reverse Polarity Protection
• Overtemperature Protection
• Output Short-Circuit Proof to Ground and Supply
• SOT-23 Package

2 Applications

• Off-board Sensor Supply
• High-Precision Sensor Tracking

3 Description

The TPS7B4250-Q1 device is a monolithic, integrated low-dropout voltage tracker. The device is available in a SOT-23 package. The TPS7B4250-Q1 device is designed to supply off-board sensors in an automotive environment. The IC has integrated protection for overload, over temperature, reverse polarity, and output short-circuit to the battery and ground.

A reference voltage applied at the adjust-input pin, ADJ, regulates supply voltages up to $V_{\text{IN}} = 45 \text{ V}$ with high accuracy and loads up to 50 mA.

By setting the adjust/enable input pin, ADJ/EN, to low, the TPS7B4250-Q1 device switches to standby mode which reduces the quiescent current to the minimum value.

4 Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS7B4250-Q1</td>
<td>SOT-23 (5)</td>
<td>2.90 mm x 1.60 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
## Changes from Original (October 2013) to Revision A

<table>
<thead>
<tr>
<th>Change Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Changed CDM ESD Classification level from C3B to C4 throughout document</td>
<td>1</td>
</tr>
<tr>
<td>Changed $V_{\text{OUT}}$ min value from –0.3 to –1 in the Absolute Maximum Ratings table</td>
<td>5</td>
</tr>
<tr>
<td>Added transient current flow to ESD rating in the Absolute Maximum Ratings table</td>
<td>5</td>
</tr>
<tr>
<td>Changed HBM absolute maximum rating from 2 kV to 4 kV</td>
<td>5</td>
</tr>
<tr>
<td>Deleted relevant ESR value from Recommended Operating Conditions table</td>
<td>5</td>
</tr>
<tr>
<td>Added greater-than-or-equal-to ($\geq$) value to $V_{\text{ADJ/EN}}$ in condition statement of the Electrical Characteristics table</td>
<td>6</td>
</tr>
<tr>
<td>Added $V_{\text{ADJ}} = 1.5$ V to both test conditions for $V_{\text{UVLO}}$ parameter in the Electrical Characteristics table</td>
<td>6</td>
</tr>
<tr>
<td>Changed max value for load regulation parameter from 3 to 4 in the Electrical Characteristics table</td>
<td>6</td>
</tr>
<tr>
<td>Changed max value for the current consumption test condition where $I_{\text{O}} = 0.5$ mA from 80 to 90 in the Electrical Characteristics table</td>
<td>6</td>
</tr>
<tr>
<td>Added the Detailed Description section</td>
<td>9</td>
</tr>
<tr>
<td>Added the TPS7B4250 block diagram</td>
<td>9</td>
</tr>
</tbody>
</table>
5 Pin Configuration and Functions

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADJ/EN</td>
<td>I</td>
<td>This pin connects to the reference voltage. A low signal disables the IC and a high signal enables the device. Connected the voltage reference directly or with a voltage divider for lower output voltages. To compensate for line influences, TI recommends to place a capacitor close to the IC pins.</td>
</tr>
<tr>
<td>GND</td>
<td>G</td>
<td>Internally connected to pin 5</td>
</tr>
<tr>
<td>GND</td>
<td>G</td>
<td>Internally connected to pin 2</td>
</tr>
<tr>
<td>V_IN</td>
<td>I</td>
<td>This pin is the device supply. To compensate for line influences, TI recommends to place a capacitor close to the IC pins.</td>
</tr>
<tr>
<td>V_OUT</td>
<td>O</td>
<td>V_OUT is an external capacitor that is required between V_OUT and GND with respect to the capacitance and ESR requirements given in the Recommended Operating Conditions.</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage, unregulated input, (V_{\text{IN}})(^{(2),(3)})</td>
<td>–20</td>
<td>45</td>
<td>V</td>
</tr>
<tr>
<td>Output voltage, regulated output, (V_{\text{OUT}})</td>
<td>–1</td>
<td>22</td>
<td>V</td>
</tr>
<tr>
<td>Adjust input and enable input voltage, (\text{ADJ/EN})(^{(2),(3)})</td>
<td>–0.3</td>
<td>22</td>
<td>V</td>
</tr>
<tr>
<td>ADJ Voltage minus input voltage (ADJ–(V_{\text{IN}}), (V_{\text{IN}} &gt; 0) V)</td>
<td>7</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Operating junction temperature, (T_{\text{J}})</td>
<td>–40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature, (T_{\text{stg}})</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(1\) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(2\) All voltage values are with respect to ground, GND.

\(3\) Absolute maximum voltage.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{(ESD)}}) Electrostatic discharge</td>
<td>±4000</td>
<td>V</td>
</tr>
</tbody>
</table>

\(1\) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{IN}}) Unregulated input</td>
<td>4</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{OUT}}) regulated output</td>
<td>1.5</td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>(\text{ADJ/EN}) Adjust input and enable input voltage</td>
<td>1.5</td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>(\text{ADJ–}V_{\text{IN}}) ADJ voltage minus input voltage</td>
<td>5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(C_{\text{OUT}}) Output capacitor requirements(^{(2)})</td>
<td>1</td>
<td>50</td>
<td>µF</td>
</tr>
<tr>
<td>(\text{ESR}_{\text{OUT}}) Output ESR requirements</td>
<td>0.001</td>
<td>20</td>
<td>Ω</td>
</tr>
<tr>
<td>(T_{\text{J}}) Operating junction temperature</td>
<td>–40</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(1\) Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

\(2\) The minimum output capacitance requirement is applicable for a worst-case capacitance tolerance of 30%.

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1),(2)})</th>
<th>TPS7B4250-Q1</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DBV (SOT-23)</td>
<td></td>
</tr>
<tr>
<td>(R_{\text{JA}}) Junction-to-ambient thermal resistance</td>
<td>171.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{\text{JC(top)}}) Junction-to-case (top) thermal resistance</td>
<td>81.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{\text{JB}}) Junction-to-board thermal resistance</td>
<td>31.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{\text{JT}}) Junction-to-top characterization parameter</td>
<td>4.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{\text{JB}}) Junction-to-board characterization parameter</td>
<td>31.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{\text{JC(bot)}}) Junction-to-case (bottom) thermal resistance</td>
<td>N/A</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

\(1\) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report (SPRA953).

\(2\) The thermal data is based on the JEDEC standard high K profile, JESD 51-7. Two-signal, two-plane, four-layer board with 2-oz. copper. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated.
### 6.5 Electrical Characteristics

\( V_I = 13.5 \text{ V}, \ 18 \text{ V} \geq V_{\text{ADJ/EN}} \geq 1.5 \text{ V}, \ T_J = -40^\circ \text{C} \text{ to } 150^\circ \text{C} \) unless otherwise stated

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{UVLO}} )</td>
<td>( V_{\text{IN}} ) undervoltage detection</td>
<td>Ramp up ( V_I ) until the output turns on, ( V_{\text{ADJ}} = 1.5 \text{ V} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.65</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Ramp down ( V_I ) until the output turns off, ( V_{\text{ADJ}} = 1.5 \text{ V} )</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Delta V_O )</td>
<td>Output-voltage tracking accuracy</td>
<td>( \Delta V_O = 100 \text{ µA} ) ( \leq 1 \text{ mA}, \ \ V_I = 4 \text{ V} ) ( \leq 40 \text{ V}, \ \ 1.5 \text{ V} &lt; V_{\text{ADJ}} &lt; \ V_I - 0.3 \text{ V} )</td>
<td>-4</td>
<td>4</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \Delta V_O = 1 \text{ mA} ) ( \leq 50 \text{ mA}, \ \ V_I = 4 \text{ V} ) ( \leq 40 \text{ V}, \ \ 1.5 \text{ V} &lt; V_{\text{ADJ}} &lt; \ V_I - 1.5 \text{ V} )</td>
<td>-5</td>
<td>5</td>
<td>mV</td>
</tr>
<tr>
<td>( \Delta V_{O,\text{IL}} )</td>
<td>Load regulation steady-state</td>
<td>( I_O = 1 \text{ mA} ) ( \leq 30 \text{ mA} )</td>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Delta V_{O,\text{AVL}} )</td>
<td>Line regulation steady-state</td>
<td>( I_O = 10 \text{ mA}, \ \ V_I = 6 \text{ V} ) ( \leq 40 \text{ V} )</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>Power-supply ripple rejection</td>
<td>Frequency = 100 Hz, ( V_{\text{IP}} = 0.5 \text{ V} ) ( \text{pp}, I_O = 5 \text{ mA}, C_O = 2.2 \mu \text{F} )</td>
<td>60</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{dropout}} )</td>
<td>Dropout voltage, ( V_{\text{dropout}} = V_I - V_O )</td>
<td>( I_O = 10 \text{ mA}, \ \ V_I \geq 4 \text{ V} ) ((1))</td>
<td>150</td>
<td>265</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_O = 50 \text{ mA}, \ \ V_I \geq 4 \text{ V} ) ((1))</td>
<td>550</td>
<td>1000</td>
<td>mV</td>
</tr>
<tr>
<td>( I_L )</td>
<td>Output-current limitation</td>
<td>( V_O ) short to GND</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>100</td>
<td>500</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_R )</td>
<td>Reverse current at ( V_{\text{IN}} )</td>
<td>( V_I = 0 \text{ V}, \ \ V_O = 20 \text{ V}, \ \ V_{\text{ADJ}} = 5 \text{ V} )</td>
<td>-5</td>
<td>0</td>
<td>µA</td>
</tr>
<tr>
<td>( I_{\text{RIN1}} )</td>
<td>Reverse current at negative input voltage</td>
<td>( V_I = -20 \text{ V}, \ \ V_O = 0 \text{ V}, \ \ V_{\text{ADJ}} = 5 \text{ V} )</td>
<td>-5</td>
<td>0</td>
<td>µA</td>
</tr>
<tr>
<td>( I_{\text{RIN2}} )</td>
<td></td>
<td>( V_I = -20 \text{ V}, \ \ V_O = 20 \text{ V}, \ \ V_{\text{ADJ}} = 5 \text{ V} )</td>
<td>-5</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>( T_{SD} )</td>
<td>Thermal shutdown temperature</td>
<td>( T_J ) increasing because of power dissipation generated by the IC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>175</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>( I_Q )</td>
<td>Current consumption</td>
<td>( V_{\text{ADJ}} &lt; 0.8 \text{ V}, \ \ T_A \leq 85^\circ \text{C} )((2))</td>
<td>7.5</td>
<td>15</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{\text{ADJ}} &lt; 0.8 \text{ V}, \ \ T_A \leq 125^\circ \text{C} )</td>
<td>20</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_O = 0.5 \text{ mA}, \ \ V_{\text{ADJ}} = 5 \text{ V} )</td>
<td>40</td>
<td>90</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_O = 30 \text{ mA}, \ \ V_{\text{ADJ}} = 5 \text{ V} )</td>
<td>150</td>
<td>350</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{ADJ}} )</td>
<td>Adjust-input and enable-input current</td>
<td>( V_{\text{ADJ}} = 5 \text{ V} )</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{ADJ,low}} )</td>
<td>Adjust and enable low signal valid</td>
<td>( V_O = 0 \text{ V} )</td>
<td>0.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{ADJ,high}} )</td>
<td>Adjust and enable high signal valid</td>
<td>(</td>
<td>V_O - V_{\text{ADJ}}</td>
<td>&lt; 5 \text{ mV} )</td>
<td>1.5</td>
</tr>
</tbody>
</table>

(1) Measured when the output voltage \( V_O \) has dropped 10 mV from the typical value.
(2) Ensured by design.
6.6 Typical Characteristics

**Figure 1. Dropout Voltage vs Temperature**

- Graph showing dropout voltage vs temperature.
- Conditions: $V_I = V_{ADJ} = 4\, \text{V}$, $I_O = 10\, \text{mA}$.

**Figure 2. Dropout Voltage vs Output Current**

- Graph showing dropout voltage vs output current.
- Conditions: $V_I = V_{ADJ} = 4\, \text{V}$.

**Figure 3. Ground Current vs Output Current**

- Graph showing ground current vs output current.
- Conditions: $V_I = 13.5\, \text{V}$, $V_{ADJ} = 5\, \text{V}$.

**Figure 4. Ground Current vs Temperature**

- Graph showing ground current vs temperature.
- Conditions: $V_I = 13.5\, \text{V}$.

**Figure 5. Current-limit vs Temperature**

- Graph showing current-limit vs temperature.
- Conditions: $V_I = V_{ADJ} = 5\, \text{V}$.

**Figure 6. Tracking Error vs Temperature**

- Graph showing tracking error vs temperature.
- Conditions: $V_I = V_{ADJ} = 5\, \text{V}$, $I_O = 1\, \text{mA, 50 mA}$.
Typical Characteristics (continued)

**Figure 7. Input Voltage vs Output Voltage**

- $V_{ADJ} = 5 \text{ V}$
- $V_I = 9 \text{ to } 16 \text{ V}$
- 2.2-µF ceramic output capacitor

**Figure 8. Reference Voltage vs Output Voltage**

- $V_{I} = 13.5 \text{ V}$
- $V_{ADJ} = 5 \text{ V}$
- $I_O = 5 \text{ to } 30 \text{ mA}$
- 2.2-µF ceramic output capacitor

**Figure 9. Line Transient**

- $V_I = 13.5 \text{ V}$
- $C_O = 2.2 \text{ µF}$
- $I_{LOAD} = 25 \text{ mA}$

**Figure 10. Load Transient**

- $V_I = 13.5 \text{ V}$
- $C_O = 2.2 \text{ µF}$
- $I_{LOAD} = 25 \text{ mA}$

**Figure 11. Power-Supply Rejection Ratio vs Frequency**

- $V_I = 13.5 \text{ V}$
- $C_O = 2.2 \text{ µF}$
- $I_{LOAD} = 25 \text{ mA}$

**Figure 12. ESR Stability vs Load Capacitance**

- $ESR$ of $C_O$ (Ω)
7 Detailed Description

7.1 Overview
The TPS7B4250-Q1 device is a monolithic integrated low-dropout voltage tracker with ultra-low tracking tolerance. Several types of protection circuits are also integrated in the device such as output current limitation, reverse polarity protection, and thermal shutdown in case of over temperature.

7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 Regulated Output (\(V_{\text{OUT}}\))
\(V_{\text{OUT}}\) is the regulated output based on the reference voltage. The output has current limitation. During initial power up, the regulator has an incorporated soft start to control the initial current through the pass element.

7.3.2 Undervoltage Shutdown
The device has an internally-fixed undervoltage shutdown threshold. Undervoltage shutdown activates when the input voltage on \(V_{\text{IN}}\) drops below UVLO. This activation ensures the regulator is not latched into an unknown state during low input supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up similar to a standard power-up sequence when the input voltage is above the required levels.
Feature Description (continued)

7.3.3 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 175°C which allows the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The internal protection circuitry of the TPS7B4250-Q1 device has been designed to protect against overload conditions. The circuitry was not intended to replace proper heat-sinking. Continuously running the TPS7B4250-Q1 device into thermal shutdown degrades device reliability.

7.3.4 \( V_{\text{OUT}} \) Short to Battery

The TPS7B4250-Q1 device survives a short to battery when the output is shorted to the battery as shown in Figure 13. No damage occurs to the device. A short to the battery can also occur when the device is powered by an isolated supply at a lower voltage as shown in Figure 14. In this case the TPS7B4250-Q1 supply input voltage is set at 7 V when a short to battery (14 V typical) occurs on \( V_{\text{OUT}} \) which typically runs at 5 V. The continuous reverse current flows out through \( V_{\text{IN}} \) is less than 5 µA.

7.3.5 Tracking Regulator with ENABLE Circuit

By pulling the reference voltage of the device below 0.8 V, the IC disables and enters a sleep state where the device draws 7.5 µA (typical) from the power supply. In a real application, the reference voltage is generally sourced from another LDO voltage rail. A case where the device must be disabled without a shutdown of the reference voltage can occur. In such case, the device can be configured as shown in Figure 15. The TPS7A6650-Q1 device is a 150-mA LDO with ultra-low quiescent current that is used as a reference voltage to the TPS7B4250-Q1 device and also as a power supply to the ADC. In a configuration as shown in Figure 15, the status of the device is controlled by an MCU I/O.
7.4 Device Functional Modes

7.4.1 Operation With \( V_I < 4 \) V

The device operates with input voltages above 4 V. The maximum UVLO voltage is 3 V and operates at input voltage above 4 V. The device can also operate at lower input voltages; no minimum UVLO voltage is specified. At input voltages below the actual UVLO voltage, the device does not operate.

7.4.2 Operation With ADJ/EN Control

The rising-edge threshold voltage of the ADJ/EN pin is 1.5 V (maximum). When the EN pin is held above that voltage and the input voltage is above the 4 V, the device becomes active. The enable falling edge is 0.8 V (minimum). When the EN pin is held below that voltage the device is disabled, the IC quiescent current is reduced in this state.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
Based on the end-application, different values of external components can be used. An application can require a larger output capacitor during fast load steps to prevent a reset from occurring. TI recommends a low ESR ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.

8.2 Typical Application
Figure 16 show typical application circuit for the TPS7B4250-Q1 device.

8.2.1 Design Requirements
For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>4 to 40 V</td>
</tr>
<tr>
<td>ADJ reference voltage</td>
<td>1.5 to 18 V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>1.5 to 18 V</td>
</tr>
<tr>
<td>Output current rating</td>
<td>50 mA</td>
</tr>
<tr>
<td>Output capacitor range</td>
<td>1 µF to 50 µF</td>
</tr>
<tr>
<td>Output capacitor ESR range</td>
<td>1 mΩ to 20 Ω</td>
</tr>
</tbody>
</table>
8.2.2 Detailed Design Procedure

To begin the design process, determine the following:
- Input voltage range
- Reference voltage
- Output voltage
- Output current rating
- Input capacitor
- Output capacitor

8.2.2.1 External Capacitors

An input capacitor, $C_I$, is recommended to buffer line influences. Connect the capacitors close to the IC pins.

The output capacitor for the TPS7B4250-Q1 device is required for stability. Without the output capacitor, the regulator oscillates. The actual size and type of the output capacitor can vary based on the application load and temperature range. The effective series resistance (ESR) of the capacitor is also a factor in the IC stability. The worst case is determined at the minimum ambient temperature and maximum load expected. To ensure stability of TPS7B4250-Q1 device, the device requires an output capacitor between 1 µF and 50 µF with an ESR range between 0.001 Ω and 20 Ω that can cover most types of capacitor ESR variation under the recommend operating conditions. As a result, the output capacitor selection is flexible.

The capacitor must also be rated at all ambient temperature expected in the system. To maintain regulator stability down to –40°C, use a capacitor rated at that temperature.

8.2.3 Application Curves

![Figure 17. Power Up](image)

![Figure 18. Power Down](image)

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 4 V to 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B4250-Q1 device, adding an electrolytic capacitor with a value of 10-µF and a ceramic bypass capacitor at the input is recommended.
10 Layout

10.1 Layout Guidelines

10.1.1 Package Mounting

Solder-pad footprint recommendations for the TPS7B4250-Q1 device are available in the *Mechanical, Packaging, and Orderable Information* section and at [www.ti.com](http://www.ti.com).

10.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance such as PSRR, output noise, and transient response, TI recommends to design the board with separate ground planes for $V_{IN}$ and $V_{OUT}$, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and ensure stability. Every capacitor must be placed as close as possible to the device and on the same side of the PCB as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because of the negative impact on system performance. Vias and long traces can also cause instability.

If possible, and to ensure the maximum performance denoted in this product data sheet, use the same layout pattern used for TPS7B4250 evaluation board, available at [www.ti.com](http://www.ti.com).

10.2 Layout Example

![Figure 19. TPS7B4250-Q1 Layout Example](image-url)
10.3 Power Dissipation and Thermal Considerations

Device power dissipation is calculated with Equation 1.

\[ P_D = I_O \times (V_I - V_O) + I_Q \times V_I \]

where
- \( P_D \) = continuous power dissipation
- \( I_O \) = output current
- \( V_I \) = input voltage
- \( V_O \) = output voltage
- \( I_Q \) = quiescent current

(1)

As \( I_Q \ll I_O \), the term \( I_Q \times V_I \) in Equation 1 can be ignored.

For a device under operation at a given ambient air temperature (\( T_A \)), calculate the junction temperature (\( T_J \)) with Equation 2.

\[ T_J = T_A + (\theta_{JA} \times P_D) \]

where
- \( \theta_{JA} \) = junction-to-junction-ambient air thermal impedance

(2)

A rise in junction temperature because of power dissipation can be calculated with Equation 3.

\[ \Delta T = T_J - T_A = (\theta_{JA} \times P_D) \]

(3)

For a given maximum junction temperature (\( T_{JM} \)), the maximum ambient air temperature (\( T_{AM} \)) at which the device can operate can be calculated with Equation 4.

\[ T_{AM} = T_{JM} - (\theta_{JA} \times P_D) \]

(4)
11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support
For the PSpice model, see the TPS7B4250 PSpice Transient Model (SLV976).

11.2 Documentation Support

11.2.1 Related Documentation
For related documentation see the following:
- Various Applications for Voltage-Tracking LDO (SLVA789)
- TPS7B4250 Evaluation Module (SLVU975)
- TPS7B4250-Q1 Pin FMEA (SLVA738)

11.3 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resource
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community Ti's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support Ti's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks
E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS7B4250QDBVQ1</td>
<td>PREVIEW</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 125</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPS7B4250QDBVRQ1</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>PA3Q</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp**: - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material**: Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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### TAPE AND REEL INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS7B4250QDBVRQ1</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>178.0</td>
<td>9.0</td>
<td>3.3</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*

**Notes:**
- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

---

**TAPE DIMENSIONS**

- K0
- P1

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- Q1
- Q2
- Q3
- Q4

- P1: Pitch between successive cavity centers
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS7B4250QDBVRQ1</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>190.0</td>
<td>190.0</td>
<td>30.0</td>
</tr>
</tbody>
</table>
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
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