1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, $T_A$
  - Junction temperature: –40°C to +150°C, $T_J$
- Wide input operating voltage range (3 V to 40 V):
  - Absolute maximum input voltage range: –40 V to +45 V
- Wide output voltage range: 2 V to 40 V
- Maximum output current: 70 mA
- Very-tight, output-tracking tolerance: 5 mV (max)
- Low dropout voltage: 500 mV (max) at 70 mA
- Combined reference and enable functionalities
- Low quiescent current at light load: 35 μA
- Wide $C_{OUT}$ and ESR range:
  - Stable with 1-µF to 200-µF ceramic output capacitor, 1-mΩ to 3-Ω ESR
- Integrated protection features:
  - Reverse current protection
  - Reverse polarity protection
  - Overtemperature protection
  - Protection against output short-circuit to ground and supply
- Available in two 5-pin SOT-23 packages:
  - Standard SOT-23 (DBV)
  - Thermally enhanced SOT-23 (DYB)

2 Applications

- Powertrain pressure sensors
- Powertrain temperature sensors
- Powertrain exhaust sensors
- Powertrain fluid concentration sensors
- Body control modules (BCM)

3 Description

The TPS7B4255-Q1 is a low-dropout (LDO) voltage-tracking regulator, with high tracking accuracy and excellent load and line transient response. The device is available in two 5-pin, SOT-23 packages (DBV and DYB). The TPS7B4255-Q1 is designed to supply off-board sensors in automotive applications such as powertrain systems. Because the risk of failure in cables that deliver off-board power is high, the device comes with integrated protection features against fault conditions such as reverse current (short to battery), reverse polarity, output short to ground (current limit), and overtemperature (thermal shutdown). The device is designed to handle a 45-V (absolute maximum) input voltage and survive the automotive load dump transient conditions.

A reference voltage applied at the ADJ/EN pin is effectively tracked at the OUT pin with very tight tolerance for loads up to 70 mA. The TPS7B4255-Q1 can therefore deliver the power-supply voltage to the off-board sensors with high precision, which can help improve the reliability and accuracy of measurements made using ratiometric sensors.

By setting the ADJ/EN input pin low, the TPS7B4255-Q1 switches to standby mode and reduces the quiescent current of the LDO to less than 3.25 μA.

Package Information

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS7B4255-Q1</td>
<td>DBV (SOT-23, 5)</td>
<td>2.9 mm × 2.8 mm</td>
</tr>
<tr>
<td></td>
<td>DYB (SOT-23, 5)</td>
<td>2.93 mm × 2.7 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Typical Application

![Typical Application Diagram]
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2022) to Revision A (August 2023) ......................................................... 1

• Changed document status from Advance Information to Production Data ........................................... 1
5 Pin Configuration and Functions

[Diagram of 5-pin configuration]

Figure 5-1. DBV Package, 5-Pin SOT-23 (Top View)

Figure 5-2. DYB Package, 5-Pin SOT-23 (Top View)

Table 5-1. Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>DBV</th>
<th>DYB</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADJ/EN</td>
<td>1</td>
<td>1</td>
<td>I</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>2, 5</td>
<td>G</td>
</tr>
<tr>
<td>IN</td>
<td>3</td>
<td>3</td>
<td>I</td>
</tr>
<tr>
<td>NC</td>
<td>5</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>OUT</td>
<td>4</td>
<td>4</td>
<td>O</td>
</tr>
</tbody>
</table>

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>PIN</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>Unregulated input voltage</td>
<td>$-40$</td>
<td>$45$</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Tracker output voltage</td>
<td>$-5$</td>
<td>$45$</td>
</tr>
<tr>
<td>$V_{ADJ/EN}$</td>
<td>Adjustable reference and enable input voltage</td>
<td>$-0.3$</td>
<td>$45$</td>
</tr>
<tr>
<td>$V_{IN} - V_{OUT}$</td>
<td>Input output voltage difference</td>
<td>$-40$</td>
<td>$40$</td>
</tr>
<tr>
<td>$T_J$</td>
<td>Operating junction temperature</td>
<td>$-40$</td>
<td>$150$</td>
</tr>
<tr>
<td>$T_{STG}$</td>
<td>Storage temperature</td>
<td>$-65$</td>
<td>$150$</td>
</tr>
</tbody>
</table>

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect the device reliability, functionality, performance, and shorten the device lifetime.
6.2 ESD Ratings

<table>
<thead>
<tr>
<th>$V_{(ESD)}$</th>
<th>Electrostatic discharge</th>
<th>Human-body model (HBM), per AEC Q100-002(^{(1)})</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Charged-device model (CDM), per AEC Q100-011</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>All pins</td>
<td>±2000</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Corner pins</td>
<td>±500</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>3</td>
<td>40</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>2</td>
<td>40</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{ADJ}$</td>
<td>0</td>
<td>70</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>0.001</td>
<td>3</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>$R_{\theta JA}$</td>
<td>176.3</td>
<td>127.8</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>$R_{\theta JC(top)}$</td>
<td>75.6</td>
<td>59.9</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>$R_{\theta JB}$</td>
<td>44.4</td>
<td>16.6</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>$\Psi_{JT}$</td>
<td>17.9</td>
<td>4.4</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>$\Psi_{JB}$</td>
<td>44.1</td>
<td>16.4</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>$R_{\theta JC(bot)}$</td>
<td>N/A</td>
<td>N/A</td>
<td>°C/W</td>
<td></td>
</tr>
</tbody>
</table>

(1) For robust EMI performance the minimum input capacitance recommended is 500 nF.
(2) Effective output capacitance of 500 nF minimum required for stability.

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)}) (^{(2)})</th>
<th>TPS7B4255-Q1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DBV (SOT-23)</td>
</tr>
<tr>
<td></td>
<td>5 PINS</td>
</tr>
<tr>
<td>$R_{\theta JA}$</td>
<td>176.3</td>
</tr>
<tr>
<td>$R_{\theta JC(top)}$</td>
<td>75.6</td>
</tr>
<tr>
<td>$R_{\theta JB}$</td>
<td>44.4</td>
</tr>
<tr>
<td>$\Psi_{JT}$</td>
<td>17.9</td>
</tr>
<tr>
<td>$\Psi_{JB}$</td>
<td>44.1</td>
</tr>
<tr>
<td>$R_{\theta JC(bot)}$</td>
<td>N/A</td>
</tr>
</tbody>
</table>

(1) The thermal data is based on the JEDEC standard high K profile, JESD 51-7, two-signal, two-plane, four-layer board with 2-oz. copper. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated.
(2) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
6.5 Electrical Characteristics

specified at $T_J = -40^\circ C$ to $+150^\circ C$, $V_{IN} = 13.5 V$, $I_{OUT} = 100 \mu A$, $C_{OUT} = 1 \mu F$, $C_{IN} = 1 \mu F$, and $V_{ADJ} = 5 V$ (unless otherwise noted); typical values are at $T_J = 25^\circ C$.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Delta V_{OUT}$</td>
<td>Output voltage tracking accuracy</td>
<td>$V_{IN} = V_{OUT} + 600 mV$ to $40 V$, $I_{OUT} = 100 \mu A$ to $70 mA$</td>
<td>$-5$</td>
<td>$5$</td>
<td>mV</td>
</tr>
<tr>
<td>$\Delta V_{OUT(IN)}$</td>
<td>Line regulation</td>
<td>$V_{IN} = V_{OUT} + 600 mV$ to $40 V$</td>
<td>$0.5$</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$\Delta V_{OUT(LOAD)}$</td>
<td>Load regulation</td>
<td>$V_{IN} = V_{OUT} + 600 mV$, $I_{OUT} = 100 \mu A$ to $70 mA$ (1)</td>
<td>$0.6$</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$I_Q$</td>
<td>Quiescent current</td>
<td>$V_{IN} = 5.6 V$ to $40 V$, $I_{OUT} = 100 \mu A$, $T_J = 25^\circ C$</td>
<td>$35$</td>
<td>$40$</td>
<td>$\mu A$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} = 5.6 V$ to $40 V$, $I_{OUT} = 100 \mu A$, $-40^\circ C &lt; T_J &lt; 85^\circ C$</td>
<td>$45$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} = 5.6 V$ to $40 V$, $I_{OUT} = 100 \mu A$</td>
<td>$50$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{GND}$</td>
<td>Ground current</td>
<td>$V_{IN} = 5.6 V$ to $40 V$, $I_{OUT} = 70 mA$, $T_J = 25^\circ C$</td>
<td>$470$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} = 5.6 V$ to $40 V$, $I_{OUT} = 100 \mu A$</td>
<td>$550$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DO}$</td>
<td>Dropout voltage</td>
<td>$I_{OUT} = 70 mA$, $V_{ADJ} \geq 5 V$, $V_{IN} = V_{ADJ}$</td>
<td>$500$</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{OUT} = 50 mA$, $V_{ADJ} \geq 5 V$, $V_{IN} = V_{ADJ}$</td>
<td>$365$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{SHUTDOWN}$</td>
<td>Shutoff supply current ($I_{GND}$)</td>
<td>$V_{ADJ} = 0 V$</td>
<td>$3.25$</td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{ADJ/EN}$</td>
<td>ADJ/EN pin current</td>
<td>$3.25$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{UVLO(RISING)}$</td>
<td>Raising input supply UVLO</td>
<td>$V_{IN}$ rising</td>
<td>$2.6$</td>
<td>$2.7$</td>
<td>$V$</td>
</tr>
<tr>
<td>$V_{UVLO(FALLING)}$</td>
<td>Falling input supply UVLO</td>
<td>$V_{IN}$ falling</td>
<td>$2.3$</td>
<td>$2.4$</td>
<td>$2.5$</td>
</tr>
<tr>
<td>$V_{UVLO(HYST)}$</td>
<td>UVLO hysteresis</td>
<td>$300$</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$V_L$</td>
<td>Adjustable and enable logic input low level</td>
<td>$0.85$</td>
<td></td>
<td></td>
<td>$V$</td>
</tr>
<tr>
<td>$V_H$</td>
<td>Adjustable and enable logic input high level</td>
<td>$1.75$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{CL}$</td>
<td>Output current limit</td>
<td>$V_{IN} = V_{OUT} = 1 V$, $V_{OUT}$ short to $90% \times V_{ADJ}$</td>
<td>$75$</td>
<td>$105$</td>
<td>$130$</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power-supply ripple rejection</td>
<td>$V_{IN} = V_{OUT} = 1 V$, frequency $= 100$ Hz, $I_{OUT} = 70 mA$</td>
<td>$80$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_o$</td>
<td>Output noise voltage</td>
<td>$V_{OUT} = 3.3 V$, $I_{OUT} = 1 mA$, $BW = 10$ Hz to $100$ kHz, a $5 \mu V_{RMS}$ reference is used for this measurement</td>
<td>$150$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{REV}$</td>
<td>Reverse current at $V_N$</td>
<td>$V_{IN} = 0 V$, $V_{OUT} = 20 V$, $V_{ADJ} = 5 V$</td>
<td>$-0.25$</td>
<td>$0.25$</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{REV(N1)}$</td>
<td>Reverse current at negative $V_N$</td>
<td>$V_{IN} = -20 V$, $V_{OUT} = 20 V$, $V_{ADJ} = 5 V$</td>
<td>$-0.5$</td>
<td>$0.5$</td>
<td></td>
</tr>
<tr>
<td>$I_{REV(N2)}$</td>
<td>Reverse current at negative $V_N$</td>
<td>$V_{IN} = -20 V$, $V_{OUT} = 0 V$, $V_{ADJ} = 5 V$</td>
<td>$-0.5$</td>
<td>$0.5$</td>
<td></td>
</tr>
<tr>
<td>$T_J$</td>
<td>Junction temperature</td>
<td>$-40$</td>
<td>$150$</td>
<td></td>
<td>$^\circ C$</td>
</tr>
<tr>
<td>$T_{SD(SHUTDOWN)}$</td>
<td>Junction shutdown temperature</td>
<td>$175$</td>
<td></td>
<td></td>
<td>$^\circ C$</td>
</tr>
<tr>
<td>$T_{SHUTDOWN}$</td>
<td>Hysteresis of thermal shutdown</td>
<td>$15$</td>
<td></td>
<td></td>
<td>$^\circ C$</td>
</tr>
</tbody>
</table>

(1) Power dissipation is limited to 2 W for device production testing purposes. The power dissipation can be higher during normal operation. Please see the thermal dissipation section for more information on how much power the device can dissipate while maintaining a junction temperature below 150°C.

6.6 Timing Characteristics

specified at $V_{IN} = 13.5 V$, $I_{OUT} = 100 \mu A$, $C_{OUT} = 1 \mu F$, $C_{IN} = 1 \mu F$, and $V_{ADJ} = 5 V$ (unless otherwise noted), and $V_{ADJ} = 5 V$ (unless otherwise noted); typical values are at $T_J = 25^\circ C$.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timing Characteristics</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{startup}$</td>
<td>Start-up time</td>
<td>$255$</td>
<td></td>
<td></td>
<td>$\mu s$</td>
</tr>
</tbody>
</table>

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Product Folder Links: TPS7B4255-Q1
6.7 Typical Characteristics

**Figure 6-1. Tracking Error vs Ambient Temperature**

![Tracking Error vs Ambient Temperature](image)

---

**Figure 6-2. Load Regulation**

![Load Regulation](image)

---

**Figure 6-3. Line Regulation**

![Line Regulation](image)

---

**Figure 6-4. Line Regulation**

![Line Regulation](image)

---

**Figure 6-5. Output Voltage vs Input Voltage**

![Output Voltage vs Input Voltage](image)

---

**Figure 6-6. Output Voltage vs Adjustable Reference Voltage**

![Output Voltage vs Adjustable Reference Voltage](image)
6.7 Typical Characteristics (continued)

![Graph of Dropout Voltage vs Ambient Temperature](image1)

*Figure 6-7. Dropout Voltage vs Ambient Temperature*

![Graph of Dropout Voltage vs Output Current](image2)

*Figure 6-8. Dropout Voltage vs Output Current*

![Graph of Ground Current vs Output Current](image3)

*Figure 6-9. Ground Current vs Output Current*

![Graph of Ground Current vs Ambient Temperature](image4)

*Figure 6-10. Ground Current vs Ambient Temperature*

![Graph of Ground Current vs Input Voltage](image5)

*Figure 6-11. Ground Current vs Input Voltage*

![Graph of Current Limit vs Ambient Temperature](image6)

*Figure 6-12. Current Limit vs Ambient Temperature*
6.7 Typical Characteristics (continued)

**Figure 6-13. Current Limit Profile vs. Output Voltage**

- Current Limit (mA)
  - 0
  - 20
  - 40
  - 60
  - 80
  - 100

- % of V\textsubscript{OUT(NOM)}
  - 0
  - 25
  - 50
  - 75
  - 100

- V\textsubscript{IN} = 13.5 V, V\textsubscript{ADJ} = 5 V

**Figure 6-14. Adjustable Pin Current vs Adjustable Pin Voltage**

- I\textsubscript{ADJ} (μA)
  - 2
  - 4
  - 6
  - 8
  - 10
  - 12

- V\textsubscript{ADJ} (V)
  - 0
  - 0.05
  - 0.1
  - 0.15
  - 0.2
  - 0.25

- V\textsubscript{IN} = 13.5 V, I\textsubscript{OUT} = 0 mA

**Figure 6-15. Reverse Current vs Output Voltage**

- I\textsubscript{REV} (μA)
  - 0
  - 5
  - 10
  - 15
  - 20
  - 25
  - 30
  - 35
  - 40

- V\textsubscript{OUT} (V)
  - 0
  - 0.05
  - 0.1
  - 0.15
  - 0.2
  - 0.25

- V\textsubscript{IN} = 0 V, V\textsubscript{ADJ} = 5 V

**Figure 6-16. Reverse Current vs Input Voltage**

- I\textsubscript{REV} (μA)
  - -0.4
  - -0.3
  - -0.2
  - -0.1
  - 0
  - 0.1
  - 0.2

- V\textsubscript{OUT} = 0 V, V\textsubscript{ADJ} = 5 V

**Figure 6-17. Power-Supply Rejection Ratio vs Frequency**

- PSRR (dB)
  - 0
  - 20
  - 40
  - 60
  - 80
  - 100
  - 120
  - 140

- Frequency (Hz)
  - 1x10\(^{1}\)
  - 1x10\(^{2}\)
  - 1x10\(^{3}\)
  - 1x10\(^{4}\)
  - 1x10\(^{5}\)
  - 1x10\(^{6}\)
  - 1x10\(^{7}\)

- V\textsubscript{IN} = 13.5 V, V\textsubscript{ADJ} = 5 V, C\textsubscript{OUT} = 10 μF, T\textsubscript{AMB} = 25°C

**Figure 6-18. Line Transient**

- V\textsubscript{IN} = 13.5 V, V\textsubscript{ADJ} = 5 V, C\textsubscript{OUT} = 10 μF, V\textsubscript{IN} ramp rate = 1 V/μs

V\textsubscript{ADJ} = 5 V, C\textsubscript{OUT} = 10 μF, V\textsubscript{IN} = 9 V to 16 V,
6.7 Typical Characteristics (continued)

Figure 6-19. Load Transient

$V_{IN} = 13.5$ V, $V_{ADJ} = 5$ V, $C_{OUT} = 10 \mu$F, $I_{OUT} = 1$ mA to 30 mA, $I_{OUT}$ ramp rate = 1 A/$\mu$s

Figure 6-20. Start-Up Profile

$V_{IN} = 13.5$ V, $V_{ADJ} = 5$ V, $V_{IN}$ rate of rise = 1 V/$\mu$s, $C_{OUT} = 1$ $\mu$F

Figure 6-21. ESR vs Load Capacitance

$1 \text{ m}\Omega \leq ESR \leq 3 \Omega, 1 \mu$F $\leq C_{OUT} \leq 200 \mu$F
7 Detailed Description

7.1 Overview

The TPS7B4255-Q1 is an integrated, low-dropout (LDO) voltage tracker with ultra-low tracking tolerance. Because of the high risk of cable shorts when powering sensors off-board, multiple protection features are built into the LDO including short to battery, short to GND, and reverse current protection.

This device features thermal shutdown protection, brick-wall current limiting, undervoltage lockout (UVLO), reverse current, and reverse polarity protection.

7.2 Functional Block Diagram

![Figure 7-1. Functional Block Diagram](image)

7.3 Feature Description

7.3.1 Tracker Output Voltage (V_{OUT})

This device is a tracking LDO; thus, with sufficient V_{IN} (≥3 V) applied, the output voltage is determined by the voltage provided to the ADJ/EN pin. The LDO remains disabled as long as V_{ADJ/EN} is less than V_{IL}. When V_{ADJ/EN} exceeds V_{IH}, the output begins to rise to the voltage on the ADJ/EN pin. The output rises linearly as determined by the load, the output capacitor, and the current limit. When the voltage reaches the level on the ADJ/EN pin, the output voltage remains within 5 mV from the voltage set on the ADJ/EN pin over all specified operating conditions.
7.3.1.1 Output Voltage Equal to the Reference Voltage

As shown in Figure 7-2, connect the external reference voltage directly to the ADJ/EN pin. When connected properly, and as given in Equation 1, the LDO output voltage is equal to the reference voltage.

\[ V_{OUT} = V_{REF} \]  

\[ (1) \]

![Figure 7-2. Tracker Output Voltage Equal to the Reference Voltage](image)

7.3.1.2 Output Voltage Less Than the Reference Voltage

Connecting an external resistor divider at the ADJ/EN pin, as shown in Figure 7-3, can help generate an output voltage that is lower than the reference voltage. Both the \( R_1 \) and \( R_2 \) resistors must be less than 100 kΩ in value. Equation 2 calculates \( V_{OUT} \).

\[ V_{OUT} = \frac{V_{REF} \times R_2}{R_1 + R_2} \]

\[ (2) \]

![Figure 7-3. Tracker Output Voltage Lower Than the Reference Voltage](image)
7.3.2 Reverse Current Protection

The TPS7B4255-Q1 incorporates a back-to-back PMOS topology that protects the device from damage against a fault condition, resulting in $V_{OUT}$ being higher than $V_{IN}$ and the subsequent flow of reverse current. No damage occurs to the device if this fault condition occurs, provided the **Absolute Maximum Ratings** are not violated. This integrated protection feature eliminates the need for an external diode. The reverse current comparator typically responds to a reverse voltage condition in 1 µs, and along with the body diode of the blocking PMOS transistor, limits the reverse current to $I_{REV}$.

7.3.3 Undervoltage Lockout

The device has an internally fixed undervoltage lockout threshold. Undervoltage lockout activates when the input voltage $V_{IN}$ drops below the undervoltage lockout (UVLO) level; see the $V_{UVLO(FALLING)}$ parameter in the **Electrical Characteristics** table. This activation makes sure the regulator is not latched into an unknown state during a low input supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up in the standard power-up sequence when the input voltage recovers to the required level (see the $V_{UVLO(RISING)}$ parameter in the **Electrical Characteristics** table).

7.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 175°C, which allows the device to cool. When the junction temperature cools to approximately 160°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle off and on until the excessive power dissipation condition is removed. This cycling limits the dissipation of the regulator, thus protecting the regulator from damage as a result of overheating.

The internal protection circuitry of the TPS7B4255-Q1 is designed to protect against overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the TPS7B4255-Q1 into thermal shutdown degrades device reliability.

7.3.5 Current Limit

The device has an internal current limit circuit to protect the device during overcurrent or shorting conditions. The current limit circuit, as shown in **Figure 7-4**, is a brick-wall scheme. When the device is in current limit, the device sources $I_{CL}$ and the output voltage is not regulated. In this scenario, the output voltage depends on the load impedance.

![Figure 7-4. Current Limit: Brick-Wall Scheme](image-url)
During a current limit event, the potential for high power dissipation exists because of the elevated current level and the increased input-to-output differential voltage ($V_{IN} - V_{OUT}$). If the device heats enough, the device can enter thermal shutdown. If the current-limit condition is not removed when the device turns back on after cooling, the device can enter thermal shutdown again and continue this cycle until the current limit condition is removed. The device survives this fault, but repeatedly operating in this mode degrades long-term reliability.

### 7.3.6 Output Short to Battery

When the output is shorted to the supply (as shown in Figure 7-5), the TPS7B4255-Q1 survives and no damage occurs to the device. As shown in Figure 7-6, a short to the supply can also occur when the device is powered by an isolated supply at a lower voltage. In this example, the TPS7B4255-Q1 supply input voltage is set at 7 V when a short to the main supply (14 V typical) occurs on $V_{OUT}$, which typically runs at 5 V. The device survives without damage, and the back-to-back PMOS topology helps limit the continuous reverse current that flows out through $V_{IN}$ to less than 0.25 μA.

![Figure 7-5. Output Voltage Short to Battery](image1.png)

![Figure 7-6. Output Voltage Higher Than the Input](image2.png)
7.3.7 Tracking Regulator With an Enable Circuit

Pulling the reference voltage below $V_{IL}$ disables the device, and the device enters a sleep state where the device draws 3.25 μA (maximum) from the power supply. In a typical application, the reference voltage is generally sourced from another LDO voltage rail. A scenario where the device must be disabled without a shutdown of the reference voltage can occur; the device can be configured as shown in Figure 7-7 in this case. The TPS7B84-Q1 is a 150-mA LDO with ultra-low quiescent current that provides the reference voltage to both the TPS7B4255-Q1 and the ADC. The operational status of the device is controlled by a microcontroller (MCU) input or output (I/O).

Figure 7-7. Tracking an LDO With an Enable Circuit
7.4 Device Functional Modes

Table 7-1 shows the conditions that lead to the different modes of operation. See the Electrical Characteristics table for parameter values.

<table>
<thead>
<tr>
<th>OPERATING MODE</th>
<th>PARAMETER</th>
<th>V&lt;sub&gt;IN&lt;/sub&gt;</th>
<th>V&lt;sub&gt;ADJ/EN&lt;/sub&gt;</th>
<th>I&lt;sub&gt;OUT&lt;/sub&gt;</th>
<th>T&lt;sub&gt;J&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal operation</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; &gt; V&lt;sub&gt;OUT(Nom)&lt;/sub&gt; + V&lt;sub&gt;DO&lt;/sub&gt; and V&lt;sub&gt;IN&lt;/sub&gt; ≥ V&lt;sub&gt;IN(min)&lt;/sub&gt;</td>
<td>V&lt;sub&gt;ADJ/EN&lt;/sub&gt; &gt; V&lt;sub&gt;IH&lt;/sub&gt;</td>
<td>I&lt;sub&gt;OUT&lt;/sub&gt; ≤ I&lt;sub&gt;OUT(max)&lt;/sub&gt;</td>
<td>T&lt;sub&gt;J&lt;/sub&gt; &lt; T&lt;sub&gt;SD(shutdown)&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>Dropout operation</td>
<td>V&lt;sub&gt;IN(min)&lt;/sub&gt; &lt; V&lt;sub&gt;IN&lt;/sub&gt; &lt; V&lt;sub&gt;OUT(Nom)&lt;/sub&gt; + V&lt;sub&gt;DO&lt;/sub&gt;</td>
<td>V&lt;sub&gt;ADJ/EN&lt;/sub&gt; &gt; V&lt;sub&gt;IH&lt;/sub&gt;</td>
<td>I&lt;sub&gt;OUT&lt;/sub&gt; ≤ I&lt;sub&gt;OUT(max)&lt;/sub&gt;</td>
<td>T&lt;sub&gt;J&lt;/sub&gt; &lt; T&lt;sub&gt;SD(shutdown)&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>Disabled (any true condition disables the device)</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; &lt; V&lt;sub&gt;UVLO&lt;/sub&gt;</td>
<td>V&lt;sub&gt;ADJ/EN&lt;/sub&gt; &lt; V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>Not applicable</td>
<td>T&lt;sub&gt;J&lt;/sub&gt; &gt; T&lt;sub&gt;SD(shutdown)&lt;/sub&gt;</td>
<td></td>
</tr>
</tbody>
</table>

The device turns on when V<sub>IN</sub> is greater than V<sub>UVLO(RISING)</sub> and V<sub>ADJ/EN</sub> is greater than the enable rising threshold V<sub>IH</sub>.

7.4.1 Normal Operation

The device output voltage V<sub>OUT(Nom)</sub> tracks the reference voltage V<sub>ADJ/EN</sub> when the following conditions are met:

- The input voltage is at least 3 V (V<sub>IN(min)</sub>) and greater than the nominal output voltage plus the dropout voltage (V<sub>OUT(nom)</sub> + V<sub>DO</sub>)
- The reference voltage at the ADJ/EN pin is greater than the enable rising threshold V<sub>IH</sub> and stays stable at V<sub>OUT(Nom)</sub>
- The output current is less than I<sub>OUT(max)</sub> (I<sub>OUT</sub> ≤ 70 mA)
- The device junction temperature is less than the thermal shutdown temperature (T<sub>J</sub> < T<sub>SD</sub>)

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, V<sub>IN</sub> < V<sub>OUT(NOM)</sub> + V<sub>DO</sub>, directly after being in a normal regulation state, but not during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage (V<sub>OUT(NOM)</sub> + V<sub>DO</sub>), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the saturation region.

7.4.3 Operation With V<sub>IN</sub> < 3 V

For input voltages below 3 V and above V<sub>UVLO(FALLING)</sub>, the LDO continues to operate but certain circuits can possibly not have the proper headroom to operate within specification. When the input voltage drops below V<sub>UVLO(FALLING)</sub> the device shuts off.

7.4.4 Disable With ADJ/EN Control

The ADJ/EN pin operates as both the reference and the enable pin to the LDO. The output of the device can be shutdown by forcing V<sub>ADJ/EN</sub> less than V<sub>IL</sub>. When disabled, the pass transistor is turned off, the internal circuits are shutdown, and the LDO is in a low-power mode.
8 Application and Implementation

Note
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information
8.1.1 Dropout Voltage

Dropout voltage ($V_{DO}$) is defined as the input voltage minus the output voltage ($V_{IN} - V_{OUT}$) when the pass transistor is fully on. This condition arises when the input voltage falls to the point where the error amplifier must drive the gate of the pass transistor to the rail and has no remaining headroom for the control loop to operate. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage directly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage follows, minus the dropout voltage ($V_{DO}$).

In dropout mode, the output is no longer regulated, and transient performance is severely degraded. The device loses PSRR, and load transients can cause large output voltage deviation.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated output current ($I_{RATED}$, see the Recommended Operating Conditions table), the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}}$$  (3)

8.1.2 Reverse Current

The TPS7B4255-Q1 incorporates reverse current protection that prevents damage from a fault condition, resulting in $V_{OUT}$ being higher than $V_{IN}$. During such a fault condition, where the $V_{IN}$ and $V_{OUT}$ absolute maximum ratings are not violated and $V_{OUT} - V_{IN}$ is less than 40 V, no damage occurs and less than 0.5 μA of reverse current flows through the LDO. The reverse current comparator typically responds to a reverse voltage condition and, along with the body diode of the blocking PMOS transistor, limits the reverse current in 1 μs.
8.2 Typical Application

Figure 8-1 shows a typical application circuit for the TPS7B4255-Q1.

![Typical Application Schematic](image)

8.2.1 Design Requirements

Use the parameters listed in Table 8-1 for this design example.

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>3 V to 40 V</td>
</tr>
<tr>
<td>ADJ/EN reference voltage</td>
<td>2 V to 40 V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>2 V to 40 V</td>
</tr>
<tr>
<td>Output current rating</td>
<td>70 mA</td>
</tr>
<tr>
<td>Output capacitor range</td>
<td>1 µF to 200 µF</td>
</tr>
<tr>
<td>Output capacitor ESR range</td>
<td>1 mΩ to 3 Ω</td>
</tr>
</tbody>
</table>

Table 8-1. Design Parameters
8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Selection

Depending on the end application, different values of external components can be used. An application can require a larger output capacitor during fast load steps to prevent a reset from occurring. Use a low ESR ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.

The TPS7B4255-Q1 requires an output capacitor of at least 1 µF (500 nF or larger capacitance) for stability and an equivalent series resistance (ESR) between 0.001 Ω and 3 Ω. Without the output capacitor, the regulator oscillates. For best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitor is 200 µF.

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND, connected close to the device pins. Some input supplies have a high impedance; thus, placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast rise-time load transients are anticipated, or if the device is located several inches from the input power source.

8.2.3 Application Curves

![Figure 8-2. Power-Up](image)

![Figure 8-3. Power-Down](image)

![Figure 8-4. Dropout Exit Recovery](image)
8.3 Power Supply Recommendations
The device is designed to operate from an input voltage supply range from 3 V to 40 V.

8.4 Layout
8.4.1 Layout Guidelines
For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close as possible to each other, connected by a wide, component-side, copper surface. Using vias and long traces to the input and output capacitors is strongly discouraged and negatively affects system performance. Use a ground reference plane either embedded in the PCB or located on the bottom side of the PCB opposite the components. This reference plane serves to provide accuracy of the output voltage, shield noise, and behaves similarly to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

8.4.1.1 Package Mounting
Solder-pad footprint recommendations for the TPS7B4255-Q1 are available at the end of this document and at www.ti.com.
TI's DYB package footprint can be used for both the DYB package as well as the DBV package for easy multisourcing.

8.4.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance
To improve AC performance (such as PSRR, output noise, and transient response), design the board with separate ground planes for \( V_{\text{IN}} \) and \( V_{\text{OUT}} \), with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must connect directly to the GND pin of the device.
Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and ensure stability. Every capacitor must be placed as close as possible to the device and on the same side of the printed circuit board (PCB) as the regulator.
Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. Using vias and long traces is strongly discouraged because of the negative impact on system performance. Vias and long traces can also cause instability.
If possible, and to make sure that the maximum performance is as denoted in this product data sheet, use the same layout pattern used for the TPS7B4255-Q1 evaluation board, available at www.ti.com.

8.4.1.3 Power Dissipation and Thermal Considerations
Equation 4 calculates the device power dissipation.

\[
P_D = I_{\text{OUT}} \times (V_{\text{IN}} - V_{\text{OUT}}) + I_Q \times V_{\text{IN}}
\]

(4)

where:
- \( P_D \) = Continuous power dissipation
- \( I_{\text{OUT}} \) = Output current
- \( V_{\text{IN}} \) = Input voltage
- \( V_{\text{OUT}} \) = Output voltage
- \( I_Q \) = Quiescent current

Because \( I_Q \) is much less than \( I_{\text{OUT}} \), the term \( I_Q \times V_{\text{IN}} \) in Equation 4 can be ignored.

Calculate the junction temperature \( (T_J) \) with Equation 5 for a device under operation at a given ambient air temperature \( (T_A) \).

\[
T_J = T_A + (R_{\text{Theta JA}} \times P_D)
\]

(5)
where:
- \( R_{\theta JA} \) = Junction-to-junction-ambient air thermal impedance

Equation 6 calculates a rise in junction temperature because of power dissipation.

\[
\Delta T = T_J - T_A = (R_{\theta JA} \times P_D)
\]  

(6)

The maximum ambient air temperature (\( T_{\text{AMAX}} \)) at which the device can operate can be calculated with Equation 7 for a given maximum junction temperature (\( T_{\text{JMAX}} \)).

\[
T_{\text{AMAX}} = T_{\text{JMAX}} - (R_{\theta JA} \times P_D)
\]  

(7)

8.4.1.4 Thermal Performance Versus Copper Area

The most used thermal resistance parameter \( R_{\theta JA} \) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The \( R_{\theta JA} \) recorded in the Thermal Information table is determined by the JEDEC standard (Figure 8-5), PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, \( R_{\theta JA} \) is actually the sum of the package junction-to-case (bottom) thermal resistance (\( R_{\theta JC\text{bot}} \)) plus the thermal resistance contribution by the PCB copper.

Figure 8-5. JEDEC Standard 2s2p PCB

Figure 8-6 through Figure 8-9 illustrate the functions of \( R_{\theta JA} \) and \( \psi_{JB} \) versus copper area and thickness for the DBV package and DYB package. These plots are generated with a 101.6-mm \( \times \) 101.6-mm \( \times \) 1.6-mm PCB of two and four layers. For the 4-layer board, inner planes use 1-oz copper thickness. For the 4-layer board, inner planes use 1-oz copper thickness. A 4 \( \times \) 5 (DBV and DYB package) array of thermal vias with a 300-\( \mu \)m drill diameter and 25-\( \mu \)m copper plating is located as close as practical to the GND pin of the device. The thermal vias connect the top layer, the bottom layer and, in the case of the 4-layer board, the first inner GND plane. Each of the layers has a copper plane of equal area. The PowerPAD™ Thermally Enhanced Package application note discusses the impact that thermal vias have on thermal performance.
As shown in Figure 8-7, $\psi_{JB}$ increases with additional connecting copper area. The reason for this increase is that the board temperature is measured at the copper near the GND pin, and because the GND pin is fused to the die pad, more heat escapes through the GND pin when more copper is connected to the pad, and thus the temperature at this point is higher. Consequently the $\psi_{JB}$ increases. This increase does not imply that heat sinking for the device is reduced when more connecting copper is added. Increasing connecting copper area always increases board-level heat sinking for the device. Furthermore, the boards used for Figure 8-7 have vias connecting to internal copper planes. Therefore, $\psi_{JB}$ is much higher than what is specified in the Thermal Information table, which uses the high-K board layout specified in JESD51-7 that has no thermal vias.
8.4.2 Layout Examples

Circles denote PCB via connections

Figure 8-10. DYB Package Layout Example

Circles denote PCB via connections

Figure 8-11. DBV Package Layout Example
9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>( V_{\text{OUT}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS7B4255Q ( \text{yyyR Q1} )</td>
<td>( Q ) indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. ( \text{yyy} ) is the package designator. ( R ) is the packaging quantity. ( \text{Q1} ) indicates that this device is an automotive grade (AEC-Q100) device.</td>
</tr>
</tbody>
</table>

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on Subscribe to updates to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer’s go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI’s Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
10.1 Mechanical Data

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.
# PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
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<tbody>
<tr>
<td>PTPS7B4255QDYBRQ1</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DYB</td>
<td>5</td>
<td>3000</td>
<td>TBD</td>
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<td>-40 to 125</td>
<td></td>
<td>Samples</td>
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<tr>
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<td>3000</td>
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<td>NIPDAU</td>
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<td>2Q6T</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS7B4255-Q1:**

- Catalog: TPS7B4255

**NOTE:** Qualified Version Definitions:

- Catalog - TI's standard catalog product
### TAPE AND REEL INFORMATION

#### REEL DIMENSIONS

- **Reel Diameter**

#### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component length
- **B0**: Dimension designed to accommodate the component thickness
- **K0**: Overall width of the carrier tape
- **W**: Pitch between successive cavity centers

#### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component thickness
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Pocket Quadrants**
- **Sprocket Holes**
- **User Direction of Feed**

*All dimensions are nominal*

<table>
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<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>180.0</td>
<td>8.4</td>
<td>3.2</td>
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<td>8.0</td>
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# TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
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<td>185.0</td>
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.