1 Features
- Controlled peak input current to prevent over-stressing of the electronic transformer
- Allows Either Step-Up or Step-Up/Down Operation
- Compatible to Generic Electronic Transformers
- Compatible to Magnetic Transformers and DC Power Supplies
- Integrated Active Low-Side Input Rectifiers
- Compact and Simple Circuit
- >85% Efficiency (12-VDC Input)
- Power Factor > 0.9 (Full Load With AC input)
- Hysteresis Control Scheme
- Output Overvoltage Protection
- Overtemperature Shutdown
- 10-pin Thermally Enhanced Very-Thin Fine Pitch Small-Outline Package

2 Applications
- MR16/AR111 LED Lamps
- Lighting System Using Electronic Transformer
- General Lighting Systems That Require a Boost / SEPIC LED Driver

3 Description
The TPS92560 is a simple LED driver designed to drive high-power LEDs by drawing constant current from the power source. The device is ideal for MR16 and AR111 applications, which require good compatibility to DC and AC voltages and electronic transformers. The hysteretic control scheme does not need control loop compensation while providing the benefits of fast transient response and high power factor. The patent pending feedback control method allows the output power to be determined by the number of LED used without component change. The TPS92560 supports both boost and SEPIC configurations for the use of different LED modules.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS92560</td>
<td>HVSSOP  (10)</td>
<td>3.00 mm × 3.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2013) to Revision B

- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ................................................................. 1
# 5 Pin Configuration and Functions

## Pin Functions

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
<th>APPLICATION INFORMATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GATE</td>
<td>Gate driver output pin</td>
<td>Connect to the Gate terminal of the low-side N-channel Power FET</td>
</tr>
<tr>
<td>2</td>
<td>SRC</td>
<td>Gate driver return</td>
<td>Connect to the Source terminal of the low-side N-channel Power FET</td>
</tr>
<tr>
<td>3</td>
<td>VCC</td>
<td>VCC regulator output</td>
<td>Connect 0.47-μF decoupling capacitor from this pin to SRC pin</td>
</tr>
<tr>
<td>4</td>
<td>SEN</td>
<td>Current sense pin</td>
<td>Kelvin-sense current sensing input. Should connect to the current sensing resistor, RSEN.</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>Analog ground</td>
<td>Reference point for current sensing.</td>
</tr>
<tr>
<td>6</td>
<td>ADJ</td>
<td>LED current adjust pin</td>
<td>Connect to resistor divider from LED top voltage rail to set LED current</td>
</tr>
<tr>
<td>7</td>
<td>VP</td>
<td>Power supply of the IC</td>
<td>Connect it to the LED top voltage rail (for boost) or Connect it through a diode from LED top voltage rail (for SEPIC)</td>
</tr>
<tr>
<td>8</td>
<td>AC2</td>
<td>Power return terminal</td>
<td>Connect to AC or DC input terminal</td>
</tr>
<tr>
<td>9</td>
<td>PGND</td>
<td>Power ground</td>
<td>Connect to system ground plane</td>
</tr>
<tr>
<td>10</td>
<td>AC1</td>
<td>Power return terminal</td>
<td>Connect to AC or DC input terminal</td>
</tr>
<tr>
<td>PowerPAD™</td>
<td>—</td>
<td>Thermal DAP</td>
<td>Connect to system ground plane for heat dissipation</td>
</tr>
</tbody>
</table>

---

*PowerPAD™ — Thermal DAP*
6 Specifications

6.1 Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.\(^1\)

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRC, SEN, ADJ</td>
<td>–0.3</td>
<td>5 V</td>
</tr>
<tr>
<td>AC1, AC2</td>
<td>–1</td>
<td>45 V</td>
</tr>
<tr>
<td>VP</td>
<td>–0.3</td>
<td>45 V</td>
</tr>
<tr>
<td>VCC</td>
<td>–0.3</td>
<td>12 V</td>
</tr>
<tr>
<td>(T_J)</td>
<td>–40</td>
<td>125 °C</td>
</tr>
<tr>
<td>(T_{stg})</td>
<td>–65</td>
<td>150 °C</td>
</tr>
</tbody>
</table>

\(^1\) Absolute Maximum Ratings are limits which damage to the device may occur. Operating ratings are conditions under which operation of the device is intended to be functional. For specified specifications and test conditions, see the electrical characteristics.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^1)</td>
<td>±1500 V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(^2)</td>
<td>±1000 V</td>
</tr>
</tbody>
</table>

\(^1\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

\(^2\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VP</td>
<td>6.5</td>
<td>42</td>
<td>V</td>
</tr>
<tr>
<td>(T_J)</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^1)</th>
<th>TPS92560</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{JA}) Junction-to-ambient thermal resistance</td>
<td>55.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JC(top)}) Junction-to-case (top) thermal resistance</td>
<td>43.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JB}) Junction-to-board thermal resistance</td>
<td>32.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\Psi_{JT}) Junction-to-top characterization parameter</td>
<td>1.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\Psi_{JB}) Junction-to-board characterization parameter</td>
<td>31.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JC(bot)}) Junction-to-case (bottom) thermal resistance</td>
<td>5.0</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

\(^1\) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
6.5 Electrical Characteristics

Over recommended operating conditions with \(-40^\circ C \leq T_J \leq 125^\circ C\). Unless otherwise stated the following conditions apply: \(V_{VP} = 12V\).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_{IN})</td>
<td>(V_{IN}) Operating current</td>
<td>6.5 V &lt; (V_{VP}) &lt; 42 V</td>
<td>0.7</td>
<td>1.4</td>
<td>1.95 mA</td>
</tr>
<tr>
<td>(V_{CC})</td>
<td>(V_{CC}) Regulated voltage (^{(1)})</td>
<td>(I_{CC} \leq 10 mA, C_{VCC} = 0.47 \mu F)</td>
<td>7.82</td>
<td>8.45</td>
<td>9.08 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(12 V &lt; (V_{VP}) &lt; 42 V)</td>
<td>5.22</td>
<td>5.8</td>
<td>6.18 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(I_{CC} = 0 mA, C_{VCC} = 0.47 \mu F)</td>
<td>1.96</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>(I_{CC-LIM})</td>
<td>(V_{CC}) Current limit</td>
<td>(V_{CC} = 0 V) 6.5 V &lt; (V_{VP}) &lt; 42 V</td>
<td>21</td>
<td>30</td>
<td>39 mA</td>
</tr>
<tr>
<td>(V_{CC-UVLO-UTH})</td>
<td>(V_{CC}) UVLO upper threshold</td>
<td></td>
<td>5</td>
<td>5.38</td>
<td>5.76 V</td>
</tr>
<tr>
<td>(V_{CC-UVLO-LOTH})</td>
<td>(V_{CC}) UVLO lower threshold</td>
<td></td>
<td>4.63</td>
<td>4.98</td>
<td>5.33 V</td>
</tr>
<tr>
<td>(V_{CC-UVLO-HYS})</td>
<td>(V_{CC}) UVLO hysteresis</td>
<td></td>
<td>190</td>
<td>400</td>
<td>640 mV</td>
</tr>
</tbody>
</table>

**MOSFET GATE DRIVER**

| \(V_{GATE-HIGH}\) | Gate driver output high | w.r.t. SRC \(C_{GATE} = 1 nF\) across \(GATE\) | 7.61 | 8.1 | 8.5 V |
| \(V_{GATE-LOW}\) | Gate driver output low | w.r.t. SRC \(C_{GATE} = 1 nF\) across \(GATE\) | 10.0 | 180 | 290 mV |
| \(I_{RISE}\) | \(V_{GATE}\) Rise time | \(C_{GATE} = 1 nF\) across \(GATE\) and \(SRC\) | 22 | | ns |
| \(I_{FALL}\) | \(V_{GATE}\) Fall time | \(C_{GATE} = 1 nF\) across \(GATE\) and \(SRC\) | 14 | | ns |
| \(I_{RISE-PG-DELAY}\) | \(V_{GATE}\) Low-to-high propagation delay | \(C_{GATE} = 1 nF\) across \(GATE\) and \(SRC\) | 68 | | ns |
| \(I_{FALL-PG-DELAY}\) | \(V_{GATE}\) High-to-low propagation delay | \(C_{GATE} = 1 nF\) across \(GATE\) and \(SRC\) | 84 | | ns |

**CURRENT SOURCE AT ADJ PIN**

| \(I_{ADJ-STARTUP}\) | Output current of ADJ pin at start-up | \(V_{ADJ} = 0 V\) | 16 | 20 | 24 µA |
| \(I_{ADJ-ELEC-XFR}\) | Output current of ADJ pin for electronic transformers | \(V_{ADJ} = 0 V\) | 8 | 11.5 | 15 µA |
| \(I_{ADJ-MAG-XFR}\) | Output current of ADJ pin for inductive transformers | \(V_{ADJ} = 0 V\) | 7 | 9.5 | 12 µA |

**CURRENT SENSE COMPARATOR**

| \(V_{SEN-UPPER-TH}\) | \(V_{SEN}\) Upper threshold over \(V_{ADJ}\) | \(V_{SEN-ADJ} = 0.2 V\), \(V_{GATE}\) at falling edge | 8.9 | 14.9 | 20.9 mV |
| \(V_{SEN-LOWER-TH}\) | \(V_{SEN}\) Lower threshold over \(V_{ADJ}\) | \(V_{SEN-ADJ} = 0.2 V\), \(V_{GATE}\) at rising edge | -20.6 | -14.9 | -8.8 mV |
| \(V_{SEN-HYS}\) | \(V_{SEN}\) Hysteresis \((V_{SEN-UPPER-TH} - V_{SEN-LOWER-TH})\) | | 22.5 | 29.8 | 37.5 mV |
| \(V_{SEN-OFFSET}\) | \(V_{SEN}\) Offset w.r.t. \(V_{ADJ}\) \((V_{SEN-UPPER-TH} + V_{SEN-LOWER-TH})/2\) | | -3.5 | 0.02 | 3.5 mV |

**ACTIVE LOW-SIDE INPUT RECTIFIERS**

| \(R_{ACn-ON}\) | In resistance of AC1 and AC2 to GND | \(I_{ACn} = 200 mA\) | 300 | 570 | mΩ |
| \(V_{ACn-ON-TH}\) | Turn ON voltage threshold of AC1 and AC2 | \(V_{ACn}\) Decreasing, \(T_J = 25^\circ C\) | 36 | 52 | 67 mV |
| \(V_{ACn-OFF-TH}\) | Turn OFF voltage threshold of AC1 and AC2 | \(V_{ACn}\) Increasing, \(T_J = 25^\circ C\) | 77 | 90 | 104 mV |
| \(V_{ACn-TH-HYS}\) | Hysteresis voltage of AC1 and AC2 | \(V_{ACn-OFF-TH} - V_{ACn-ON-TH}\) | 39 | | mV |

\(^{(1)}\) \(V_{CC}\) provides self bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.
Electrical Characteristics (continued)

Over recommended operating conditions with -40°C ≤ TJ ≤ 125°C. Unless otherwise stated the following conditions apply: \( V_{VP} = 12\,\text{V} \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{AC-OFF} )</td>
<td>Off current of AC1 and AC2 ( V_{ACn} = 45,\text{V} )</td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>OUTPUT OVERVOLTAGE-PROTECTION (OVP)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{ADJ-OVP-UPTH} )</td>
<td>Output overvoltage-detection upper threshold ( V_{ADJ} ) increasing, ( V_{GATE} ) at falling edge</td>
<td>0.353</td>
<td>0.384</td>
<td>0.415</td>
<td>V</td>
</tr>
<tr>
<td>( V_{ADJ-OVP-LOTH} )</td>
<td>Output overvoltage-detection lower threshold ( V_{ADJ} ) decreasing, ( V_{GATE} ) at rising edge</td>
<td>0.312</td>
<td>0.339</td>
<td>0.366</td>
<td>V</td>
</tr>
<tr>
<td>( V_{ADJ-OVP-HYS} )</td>
<td>Output overvoltage-detection hysteresis ( V_{ADJ-OVP-UPTH} ) - ( V_{ADJ-OVP-LOTH} )</td>
<td>25</td>
<td>46</td>
<td>67</td>
<td>mV</td>
</tr>
<tr>
<td>THERMAL SHUTDOWN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_{SD} )</td>
<td>Thermal shutdown temperature ( T_{J} ) rising</td>
<td></td>
<td></td>
<td>165</td>
<td>°C</td>
</tr>
<tr>
<td>( T_{SD-HYS} )</td>
<td>Thermal shutdown temperature hysteresis ( T_{J} ) falling</td>
<td></td>
<td></td>
<td>30</td>
<td>°C</td>
</tr>
</tbody>
</table>
6.6 Typical Characteristics

All curves taken for the boost circuit are with 500-mA nominal input current and 6 serial LEDs. All curves taken for the SEPIC circuit are with 500-mA nominal input current and 3 serial LEDs.\( T_A = -40°C \) to 125°C, unless otherwise specified.

![Figure 1. Operation Current vs Temperature](image1)

![Figure 2. VCC vs Temperature (I_{\text{VCC}} = 0 \text{ mA})](image2)

![Figure 3. VCC UVLO Rising Threshold vs Temperature](image3)

![Figure 4. VCC UVLO Falling Threshold vs Temperature](image4)

![Figure 5. ACn Turn Off Threshold vs Temperature](image5)

![Figure 6. ACn Turn On Threshold vs Temperature](image6)
Typical Characteristics (continued)

All curves taken for the boost circuit are with 500-mA nominal input current and 6 serial LEDs. All curves taken for the SEPIC circuit are with 500-mA nominal input current and 3 serial LEDs, \( T_A = -40^\circ\text{C} \) to \( 125^\circ\text{C} \), unless otherwise specified.

Figure 7. Output Current (BOOST) vs Temperature

Figure 8. Output Current (SEPIC) vs Temperature

Figure 9. Output Power (BOOST) vs Temperature

Figure 10. Output Power (SEPIC) vs Temperature

Figure 11. Efficiency (BOOST) vs Temperature

Figure 12. Efficiency (SEPIC) vs Temperature
7 Detailed Description

7.1 Overview

The TPS92560 is a simple hysteretic control switching LED driver for MR16 or AR111 lighting applications. The device accepts DC voltage, AC voltage and electronic transformer as an input power source. The compact application circuit can fit into a generic case of MR16 lamps easily. The hysteretic inductor current control scheme requires no small signal control loop compensation and maintains constant average input current to secure high compatibility to different kinds of input power source. The TPS92560 can be configured to either a step-up or step-up/down LED driver for the use of different number of LEDs. The patent pending current control mechanism allows the use of a single set of component and PCB layout for serving different output power requirements by changing the number of LEDs. The integrating of the active low-side input rectifiers reduces the power loss for voltage rectification and saves two external diodes of a generic bridge rectifier to aim for a simple end application circuit. When the driver is used with an AC voltage source or electronic transformer, the current regulation level increases accordingly to maintain an output current close to the level that when it is used with a DC voltage source. With the output overvoltage protection and over-temperature shutdown functions, the TPS92560 is specifically suitable for the applications that are space limited and need wide acceptance to different power sources.

7.2 Functional Block Diagram
7.3 Feature Description

7.3.1 VCC Regulator
The VCC pin is the output of the internal linear regulator for providing an 8.45V typical supply voltage to the MOSFET driver and internal circuits. The output current of the VCC pin is limited to 30mA typical. A low ESR ceramic capacitor of 0.47-μF or higher capacitance should be connected across the VCC and SRC pins to supply transient current to the MOSFET driver.

7.3.2 MOSFET Driver
The GATE pin is the output of the gate driver which referenced to the SRC pin. The gate driver is powered directly by the VCC regulator which the maximum gate driving current is limited to 30 mA (typical). To prevent hitting the VCC current limit, TI suggests using a low gate charge MOSFET when high switching frequency is needed.

7.3.3 ADJ Pin
The voltage on the ADJ pin determines the reference voltage for the input current regulation. Typically, the ADJ pin voltage is divided from the output voltage of the circuit by a voltage divider, thus the average input current is adjusted with respect to the number of LEDs used. The voltage of the ADJ pin determines the input current following the expression:

\[
I_{\text{IN(nom)}} = \frac{V_{\text{VP}}}{R_{\text{SEN}}} \times \frac{R_{\text{ADJ}_2}}{R_{\text{ADJ}_1} + R_{\text{ADJ}_2}}
\]  

(1)

7.3.3.1 Output OVP
In the TPS92560, a function of output overvoltage protection (OVP) is provided to prevent damaging the circuit due to an open circuit of the LED. The OVP function is implemented to the ADJ pin. When the voltage of the ADJ pin exceeds 0.384V typical, the OVP circuit disables the MOSFET driver and turns off the main switch to allow the output capacitor to discharge. As the voltage of the ADJ pin decreases to below 0.353 V (typical), the MOSFET driver is enabled and the TPS92560 returns to normal operation. The triggering threshold of the output voltage is determined by the value of the resistors \( R_{\text{ADJ}_1} \) and \( R_{\text{ADJ}_2} \), which can be calculated using the following equation:

\[
V_{\text{VP}} \times \frac{R_{\text{ADJ}_2}}{R_{\text{ADJ}_1} + R_{\text{ADJ}_2}} \leq 0.384V
\]  

(2)

When defining the OVP threshold voltage, it is necessary to certain that the OVP threshold voltage does not exceed the rated voltage of the output rectifier and capacitor to avoid damaging of the circuit.

7.3.4 AC1 and AC2 Pins
The TPS92560 provides two internal active rectifiers for input voltage rectification. Each internal rectifier connects across the ACn pin to GND. These internal active rectifiers function as the low-side diode rectifiers of a generic bridge rectifier. The integrating of the active rectifiers helps in saving two external diodes of a bridge rectifier along with an improvement of power efficiency. For high power applications, for instance, 12-W output power, external diode rectifiers can be added across the ACn pin to GND to reduce heat dissipation on the TPS92560.
Feature Description (continued)

7.3.5 Detection of Power Source

Both the voltages of a generic AC source (50/60Hz) and an electronic transformer carry certain amount of dead time inherently, as shown in Figure 13. The existing of the dead time leads to a drop of the RMS input power to the driver circuit. In order to compensate the drop of the RMS input power, the ADJ pin sources current to the resistor, $R_{ADJ2}$, to increase the reference voltage for the current regulation loop and in turn increase the RMS input power accordingly when an AC voltage source or electronic transformer is detected. The output current of the ADJ pin for an AC input voltage and electronic transformer are 9.5 $\mu$A and 11.5 $\mu$A typical respectively. Practically the amount of the power for compensating the dead time of the input power source differs case to case depending on the characteristics of the power source, the value of the $R_{ADJ1}$ and $R_{ADJ2}$ might need a fine adjustment in accordance to the characteristics of the power source. The additional output power for compensating the dead time of the power sources ($\Delta P_{LED}$) are calculated using the following Equation 3 and Equation 4.

For 50/60Hz AC power source:

$$\Delta P_{LED-50/60 \text{ Hz}} = V_{IN} \times \frac{R_{ADJ2} \times 9.5 \ \mu A}{R_{SEN}} \times \eta$$  \hspace{1cm} (3)

For electronic transformer:

$$\Delta P_{LED-ELECT-XFR} = V_{IN} \times \frac{R_{ADJ2} \times 11.5 \ \mu A}{R_{SEN}} \times \eta$$  \hspace{1cm} (4)

7.3.6 Current Regulation

In the TPS92560, the input current regulation is attained by limiting the peak and valley of the inductor current. Practically the inductor current sensing is facilitated by detecting the voltage on the resistor, $R_{SEN}$. Because the current flows through the $R_{SEN}$ is a sum total of the currents of the main switch and LEDs, the voltage drop on the $R_{SEN}$ reflects the current of the inductor that is identical to the input current to the LED driver circuit. Figure 14 shows the waveform of the inductor current ripple with the peak and valley values controlled.
The voltage of the ADJ pin is determined by the forward voltage of the LED and divided from the $V_{VP}$ by a resistor divider. The equation for calculating the $V_{ADJ}$ as shown in Equation 5.

$$V_{ADJ} = V_{VP} \times \frac{R_{ADJ2}}{R_{ADJ1} + R_{ADJ2}} \quad (5)$$

In steady state, the voltage drop on the $R_{ADJ1}$ is identical to the forward voltage of the LED ($V_{LED}$) and the voltage across the $R_{ADJ2}$ is identical to the voltage across the $R_{SEN}$. The LED current, $I_{LED}$, is then calculated following the equations:

In steady state:

$$V_{LED} = V_{RADJ1} \quad (6)$$

$$V_{SEN} = V_{RADJ2} \quad (7)$$

$$I_{IN(nom)} = \frac{V_{SEN}}{R_{SEN}} \quad (8)$$

Since

$$P_{LED} = P_{IN} \times \eta \quad \text{where } \eta \text{ is the conversion efficiency} \quad (9)$$

Thus,

$$V_{LED} \times I_{LED} = V_{IN} \times I_{IN(nom)} \times \eta \quad (10)$$

Put the expressions (2) to (4) into (5):

$$I_{LED} = V_{IN} \times \frac{I_{RADJ2} \times R_{RADJ2}}{I_{RADJ1} \times R_{RADJ1} \times R_{SEN}} \times \eta \quad (11)$$

Due to the high input impedance of the ADJ pin, the current flows into the ADJ pin can be neglected and thus $I_{RADJ1}$ equals $I_{RADJ2}$. The LED current is then calculated following the expressions below:

$$I_{LED} = V_{IN} \times \frac{R_{RADJ2}}{R_{RADJ1} \times R_{SEN}} \times \eta \quad (12)$$

Practically, the conversion efficiency of a boost circuit is almost a constant around 85%. Being assumed that the efficiency term in the $I_{LED}$ expression is a constant, the LED current depends solely on the magnitude of the input voltage, $V_{IN}$. Without changing a component, the output power of the typical application circuits of the TPS92560 is adjustable by using different number of LEDs.

The output power is calculated by following the expression:

$$P_{out} = V_{OUT} \times I_{OUT}$$
Feature Description (continued)

\[
P_{\text{LED}} = V_{\text{LED}} \times V_{\text{IN}} \times \frac{R_{\text{ADJ2}}}{R_{\text{ADJ1}} \times R_{\text{SEN}}} \times \eta
\]  

(13)

7.3.7 Switching Frequency (Boost Configuration)

In the following sections, the equations and calculations are limited to the boost configuration only (that is, the LED forward voltage higher than the input voltage), unless otherwise specified. The application information for the SEPIC and other circuit topologies are available in separate application notes and reference designs. In the boost configuration, including the propagation delay of the control circuit, the ON and OFF times of the main switch are calculated using Equation 14 and Equation 15.

\[
t_{\text{ON}} = \left( \frac{V_{\text{SEN-UPPER-TH}} \times L}{R_{\text{SEN}} \times [V_{\text{IN}} - V_D - I_{\text{IN(nom)}} \times (R_L + R_{\text{DS(ON)}} + R_{\text{SEN}} + R_{\text{AC-FET}})]} + t_{\text{FALL-PG-DELAY}} \right) \times 2
\]

(14)

\[
t_{\text{OFF}} = \left( \frac{V_{\text{SEN-LOWER-TH}} \times L}{R_{\text{SEN}} \times [V_{\text{LED}} - V_{\text{IN}} - 2V_D - I_{\text{IN(nom)}} \times (R_L + R_{\text{SEN}} + R_{\text{AC-FET}})]} + t_{\text{RISE-PG-DELAY}} \right) \times 2
\]

(15)

In the previous equations, the \( V_D \) is the forward voltage of \( D_3 \), \( R_L \) is the DC resistance of \( L_1 \), \( R_{\text{DS(ON)}} \) is the ON resistance of \( Q_1 \) and \( R_{\text{AC-FET}} \) is the turn ON resistance of the internal active rectifier with respect to the typical application circuit diagram.

Practically the resistance of the \( R_L \), \( R_{\text{DS}(\text{ON})} \), and \( R_{\text{AC-FET}} \) is in the order of several tenth of m\( \Omega \), by assuming a 0.5-V diode forward voltage and the sum total of the \( R_L \), \( R_{\text{DS(ON)}} \), and \( R_{\text{AC-FET}} \) is close to 1 \( \Omega \), the on and off times of \( Q_1 \) can be approximated using the Equation 16 and Equation 17.

\[
t_{\text{ON}} = \left( \frac{14.9mV \times L}{R_{\text{SEN}} \times [V_{\text{IN}} - 0.5V - I_{\text{IN(nom)}} \times (1 + R_{\text{SEN}})]} + 84ns \right) \times 2
\]

(16)

\[
t_{\text{OFF}} = \left( \frac{14.9mV \times L}{R_{\text{SEN}} \times [V_{\text{LED}} - V_{\text{IN}} - 1V - I_{\text{IN(nom)}} \times (1 + R_{\text{SEN}})]} + 68ns \right) \times 2
\]

(17)

With the switching on and OFF times determined, the switching frequency can be calculated using Equation 18.

\[
f_{\text{SW}} = \frac{1}{t_{\text{ON}} + t_{\text{OFF}}}
\]

(18)

Because of the using of hysteretic control scheme, the switching frequency of the TPS92560 in steady state is dependent on the input voltage, output voltage and inductance of the inductor. Generally a 1-MHz to 1.5-MHz switching frequency is suggested for applications using an electronic transformer as the power source.

7.3.8 Inductor Selection (Boost Configuration)

Because of the using of the hysteretic control scheme, the switching frequency of the TPS92560 in a boost configuration can be adjusted in accordance to the value of the inductor being used. Derived from the equations (12) and (13), the value of the inductor can be determined base on the desired switching frequency by using Equation 19.

\[
L = \left( \frac{1}{f_{\text{SW}} - 304ns} \times R_{\text{SEN}} \right) \times \frac{1}{V_{\text{IN}} - 0.5V - I_{\text{IN(nom)}} \times (1 + R_{\text{SEN}}) + \frac{1}{V_{\text{LED}} - V_{\text{IN}} - 1V - I_{\text{IN(nom)}} \times (1 + R_{\text{SEN}})}} \times 29.8mV
\]

(19)

When selecting the inductor, it is essential to ensure the peak inductor current does not exceed the the factory suggested saturation current of the inductor. The values of the peak and valley inductor current are calculated using the following equations:

Peak inductor current:
Feature Description (continued)

\[
I_{L(\text{peak})} = \frac{[V_{\text{IN}} - V_D - I_{\text{IN(nom)}}] \times (R_L + R_{\text{DS(on)}} + R_{\text{SEN}} + R_{\text{AC-FET}}) \times t_{\text{ON}}}{2L} + I_{\text{IN(nom)}}
\]  

(20)

Valley inductor current:

\[
I_{L(\text{valley})} = I_{\text{IN(nom)}} - \frac{[V_{\text{LED}} - V_{\text{IN}} - 2V_D - I_{\text{IN(nom)}}] \times (R_L + R_{\text{SEN}} + R_{\text{AC-FET}}) \times t_{\text{OFF}}}{2L}
\]  

(21)

Assume the total resistance of the \(R_L\), \(R_{\text{DS(on)}}\) and \(R_{\text{AC-FET}}\) is 1 \(\Omega\) and the diode drop, \(V_D\) equal to 1 V, the peak and valley currents of the inductor can be approximated using Equation 22 and Equation 23.

\[
I_{L(\text{peak})} \approx \frac{[V_{\text{IN}} - 0.5V - I_{\text{IN(nom)}}] \times (1 + R_{\text{SEN}}) \times t_{\text{ON}}}{2L} + I_{\text{IN(nom)}}
\]  

(22)

\[
I_{L(\text{valley})} \approx I_{\text{IN(nom)}} - \frac{[V_{\text{LED}} - V_{\text{IN}} - 1V - I_{\text{IN(nom)}}] \times (1 + R_{\text{SEN}}) \times t_{\text{OFF}}}{2L}
\]  

(23)

In order not to saturate the inductor, an inductor with a factory guaranteed saturation current \(I_{\text{SAT}}\) 20% higher than the \(I_{L(\text{peak})}\) is suggested. Thus the \(I_{\text{SAT}}\) of the inductor should fulfill the following requirement:

\[
I_{\text{SAT}} \geq I_{L(\text{peak})} \times 1.2
\]  

(24)

7.3.9 Input Surge Voltage Protection

When use with an electronic transformer, the surge voltage across the input terminals can be sufficiently high to damage the TPS92560 depending on the characteristics of the electronic transformer. To against potential damaging due to the input surge voltage, a 36-V Zener diode can be connected across the input bridge rectifier as shown in Figure 15.

![Figure 15. Input Surge Voltage Protection Using an External Zener Diode](image)

7.4 Device Functional Modes

7.4.1 Thermal Shutdown

The TPS92560 includes a thermal shutdown circuitry that ceases the operation of the device to avoid permanent damage. The threshold for thermal shutdown is 165°C with a 30°C hysteresis typical. During thermal shutdown the VCC regulator is disabled and the MOSFET is turned off.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
In the applications that need true regulation of the LED current, the intrinsic input current control loop can be changed to monitor the LED current by adding an external LED current sensing circuit. Figure 18 and Figure 23 show the example circuits for true LED current regulation in boost and SEpic configurations respectively. In the circuits, the U3 (TL431) maintains a constant 2.5-V voltage drop on the resistors, R3 and R7. Because the U2 (TL431) maintains a constant voltage drop on the R3, the power dissipation on the output current sensing resistor, R7 can be minimized by setting a low voltage drop on the R7. Because the change of the current flowing through the R7 reflects in the change of the cathode current of U3 and eventually adjusts the ADJ pin voltage of the TPS92560, the LED current is regulated independent of the change of the input voltage.

Figure 16. Typical Application Circuit of the TPS92560 Using SEpic Configuration

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8.2 Typical Applications

8.2.1 Boost Application Design Example

Figure 17. Typical Application Circuit of the TPS92560 Using Boost Configuration

Figure 18. TPS92560 in Boost Configuration With Input Current Regulation
Typical Applications (continued)

8.2.1.1 Design Requirements

The specifications of the boost application circuit in Figure 18 are as listed as follows:

- Input Voltage: $V_{IN} = 12$ V
- LED Stack Voltage: $V_{LED} = 21$ V
- Input Current: $I_{IN(nom)} = 500$ mA
- Input Power = 6 W
- overvoltage Level: $V_{VP(OVP)} = 40$ V
- Switching Frequency: $f_{SW} = 1.4$ MHz

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Calculate Values for the ADJ Resistors

First choose a value for $R_{ADJ2}$ in the range of 1 kΩ and 10 kΩ. For this example $R_{ADJ2} = 1$ kΩ is chosen. Then calculate $R_{ADJ1}$ for the desired OVP level using Equation 25.

$$R_{ADJ1} = \frac{V_{VP(OVP)} - 0.384V}{0.384} \times \frac{R_{ADJ2}}{1kΩ} = 103kΩ$$

Choose the nearest standard resistor value of $R_{ADJ1} = 102$ kΩ.

8.2.1.2.2 Calculate the Sense Voltage and Sense Resistor Value

Given the calculated ADJ resistor values the sense voltage ($V_{SEN}$) can be calculated using Equation 26.

$$V_{SEN} = V_{ADJ} = R_{ADJ2} \times \frac{V_{LED}}{R_{ADJ1}} = 1kΩ \times \frac{21V}{102kΩ} = 206mV$$

Given a current sense voltage of 206 mV the current sense resistor value ($R_{SEN}$) can be calculated using Equation 27.

$$R_{SEN} = \frac{V_{SEN}}{I_{IN(nom)}} = \frac{206mV}{500mA} = 0.412Ω$$

The nearest standard value if 0.412Ω so choose $R_{SEN} = 0.412Ω$.

8.2.1.2.3 Calculate the Inductor Value

Given a desired switching frequency of 1.4 MHz the inductor value can be calculated using Equation 28.

$$L = \frac{1}{29.8mV} \times \left( \frac{1}{f_{SW} - 304ns} \times R_{SEN} \right)$$

$$L = \frac{1}{29.8mV} \times \left( \frac{1}{1.4MHz - 304ns} \times 0.412Ω \right) = 24.7µH$$

Choose the closest standard inductor value of $L = 22$ µH.
Typical Applications (continued)

8.2.1.3 Application Curve

![Graph showing efficiency vs. ambient temperature]

**Figure 19. Efficiency**

8.2.2 Boost Application Circuit With LED Current Regulation

![Circuit diagram with labels]

**Figure 20. Using the TPS92560 in Boost Configuration With LED Current Regulation**

8.2.2.1 Design Requirements

The specifications of the boost application circuit in Figure 18 are as follows:

- Objective input voltage: 3 VDC to 18 VDC / 12 VAC (50 Hz or 60 Hz) / Generic MR16 electronic transformer
- LED forward voltage: 20 VDC typical
- Output current: 300 mA typical (at 12-VDC input)
- Output power: 6 W typical (at 12-VDC input)
Typical Applications (continued)

8.2.2.2 Application Curves

All curves taken at $V_{IN} = 3$ V to 18 VDC in boost configuration, with 300mA nominal output current, 6 serial LEDs. $T_A = 25^\circ C$.

![Figure 21. LED Current vs Input Voltage](image1)

![Figure 22. Efficiency vs Input Voltage](image2)

8.2.3 SEPIC Application Circuit With LED Current Regulation

8.2.3.1 Design Requirements

The specifications of the SEPIC application circuit in Figure 18 are as listed as follows:

- Objective input voltage: 3 VDC to 18 VDC / 12 VAC (50 Hz or 60 Hz) / Generic MR16 electronic transformer
- LED forward voltage: 13 VDC typical
- Output current: 300 mA typical (at 12-VDC input)
- Output power: 4 W typical (at 12-VDC input)
Typical Applications (continued)

8.2.3.2 Application Curves

All curves taken at $V_{IN} = 3$ V to 18 VDC in SEPIC configuration, with 300-mA nominal output current, 4 serial LEDs. $T_A = 25^\circ$C.

Figure 24. LED Current vs Input Voltage

Figure 25. Efficiency vs Input Voltage
9 Power Supply Recommendations

Use any AC or DC power supply capable of the supply voltage required for the application and a power output capability greater than the total circuit input power.

10 Layout

10.1 Layout Guidelines

The VP input capacitor and ADJ resistors/capacitor should be placed as close to the IC as possible. The VCC capacitor should also be placed close to the device. Minimize the switching node area (connection between Q1, L1, and D3) and keep the discontinuous current switching path as short as possible. This includes the loop formed by Q1, COUT, and the diode D3 (designated by the red arrows). The ground connections for the TPS92560 and RSEN should be tied closely together with a solid ground plane. The node connecting the SEN pin, SRC pin, the source of Q1, CVCC, and COUT should be small with all components connected closely together.

10.2 Layout Example

Figure 26. TPS92560 Layout Example
11 Device and Documentation Support

11.1 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI’s views; see TI’s Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks
PowerPAD, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary
**SLYZ022 — TI Glossary.** This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
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<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
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<tbody>
<tr>
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<td>ACTIVE</td>
<td>HVSSOP</td>
<td>DGQ</td>
<td>10</td>
<td>1000</td>
<td>Green</td>
<td>SN</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>SN3B</td>
<td></td>
</tr>
<tr>
<td>TPS92560DGQR/NOPB</td>
<td>ACTIVE</td>
<td>HVSSOP</td>
<td>DGQ</td>
<td>10</td>
<td>3500</td>
<td>Green</td>
<td>SN</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>SN3B</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

```
<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0  (mm)</th>
<th>B0  (mm)</th>
<th>K0  (mm)</th>
<th>P1  (mm)</th>
<th>W  (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS92560DGQ/NOPB</td>
<td>HVSSOP</td>
<td>DGQ</td>
<td>10</td>
<td>1000</td>
<td>178.0</td>
<td>12.4</td>
<td>5.3</td>
<td>3.4</td>
<td>1.4</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>TPS92560DGQR/NOPB</td>
<td>HVSSOP</td>
<td>DGQ</td>
<td>10</td>
<td>3500</td>
<td>330.0</td>
<td>12.4</td>
<td>5.3</td>
<td>3.4</td>
<td>1.4</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
```

*All dimensions are nominal.*

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**TAPE DIMENSIONS**

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

---

**REEL DIMENSIONS**

- **Reel Diameter**
- **Reel Width (W1)**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- Sprocket Holes
- User Direction of Feed
- Pocket Quadrants

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### TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS92560DGQ/NOPB</td>
<td>HVSSOP</td>
<td>DGQ</td>
<td>10</td>
<td>1000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPS92560DGQR/NOPB</td>
<td>HVSSOP</td>
<td>DGQ</td>
<td>10</td>
<td>3500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

11. Board assembly site may have different recommendations for stencil design.
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