

Technical documentation





TPS92620-Q1

SLVSGW5A - NOVEMBER 2022 - REVISED JANUARY 2024

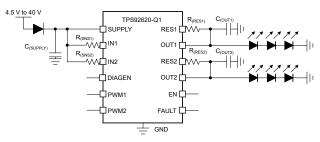
## TPS92620-Q1 Two-Channel, Automotive, High-Side LED Driver with Thermal Sharing

## 1 Features

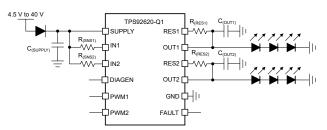
TEXAS

INSTRUMENTS

- AEC-Q100 qualified for automotive applications:
   Temperature grade 1: -40°C to 125°C, T<sub>A</sub>
- Wide input voltage range: 4.5V to 40V
- Thermal sharing by external shunt resistor
- · Low supply current in fault mode
- Ultra low shutdown current in sleep mode (only for HVSSOP package)
- Two high-precision current regulation:
  - Up to 250mA current output for each channel
  - ±5% accuracy over full temperature range
  - Independent current setting by resistor
  - Independent PWM pin for brightness control
- Low dropout voltage:
  - Maximum dropout: 600mV for 250mA
- Diagnostics and protection
  - LED open-circuit with auto-recovery
  - LED short-to-GND with auto-recovery
  - Diagnostic enable with adjustable threshold
  - Fault bus configurable as either one-fails–all-fail or only-failed-channel off (N-1)
  - Thermal shutdown
- Operation junction temperature range:-40°C to 150°C



## Typical Application Diagram (HVSSOP package)



## Typical Application Diagram (WSON package)

## 2 Applications

- Automotive exterior rear light: rear lamp, center high mounted stop lamp, side marker
- Automotive exterior small light: door handle, blind spot detection indicator, charging inlet
- Automotive interior light: overhead console, reading lamp
- General-purpose LED driver applications

## **3 Description**

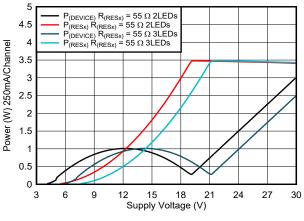
The TPS92620-Q1 two-channel LED driver includes an unique thermal management design to reduce temperature rising on the device. The TPS92620-Q1 is a linear driver directly powered by automotive batteries with large voltage variations to output full current loads up to 250mA per channel. External shunt resistors are leveraged to share output current and dissipate power out of the driver. The device full-diagnostic capabilities include LED open, LED short-to-GND circuit, and device overtemperature protection.

The one-fails–all-fail feature of TPS92620-Q1 can work together with other LED drivers, such as the TPS9261x-Q1, TPS9262x-Q1, TPS9263x-Q1, and TPS92830-Q1 devices, to address different requirements.

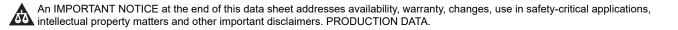
#### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)		
TPS92620-Q1	DGN (HVSSOP, 12)	3.00mm × 4.00mm		
TF 392020-QT	DRR (WSON, 12)	3.00mm × 3.00mm		

(1) For all available packages, see the orderable addendum at the end of the data sheet.



**Power Dissipation on Device** 





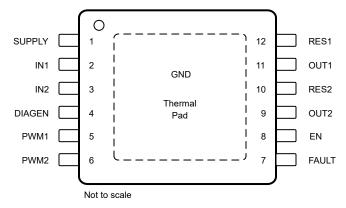
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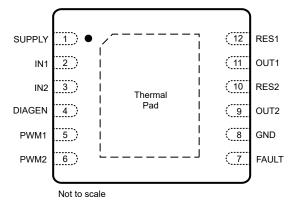
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## **4** Pin Configuration and Functions



### Figure 4-1. DGN Package 12-Pin HVSSOP With PowerPAD<sup>™</sup> Integrated Circuit Package (Top View)



## Figure 4-2. DRR Package 12-Pin WSON With PowerPAD<sup>™</sup> Integrated Circuit Package (Top View)

#### Table 4-1. HVSSOP Pin Functions

P	IN	- I/O	DESCRIPTION
NAME	NO.	1/0	DESCRIPTION
SUPPLY	1	I	Device power supply
IN1	2	I	Current input for channel 1
IN2	3	I	Current input for channel 2
DIAGEN	4	I	Enable pin for LED open-circuit detection to avoid false open diagnostics during low-dropout operation.
PWM1	5	I	PWM input for OUT1 and RES1 current output ON and OFF control
PWM2	6	I	PWM input for OUT2 and RES2 current output ON and OFF control
FAULT	7	I/O	Fault output, support one-fails–all-fail fault bus
EN	8	I	Device enable pin
OUT2	9	0	Current output for channel 2
RES2	10	0	Current output for channel 2 with external thermal resistor
OUT1	11	0	Current output for channel 1
RES1	12	0	Current output for channel 1 with external thermal resistor
DAP	13	-	GND/ Thermal Pad



#### Table 4-2. WSON Pin Functions

P	N	1/0	DESCRIPTION
NAME	NO.		DESCRIPTION
SUPPLY	1	I	Device power supply
IN1	2	I	Current input for channel 1
IN2	3	I	Current input for channel 2
DIAGEN	4	I	Enable pin for LED open-circuit detection to avoid false open diagnostics during low-dropout operation.
PWM1	5	I	PWM input for OUT1 and RES1 current output ON and OFF control
PWM2	6	I	PWM input for OUT2 and RES2 current output ON and OFF control
FAULT	7	I/O	Fault output, support one-fails–all-fail fault bus
GND	8	-	Ground
OUT2	9	0	Current output for channel 2
RES2	10	0	Current output for channel 2 with external thermal resistor
OUT1	11	0	Current output for channel 1
RES1	12	0	Current output for channel 1 with external thermal resistor



## **5** Specifications

#### **5.1 Absolute Maximum Ratings**

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply	SUPPLY	-0.3	45	V
High-voltage input	DIAGEN, IN1, IN2, PWM1, PWM2, EN	-0.3	V <sub>(SUPPLY)</sub> + 0.3	V
High-voltage output	OUT1, OUT2, RES1, RES2	-0.3	V <sub>(SUPPLY)</sub> + 0.3	V
Fault bus	FAULT	-0.3	V <sub>(SUPPLY)</sub> + 0.3	V
TJ	Operating junction temperature	-40	150	°C
T <sub>stg</sub>	Storage temperature	-40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

#### 5.2 ESD Ratings

				VALUE	UNIT
		Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD Classification Level 1C		±2000	
V <sub>(ESD)</sub> Electrostatic discharge	Charged-device model (CDM), per AEC	All pins	±500	V	
			Corner pins (SUPPLY, RES1, FAULT, PWM2)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### **5.3 Recommended Operating Conditions**

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM MAX	UNIT
SUPPLY	Device supply voltage	4.5	40	V
IN1, IN2	Sense voltage	V <sub>(SUPPL</sub>	V	
EN	Device EN pin	0 V <sub>(SUPPLY)</sub>		V
PWM1, PWM2	PWM inputs	0	V <sub>(SUPPLY)</sub>	V
DIAGEN	Diagnostics enable pin	0	V <sub>(SUPPLY)</sub>	V
OUT1, OUT2, RES1, RES2	Driver output	0	V <sub>(SUPPLY)</sub>	V
FAULT	Fault bus	0	V <sub>(SUPPLY)</sub>	V
Operating ambient temper	ature, T <sub>A</sub>	-40 125		°C

#### **5.4 Thermal Information**

		TPS92		
	THERMAL METRIC <sup>(1)</sup>	DRR (WSON)	DGN (HVSSOP)	UNIT
		12 PINS	12 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	51.2	39.7	°C/W
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	50.7	60.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	25.2	15.5	°C/W
ΨJT	Junction-to-top characterization parameter	1.3	2.6	°C/W
Ψјв	Junction-to-board characterization parameter	25.2	15.5	°C/W
R <sub>0JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	9.4	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

### **5.5 Electrical Characteristics**

 $V_{(SUPPLY)}$  = 5V to 40V,  $V_{(EN)}$  = 3.3V,  $T_J$  = -40°C to +150°C unless otherwise noted

BiAS         V[POR_ning)         Supply voltage POR failing threshold         3.6         4.0           V[POR_ning)         Supply voltage POR failing threshold         3.0         3.4         13.5         18.0           (sp)         Device shuddwon current         V(EN) = 0V         13.5         18.0         13.5         18.0           (gaussent)         Device supply current in fault mode         PWM = HIGH, FAULT externally pulled LOW         0.21         0.32         0.45           LOGIC INPUTS (DLGEN, PWM, EN)          1.04 togic-ingh voltage, EN         2.0         0.7           V[E(RN)         Input logic-ingh voltage, EN         2.0         0.7         1.14         1.2         1.26           V[E(RN)         Input logic-ingh voltage, EN         V[E]         1.04         1.1         1.155         3.0         4.5           V[E(RN)         Input logic-ingh voltage, DIAGEN         1.045         1.1         1.155         1.1         1.155           V[E(RNM)         Input logic-ingh voltage, PVM         1.014         1.2         1.26         2.00         2.00         2.00         2.00         2.00         2.00         2.00         2.00         2.00         2.00         2.00         2.00         2.00         2.00         2.00 <th>V           0         uA           6         mA           5         mA           7         V           V         V</th>	V           0         uA           6         mA           5         mA           7         V           V         V
Construction         Surply voltage POR falling threshold         3.0         3.4           Itsp:         Device shutdown current         V <sub>[EN]</sub> = 0V         13.5         18.0           Itsp:         Device shutdown current         PWM = HIGH         1.2         1.6           Itsp:         Device standby ground current         PWM = HIGH         0.21         0.32         0.45           LGGIC INPUTS (DIAGEN, PWM, EN)         Input logic-low voltage, EN         2.0         0.7           Vit_(EN)         Input logic-low voltage, EN         2.0         0.7           Vit_(EN)         Input logic-low voltage, DIAGEN         1.045         1.1         1.155           Vit_(IDAGEN)         Input logic-low voltage, DIAGEN         1.045         1.1         1.155           Vit_(IDAGEN)         Input logic-low voltage, PVM         1.045         1.1         1.155           Vit_(IPVMA)         Input logic-low voltage, PVM         1.045         1.1         1.155           Vit_(IPVMA)         Input logic-low voltage, PVM         1.045         1.1         1.155           Vit_(IPVMA)         Input logic-high voltage, PVM         1.045         1.14         1.2         1.26           CONSTANT-CURRENT DRIVER         Voltage dropout prown sing threach channel         100%	V           0         uA           6         mA           5         mA           7         V           V         V
$ \begin{array}{ c c c c c c } \hline levice shutdown current & V_{(EN)} = 0V & 13.5 & 18.0 \\ l_{(Quiescent)} & Device shutdown current & PWM = HIGH & 1.2 & 1.6 \\ l_{(Quiescent)} & Device standby ground current & PWM = HIGH & 1.2 & 1.6 \\ l_{(FALLT)} & Device supply current in fault mode & PWM = HIGH, FAULT externally pulled LOW & 0.21 & 0.32 & 0.45 \\ \hline LOGIC INPUTS (DIAGEN, PWM, EN) & Vullescent & V_{(EN)} & Vullescent & 0.77 \\ Vulle(N) & Input logic-low voltage, EN & 2.0 \\ \hline Vulle(N) & Input logic-low voltage, DIAGEN & 1.0 & 1.5 & 3.0 & 4.5 \\ \hline Vulle(N) & Input logic-low voltage, DIAGEN & 1.0 & 1.5 & 3.0 & 4.5 \\ \hline Vulle(N) & Input logic-low voltage, DIAGEN & 1.0 & 1.14 & 1.2 & 1.26 \\ \hline Vulle(N) & Input logic-low voltage, DIAGEN & 1.0 & 1.14 & 1.2 & 1.26 \\ \hline Vulle(NAGEN) & Input logic-low voltage, PWM & 1.0 & 1.14 & 1.2 & 1.26 \\ \hline Vulle(NAGEN) & Input logic-low voltage, PWM & 1.0 & 1.14 & 1.2 & 1.26 \\ \hline Vulle(NAGEN) & Input logic-low voltage, PWM & 1.0 & 1.14 & 1.2 & 1.26 \\ \hline CONSTANT-CURRENT DRIVER & 1.0 & 1.0 & 5 & 2.50 \\ \hline V(CS, REG) & Sense-resistor regulation voltage & T_A = -40^{\circ}C to +125^{\circ}C & 144 & 150 & 156 \\ ALL \DeltaV(CS, acd) & Device output-current for each channel & 100% duty cycle & 5 & 2.50 \\ \hline V(CS, REG) & Sense-resistor range & 0.576 & 31.2 \\ \hline V(DROPOUT) & Vultage dropout from INx to OUTx, RESx open & current setting of 150mA & 1.80 & 350 \\ \hline V(DROPOUT) & Vultage dropout from INx to RESx, OUTx open & current setting of 250mA & 600 & 1200 \\ \hline V(RESA) & Ratio of RESx current to total current & l_{RESA}/I(CUTx, Tar), V(INS) - V(RESx) > 1V, gs \\ \hline DACONSTICS & V(DROPOUT) & 180 & 300 & 420 \\ \hline V(OPEN, In, failing) & LED open rising threshold, V(N) - V(OUT) & V(RESx) > 1V, gs \\ \hline V(RES, In, failing) & Channel output short-to-ground failing threshold & 1.14 & 1.2 & 1.28 \\ \hline V(CS, In, failing) & Channel output short-to-ground failing threshold & 0.855 & 0.9 & 0.94 \\ \hline V(RS, In, failing) & Channel output short-to-ground failing threshold & 0.855 & 0.9 & 0.94 \\ \hline V(SG, In, failing) & Channel output short-to-ground fail$	) uA 6 mA 5 mA 7 V V
Iso         Device shutdown current $V_{(EN)} = 0V$ 13.5         18.0           Iquiescont)         Device standby ground current         PWM = HIGH, FAULT externally pulled LOW         0.21         0.32         0.45           Iquiescont)         Device supply current in fault mode         PWM = HIGH, FAULT externally pulled LOW         0.21         0.32         0.45           LGGIC INPUTS (DIAGEN, PWM, EN)         Input logic-high voltage, EN         2.0         0.7           VI <sub>REN</sub> )         Input logic-high voltage, EN         2.0         0.7           VI <sub>REN</sub> )         Input logic-high voltage, DIAGEN         2.0         0.7           VI <sub>REN</sub> , Duildown current         V <sub>(EN)</sub> = 12V         1.5         3.0         4.5           VI <sub>RENON</sub> Input logic-high voltage, DIAGEN         1.045         1.1         1.155           VI <sub>RENON</sub> Input logic-high voltage, PWM         1.045         1.1         1.155           VI <sub>RENON</sub> Input logic-high voltage, PWM         1.046         1.1         1.155           VI <sub>RENON</sub> Input logic-high voltage, PWM         1.046         1.1         1.155           VI <sub>RENON</sub> Input logic-high voltage, PWM         1.046         1.1         1.155           VI <sub>RENON</sub> Reserversit	6 mA 5 mA 7 V V
	5 mA 7 V V
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LOGIC INPUTS (DIAGEN, PWM, EN)         Input logic-low voltage, EN         0.7 $V_{It(EN)}$ Input logic-low voltage, EN         2.0 $V_{It(REN)}$ Input logic-low voltage, EN         2.0 $V_{It(REN)}$ Input logic-low voltage, DIAGEN         1.045 $V_{It(DIAGEN)}$ Input logic-low voltage, DIAGEN         1.045 $V_{It(DIAGEN)}$ Input logic-low voltage, DIAGEN         1.14         1.2 $V_{It(PWM)}$ Input logic-low voltage, PWM         1.045         1.1         1.155 $V_{It(PWM)}$ Input logic-low voltage, PWM         1.045         1.1         1.155 $V_{It(PWM)}$ Input logic-low voltage, PWM         1.14         1.2         1.26 $V_{ICS, REG)$ Sense-resistor range $V_{ICS, REG)$ Channel ontent mismatch	V
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$\begin{split} & \begin{array}{ll} \begin{tabular}{ lem_pulldown }{lem_pulldown } & EN pull down current & V_{(EN)} = 12V & 1.5 & 3.0 & 4.5 \\ \hline V_{IL(DIAGEN)} & Input logic-low voltage, DIAGEN & 1.045 & 1.1 & 1.155 \\ \hline V_{IL(DIAGEN)} & Input logic-high voltage, DIAGEN & 1.045 & 1.1 & 1.155 \\ \hline V_{IL(PVM)} & Input logic-high voltage, PWM & 1.045 & 1.1 & 1.155 \\ \hline V_{IL(PVM)} & Input logic-high voltage, PWM & 1.045 & 1.1 & 1.155 \\ \hline V_{IL(PVM)} & Input logic-high voltage, PWM & 1.045 & 1.1 & 1.155 \\ \hline V_{IL(PVM)} & Input logic-high voltage, PWM & 1.045 & 1.1 & 1.155 \\ \hline V_{IL(PVM)} & Input logic-high voltage, PWM & 1.045 & 1.1 & 1.155 \\ \hline V_{IL(PVM)} & Input logic-high voltage, PWM & 1.045 & 1.1 & 1.155 \\ \hline V_{IL(PVM)} & Input logic-high voltage, PWM & 1.045 & 1.1 & 1.2 & 1.26 \\ \hline CONSTANT-CURRENT DRIVER & & & & & & & & & & & & & & & & & & &$	i uA
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CONSTANT-CURRENT DRIVER           Il_(OUTx_Tot)         Device output-current for each channel         100% duty cycle         5         250           V(cS_REG)         Sense-resistor regulation voltage $T_A = -40^{\circ}$ C to $+125^{\circ}$ C         144         150         156           ALL $\Delta V_{(CS_2c2)}$ Channel to channel mismatch $\Delta V_{(CS_2c2)} = 1 - V_{(CS_REG)} / V_{avg(CS_REG)}$ $-3$ $+3$ ALL $\Delta V_{(CS_d2d)}$ Device to device mismatch $\Delta V_{(CS_d2d)} = 1 - V_{avg(CS_REG)} / V_{nom(CS_REG)}$ $-4$ $+4$ R(CS_REG)         Sense-resistor range $0.576$ $31.2$ $0.576$ $31.2$ V(DROPOUT)         Voltage dropout from INx to OUTx, RESx open         current setting of 150mA $180$ $350$ $700$ V(DROPOUT)         Ratio of RESx current to total current $I_{RESx}/I_{(OUTx_Tot)}, V_{(INX)} - V_{(RESx)} > 1V,$ $95$ $95$ DIAGNOSTICS           V(open_th_rising)         LED open rising threshold, $V_{(IN)} - V_{(OUT)}$ $180$ $300$ $420$ $V(sG_th_rising)$ LED open falling threshold, $V_{(IN)} - V_{(OUT)}$ $450$ $450$ $450$ $450$ $450$ $450$ $450$	
$      I_{(OUTX\_Tot)}  Device output-current for each channel 100% duty cycle 5 2500 \\      V_{(CS\_REG)}  Sense-resistor regulation voltage T_A = -40°C to +125°C 1144 150 1566 \\      ALL \Delta V_{(CS\_c2c)}  Channel to channel mismatch \Delta V_{(CS\_c2c)} = 1 - V_{(CS\_REG)} / V_{avg(CS\_REG)} -3 +33 \\      ALL \Delta V_{(CS\_d2d)}  Device to device mismatch \Delta V_{(CS\_d2d)} = 1 - V_{avg(CS\_REG)} / V_{nom(CS\_REG)} -4 +44 \\      R_{(CS\_REG)}  Sense-resistor range 0.576 31.2 \\      V_{(DROPOUT)}  Voltage dropout from INx to OUTx, RESx open Voltage dropout from INx to RESx, OUTx open Voltage dropout from INx to RESx, OUTx open Voltage 150mA 350 700 \\      current setting of 150mA 350 700 \\      current setting of 250mA 600 1200 \\      durrent setting of 250mA 700 \\    $	v
$ \begin{array}{c} (USC_{AC}(N)) & V(CS_{AC}(N)) & V(CS_{$	) mA
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$V_{(SG\_th\_rising)}$ Channel output short-to-ground rising threshold1.141.21.26 $V_{(SG\_th\_falling)}$ Channel output short-to-ground falling threshold0.8550.90.945.Channel output $V_{(OIIT)}$ short-to-ground retry0.040.040.055	) mV
V(SG_th_failing)     Channel output short-to-ground failing threshold     0.855     0.9     0.945       .     Channel output V(outp short-to-ground retry     0.000     0.000     0.000	mV
Channel output V <sub>(OUT)</sub> short-to-ground retry	6 V
Channel output V <sub>(OUT)</sub> short-to-ground retry	5 V
I <sub>(Retry_OUTx)</sub> One of the second retry 0.64 1.14 1.528	3 mA
I <sub>(Retry_RESx)</sub> Channel output V <sub>(RES)</sub> short-to-ground retry 0.64 1.14 1.528	3 mA
FAULT	
V <sub>IL(FAULT)</sub> Logic input low threshold 0.7	7 V
V <sub>IH(FAULT)</sub> Logic input high threshold 2	V
t <sub>(FAULT rising)</sub> Fault detection rising edge deglitch time 10	μs
t <sub>(FAULT_falling)</sub> Fault detection falling edge deglitch time 20	μs
Iperation     FAULT internal pulldown current     V(FAULT) = 0.4V     2     3     4	-
I(FAULT pullup) FAULT internal pullup current 6 10 14	_
(FAULT_pullip)         FAULT leakage current         V(FAULT) = 40V         0.01         2	- ·
	P'' \
$V_{(SUPPLY)} = 12V, V_{(OUT)} = 6V, V_{(CS_{REG})} = 3.7$	μs
$t_{(PWM\_delay\_rising)} = \frac{PWM rising edge delay to 10\% of output current, t_1 as shown in Figure 6-1}{V_{(SUPPLY)} = 12V, V_{(OUT)} = 6V, V_{(CS_REG)} = 2.2$	
$150 \text{mV}, \text{R}_{(\text{SNSx})} = 30\Omega \text{ and } \text{R}_{(\text{RESx})} = 56\Omega$	



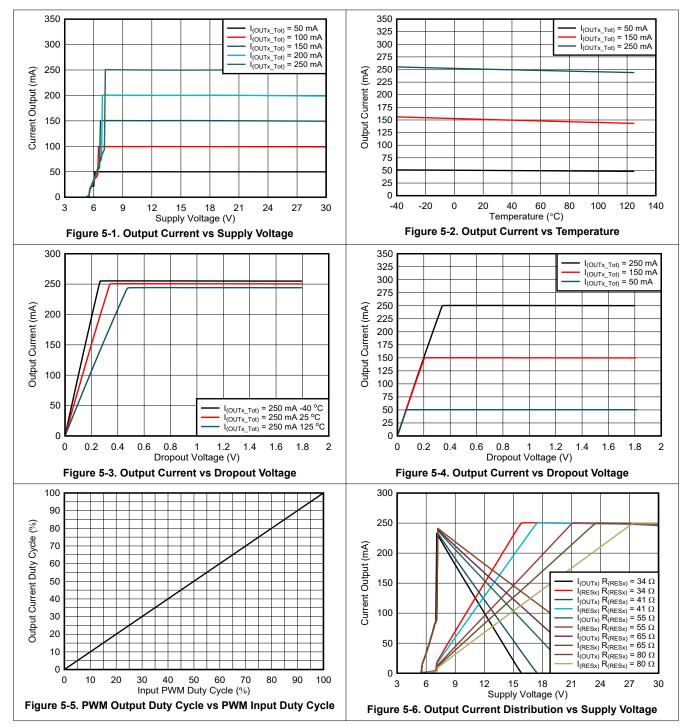
## 5.5 Electrical Characteristics (continued)

 $V_{(SUPPLY)}$  = 5V to 40V,  $V_{(EN)}$  = 3.3V,  $T_J$  = -40°C to +150°C unless otherwise noted

	PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT
t	PWM falling edge delay to 90% of output	$      V_{(SUPPLY)} = 12V, V_{(OUT)} = 6V, V_{(CS\_REG)} = 150mV, R_{(SNSx)} = 0.6\Omega, \text{ and } R_{(RESx)} = 39\Omega $		4.0		μs
t(PWM_delay_falling)	current, t <sub>2</sub> as shown in Figure 6-1	$V_{(SUPPLY)}$ = 12V, $V_{(OUT)}$ = 6V, $V_{(CS\_REG)}$ = 150mV, $R_{(SNSx)}$ = 30 $\Omega$ and $R_{(RESx)}$ = 56 $\Omega$		3.6		μs
t	Output current rising from 10% to 90%, $t_3$ as	$V_{(SUPPLY)}$ = 12V, $V_{(OUT)}$ = 6V, $V_{(CS\_REG)}$ = 150mV, $R_{(SNSx)}$ = 0.6 $\Omega$ , and $R_{(RESx)}$ = 39 $\Omega$		1.8		μs
t(Current_rising)	shown in Figure 6-1	$V_{(SUPPLY)}$ = 12V, $V_{(OUT)}$ = 6V, $V_{(CS\_REG)}$ = 150mV, $R_{(SNSx)}$ = 30 $\Omega$ and $R_{(RESx)}$ = 56 $\Omega$		1.8		μs
t	Output current falling from 90% to 10%, t4 as	$V_{(SUPPLY)}$ = 12V, $V_{(OUT)}$ = 6V, $V_{(CS\_REG)}$ = 150mV, $R_{(SNSx)}$ = 0.6 $\Omega$ , and $R_{(RESx)}$ = 39 $\Omega$		5.7		μs
t(Current_falling)	shown in Figure 6-1	$V_{(SUPPLY)}$ = 12V, $V_{(OUT)}$ = 6V, $V_{(CS\_REG)}$ = 150mV, $R_{(SNSx)}$ = 30 $\Omega$ and $R_{(RESx)}$ = 56 $\Omega$		0.3		μs
	SUPPLY rising edge to 10% output current, t <sub>5</sub> as	$V_{(SUPPLY)}$ = 12V, $V_{(OUT)}$ = 6V, $V_{(CS\_REG)}$ = 150mV, $R_{(SNSx)}$ = 0.6 $\Omega$ , and $R_{(RESx)}$ = 39 $\Omega$		96		μs
<sup>t</sup> (STARTUP)	shown in Figure 6-1	$V_{(SUPPLY)}$ = 12V, $V_{(OUT)}$ = 6V, $V_{(CS\_REG)}$ = 150mV, $R_{(SNSx)}$ = 30 $\Omega$ and $R_{(RESx)}$ = 56 $\Omega$		85		μs
t <sub>(OPEN_deg)</sub>	LED-open fault detection deglitch time, t <sub>6</sub> as shown in Figure 6-4			125		μs
t <sub>(SG_deg)</sub>	Output short-to-ground detection deglitch time, $t_7$ as shown in Figure 6-3			125		μs
t <sub>(Recover_deg)</sub>	Open and Short fault recovery deglitch time, $t_8$ as shown in Figure 6-3 and Figure 6-4			125		μs
t <sub>(FAULT_deg)</sub>	Fault pin deglitch time			20		μs
t <sub>(FAULT_recovery)</sub>	Fault recovery delay time, $t_{9}$ as shown in Figure 6-3 and Figure 6-4			50		μs
t <sub>(TSD_deg)</sub>	Thermal over temperature deglitch time			50		μs
THERMAL PROT	ECTION	•				
T <sub>(TSD)</sub>	Thermal shutdown junction temperature threshold		157	172	187	°C
T <sub>(TSD_HYS)</sub>	Thermal shutdown junction temperature hysteresis			15		°C



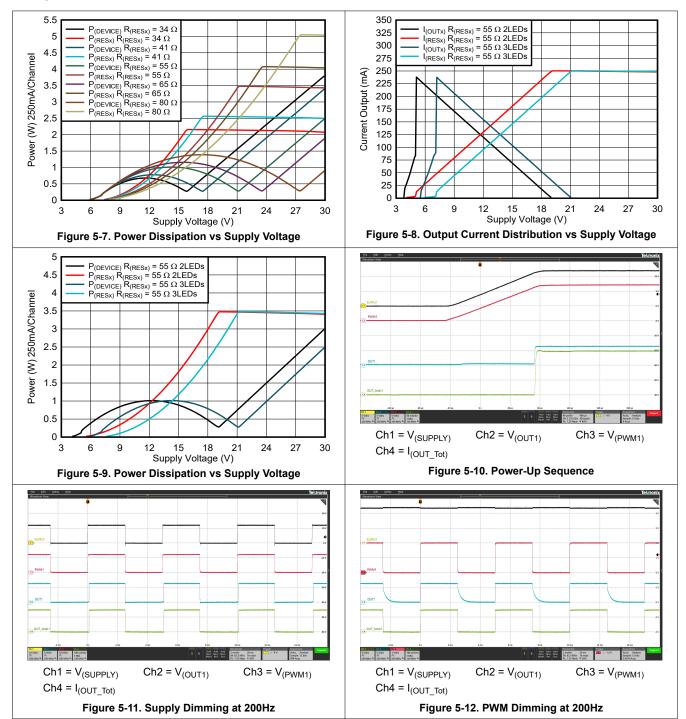
## **5.6 Typical Characteristics**



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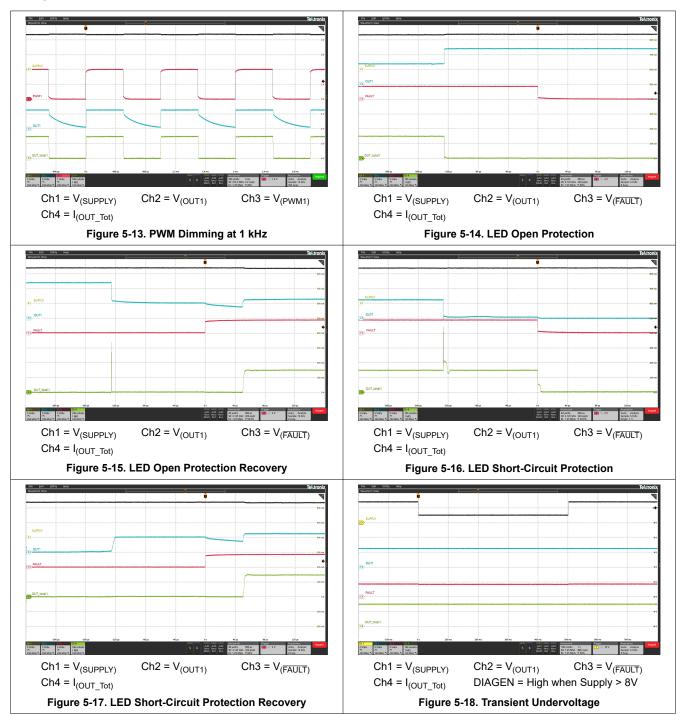


## 5.6 Typical Characteristics (continued)



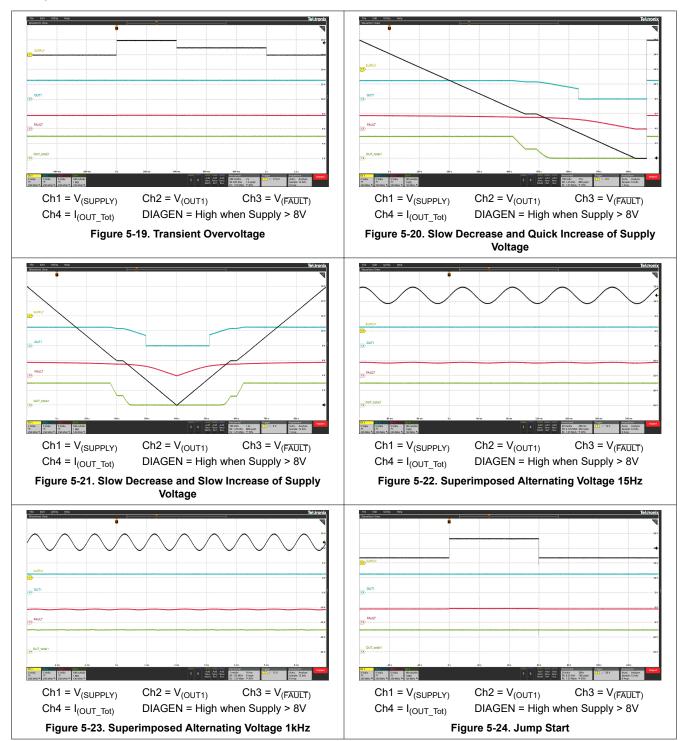


## 5.6 Typical Characteristics (continued)





### 5.6 Typical Characteristics (continued)



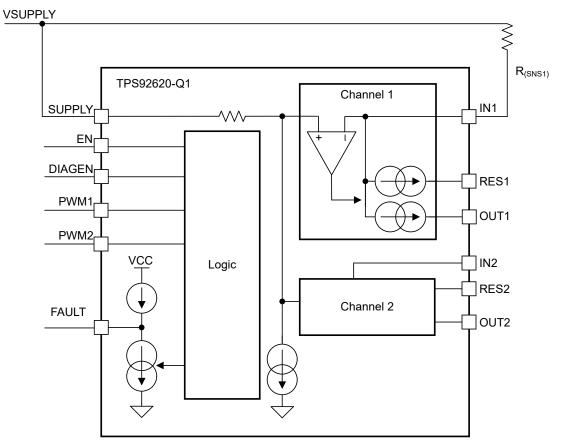


## 6 Detailed Description

## 6.1 Overview

The TPS92620-Q1 is a two-channel, high-side linear LED driver supporting external thermal sharing resistor to achieve the controllable junction temperature rising. The device can be directly powered by automotive battery and output full load up to 500mA current to LED with limited power dissipation on the device. The current output at each channel can be independently set by external R<sub>(SNSx)</sub> resistors. Current flows from the supply through the R<sub>(SNSx)</sub> resistor into the integrated current regulation circuit and to the LEDs through OUTx pin and RESx pin. TPS92620-Q1 device supports both supply control and EN/PWM control to turn LED ON and OFF. The LED brightness is also adjustable by voltage duty cycle applied on either SUPPLY or EN/PWM pins with frequency above 100Hz. The TPS92620-Q1 provides full diagnostics to keep the system operating reliably including LED open and short-circuit detection, supply POR and thermal shutdown protection. The TPS92620-Q1 can be used with other TPS9261x-Q1, TPS9262x-Q1, TPS9263x-Q1 and TPS92830-Q1 family devices together to achieve one-fails-all-fail protection by tying all FAULT pins together as a fault bus.

## 6.2 Functional Block Diagram



### 6.3 Feature Description

## 6.3.1 Power Supply (SUPPLY)

### 6.3.1.1 Power-On Reset (POR)

The TPS92620-Q1 device has an internal power-on-reset (POR) function. When power is applied to the SUPPLY pin, the internal POR circuit holds the device in reset state until  $V_{(SUPPLY)}$  is above  $V_{(POR rising)}$ .

#### 6.3.1.2 Suppply Current in Fault Mode

The TPS92620-Q1 device consumes minimal quiescent current,  $I_{(FAULT)}$ , into SUPPLY when the FAULT pin is externally pulled LOW. At the same time, the device shuts down all four output drivers.

If device detects an internal fault, it pulls down the FAULT pin by an internal typical 3-mA constant current as a fault indication to the fault bus.

#### 6.3.2 Enable and Shutdow(EN)

The TPS92620-Q1 device with HVSSOP package has an enable input. When EN is low, the device is in sleep mode with ultra low shutdown current  $I_{(SD)}$ . This low current helps to save system-level current consumption in applications where battery voltage directly connects to the device without high-side switches.

The TPS92620-Q1 device with WSON package has no EN pin. The device starts to operate as long as the SUPPLY voltage is higher than  $V_{(POR\_rising)}$ . The TPS92620-Q1 shuts down when SUPPLY voltage is lower than  $V_{(POR\_falling)}$ .

#### 6.3.3 Constant-Current Output and Setting (INx)

The TPS92620-Q1 device is a high-side current driver for driving LEDs. The device controls each output current through regulating the voltage drop on an external high-side current-sense resistor,  $R_{(SNSx)}$  independently for each channel. An integrated error amplifier drives an internal power transistor to maintain the voltage drop on the current-sense resistor  $R_{(SNSx)}$  to  $V_{(CS\_REG)}$  and therefore regulates the current output to target value. When the output current is in regulation, use Equation 1 to calculate the current value for each channel.

$$I_{(OUTx\_Tot)} = \frac{V_{(CS\_REG)}}{R_{(SNSx)}}$$

where

- V<sub>(CS REG)</sub> = 150mV
- x = 1, or 2 for output channel 1 or 2

When the supply voltage drops below total LED string forward voltage plus required headroom voltage, the sum of  $V_{(DROPOUT)}$  and  $V_{(CS\_REG)}$ , the TPS92620-Q1 is not able to deliver enough current output as set by the value of  $R_{(SNSx)}$ , and the voltage across the current-sense resistor  $R_{(SNSx)}$  is less than  $V_{(CS\_REG)}$ .

#### 6.3.4 Thermal Sharing Resistor (OUTx and RESx)

The TPS92620-Q1 device provides two current output paths for each channel. Current flows from the supply through the  $R_{(SNSx)}$  resistor into the integrated current regulation circuit and to the LEDs through OUTx pin and RESx pin. The current output on both OUTx pin and RESx pin is independently regulated to achieve total required current output. The summed current of OUTx and RESx is equal to the current through the  $R_{(SNSx)}$  resistor in the channel. The OUTx connects to anode of LEDs load in serial directly, however RESx connects to the LEDs through an external resistor to share part of the power dissipation and reduce the thermal accumulation in TPS92620-Q1.

The integrated independent current regulation in TPS92620-Q1 dynamically adjusts the output current on both OUTx and RESx output to maintain the stable summed current for LED. The TPS92620-Q1 always regulates the current output to the RESx pin as much as possible until the RESx current path is saturated, and the rest of required current is regulated out of the OUTx. As a result, the most of the current to LED outputs through

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(1)



the RESx pin when the voltage dropout is large between SUPPLY and LED required total forward voltage. In the opposite case, the most of the current to LED outputs through the OUTx pin when the voltage headroom is relative low between SUPPLY and LED required forward voltage.

#### 6.3.5 PWM Control (PWMx)

The pulse width modulation (PWM) input of the TPS92620-Q1 functions as enable for the output current. When the voltage applied on the PWM pin is higher than  $V_{IH(PWM)}$ , the relevant output current is enabled. When the voltage applied on PWM pin is lower than  $V_{IL(PWM)}$ , the output current is disabled as well as the diagnostic features. Besides output current enable and disable function, the PWM input of TPS92620-Q1 also supports adjustment of the average current output for brightness control if the frequency of applied PWM signal is higher than 100Hz, which is out of visible frequency range of human eyes. TI recommends a 200Hz PWM signal with 1% to 100% duty cycle input for brightness control. Please refer to Figure 7-4 for typical PWM dimming application.

The TPS92620-Q1 device has two PWM input pins: PWM1, PWM2 to control each of current output channel independently. PWM1 input controls the output channel 1 for both OUT1 and RES1, PWM2 input controls the output channel 2 for both OUT2 and RES2. Figure 6-1 illustrates the timing for PWM input and current output.

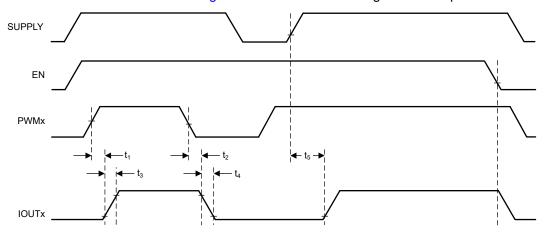


Figure 6-1. Power-On Sequence and PWM Dimming Timing

The detailed information and value of each time period in Figure 6-1 is described in TIMING section of the *Electrical Characteristics*.

#### 6.3.6 Supply Control

The TPS92620-Q1 can support supply control to turn ON and OFF output current. When the voltage applied on the SUPPLY pin is higher than the LED string forward voltage plus needed headroom voltage at required current, and the PWM pin voltage is high, the output current is turned ON and well regulated. However, if the voltage applied on the SUPPLY pin is lower than  $V_{(POR_falling)}$ , the output current is turned OFF. With this feature, the power supply voltage in designed pattern can control the output current ON and OFF. The brightness is adjustable if the ON and OFF frequency is fast enough. Because of the high accuracy design of PWM threshold in TPS92620-Q1, TI recommends a resistor divider on the PWM pin to set the SUPPLY threshold higher than LED forward voltage plus required headroom voltage as shown in Figure 6-2. The headroom voltage is basically the summation of  $V_{(DROPOUT)}$  and  $V_{(CS_REG)}$ . When the voltage on the PWM pin is higher than  $V_{IL(PWM)}$ , the output current is turned ON. However, when the voltage on the PWM pin solver than  $V_{IL(PWM)}$ , the output current is turned OFF. Use Equation 2 to calculate the SUPPLY threshold voltage.



(2)

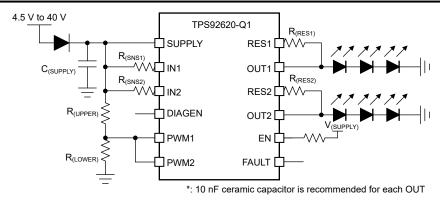


Figure 6-2. Application Schematic for Supply Control LED Brightness

$$V_{(SUPPLY\_PWM\_th\_rising)} = V_{IH(PWM)} \times \left(1 + \frac{R_{(UPPER)}}{R_{(LOWER)}}\right)$$

where

V<sub>IH(PWM)</sub> = 1.26V (maximum)

#### 6.3.7 Diagnostics

The TPS92620-Q1 device provides advanced diagnostics and fault-protection features for automotive exterior lighting systems. The device can detect and protect fault from LED-string short-to-GND, LED-string open-circuit and junction overtemperature scenarios. The device also supports a one-fails–all-fail fault bus design that can flexibly fit different regulatory requirements.

#### 6.3.7.1 LED Short-to-GND Detection

The TPS92620-Q1 device has LED short-to-GND detection. The LED short-to-GND detection monitors the output voltage when the output current is enabled. After a short-to-GND LED failure is detected, the device turns off the faulty channel and retries automatically, regardless of the state of the PWM input. If the retry mechanism detects the removal of the LED short-to-GND fault, the device resumes to normal operation.

The TPS92620-Q1 monitors both V<sub>(OUTx)</sub> voltage and V<sub>(RESx)</sub> voltage of each channel and compares it with the internal reference voltage to detect a short-to-GND failure. If V<sub>(OUTx)</sub> or V<sub>(RESx)</sub> voltage falls below V<sub>(SG th falling)</sub> longer than the deglitch time of t<sub>(SG\_deg)</sub>, the device asserts the short-to-GND fault and pulls low the FAULT pin. During the deglitching time period, if V<sub>(OUTx)</sub> and V<sub>(RESx)</sub> rises above V<sub>(SG th rising)</sub>, the timer is reset.

After the TPS92620-Q1 has asserted a short-to-GND fault, the device turns off the faulty output channel and retries automatically with a small current. During retrying, the device sources a small current  $I_{(Retry)}$  from SUPPLY to OUT and RES to pull up the LED loads continuously. After auto-retry detects output voltage rising above  $V_{(SG\_th\_rising)}$ , it clears the short-to-GND fault and resumes to normal operation. Figure 6-3 illustrates the timing for LED short-circuit detection, protection, retry and recovery.

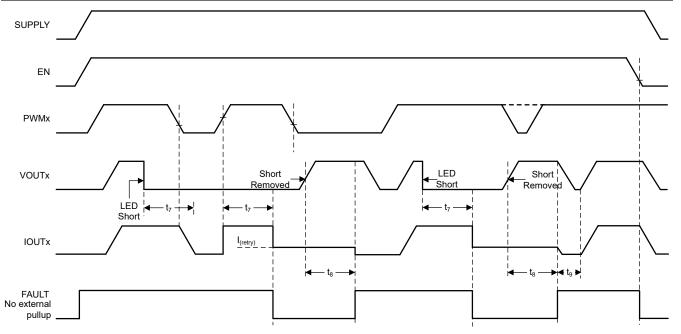


Figure 6-3. LED Short-to-GND Detection and Recovery Timing Diagram

The detailed information and value of each time period in Figure 6-3 is described in TIMING section of the *Electrical Characteristics*.

### 6.3.7.2 LED Open-Circuit Detection

The TPS92620-Q1 device has LED open-circuit detection. The LED open-circuit detection monitors the output voltage when the current output is enabled. The LED open-circuit detection is only enabled when DIAGEN is HIGH. A short-to-battery fault is also detected and recognized as an LED open-circuit fault.

The TPS92620-Q1 monitors dropout-voltage differences between the IN and OUT pins for each LED channel when PWM is HIGH. The voltage difference  $V_{(INx)} - V_{(OUTx)}$  is compared with the internal reference voltage  $V_{(OPEN\_th\_rising)}$  to detect an LED open-circuit incident. If  $V_{(OUTx)}$  rises and causes  $V_{(INx)} - V_{(OUTx)}$  less than the  $V_{(OPEN\_th\_rising)}$  voltage longer than the deglitch time of  $t_{(OPEN\_deg)}$ , the device asserts an open-circuit fault. After a LED open-circuit failure is detected, the internal constant-current sink pulls down the FAULT pin voltage. During the deglitch time period, if  $V_{(OUTx)}$  falls and makes  $V_{(INx)} - V_{(OUTx)}$  larger than  $V_{(OPEN\_th\_falling)}$ , the deglitch time ris reset.

The TPS92620-Q1 shuts down the output current regulation for the error channel after LED open-circuit fault is detected. The device sources a small current  $I_{(Retry)}$  from SUPPLY to OUT and RES when DIAGEN input is logic High. After the fault condition is removed, the device resumes normal operation and releases the FAULT pin. Figure 6-4 illustrates the timing for LED open-circuit detection, protection, retry and recovery.



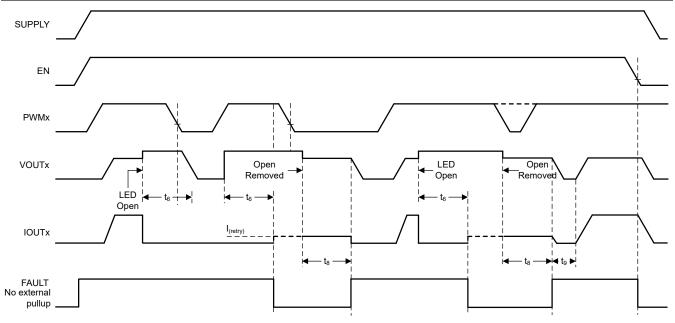


Figure 6-4. LED Open-Circuit Detection and Recovery Timing Diagram

The detailed information and value of each time period in Figure 6-4 is described in TIMING section of the *Electrical Characteristics*.

#### 6.3.7.3 LED Open-Circuit Detection Enable (DIAGEN)

The TPS92620-Q1 device supports the DIAGEN pin with an accurate threshold to disable the LED open-circuit. The DIAGEN pin can be used to enable or disable LED open-circuit detection based on SUPPLY pin voltage sensed by an external resistor divider as illustrated in Figure 6-5. When the voltage applied on DIAGEN pin is higher than the threshold  $V_{IH(DIAGEN)}$ , the device enables LED open-circuit detection. When  $V_{(DIAGEN)}$  is lower than the threshold  $V_{IL(DIAGEN)}$ , the device disables LED open-circuit detection.

Only LED open-circuit detection can be disabled by pulling down the DIAGEN pin. The LED short-to-GND detection and overtemperature protection cannot be turned off by pulling down the DIAGEN pin. Use Equation 3 to calculate the SUPPLY threshold voltage.

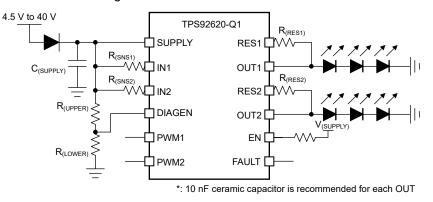


Figure 6-5. Application Schematic For DIAGEN

$$V_{(SUPPLY\_DIAGEN\_th\_falling)} = V_{IL(DIAGEN)} \times \left(1 + \frac{R_{(UPPER)}}{R_{(LOWER)}}\right)$$

(3)

where



• V<sub>IL(DIAGEN)</sub> = 1.045V (minimum)

#### 6.3.7.4 Overtemperature Protection

The TPS92620-Q1 device monitors device junction temperature. When the junction temperature reaches thermal shutdown threshold  $T_{(TSD)}$ , the output shuts down. After the junction temperature falls below  $T_{(TSD)} - T_{(TSD_{HYS})}$ , the device recovers to normal operation. During overtemperature protection, the FAULT pin is pulled low.

#### 6.3.7.5 Low Dropout Operation

When the supply voltage drops below LED string total forward voltage plus headroom voltage at required current, the TPS92620-Q1 device operates in low-dropout conditions to deliver current output as close as possible to target value. The actual current output is less than preset value due to insufficient headroom voltage for power transistor. As a result, the voltage across the sense resistor fails to reach the regulation target. The headroom voltage is the summation of  $V_{(DROPOUT)}$  and  $V_{(CS REG)}$ .

If the TPS92620-Q1 is designed to operate in low-dropout condition, the open-circuit diagnostics must be disabled by pulling the DIAGEN pin voltage lower than  $V_{IL(DIAGEN)}$ . Otherwise, the TPS92620-Q1 detects an open-circuit fault and reports a fault on the FAULT pin. The DIAGEN pin is used to avoid false diagnostics due to low supply voltage.

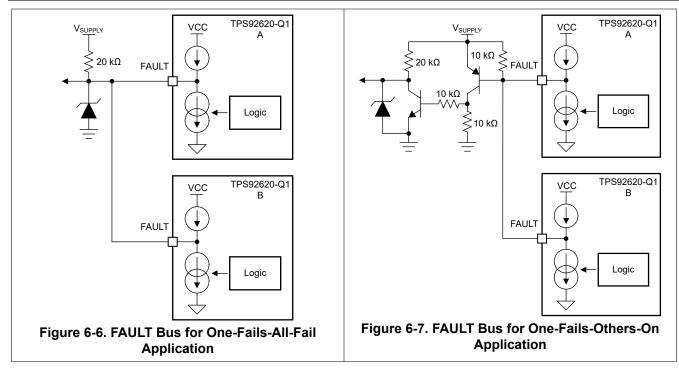
#### 6.3.8 FAULT Bus Output With One-Fails-All-Fail

During normal operation, The  $\overline{FAULT}$  pin of TPS92620-Q1 is weakly pulled up by an internal pullup current source,  $I_{(FAULT\_pullup)}$ . If any fault scenario occurs, the  $\overline{FAULT}$  pin is strongly pulled low by the internal pulldown current sink,  $I_{(FAULT\_pulldown)}$  to report out the fault alarm.

Meanwhile, the TPS92620-Q1 also monitors the  $\overline{FAULT}$  pin voltage internally. If the  $\overline{FAULT}$  pin of the TPS92620-Q1 is pulled low by external current sink below V<sub>IL(FAULT)</sub>, the current output is turned off even though there is no fault detected on owned outputs. The device does not resume to normal operation until the  $\overline{FAULT}$  pin voltage rises above V<sub>IH(FAULT)</sub>.

Based on this feature, the TPS92620-Q1 device is able to construct a FAULT bus by tying FAULT pins from multiple TPS92620-Q1 devices to achieve one-fails-all-fail function as Figure 6-6 showing. The lower side TPS92620-Q1 (B) detects any kind of LED fault and pulls low the FAULT pin. The low voltage on FAULT pin is detected by upper side TPS92620-Q1 (A) because the FAULT pins are connected of two devices. The upper side TPS92620-Q1 (A) turns off all output current for each channel as a result. If the FAULT pins of each TPS92620-Q1 are all connected to drive the base of an external PNP transistor as illustrated in Figure 6-7, the one-fails-all-fail function is disabled and only the faulty channel device is turned off.







### 6.3.9 FAULT Table

#### Table 6-1. Fault Table With DIAGEN = HIGH (Full Function)

FAULT BUS STATUS	FAULT TYPE	DETECTION MECHANISM	FAILT BUS					
FAULT = H	Open circuit or short-to-supply	V <sub>(IN)</sub> - V <sub>(OUT)</sub> < V <sub>(OPEN_th_rising)</sub>	EN = H and PWMx = H	t <sub>(OPEN_deg)</sub>	Constant- current pulldown	Device turns failed output off and retries with constant current I <sub>(retry)</sub> , ignoring the PWM input.	Auto recovery	
	Short-to-ground	$V_{(OUT)} < V_{(SG_{th_{falling}})} \\ OR \\ V_{(RES)} < V_{(SG_{th_{falling}})}$	EN = H and PWMx = H	t <sub>(SG_deg)</sub>	Constant- current pulldown	Device turns failed output off and retries with constant current I <sub>(retry)</sub> , ignoring the PWM input.	Auto recovery	
	Overtemperature	$T_J > T_{(TSD)}$	EN = H	t <sub>(TSD_deg)</sub>	Constant- current pulldown	Device turns all output channels off.	Auto recovery	
FAULT = L	Fault is detected	Device turns a	Device turns all remained channels off and keeps retry on the failed channels. After the Fault pin is released, all channels are turned on after t <sub>(FAULT recovery)</sub> time.					
	No fault is detected		Device turns all output channels off.					

## Table 6-2. Fault Table With DIAGEN = LOW (Full Function)

FAULT BUS STATUS	FAULT TYPE	DETECTION MECHANISM	CURRENT OUTPUT	DEGLITCH TIME	FAULT BUS	FAULT HANDLING ROUTINE	FAULT RECOVERY				
	Open circuit or short-to-supply	Ignored									
FAULT = H	Short-to-ground	V <sub>(OUT)</sub> < V(SG_th_falling) OR V <sub>(OUT)</sub> < V(SG_th_falling)	EN = H and PWMx = H	t <sub>(SG_deg)</sub>	Constant- current pulldown	Device turns output off and retries with constant current I <sub>(retry)</sub> , ignoring the PWM input.	Auto recovery				
	Overtemperature	$T_J > T_{(TSD)}$	EN = H	t <sub>(TSD_deg)</sub>	Constant- current pulldown	Device turns all output channels off.	Auto recovery				
FAULT = L	Fault is detected	Device turns all remained channels off and keeps retry on the failed channels. After the Fault pin is released, all channels are turned on after t <sub>(FAULT_recovery)</sub> time.									
	No fault is detected			Device tur	ns all output cha	innels off.					



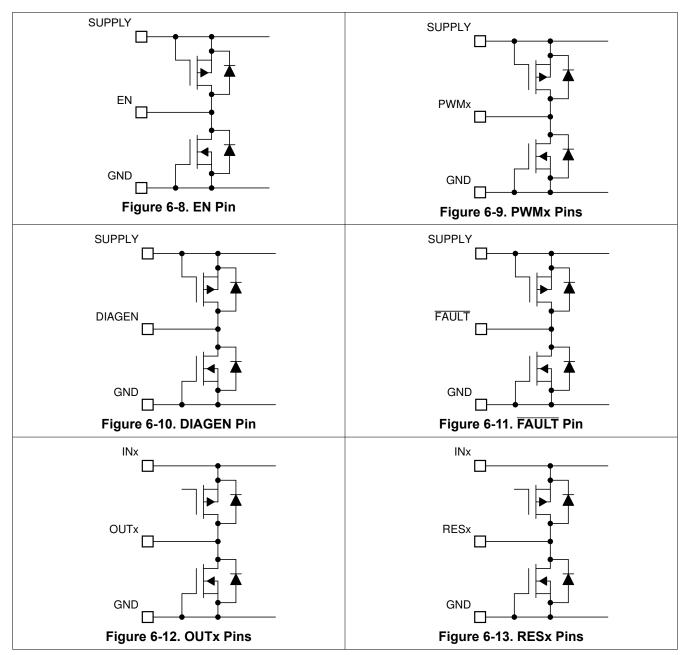
#### 6.3.10 LED Fault Summary

	Table 6-3. LED Connection Fault Summary								
Case 1	Case 2	Case 3	Case 4						
LED Short-to-GND Fault	LED Short-to-GND Fault	LED Short-to-GND Fault	LED Short-to-GND Fault						
Case 5	Case 6	Case 7	Case 8						
		The sx of the system of the sy							
LED Open Fault	LED Open Fault No Fault		LED Open Fault						
Case 9	Case 10	Case 11	Case 12						
No Fault	No Fault	LED Open Fault	No Fault						

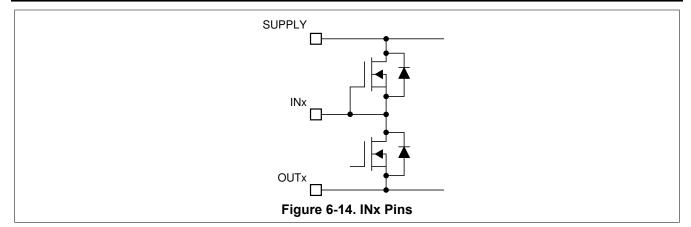
#### Table 6-3. LED Connection Fault Summary



## 6.3.11 IO Pins Inner Connection









### 6.4 Device Functional Modes

#### 6.4.1 Undervoltage Lockout, V<sub>(SUPPLY)</sub> < V<sub>(POR\_rising)</sub>

When the device is in undervoltage lockout status, the TPS92620-Q1 device disables all functions until the supply rises above the  $V_{(POR \ rising)}$  threshold.

#### 6.4.2 Normal Operation V<sub>(SUPPLY)</sub> ≥ 4.5V

The device drives an LED string in normal operation. With enough voltage drop across SUPPLY and OUT, the device can drive the output in constant-current mode.

#### 6.4.3 Low-Voltage Dropout Operation

When the device drives an LED string in low-dropout operation, if the  $V_{(DROPOUT)}$  is less than the open-circuit detection threshold, the device can report a false open-circuit fault. TI recommends only enabling the open-circuit detection when the voltage across the IN and OUTx is higher than the maximum voltage of LED open rising threshold to avoid a false open-circuit detection.

#### 6.4.4 Fault Mode

When the TPS92620-Q1 detects a fault, the device tries to pull down the  $\overline{FAULT}$  pin with a constant current. If the FAULT bus is pulled down, the device switches to fault mode and consumes a fault current of I<sub>(FAULT)</sub>.



## 7 Application and Implementation

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

#### 7.1 Application Information

In automotive lighting applications, thermal performance and LED diagnostics are always design challenges for linear LED drivers.

The TPS92620-Q1 device is capable of detecting LED open-circuit and LED short-circuits. To increase current driving capability, the TPS92620-Q1 device supports using an external shunt resistor to help dissipate heat as the following section, *Thermal Sharing Resistor (OUTx and RESx)*, describes. This method provides a low-cost solution of using external resistors to minimize thermal accumulation on the device itself due to large voltage difference between input voltage and LED string forward voltage, while still keeping high accuracy of the total current output.

#### 7.2 Typical Applications

#### 7.2.1 BCM Controlled Rear Lamp With One-Fails-All-Fail Setup

The multiple TPS92620-Q1 devices are capable of driving different functions for automotive rear lamp including stop, turn indicator, tail, fog, reverse and center-high-mounted-stop-lamp. The one-fails-all-fail single lamp mode can be easily achieved by FAULT bus by shorting the FAULT pins.

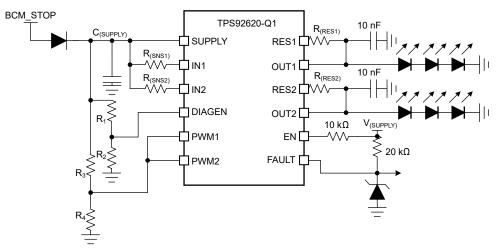


Figure 7-1. Typical Application Schematic

#### 7.2.1.1 Design Requirements

Input voltage range is from 9V to 16V, and a total 6 strings with 3 LEDs in each string are required to achieve stop function. The LED maximum forward voltage,  $V_{F\_MAX}$  is 2.5V for each LED, while the minimum forward voltage,  $V_{F\_MIN}$  is 1.9V. The current requirement for each LED,  $I_{(LED)}$  is 130mA. The LED brightness and ON and OFF control is manipulated by body control module (BCM) directly by connecting and disconnecting the power supply to the LED load.

#### 7.2.1.2 Detailed Design Procedure

**Step 1**: Use Equation 4 to determine the current sensing resistor,  $R_{(SNSx)}$ .



$$R_{(SNSx)} = \frac{V_{(CS\_REG)}}{I_{(OUTx\_Tot)}}$$

where

- V<sub>(CS REG)</sub> = 150mV (typical)
- $I_{(OUTx Tot)} = 130 \text{mA}$

According to design requirements, output current for each channel is same so that the  $R_{(SNS1)} = R_{(SNS2)} = 1.15\Omega$ . Two resistors in parallel can be used to achieve equivalent resistance when sense resistor is not a standard decade resistance value.

**Step 2**: Design the current distribution between  $I_{(OUTx)}$  and  $I_{(RESx)}$ , and use Equation 5 to calculate the current sharing resistor,  $R_{(RESx)}$ . The  $R_{(RESx)}$  value actually decides the current distribution for  $I_{(OUTx)}$  path and  $I_{(RESx)}$  path. TI recommends the current sharing resistor  $R_{(RESx)}$  to consume 50% of the total current at typical supply operating voltage.

$$R_{(RESx)} = \frac{V_{(SUPPLY)} - V_{(OUTx)}}{I_{(OUTx\_Tot)} \times 0.5}$$

where

- V<sub>(SUPPLY)</sub> = 12V (typical)
- I<sub>(OUTx Tot)</sub> = 130mA

The calculated result for  $R_{(RESx)}$  resistor value including  $R_{(RES1)}$ ,  $R_{(RES2)}$  is 85.4 $\Omega$  when  $V_{(OUTx)}$  is typical 3 × 2.15V = 6.45V.

**Step 3**: Design the threshold voltage of SUPPLY to enable the LED open-circuit diagnostics, and calculate voltage divider resistor value for *R1* and *R2* on DIAGEN pin.

The maximum forward voltage of LED-string is  $3 \times 2.5V = 7.5V$ . To avoid the open-circuit fault reported in low-dropout operation conditions, additional headroom between SUPPLY and OUTx must be considered. The TPS92620-Q1 device must disable open-circuit detection when the supply voltage is below LED-string maximum forward voltage plus V<sub>(OPEN\_th\_rising)</sub> and V<sub>(CS\_REG)</sub>. Use Equation 6 to calculate the voltage divider resistor, R1 and R2 value.

$$R_{1} = \left(\frac{V_{(OPEN\_th\_rising)} + V_{(CS\_REG)} + V_{(OUTx)}}{V_{IL(DIAGEN)}} - 1\right) \times R_{2}$$

where

- V<sub>(OPEN\_th\_rising)</sub> = 420mV (maximum)
- V<sub>(CS\_REG)</sub> = 156mV
- $V_{IL(DIAGEN)} = 1.045V$  (minimum)
- $R_2 = 10k\Omega$  (recommended)

The calculated result for R1 is 67.3k $\Omega$  when V<sub>(OUTx)</sub> maximum voltage is 7.5V and V<sub>(CS REG)</sub> is 156mV.

**Step 4**: Design the threshold voltage of SUPPLY to turn on and off each channel of LED, and calculate voltage divider resistor value for *R3* and *R4* on PWM input pin.

The minimum forward voltage of LED string is  $3 \times 1.9V = 5.7V$ . To make sure the current output on each of LED-string is normal, each LED-string must be turned off when SUPPLY voltage is lower than LED minimum required forward voltage plus dropout voltage between INx to OUTx and V<sub>(CS\_REG)</sub>. Use Equation 7 to calculate the voltage divider resistor, R3 and R4 value.

(4)

(5)

(6)



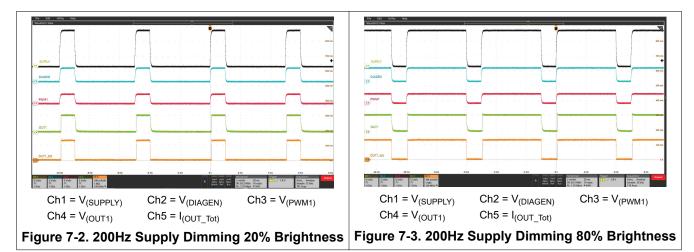
$$R_{3} = \left(\frac{V_{(DROPOUT)} + V_{(CS\_REG)} + V_{(OUTx)}}{V_{IH(PWM)}} - 1\right) \times R_{4}$$

where

- V<sub>(DROPOUT)</sub> = 300mV (typical)
- V<sub>(CS\_REG)</sub> = 156mV (maximum)
- V<sub>IH(PWM)</sub> = 1.26V (maximum)
- $R_4 = 10\dot{k}\Omega$  (recommended)

The calculated result for R3 is 38.9k $\Omega$  when V<sub>(OUTx)</sub> minimum voltage is 5.7V and V<sub>(CS REG)</sub> is 156mV.

### 7.2.1.3 Application Curves



#### 7.2.2 Independent PWM Controlled Rear Lamp By MCU

The TPS92620-Q1 device can drive the each current output channel independently by PWM input at PWM1, PWM2 ,PWM3 and PWM4 pins. The PWM input signals comes from MCU to achieve sequential turn indicator feature.

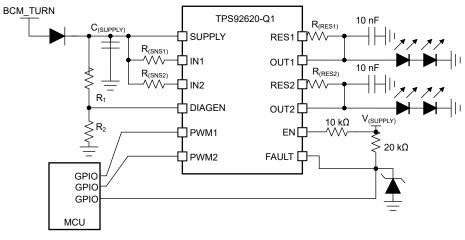
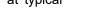


Figure 7-4. Typical Application Schematic

(7)



## Product Folder Links: TPS92620-Q1

#### 7.2.2.1 Design Requirements

Input voltage range is from 9V to 16V, and a total 2 strings with 2 LEDs in each string are required to achieve turn indicator function. The LED maximum forward voltage, V<sub>F MAX</sub> is 2.5V for each LED, however the minimum forward voltage, V<sub>F MIN</sub> is 1.9V. Each LED current is 130mA and each output channel is independent controlled by MCU through individual GPIO.

#### 7.2.2.2 Detailed Design Procedure

**Step 1**: Use Equation 8 to determine the current sensing resistor,  $R_{(SNSx)}$ .

 $R_{(SNSx)} = \frac{V_{(CS\_REG)}}{I_{(OUTx\_Tot)}}$ 

where

- V<sub>(CS\_REG)</sub> = 150mV (typical)
   I<sub>(OUTx\_Tot)</sub> = 130mA

According to design requirements, output current for each channel is same so that the calculated R<sub>(SNS1)</sub> =  $R_{(SNS2)} = 1.15\Omega.$ 

Step 2: Design the current distribution between I(OUTx) and I(RESx), and use Equation 9 to calculate the current sharing resistor, R<sub>(RESx)</sub>. The R<sub>(RESx)</sub> value actually decides the current distribution for I<sub>(OUTx)</sub> path and I<sub>(RESx)</sub> path, basic principle is to design the R(RESX) to consume appropriate 50% total power dissipation at typical supply operating voltage.

#### where

where

28

- V<sub>(SUPPLY)</sub> = 12V (typical)
- I<sub>(OUTx Tot)</sub> = 130mA (maximum)

 $R_{(RESx)} = \frac{V_{(SUPPLY)} - V_{(OUTx)}}{I_{(OUTx - Tot)} \times 0.5}$ 

The calculated result for R<sub>(RESx)</sub> resistor value including R<sub>(RES1)</sub>, R<sub>(RES2)</sub> is 117Ω when V<sub>(OUTx)</sub> is typical 2 × 2.2V = 4.4 V.

Step 3: Design the threshold voltage of SUPPLY to enable the LED open circuit, and calculate voltage divider resistor value for R1 and R2 on the DIAGEN pin.

The maximum forward voltage of LED-string is 2 × 2.5V = 5V. To avoid the open-circuit fault reported in low-dropout operation conditions, additional headroom between SUPPLY and OUTx must be considered. The TPS92620-Q1 device must disable open-circuit detection when the supply voltage is below LED-string maximum forward voltage plus V<sub>(OPEN th rising)</sub> and V<sub>(CS REG)</sub>. Use Equation 10 to calculate the voltage divider resistor, R1 and R2 value.

$$R_{1} = \left(\frac{V_{(OPEN\_th\_rising)} + V_{(CS\_REG)} + V_{(OUTx)}}{V_{IL(DIAGEN)}} - 1\right) \times R_{2}$$

- V<sub>(OPEN th rising)</sub> = 420mV (maximum)
- $V_{(CS REG)} = 156 mV (maximum)$
- $V_{IL(DIAGEN)} = 1.045V$  (minimum)

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 $R_2 = 10k\Omega$  (recommended)



(8)

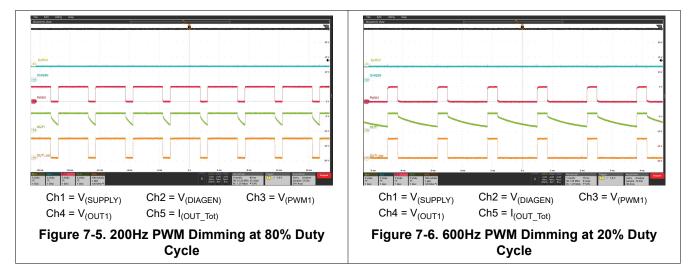
(10)

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The calculated result for R1 is 43.4k $\Omega$  when V<sub>(OUTx)</sub> maximum voltage is 5V and V<sub>(CS REG)</sub> is 156mV.

### 7.2.2.3 Application Curves



## 7.3 Power Supply Recommendations

The TPS92620-Q1 is designed to operate from an automobile electrical power system within the range specified in *Power Supply*. The  $V_{(SUPPLY)}$  input must be protected from reverse voltage and voltage dump condition over 40V. The impedance of the input supply rail must be low enough that the input current transient does not cause drop below LED string required forward voltage. If the input supply is connected with long wires, additional bulk capacitance can be required in addition to normal input capacitor.

## 7.4 Layout

#### 7.4.1 Layout Guidelines

Thermal dissipation is the primary consideration for TPS92620-Q1 layout.

- TI recommends large thermal dissipation area in both top and bottom layers of PCB. The copper pouring area in same layer with TPS92620-Q1-Q1 footprint must directly cover the thermal pad land of the device with wide connection as much as possible. The copper pouring in opposite PCB layer or inner layers must be connected to thermal pad directly through multiple thermal vias.
- TI recommends to place R<sub>(RESx)</sub> resistors away from the TPS92620-Q1 device with more than 20-mm distance, because R<sub>(RESx)</sub> resistors are dissipating some amount of the power as well as the TPS92620-Q1. Place two heat source components apart to reduce the thermal accumulation concentrated at small PCB area. The large copper pouring area is also required surrounding the R<sub>(RESx)</sub> resistors for helping thermal dissipating.

The noise immunity is the secondary consideration for TPS92620-Q1 layout.

- TI recommends to place the noise decoupling capacitors for SUPPLY pin as close as possible to the pins.
- TI recommends to place the R<sub>(SNSx)</sub> resistor as close as possible to the INx pins with the shortest PCB track to SUPPLY pin.



#### 7.4.2 Layout Example

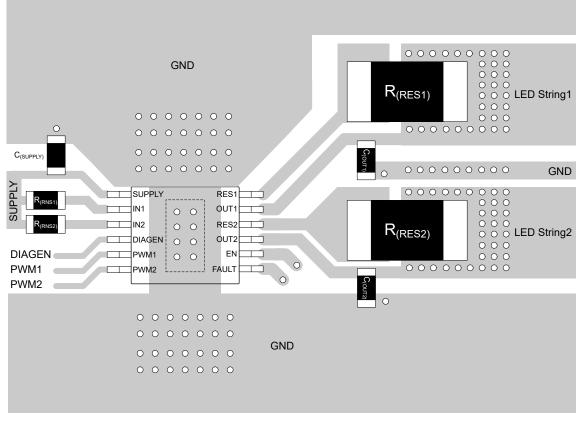


Figure 7-7. TPS92620-Q1 Example Layout Diagram



## 8 Device and Documentation Support

#### 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 8.2 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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#### 8.3 Trademarks

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#### 8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

#### **9 Revision History**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

С	hanges from Revision * (November 2022) to Revision A (January 2024)	Page
•	Updated HVSSOP package pin names, changing the GND pin to the EN pin to all appropriote images	1
•	Updated HVSSOP Package diagram, changing the GND pin to the EN pin t	1
•	Updated HVSSOP package Information to include EN	3
•	Removed HVSSOP package product preview note	3
•	Updated Specifications to include EN pin information	
•	Updated Functional Block Diagram	12
•	Updated Enable and Shutdow(EN) description	13
•	Updated Figure 6-1 with EN pin information	14
•	Updated LED Short-to-GND Detection and Recovery Timing Diagram to include EN pin information	15
•	Updated LED Open-Circuit Detection and Recovery Timing Diagram to include EN pin information	16
•	Updated Application Schematic For DIAGEN to include EN pin information	17
•	Updated Fault Table With DIAGEN = HIGH (Full Function) to include EN logic information	20
•	Updated Typical Application Schematic to include EN pin information	25
•	Updated Typical Application Schematic to include EN pin information	27
•	Updated TPS92620-Q1 Example Layout Diagram	30



## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92620QDGNRQ1	ACTIVE	HVSSOP	DGN	12	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	620Q	Samples
TPS92620QDRRRQ1	ACTIVE	WSON	DRR	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	92620Q	Samples

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## PACKAGE OPTION ADDENDUM

26-Apr-2024



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## TAPE AND REEL INFORMATION





#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92620QDGNRQ1	HVSSOP	DGN	12	5000	330.0	12.4	5.2	4.3	1.45	8.0	12.0	Q1
TPS92620QDRRRQ1	WSON	DRR	12	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2



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## PACKAGE MATERIALS INFORMATION

29-Apr-2024



\*All dimensions are nominal

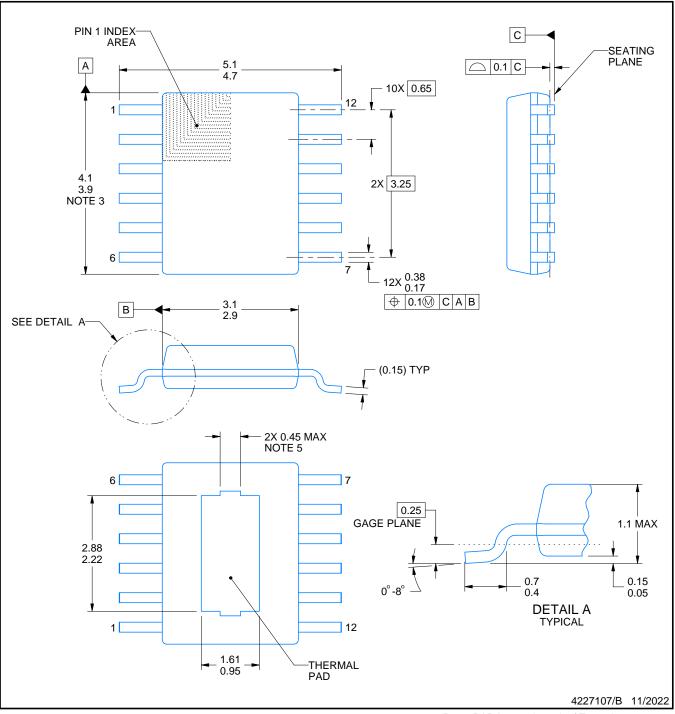
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92620QDGNRQ1	HVSSOP	DGN	12	5000	356.0	356.0	35.0
TPS92620QDRRRQ1	WSON	DRR	12	3000	367.0	367.0	35.0

# **DGN0012A**

## **PACKAGE OUTLINE**

# PowerPAD<sup>™</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. No JEDEC registration as of September 2020.
   5. Features may differ or may not be present.

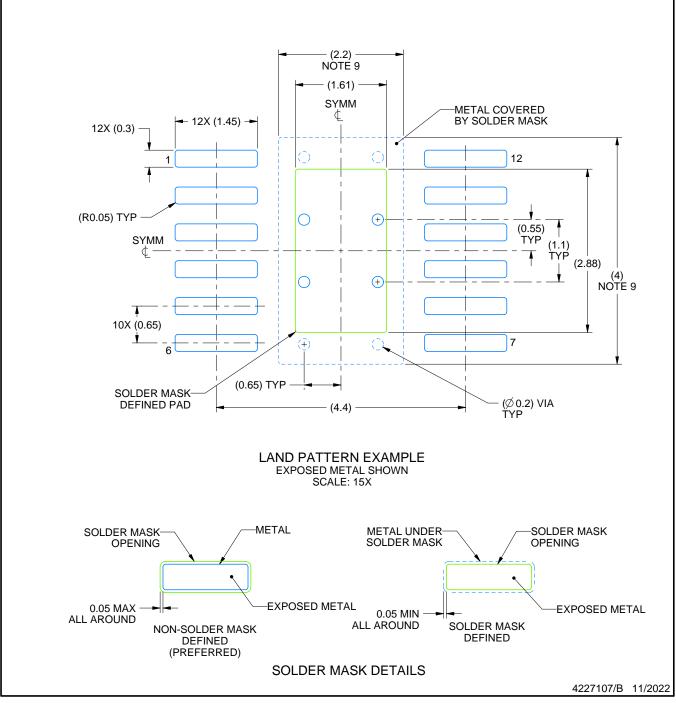


# DGN0012A

# **EXAMPLE BOARD LAYOUT**

# PowerPAD<sup>™</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).

9. Size of metal pad may vary due to creepage requirement.

10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

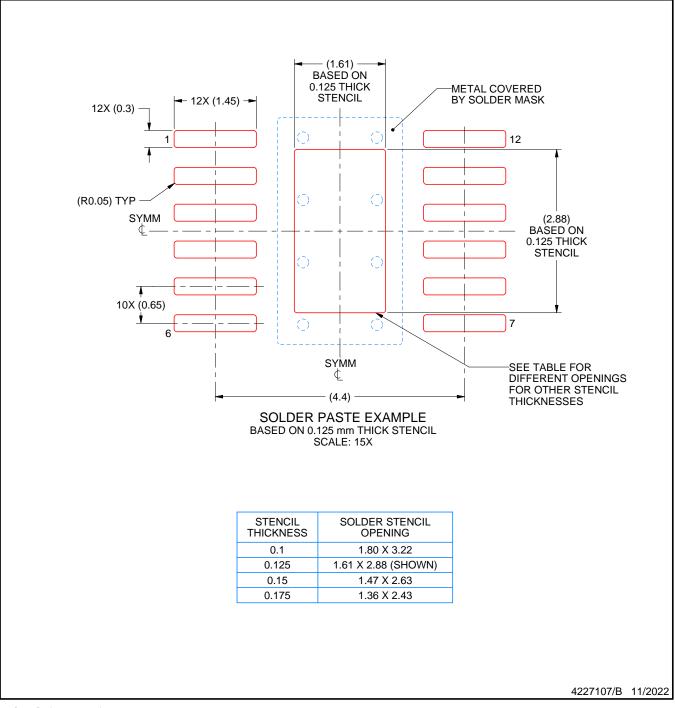


# DGN0012A

## **EXAMPLE STENCIL DESIGN**

# PowerPAD<sup>™</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 12. Board assembly site may have different recommendations for stencil design.



## **DRR 12**

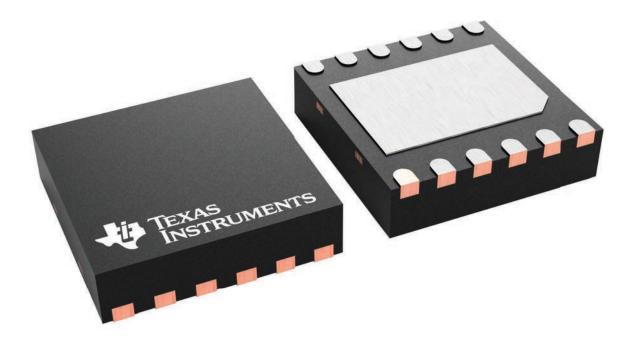
3 x 3, 0.5 mm pitch

# **GENERIC PACKAGE VIEW**

## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





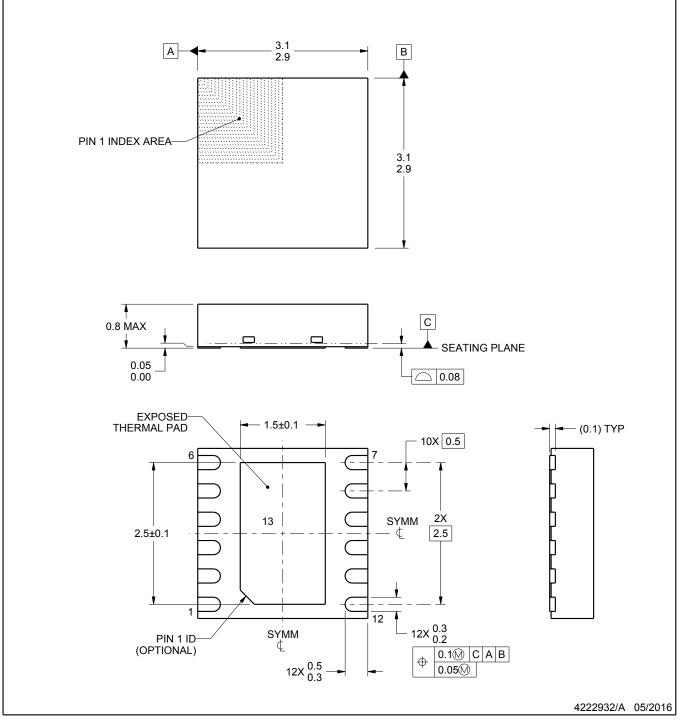
# **DRR0012C**



## **PACKAGE OUTLINE**

## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing All integrations are in minimeters. Any dimensions in parentnesis are for reference only. Dimensioning and per ASME Y14.5M.
   This drawing is subject to change without notice.
   The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

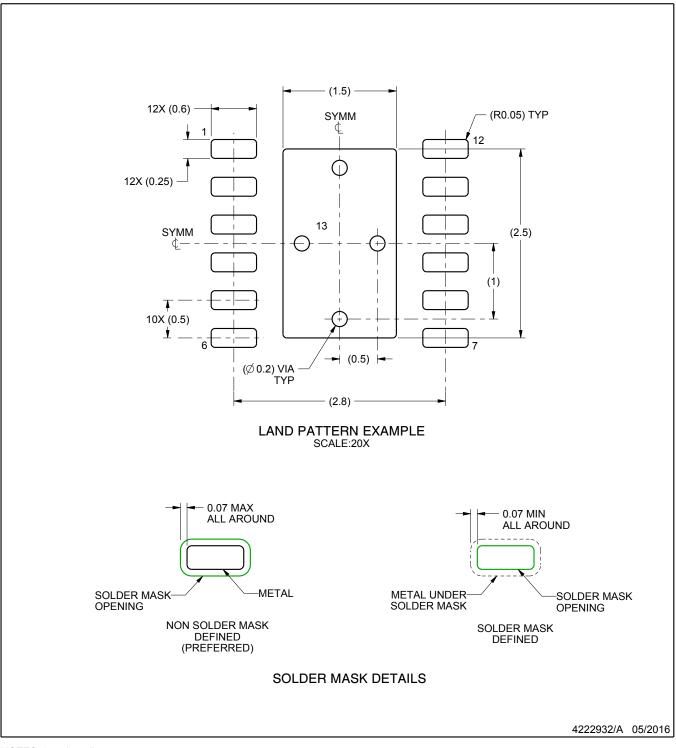


# **DRR0012C**

# **EXAMPLE BOARD LAYOUT**

## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

 Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

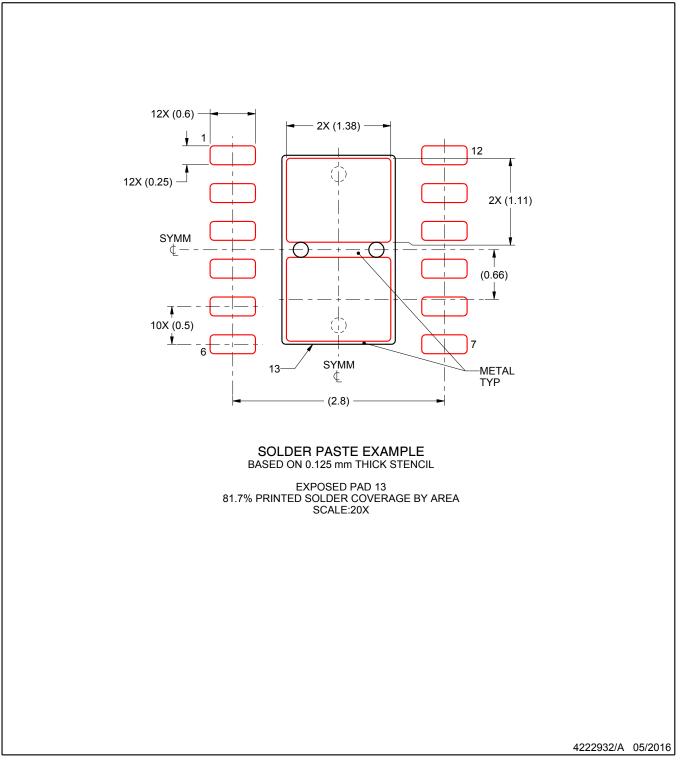


# **DRR0012C**

# **EXAMPLE STENCIL DESIGN**

## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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