TPSM5601R5Hx, 60-V Input, 1-V to 16-V Output, 1.5-A Power Module in Enhanced HotRod™ QFN Package

1 Features

- **Functional Safety-Capable**
  - Documentation available to aid functional safety system design
- 5-mm × 5.5-mm × 4-mm Enhanced HotRod™ QFN
  - **Excellent thermal performance**: up to 18-W output power at 85°C, no airflow
  - Standard footprint: single large thermal pad and all pins accessible from perimeter
- Designed for reliable and rugged applications
  - Wide input voltage range: 4.2 V to 60 V
  - Input voltage transient protection up to 66 V
  - Operating junction range: –40°C to +125°C
  - **EXT-suffix junction range**: –55°C to +125°C
- Fixed 1-MHz switching frequency
- FPWM mode of operation
- Optimized for ultra-low EMI requirements
  - Integrated shielded inductor and high-frequency bypass capacitors
  - Meets EN55011 EMI standards
  - Spread spectrum option reduces emissions
- 26-µA non-switching quiescent current
- Monotonic start-up into prebiased output
- No loop-compensation or bootstrap components
- Precision enable and input UVLO with hysteresis
- **Thermal shutdown protection with hysteresis**
- Create a custom regulator design using WEBENCH® Power Designer

2 Applications

- Field transmitters and sensors, PLC modules
- Thermostats, video surveillance, HVAC systems
- AC and servo drives, rotary encoders
- Industrial transport, asset tracking
- Negative output applications

3 Description

The TPSM5601R5Hx power module is a highly integrated 1.5-A power solution that combines a 60-V input, step-down DC/DC converter with power MOSFETs, a shielded inductor, and passives in a thermally-enhanced QFN package. The 5-mm × 5.5-mm × 4-mm, 15-pin QFN package uses Enhanced HotRod QFN technology for enhanced thermal performance, small footprint, and low EMI. The package footprint has all pins accessible from the perimeter and a single large thermal pad for simple layout and easy handling in manufacturing.

The TPSM5601R5Hx is a compact, easy-to-use power module with a wide adjustable output voltage range of 1.0 V to 16 V. The total solution requires as few as four external components and eliminates the loop compensation and magnetics part selection from the design process. The full feature set includes power good, programmable UVLO, prebias start-up, overcurrent and temperature protections, making the TPSM5601R5Hx an excellent device for powering a wide range of applications. Space-constrained applications benefit from the 5-mm × 5.5-mm package. Additionally, the TPSM5601R5HES offers extended low temperature operation of –55°C and the TPSM5601R5HS offers frequency spread-spectrum operation.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE(1)</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPSM5601R5H</td>
<td>QFN (15)</td>
<td>5.0 mm × 5.5 mm</td>
</tr>
<tr>
<td>TPSM5601R5HE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPSM5601R5HS</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
Table of Contents

1 Features............................................................. 1
2 Applications..................................................... 1
3 Description....................................................... 1
4 Revision History.................................................. 2
5 Device Comparison Table....................................... 3
6 Pin Configuration and Functions................................ 4
7 Specifications..................................................... 5
  7.1 Absolute Maximum Ratings .................................. 5
  7.2 ESD Ratings ..................................................... 5
  7.3 Recommended Operating Conditions ...................... 6
  7.4 Thermal Information ........................................... 6
  7.5 Electrical Characteristics .................................... 7
  7.6 Typical Characteristics (VIN = 12 V) ..................... 9
  7.7 Typical Characteristics (VIN = 24 V) .................... 10
  7.8 Typical Characteristics (VIN = 48 V) .................... 11
  7.9 Typical Characteristics (VIN = 60 V) .................... 12
8 Detailed Description .............................................. 13
  8.1 Overview....................................................... 13
  8.2 Functional Block Diagram ................................... 13
  8.3 Feature Description .......................................... 14
  8.4 Device Functional Modes .................................... 17
9 Applications and Implementation.............................. 18
  9.1 Application Information ..................................... 18
  9.2 Typical Application ........................................... 18
10 Power Supply Recommendations.............................. 20
11 Layout............................................................ 21
  11.1 Layout Guidelines .......................................... 21
  11.2 Layout Example .............................................. 21
12 Device and Documentation Support........................... 25
  12.1 Device Support .............................................. 25
  12.2 Documentation Support .................................... 25
  12.3 Receiving Notification of Documentation Updates ........ 25
  12.4 Support Resources .......................................... 25
  12.5 Trademarks ................................................... 25
  12.6 Electrostatic Discharge Caution ......................... 26
  12.7 Glossary ...................................................... 26
13 Mechanical, Packaging, and Orderable Information............ 26

4 Revision History

Changes from Revision A (March 2021) to Revision B (October 2021) Page
  • Added functional safety bullet ......................................................... 1

Changes from Revision * (December 2020) to Revision A (March 2021) Page
  • Changed device status from Advance Information to Production Data........................................ 1

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Product Folder Links: TPSM5601R5H TPSM5601R5HE
## 5 Device Comparison Table

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPSM5601R5H</td>
<td>60-V input voltage, 1-V to 16-V output voltage, 1.5-A power module, fixed 1-MHz switching, operating junction temperature range: –40°C to +125°C</td>
</tr>
<tr>
<td>TPSM5601R5HS</td>
<td>Equivalent to TPSM5601R5H, but with spread spectrum operation</td>
</tr>
<tr>
<td>TPSM5601R5HEXT</td>
<td>Equivalent to TPSM5601R5H, but with extended junction temperature range: –55°C to +125°C</td>
</tr>
</tbody>
</table>
6 Pin Configuration and Functions

Table 6-1. Pin Functions

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>NAME</th>
<th>TYPE(1)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>AGND</td>
<td>G</td>
<td>Analog ground. Zero voltage reference for internal references and logic. All electrical parameters are measured with respect to this pin. <strong>This pin must be connected to PGND at a single point.</strong> See Section 11.2 for a recommended layout.</td>
</tr>
<tr>
<td>5</td>
<td>DNC</td>
<td>—</td>
<td>Do not connect. Do not connect this pin to ground, to another pin, or to any other voltage. This pin is connected to the internal bootstrap capacitor. This pin must be soldered to an isolated pad.</td>
</tr>
<tr>
<td>2</td>
<td>EN</td>
<td>I</td>
<td>Enable pin. This pin turns the converter on when pulled high and turns off the converter when pulled low. This pin can be connected directly to VIN. <strong>Do not float.</strong> This pin can be used to set the input undervoltage lockout with two resistors. See Section 8.3.4.</td>
</tr>
<tr>
<td>9</td>
<td>FB</td>
<td>I</td>
<td>Feedback input. Connect the mid-point of the feedback resistor divider to this pin. Connect the upper resistor (R_{FB1}) of the feedback divider to V_{OUT} at the desired point of regulation. Connect the lower resistor (R_{FB2}) of the feedback divider to AGND.</td>
</tr>
<tr>
<td>3, 6, 13</td>
<td>NC</td>
<td>—</td>
<td>Not connected. These pins are not connected to any circuitry within the module. Leaving these pins unconnected to any other signal increases spacing near the high voltage pins (VIN, SW, EN, DNC). However, if the high voltage spacing is not needed in the application, connecting these pins to the PGND plane can help to enhance shielding and thermal performance.</td>
</tr>
<tr>
<td>15</td>
<td>PGND</td>
<td>G</td>
<td>Power ground. This is the return current path for the power stage of the device. Connect this pad to the input supply return, load return, and capacitors associated with the VIN and VOUT pins. See Section 11.2 for a recommended layout.</td>
</tr>
<tr>
<td>12</td>
<td>PGOOD</td>
<td>O</td>
<td>Power-good pin. Open-drain output that asserts low if the feedback voltage is not within the specified window thresholds. A 10-kΩ to 100-kΩ pullup resistor is required and can be tied to the V5V pin or other DC voltage less than 18 V. If not used, this pin can be left open or connected to PGND.</td>
</tr>
<tr>
<td>4</td>
<td>SW</td>
<td>O</td>
<td>Switch node. Do not place any external component on this pin or connect to any signal.</td>
</tr>
<tr>
<td>1, 14</td>
<td>VIN</td>
<td>I</td>
<td>Input supply voltage. Connect the input supply to these pins. Connect input capacitors between these pins and PGND in close proximity to the device.</td>
</tr>
<tr>
<td>7, 8</td>
<td>VOUT</td>
<td>O</td>
<td>Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external output capacitors between these pins and PGND.</td>
</tr>
<tr>
<td>11</td>
<td>V5V</td>
<td>O</td>
<td>Internal 5-V LDO output. Supplies internal control circuits. Do not connect to external loads. This pin can be used as logic supply for PGOOD pin.</td>
</tr>
</tbody>
</table>

(1) G = Ground, I = Input, O = Output

---

Figure 6-1. 15-Pin QFN RDA Package (Top View)
7 Specifications

7.1 Absolute Maximum Ratings

Over the operating ambient temperature range\(^{(1)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN to PGND</td>
<td>–0.3</td>
<td>66</td>
<td>V</td>
</tr>
<tr>
<td>EN to AGND(^{(2)})</td>
<td>–0.3</td>
<td>(V_{IN} + 0.3)</td>
<td>(\text{V, } V_{IN} &lt; 0)</td>
</tr>
<tr>
<td>PGOOD to AGND(^{(3)})</td>
<td>–0.3</td>
<td>22</td>
<td>(\text{V, } V_{IN} &lt; 0)</td>
</tr>
<tr>
<td>FB to AGND</td>
<td>–0.3</td>
<td>5.5</td>
<td>(\text{V, } V_{IN} &lt; 0)</td>
</tr>
<tr>
<td>AGND to PGND</td>
<td>–0.3</td>
<td>0.3</td>
<td>(\text{V, } V_{IN} &lt; 0)</td>
</tr>
<tr>
<td>VOUT to PGND(^{(2)})</td>
<td>–0.3</td>
<td>30</td>
<td>(\text{V, } V_{IN} &lt; 0)</td>
</tr>
<tr>
<td>VCC to AGND</td>
<td>0</td>
<td>5.5</td>
<td>(\text{V, } V_{IN} &lt; 0)</td>
</tr>
<tr>
<td>Operating IC junction temperature, (T_{J}) (^{(3)})</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature, (T_{stg})</td>
<td>–55</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Peak reflow case temperature</td>
<td>245</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Maximum number or reflows allowed</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mechanical vibration</td>
<td>MIL-STD-883H, Method 2007.3, 1 msec, 1/2 sine, mounted</td>
<td>20</td>
<td>G</td>
</tr>
</tbody>
</table>

\(1\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any conditions beyond those indicated in Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(2\) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V

\(3\) The ambient temperature is the air temperature of the surrounding environment. The junction temperature is the temperature of the internal power IC when the device is powered. Operating below the maximum ambient temperature, as shown in the safe operating area (SOA) curves in the typical characteristics sections, ensures that the maximum junction temperature of any component inside the module is never exceeded.

7.2 ESD Ratings

<table>
<thead>
<tr>
<th>(V_{(ESD)})</th>
<th>Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM)(^{(1)})</td>
<td>±1500</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Charged-device model (CDM)(^{(2)})</td>
<td>±1500</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

\(1\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

\(2\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
7.3 Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted) (1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage, $V_{IN}$</td>
<td>4.2</td>
<td>60</td>
<td>V</td>
</tr>
<tr>
<td>Output voltage, $V_{OUT}$</td>
<td>1</td>
<td>16 (3)</td>
<td>V</td>
</tr>
<tr>
<td>Output current, $I_{OUT}$</td>
<td>0</td>
<td>1.5</td>
<td>A</td>
</tr>
<tr>
<td>EN voltage, $V_{EN}$ (2)</td>
<td>0</td>
<td>$V_{IN}$</td>
<td>V</td>
</tr>
<tr>
<td>PGOOD pullup voltage, $V_{PGOOD}$ (2)</td>
<td>0</td>
<td>18</td>
<td>V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Non-EXT suffix device</th>
<th>EXT suffix device</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating ambient temperature, $T_A$</td>
<td>–40°C – 105°C</td>
<td>–55°C – 105°C</td>
</tr>
</tbody>
</table>

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see Section 7.5.

(2) The voltage on this pin must not exceed the voltage on the $V_{IN}$ pin by more than 0.3 V.

(3) The recommended maximum output voltage varies depending input voltage.

7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC (1)</th>
<th>TPSM5601R5Hx</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RDA (QFN)</td>
</tr>
<tr>
<td>--------------------</td>
<td>--------------</td>
</tr>
<tr>
<td>$R_{JA}$</td>
<td>Junction-to-ambient thermal resistance (2)</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>$\psi_{JT}$</td>
<td>Junction-to-top characterization parameter (3)</td>
</tr>
<tr>
<td>$\psi_{JB}$</td>
<td>Junction-to-board characterization parameter (4)</td>
</tr>
<tr>
<td>$T_{SHDN}$</td>
<td>Thermal shutdown temperature</td>
</tr>
<tr>
<td>Recovery temperature</td>
<td>158 °C</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics app-note.

(2) The junction-to-ambient thermal resistance, $R_{JA}$, applies to devices soldered directly to a 6.35 cm x 8.25 cm, four-layer PCB with 2-oz. copper. Additional airflow and PCB copper area reduces $R_{JA}$. See Section 11.2.1 for more information.

(3) The junction-to-top board characterization parameter, $\psi_{JT}$, estimates the junction temperature, $T_J$, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JT} \times P_{dis} + T_T$; where $P_{dis}$ is the power dissipated in the device and $T_T$ is the temperature of the top of the device.

(4) The junction-to-board characterization parameter, $\psi_{JB}$, estimates the junction temperature, $T_J$, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} \times P_{dis} + T_B$; where $P_{dis}$ is the power dissipated in the device and $T_B$ is the temperature of the board 1mm from the device.
7.5 Electrical Characteristics

Limits apply over $T_A = -40^\circ C$ to $+105^\circ C$ (EXT suffix device; $T_A = -55^\circ C$ to $+105^\circ C$), $V_{IN} = 24\ V$, $V_{OUT} = 3.3\ V$, $I_{OUT} = 1.5\ A$, (unless otherwise noted); Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>Input voltage range</td>
<td>4.2 (1)</td>
<td>60</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{SHDN}$</td>
<td>Shutdown supply current</td>
<td>V$<em>{EN} = 0\ V$, $I</em>{OUT} = 0\ A$</td>
<td>5</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{FB}$</td>
<td>Current into FB pin</td>
<td>0.2</td>
<td>nA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>Internal LDO output voltage appearing at the VCC pin</td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>$I_O$</td>
<td>Output current</td>
<td>$T_A = 25^\circ C$</td>
<td>0</td>
<td>1.5</td>
<td>A</td>
</tr>
<tr>
<td>$V_{HC}$</td>
<td>FB pin voltage required to trip short-circuit hiccup mode</td>
<td>0.4</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{HC}$</td>
<td>Time between current-limit hiccup burst</td>
<td>94</td>
<td>ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{EN-VCC-H}$</td>
<td>EN input level required to turn on internal LDO</td>
<td>Rising threshold</td>
<td>1.14</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{EN-VCC-L}$</td>
<td>EN input level required to turn off internal LDO</td>
<td>Falling threshold</td>
<td>0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{EN-H}$</td>
<td>EN input level required to start switching</td>
<td>Rising threshold</td>
<td>1.157</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{EN-HYS}$</td>
<td>Hysteresis below $V_{EN-H}$</td>
<td>Hysteresis below $V_{EN-H}$; falling</td>
<td>110</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$I_{LKG-EN}$</td>
<td>Enable input leakage current</td>
<td>$V_{EN} = 3.3\ V$</td>
<td>0.2</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>$V_{PG-LOW-UP}$</td>
<td>$V_{OUT}$ rising (fault)</td>
<td>% of FB voltage</td>
<td>107%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{PG-HIGH-DN}$</td>
<td>$V_{OUT}$ falling (good)</td>
<td>% of FB voltage</td>
<td>105%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{PG}$</td>
<td>Power-good flag $R_{DSON}$</td>
<td>$V_{EN} = 0\ V$</td>
<td>35</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>$V_{IN-PG}$</td>
<td>Minimum input voltage for proper PGGOOD function</td>
<td>$I_{FG} = 50\ µA$, $EN = 0\ V$</td>
<td>2</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>
7.5 Electrical Characteristics (continued)

Limits apply over TA = −40°C to +105°C (EXT suffix device; TA = −55°C to +105°C), VIN = 24 V, VOUT = 3.3 V, IOUT = 1.5 A, (unless otherwise noted); Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>PERFORMANCE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>η</td>
<td>Efficiency</td>
<td>VOUT = 3.3 V, IOUT = 0.75 A, TA = 25°C</td>
<td>81%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>η</td>
<td>Efficiency</td>
<td>VOUT = 5.0 V, IOUT = 0.75 A, TA = 25°C</td>
<td>86%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SOFT START</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tSS</td>
<td>Internal soft-start time</td>
<td>4.5</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>SWITCHING FREQUENCY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fSW</td>
<td>Switching frequency</td>
<td>IOUT = 0.75 A, TA = 25°C</td>
<td>0.85</td>
<td>1(3)</td>
<td>1.15</td>
</tr>
<tr>
<td>fSW ss</td>
<td>Switching frequency for spread spectrum device only</td>
<td>IOUT = 0.75 A, TA = 25°C</td>
<td>0.80</td>
<td>1</td>
<td>1.20</td>
</tr>
</tbody>
</table>

(1) The recommended minimum VIN is 4.2 V or (VOUT + 600 mV), whichever is greater.
(2) The overall output voltage tolerance is affected by the tolerance of the external RFBT and RFBB resistors.
(3) The typical switching frequency of this device will change based on operating conditions. See the Switching Frequency section for more information.
7.6 Typical Characteristics (VIN = 12 V)

\( T_A = 25°C \), unless otherwise noted.

---

**Figure 7-1. Efficiency**

![Efficiency Graph](image)

**Figure 7-2. Power Dissipation**

![Power Dissipation Graph](image)

**Figure 7-3. Output Voltage Ripple**

\( C_{OUT} = 2 \times 47 \mu F, 25-V, \text{ ceramic} \)

**Figure 7-4. Safe Operating Area (\( V_{OUT} = 1.2 \text{ V} \))**

Device soldered to a 63.5-mm × 82.5-mm, 4-layer PCB

**Figure 7-5. Safe Operating Area (\( V_{OUT} = 3.3 \text{ V} \))**

Device soldered to a 63.5-mm × 82.5-mm, 4-layer PCB

**Figure 7-6. Safe Operating Area (\( V_{OUT} = 5.0 \text{ V} \))**

Device soldered to a 63.5-mm × 82.5-mm, 4-layer PCB
7.7 Typical Characteristics (VIN = 24 V)

\( T_A = 25^\circ C, \) unless otherwise noted.

---

**Figure 7-7. Efficiency**

- Efficiency (%) vs. Output Current (A)
- Different output voltages (15V, 12V, 9V, 5V, 3.3V, 2.5V, 1.8V)

**Figure 7-8. Power Dissipation**

- Power Dissipation (W) vs. Output Current (A)
- Different output voltages (15V, 12V, 9V, 5V, 3.3V, 2.5V, 1.8V)

**Figure 7-9. Output Voltage Ripple**

- Output Voltage Ripple (mV) vs. Output Current (A)
- Different output voltages (15V, 12V, 9V, 5V, 3.3V, 2.5V, 1.8V)

- \( C_{OUT} = 2 \times 47\mu F, 25-V, \) ceramic

**Figure 7-10. Safe Operating Area \((V_{OUT} = 1.8 \text{ V})\)**

- Ambient Temperature (\(^\circ C\)) vs. Output Current (A)
- Different airflow rates (400LFM, 200LFM, 100LFM, Nat conv)

- Device soldered to a 63.5-mm × 82.5-mm, 4-layer PCB

**Figure 7-11. Safe Operating Area \((V_{OUT} = 5.0 \text{ V})\)**

- Ambient Temperature (\(^\circ C\)) vs. Output Current (A)
- Different airflow rates (400LFM, 200LFM, 100LFM, Nat conv)

- Device soldered to a 63.5-mm × 82.5-mm, 4-layer PCB

**Figure 7-12. Safe Operating Area \((V_{OUT} = 12 \text{ V})\)**

- Ambient Temperature (\(^\circ C\)) vs. Output Current (A)
- Different airflow rates (400LFM, 200LFM, 100LFM, Nat conv)

- Device soldered to a 63.5-mm × 82.5-mm, 4-layer PCB
7.8 Typical Characteristics (VIN = 48 V)

\[ T_A = 25°C, \text{ unless otherwise noted.} \]
7.9 Typical Characteristics (VIN = 60 V)

$T_A = 25^\circ \text{C}$, unless otherwise noted.

![Efficiency](image1)

$V_{OUT}$
- 15 V
- 12 V
- 9 V
- 5 V
- 3.3 V

![Power Dissipation](image2)

$V_{OUT}$
- 15 V
- 12 V
- 9 V
- 5 V
- 3.3 V

$C_{OUT} = 2 \times 47$-$\mu$F, 25-V, ceramic

![Output Voltage Ripple](image3)

$V_{OUT}$
- 15 V
- 12 V
- 9 V
- 5 V
- 3.3 V

Device soldered to a 63.5-mm × 82.5-mm, 4-layer PCB

![Safe Operating Area (V$_{OUT}$ = 5.0 V)](image4)

Device soldered to a 63.5-mm × 82.5-mm, 4-layer PCB

![Safe Operating Area (V$_{OUT}$ = 12 V)](image5)

Device soldered to a 63.5-mm × 82.5-mm, 4-layer PCB

![Safe Operating Area (V$_{OUT}$ = 15 V)](image6)
8 Detailed Description

8.1 Overview

The TPSM5601R5Hx converter is an easy-to-use, synchronous buck, DC-DC power module that operates from a 4.2-V to 60-V supply voltage. The device is intended for step-down conversions from 5-V, 12-V, 24-V, and 48-V unregulated, semi-regulated, or fully-regulated supply rails. With an integrated power controller, inductor, and MOSFETs, the TPSM5601R5Hx delivers up to 1.5-A DC load current, with high efficiency and ultra-low input quiescent current, in a very small solution size. Although designed for simple implementation, this device offers flexibility to optimize its usage according to the target application. Control-loop compensation is not required, reducing design time and external component count.

The TPSM5601R5Hx incorporates several features for comprehensive system requirements, including the following:

- Open-drain Power Good circuit for power-rail sequencing and fault reporting
- Monotonic start-up into prebiased loads
- Precision enable with customizable hysteresis for programmable line undervoltage lockout (UVLO)
- Overcurrent and thermal shutdown with automatic recovery

Additionally, the TPSM5601R5HxS offers frequency spread-spectrum operation. These features enable a flexible and easy-to-use platform for a wide range of applications. The pin arrangement is designed for simple PCB layout, requiring as few as four external components.

8.2 Functional Block Diagram
8.3 Feature Description

8.3.1 Adjustable Output Voltage (FB)

The TPSM5601R5Hx has an adjustable output voltage range of 1.0 V to 16 V. Setting the output voltage requires two resistors, \( R_{FBT} \) and \( R_{FBB} \) (see Figure 8-1). Connect \( R_{FBT} \) between VOUT, at the regulation point, and the FB pin. Connect \( R_{FBB} \) between the FB pin and AGND (pin 10). The recommended value of \( R_{FBT} \) is 10 kΩ. The value for \( R_{FBB} \) can be calculated using Equation 1.

\[
R_{FBB} = \frac{1.0}{V_{OUT} - 1.0} \times R_{FBT}
\]

(1)

![Figure 8-1. FB Resistor Divider](image)

Table 8-1. Standard \( R_{FBB} \) Values

<table>
<thead>
<tr>
<th>VOUT (V)</th>
<th>( R_{FBB} ) (kΩ) (^{(1)})</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>open</td>
</tr>
<tr>
<td>1.2</td>
<td>49.9</td>
</tr>
<tr>
<td>1.5</td>
<td>20.0</td>
</tr>
<tr>
<td>1.8</td>
<td>12.4</td>
</tr>
<tr>
<td>2.0</td>
<td>10.0</td>
</tr>
<tr>
<td>2.5</td>
<td>6.65</td>
</tr>
<tr>
<td>3.0</td>
<td>4.99</td>
</tr>
<tr>
<td>3.3</td>
<td>10.0</td>
</tr>
<tr>
<td>5.0</td>
<td>12.4</td>
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<td>7.5</td>
<td>10.0</td>
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<td>12</td>
</tr>
<tr>
<td>15</td>
<td>6.65</td>
</tr>
<tr>
<td>16</td>
<td>4.99</td>
</tr>
</tbody>
</table>

(1) \( R_{FBT} = 10 \text{ kΩ} \)

Selecting an \( R_{FBT} \) value of 10 kΩ is recommended for most applications. A larger \( R_{FBT} \) consumes less DC current, which is mandatory if light-load efficiency is critical. However, \( R_{FBT} \) larger than 1 MΩ is not recommended as the feedback path becomes more susceptible to noise. High feedback resistance generally requires more careful layout of the feedback path. It is important to keep the feedback trace as short as possible while keeping the feedback trace away from the noisy area of the PCB. For more layout recommendations, see Section 11.
8.3.2 Minimum Input Capacitance

The TPSM5601R5Hx requires a minimum input capacitance of 9.4 μF (2 × 4.7 μF) of ceramic type. High-quality, ceramic-type X5R or X7R capacitors with sufficient voltage rating are required. Place the input capacitors, as close as possible to both VIN pins of the device, between VIN and PGND as shown in Section 11.1. Applications with transient load requirements can benefit from adding additional bulk capacitance to the input as well.

8.3.3 Minimum Output Capacitance

The TPSM5601R5Hx requires a minimum amount of ceramic output capacitance depending on the output voltage setting. The amount of required output capacitance is shown in Figure 8-2 and is the amount of effective capacitance. The effects of DC bias and temperature variation must be considered when using ceramic capacitance. For ceramic capacitors, the package size, voltage rating, and dielectric material contributes to differences between the standard rated value and the actual effective value of the capacitance. When adding additional capacitance above the minimum, the capacitance can be ceramic type, low-ESR polymer type, or a combination of the two.

![Figure 8-2. Minimum Required Output Capacitance](image-url)
8.3.4 Precision Enable (EN), Undervoltage Lockout (UVLO), and Hysteresis (HYS)

The EN pin provides precision ON and OFF control for the TPSM5601R5Hx. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. The simplest way to enable the device is to connect EN directly to VIN. This allows the device to start up when \( V_{\text{IN}} \) is within its valid operating range. An external logic signal can also be used to drive the EN input to toggle the output on and off and for system sequencing or protection. **This input must not be allowed to float.**

The TPSM5601R5Hx implements internal undervoltage lockout (UVLO) circuitry on the VIN pin. The device is disabled when the VIN pin voltage is below the internal VIN UVLO threshold. The internal VIN UVLO rising threshold is 3.8 V (typical) with a typical hysteresis of 500 mV.

If an application requires a higher UVLO threshold, the EN input supports adjustable UVLO by connecting a resistor divider from VIN to the EN pin. Applying a voltage of \( \geq 1.14 \) V causes the device to enter standby mode, powering the internal LDO, but not producing an output voltage. Increasing the EN voltage to 1.231 V (typ.) fully enables the device, allowing it to enter start-up mode and starting the soft-start period. When the EN input is brought below 1.121 V (110 mV hysteresis), the regulator stops running and enters standby mode. Further decrease in the EN voltage to below 0.3 V completely shuts down the device.

The TPSM5601R5Hx utilizes a reference-based soft start that prevents output voltage overshoots and large inrush currents as the regulator is starting up. The rise time of the output voltage is about 4 ms.

8.3.5 Power Good (PGOOD)

The TPSM5601R5Hx provides a PGOOD signal to indicate when the output voltage is within regulation. Use the PGOOD signal for output monitoring, fault protection, or start-up sequencing of downstream converters. PGOOD is an open-drain output that requires a pullup resistor to a DC supply not greater than 18 V. V5V or VOUT can be used as the pullup voltage source. Typical range of pullup resistance is 10 kΩ to 100 kΩ. If necessary, use a resistor divider to decrease the voltage from a higher voltage pullup rail. If this function is not needed, the PGOOD pin must be grounded.

When the output voltage exceeds 95% (rising) or decreases below 105% (falling) of the setpoint, the internal PGOOD switch turns off and PGOOD can be pulled high by the external pullup. If the FB voltage falls below 93% or rises above 107% of the setpoint, the internal PGOOD switch turns on, and PGOOD is pulled low to indicate that the output voltage is out of regulation.

Note that during initial power up, a delay of about 4 ms (typical) is inserted from the time that EN is asserted to the time that the power-good flag goes high. This delay only occurs during start-up and is not encountered during normal operation of the power-good function.

8.3.6 Spread Spectrum Operation

Spread spectrum is a factory option in the TPSM5601R5HS variant. The purpose of the spread spectrum is to eliminate peak emissions at specific frequencies by spreading emissions across a wider range of frequencies than a part with fixed frequency operation. In most systems, low frequency conducted emissions from the first few harmonics of the switching frequency can be easily filtered. A more difficult design criterion is reduction of emissions at higher harmonics which fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node. The TPSM5601R5HS device with triangular spread spectrum uses a ±4% spreading rate (typical) with the modulation rate set at 16 kHz (typical). The spread spectrum is only available while the internal clock is free running at its natural frequency. Any of the following conditions override spread spectrum, turning it off:

- At high input voltages/low output voltage ratio when the device operates at minimum on time the internal clock is slowed disabling spread spectrum.
- The clock is slowed during dropout.

8.3.7 Overcurrent Protection (OCP)

The TPSM5601R5Hx is protected from overcurrent conditions using cycle-by-cycle current limiting for overload conditions and hiccup mode for short circuits. The current is compared every switching cycle to the current limit threshold. During an overcurrent condition, the output voltage decreases.
8.3.8 Thermal Shutdown
Thermal shutdown is an integrated self-protection used to limit junction temperature and prevent damage related to overheating. Thermal shutdown turns off the device when the junction temperature exceeds 170°C (typ.) to prevent further power dissipation and temperature rise. Junction temperature decreases after shutdown, and the TPSM5601R5Hx restarts when the junction temperature falls to 158°C (typ.).

8.4 Device Functional Modes

8.4.1 Active Mode
The TPSM5601R5Hx is in active mode when VIN is above the turn-on threshold and the EN pin voltage is above the EN high threshold. Connect the EN pin to VIN to allow the device to start up when a valid input voltage is applied. This allows self start-up of the TPSM5601R5Hx when the input voltage is in the operation range of 4.2 V to 60 V. Connecting a resistor divider between VIN, EN, and AGND adjusts the UVLO to delay the turn on until VIN is closer to its regulated voltage.

8.4.2 Standby Mode
Start-up and shutdown are controlled by the EN input. This input features precision thresholds, allowing the use of an external voltage divider to provide an adjustable input UVLO. Applying a voltage of ≥ 1.14 causes the device to enter standby mode, powering the internal LDO, but not producing an output voltage. Increasing the EN voltage to 1.231 V (typ.) fully enables the device, allowing it to enter start-up mode and starting the soft-start period. When the EN input is brought below 1.121 V (110-mV hysteresis), the regulator stops running and enters standby mode. Further decrease in the EN voltage to below 0.3 V completely shuts down the device.

8.4.3 Shutdown Mode
The EN pin provides ON and OFF control for the TPSM5601R5Hx. When \( V_{EN} \) is below the EN low threshold, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 5 µA at \( V_{IN} = 24 \) V.
9 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPSM5601R5Hx only requires a few external components to convert from a wide range of supply voltages to a fixed output voltage. To expedite and streamline the process of designing a TPSM5601R5Hx, WEBENCH® online software is available to generate complete designs, leveraging iterative design procedures and access to comprehensive component databases. The following section describes the design procedure to configure the TPSM5601R5Hx power module.

As mentioned previously, the TPSM5601R5Hx also integrates several optional features to meet system design requirements, including precision enable, UVLO, and PGOOD indicator. The application circuit detailed below shows TPSM5601R5Hx configuration options suitable for several application use cases. Refer to the TPSM5601R5HxEVM user's guide for more detail.

9.2 Typical Application

Figure 9-1 shows the schematic diagram of a 24-V input, 5-V output, 1.5-A converter.

![Figure 9-1. TPSM5601R5Hx Typical Schematic](image)

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 9-1 as the input parameters and follow the design procedures in Section 9.2.2.

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage $V_{\text{IN}}$</td>
<td>24 V typical</td>
</tr>
<tr>
<td>Output voltage $V_{\text{OUT}}$</td>
<td>5 V</td>
</tr>
<tr>
<td>Output current rating</td>
<td>1.5 A</td>
</tr>
</tbody>
</table>

Table 9-1. Design Example Parameters
9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM5601R5Hx device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Output Voltage Setpoint

The output voltage of the TPSM5601R5Hx device is externally adjustable using a resistor divider. The recommended value of $R_{FBT}$ is $10 \, \text{k}\Omega$. The value for $R_{FBB}$ can be selected from Table 8-1 or calculated using Equation 2:

$$R_{FBB} = \frac{V_{OUT} \times 1.0}{1.0 - V_{OUT}} \times R_{FBT}$$

(2)

For the desired output voltage of 5 V, the formula yields a value of 2.5 kΩ. Choose the closest available standard value of 2.49 kΩ for $R_{FBB}$.

9.2.2.3 Input Capacitors

The TPSM5601R5Hx requires a minimum input capacitance of $2 \times 4.7\,-\mu\text{F}$ ceramic type. High-quality ceramic type X5R or X7R capacitors with sufficient voltage rating are recommended. The voltage rating of input capacitors must be greater than the maximum input voltage.

For this design, $2 \times 4.7\,-\mu\text{F}$, 100-V ceramic capacitors are selected.

9.2.2.4 Output Capacitor Selection

The TPSM5601R5Hx requires a minimum amount of output capacitance for proper operation. The minimum amount of required output varies depending on the output voltage. See Figure 8-2 for the required output capacitance. Additional output capacitance can be added to reduce ripple voltage or for applications with transient load requirements.

For this design example, $2 \times 47\,-\mu\text{F}$, 10-V, ceramic capacitors are used.

9.2.2.5 Power Good Signal

Applications requiring a power good signal to indicate that the output voltage is present and in regulation must use a pullup resistor between the PGOOD pin and a valid voltage source.

For this design a 100-kΩ resistor is placed between the PGOOD pin and the V5V pin (the internal 5-V LDO output).
9.2.3 Application Curves

![Voltage Waveforms](image1.png)

**Figure 9-2. Start-up Waveforms**

![Voltage Waveforms](image2.png)

**Figure 9-3. Enable Shutdown Waveforms**

![Voltage Waveforms](image3.png)

**Figure 9-4. Output Ripple Waveform**

![Voltage Waveforms](image4.png)

**Figure 9-5. Transient Response Waveform**

10 Power Supply Recommendations

The TPSM5601R5Hx is designed to operate from an input voltage supply range between 4.2 V and 60 V. This input supply must be able to provide the maximum input current and maintain a voltage above the set UVLO voltage. Ensure that the resistance of the input supply rail is low enough that an input current transient does not cause a high enough drop at the TPSM5601R5Hx supply rail to cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the TPSM5601R5Hx, additional bulk capacitance can be required in addition to the ceramic input capacitance. A 47-μF electrolytic capacitor is a typical choice for this function, whereby the capacitor ESR provides a level of damping against input filter resonances. A typical ESR of 0.5 Ω provides enough damping for most input circuit configurations.
11 Layout
The performance of any switching power supply depends as much upon the layout of the PCB as the component selection. Use the following guidelines to design a PCB with the best power conversion performance, optimal thermal performance, and minimal generation of unwanted EMI.

11.1 Layout Guidelines
To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Figure 11-1 and Figure 11-2 show a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- **Connect all PGND pins together using copper plane.**
- Connect AGND pin to the PGND copper at a single point near the pin.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Place R_FB and R_FBB as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.

11.2 Layout Example

![Figure 11-1. Typical Layout](image1)

![Figure 11-2. Typical Top-Layer](image2)

![Figure 11-3. Typical Mid-Layer](image3)

![Figure 11-4. Typical PGND-Layer](image4)
11.2.1 Theta JA versus PCB Area

The amount of PCB copper as well as airflow effects the thermal performance of the device. Figure 11-5 shows the effects of copper area and airflow on the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the TPSM5601R5Hx. The junction-to-ambient thermal resistance versus PCB area is plotted for a 4-layer PCB.

To determine the required copper area for an application:
1. Determine the maximum power dissipation of the device in the application by referencing the power dissipation graphs in the Typical Characteristics.
2. Calculate the maximum $\theta_{JA}$ using Equation 3 and the maximum ambient temperature of the application.

$$\theta_{JA} = \left(125°C - T_{A(max)}\right) \left(1\text{°C/W}\right)$$

3. Reference Figure 11-5 to determine the minimum required PCB area for the application conditions.

![Figure 11-5. $\theta_{JA}$ vs PCB Area](image)

11.2.2 Package Specifications

<table>
<thead>
<tr>
<th>Table 11-1. Package Specifications Table</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>TPSM5601R5H</strong></td>
</tr>
<tr>
<td>Weight</td>
</tr>
<tr>
<td>Flammability</td>
</tr>
<tr>
<td>MTBF Calculated Reliability</td>
</tr>
</tbody>
</table>
11.2.3 EMI

The TPSM5601R5H is compliant with EN55011 radiated emissions. Figure 11-6 through Figure 11-9 show typical examples of radiated emission plots for the TPSM5601R5H. The graphs include the plots of the antenna in the horizontal and vertical positions.

11.2.3.1 EMI Plots

EMI plots were measured using the standard TPSM5601R5HEVM.

**Figure 11-6. Radiated Emissions 24-V Input, 5-V Output, 1.5-A Load**

**Figure 11-7. Radiated Emissions 24-V Input, 5-V Output, 1.5-A Load (Spread spectrum)**
Figure 11-8. Radiated Emissions 24-V Input, 12-V Output, 1.5-A Load

Figure 11-9. Radiated Emissions 48-V Input, 12-V Output, 1.5-A Load
12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.1.2 Development Support

For development support, see the following:

- For TI's reference design library, visit Ti Designs.
- To view a related device of this product, see the TPSM5601R5Hx.

12.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM5601R5H device with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

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In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, TPSM5601R5HxEVM User's Guide
- Texas Instruments, Using the TPSM5601R5Hx in an Inverting Buck-Boost Topology Application Report
- Texas Instruments, Using New Thermal Metrics Application Report
- Texas Instruments, Semiconductor and IC Package Thermal Metrics Application Report

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Trademarks

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**12.6 Electrostatic Discharge Caution**

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**12.7 Glossary**

**TI Glossary**  
This glossary lists and explains terms, acronyms, and definitions.

**13 Mechanical, Packaging, and Orderable Information**

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.
### PACKAGING INFORMATION

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<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PIns</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/ Ball material (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
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<td>B3QFN</td>
<td>RDA</td>
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<td>1000</td>
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<td>NIPDAU</td>
<td>Level-3-245C-168 HR</td>
<td>-55 to 125</td>
<td>5601R5HEXT</td>
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<td>Level-3-245C-168 HR</td>
<td>-40 to 125</td>
<td>5601R5HS</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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### TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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<tbody>
<tr>
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<td>B3QFN</td>
<td>RDA</td>
<td>15</td>
<td>1000</td>
<td>330.0</td>
<td>16.4</td>
<td>5.28</td>
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<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
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<td>330.0</td>
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**TAPE AND REEL BOX DIMENSIONS**

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<th>Package Drawing</th>
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<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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</thead>
<tbody>
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<td>RDA</td>
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<td>1000</td>
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<td>48.0</td>
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<td>RDA</td>
<td>15</td>
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<tr>
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<td>336.0</td>
<td>336.0</td>
<td>48.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
EXAMPLE BOARD LAYOUT

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
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