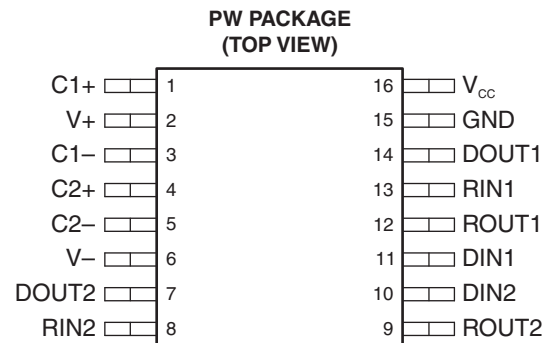


3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH ±15-kV IEC ESD PROTECTION

FEATURES

- Qualified for Automotive Applications
- ESD Protection for RS-232 Bus Pins
 - ±15-kV Human Body Model (HBM)
 - ±8 kV (IEC61000-4-2, Contact Discharge)
 - ±15 kV (IEC61000-4-2, Air-Gap Discharge)
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates With 3-V to 5.5-V V_{CC} Supply
- Operates up to 250 kbit/s
- Two Drivers and Two Receivers
- Low Supply Current: 300 μ A (Typ)
- External Capacitors: 4 \times 0.1 μ F
- Accepts 5-V Logic Input With 3.3-V Supply
- Pin Compatible to Alternative High-Speed Device (1 Mbit/s): TRSF3232E



DESCRIPTION

The TRS3232E device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV IEC ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 250 kbit/s and a maximum of 30-V/ μ s driver output slew rate.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	TSSOP – PW	Reel of 2000	TRS3232EQPWRQ1	RS32EQ

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTION TABLES

Each Driver⁽¹⁾

INPUT DIN	OUTPUT DOUT
L	H
H	L

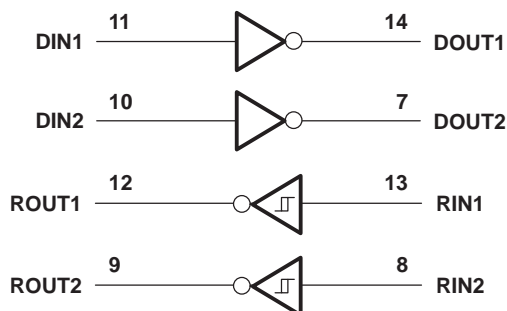
(1) H = high level, L = low level

Each Receiver⁽¹⁾

INPUT RIN	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level, Open = input disconnected or connected driver off

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage range ⁽²⁾		–0.3 V to 6 V
$V+$	Positive output supply voltage range ⁽²⁾		–0.3 V to 7 V
$V-$	Negative output supply voltage range ⁽²⁾		0.3 V to –7 V
$V+ - V-$	Supply voltage difference ⁽²⁾		13 V
V_I	Input voltage range	Drivers	–0.3 V to 6 V
		Receivers	–25 V to 25 V
V_O	Output voltage range	Drivers	–13.2 V to 13.2 V
		Receivers	–0.3 V to $V_{CC} + 0.3$ V
θ_{JA}	Package thermal impedance ⁽³⁾⁽⁴⁾		108°C/W
T_J	Operating virtual-junction temperature		150°C
T_{stg}	Storage temperature range		–65°C to 150°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.
- (3) Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

See [Figure 4](#)

		MIN	NOM	MAX	UNIT	
V_{CC}	Supply voltage	$V_{CC} = 3.3$ V	3	3.3	3.6	V
		$V_{CC} = 5$ V	4.5	5	5.5	
V_{IH}	Driver high-level input voltage, DIN	$V_{CC} = 3.3$ V	2		5.5	V
		$V_{CC} = 5$ V	2.4		5.5	
V_{IL}	Driver low-level input voltage, DIN	0		0.8	V	
V_I	Receiver input voltage	–25		25	V	
T_A	Operating free-air temperature	–40		125	°C	

- (1) Test conditions are C1–C4 = 0.1 μF at $V_{CC} = 3.3$ V \pm 0.3 V; C1 = 0.047 μF , C2–C4 = 0.33 μF at $V_{CC} = 5$ V \pm 0.5 V.

ELECTRICAL CHARACTERISTICS⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 4](#))

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT	
I_{CC}	Supply current	No load, $V_{CC} = 3.3$ V or 5 V		0.3	1	mA

- (1) Test conditions are C1–C4 = 0.1 μF at $V_{CC} = 3.3$ V \pm 0.3 V; C1 = 0.047 μF , C2–C4 = 0.33 μF at $V_{CC} = 5$ V \pm 0.5 V.
- (2) All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25^\circ\text{C}$.

DRIVER SECTION

ELECTRICAL CHARACTERISTICS⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 4](#))

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	DOUT at R _L = 3 kΩ to GND, DIN = GND	5	5.4		V
V _{OL}	Low-level output voltage	DOUT at R _L = 3 kΩ to GND, DIN = V _{CC}	–5	–5.4		V
I _{IH}	High-level input current	V _I = V _{CC}		±0.01	±1	μA
I _{IL}	Low-level input current	V _I at GND		±0.01	±1	μA
I _{OS} ⁽³⁾	Short-circuit output current	V _{CC} = 3.6 V, V _O = 0 V		±35	±60	mA
		V _{CC} = 5.5 V, V _O = 0 V		±35	±60	
r _o	Output resistance	V _{CC} , V+, and V– = 0 V, V _O = ±2 V	300	10M		Ω

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 4](#))

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT	
	Maximum data rate	C _L = 1000 pF, R _L = 3 kΩ, One DOOUT switching, See Figure 1	150	250		kbit/s	
t _{sk(p)}	Pulse skew ⁽³⁾	C _L = 150 pF to 2500 pF, R _L = 3 kΩ to 7 kΩ, See Figure 2		300		ns	
SR(tr)	Slew rate, transition region (see Figure 1)	R _L = 3 kΩ to 7 kΩ, V _{CC} = 3.3 V	C _L = 150 pF to 1000 pF		6	30	V/μs
			C _L = 150 pF to 2500 pF		4	30	

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

ESD PROTECTION

		TYP	UNIT
Driver outputs (DOOUTx)	Human-Body Model (HBM)	±15	kV
	IEC61000-4-2, Air-Gap Discharge	±15	
	IEC61000-4-2, Contact Discharge	±8	

RECEIVER SECTION

ELECTRICAL CHARACTERISTICS⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 4](#))

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = –1 mA	V _{CC} – 0.6	V _{CC} – 0.1		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.5	2.4	V
		V _{CC} = 5 V		1.8	2.4	
V _{IT–}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.2		V
		V _{CC} = 5 V	0.8	1.5		
V _{hys}	Input hysteresis (V _{IT+} – V _{IT–})			0.3		V
r _i	Input resistance	V _I = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

SWITCHING CHARACTERISTICS⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 3](#))

PARAMETER		TEST CONDITIONS	TYP ⁽²⁾	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF	300	ns
t _{PHL}	Propagation delay time, high- to low-level output		300	ns
t _{sk(p)}	Pulse skew ⁽³⁾		300	ns

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

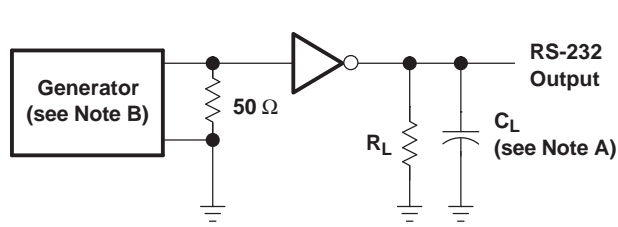
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

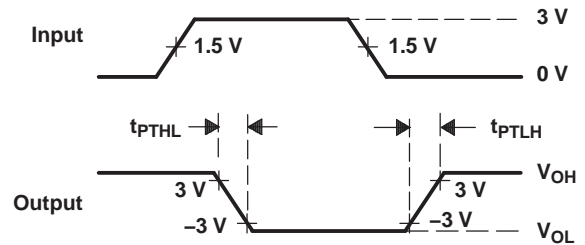
ESD PROTECTION

		TYP	UNIT
Receiver inputs (RINx)	Human-Body Model (HBM)	±15	kV
	IEC61000-4-2, Air-Gap Discharge	±15	
	IEC61000-4-2, Contact Discharge	±8	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

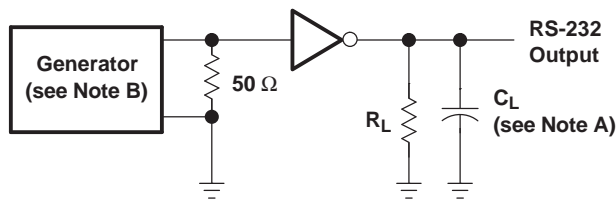


VOLTAGE WAVEFORMS

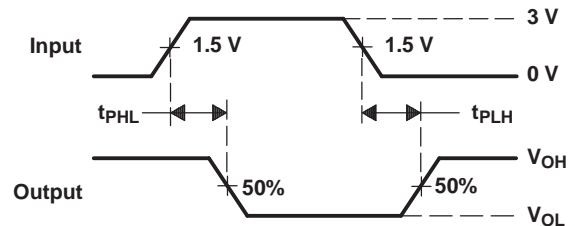
$$SR(tr) = \frac{6\text{ V}}{t_{PTHL} \text{ or } t_{PTLH}}$$

- NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 1. Driver Slew Rate



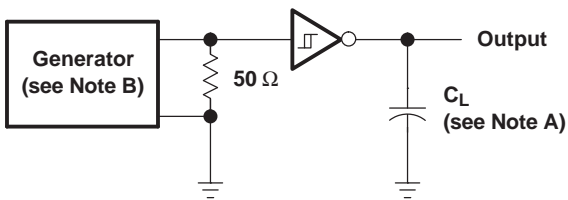
TEST CIRCUIT



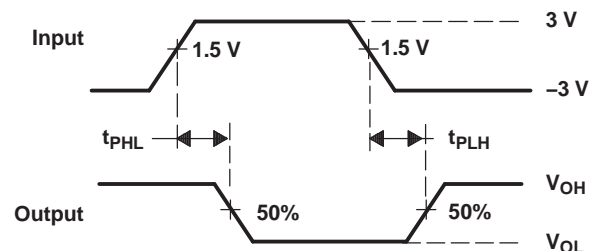
VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 2. Driver Pulse Skew



TEST CIRCUIT

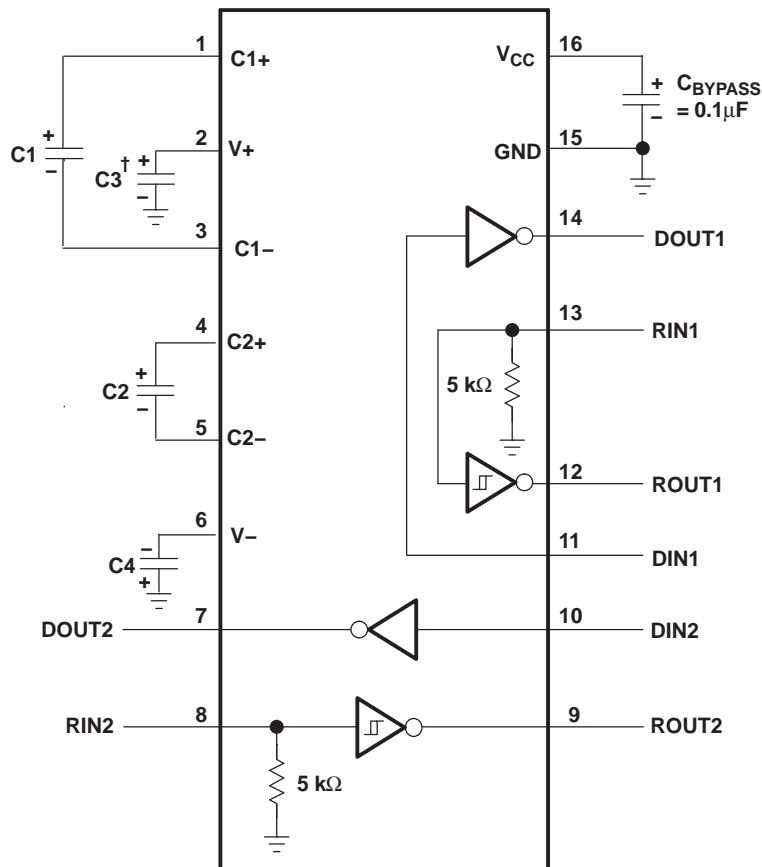


VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 3. Receiver Propagation Delay Times

APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V _{CC}	C1	C2, C3, C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

Figure 4. Typical Operating Circuit and Capacitor Values

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS3232EQPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RS32EQ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TRS3232E-Q1 :

- Catalog: [TRS3232E](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3232EQPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3232EQPWRQ1	TSSOP	PW	16	2000	853.0	449.0	35.0



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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