

TRSF3221E 3V to 5.5V Single-Channel RS-232 1Mbit Line Driver and Receiver With $\pm 15\text{kV}$ IEC ESD Protection in Small Package

1 Features

- ESD protection for RS-232 pins
 - $\pm 15\text{kV}$ Human-body model (HBM)
 - $\pm 8\text{kV}$ IEC 61000-4-2 Contact discharge
 - $\pm 15\text{kV}$ IEC 61000-4-2 Air-gap discharge
- Operates with 3V to 5.5V V_{CC} supply
- Operates up to 1Mbit/s
 - Low-speed pin-compatible device (250kbit/s) – TRSF3221E
- Available in near chip-scale package, 16-pin VQFN (RGT, 82% smaller than TSSOP package)
- Low standby current: $1\mu\text{A}$ typical
- External capacitors : $4 \times 0.1\mu\text{F}$
- Accepts 5V logic input with 3.3V supply
- Auto-powerdown feature automatically disables drivers for power savings

2 Applications

- [Industrial PCs](#)
- [Wired networking](#)
- [Data center and enterprise computing](#)
- [Battery-powered systems](#)
- [PDAs](#)
- [Notebooks](#)
- [Laptops](#)
- [Palmtop PCs](#)
- [Hand-held equipment](#)

3 Description

The TRSF3221E consists of one line driver, one line receiver, and a dual charge-pump circuit with $\pm 15\text{kV}$ IEC ESD protection pin to pin (serial-port connection pins, including GND). The TRSF3221E provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3V to 5.5V supply. The TRSF3221E operates at data signaling rates up to 1Mbit/s and a driver output slew rate of $24\text{V}/\mu\text{s}$ to $150\text{V}/\mu\text{s}$.

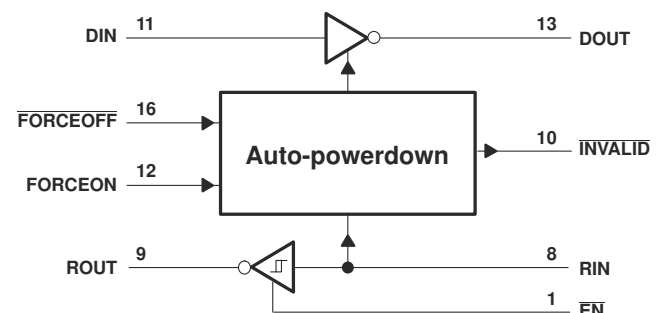
Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the TRSF3221E does not sense a valid RS-232 signal on the receiver input, the driver output is disabled. If FORCEOFF is set low and the enable ($\overline{\text{EN}}$) input is high, both the driver and receiver are shut off, and the supply current is reduced to $1\mu\text{A}$. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur. Auto-powerdown can be disabled when FORCEON and FORCEOFF are high. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to the receiver input. The INVALID output notifies the user if an RS-232 signal is present at the receiver input. INVALID is high (valid data) if the receiver input voltage is greater than 2.7V or less than -2.7V , or has been between -0.3V and 0.3V for less than $30\mu\text{s}$. INVALID is low (invalid data) if the receiver input voltage is between -0.3V and 0.3V for more than $30\mu\text{s}$. See Figure 6-5 for receiver input levels.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TRSF3221E	DB (SSOP)	6.2mm x 5.3mm
	PW (TSSOP)	5mm x 4.4mm
	RGT (VQFN)	3mm x 3mm
	SOT-23-THN (DYY, 16)	4.2mm x 2mm

(1) For more information, see Section 11.

(2) The package size (length x width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

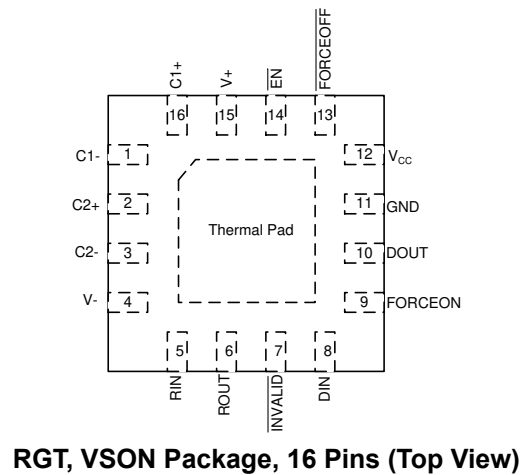
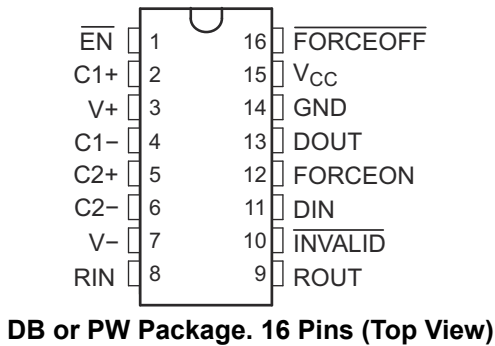
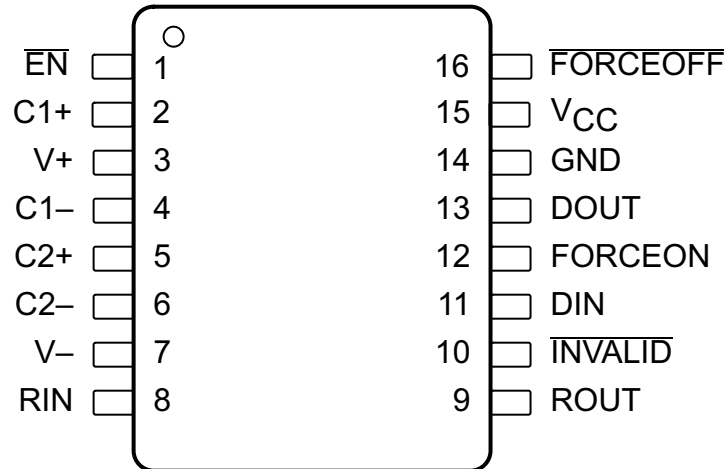


Table 4-1. Pin Functions

NAME	PIN		TYPE ⁽¹⁾	DESCRIPTION
	DB or PW	RGT		
$\overline{\text{EN}}$	1	14	--	Low input enables receiver ROUT output. High input sets ROUT to high impedance.
C1+	2	16	-	Positive lead of C1 capacitor
V+	3	15	O	Positive charge pump output for storage capacitor only
C1-	4	1	-	Negative lead of C1 capacitor
C2+	5	2	-	Positive lead of C2 capacitor
C2-	6	3	-	Negative lead of C2 capacitor
V-	7	4	O	Negative charge pump output for storage capacitor only
RIN	8	5	I	RS232 line data input (from remote RS232 system)
ROUT	9	6	O	Logic data output (to UART)
INVALID	10	7		Invalid output pin. Output low when RIN input is unpowered.
DIN	11	8	I	Logic data input (from UART)
FORCEON	12	9		Automatic power-down control input
DOUT	13	10	O	RS232 line data output (to remote RS232 system)
GRD	14	11	-	Ground
V _{CC}	15	12	-	Supply Voltage, Connect to external 3V to 5.5V power supply
FORCEOFF	16	13		Automatic power-down control input
Thermal Pad	-	Yes	-	Exposed thermal pad. Can be connected to GND or left floating.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.



Not to scale

**Figure 4-1. DYY Package
16-Pin SOT-23-THN
(Top View)**

Table 4-2. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN	1	I	Low input enables receiver ROUT output. High input sets ROUT to high impedance.
C1+	2	—	Positive terminals of the voltage-doubler charge pump capacitors
V+	3	O	5.5V supply generated by the charge pump
C1-	4	—	Negative terminals of the voltage-doubler charge pump capacitors
C2+	5	—	Positive terminals of the voltage-doubler charge pump capacitors
C2-	6	—	Negative terminals of the voltage-doubler charge pump capacitors
V-	7	O	-5.5V supply generated by the charge pump
RIN	8	I	RS-232 receiver input
ROUT	9	O	Receiver output
INVALID	10	O	Invalid output pin. Output low when RIN input is unpowered.
DIN	11	I	Driver input
FORCEON	12	I	Automatic power-down control input
DOUT	13	O	RS-232 driver output
GND	14	—	Ground
V _{CC}	15	—	3V to 5.5V supply voltage
FORCEOFF	16	I	Automatic power-down control input

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) See ⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage range ⁽²⁾	-0.3	6	V	
V+	Positive output supply voltage range ⁽²⁾	-0.3	7	V	
V-	Negative output supply voltage range ⁽²⁾	0.3	-7	V	
V+ - V-	Supply voltage difference ⁽²⁾		13	V	
V _I	Input voltage range	Driver (FORCEOFF, FORCEON, EN)	-0.3	6	V
		Receiver	-25	25	
V _O	Output voltage range	Driver	-13.2	13.2	V
		Receiver (INVALID)	-0.3	V _{CC} + 0.3	
T _J	Operating virtual junction temperature		150	°C	
T _{stg}	Storage temperature range	-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

5.2 ESD Ratings

		VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings, IEC Specifications

PIN NAME	TEST CONDITIONS	VALUE	UNIT
RIN, DOUT ⁽²⁾	HBM	±15,000	V
	IEC 61000-4-2 Contact Discharge ^{(1) (2)}	±8,000	
	IEC 61000-4-2 Air-Gap Discharge ^{(1) (2)}	±15,000	

- (1) For the RGT and PW package only, a minimum of 1µF capacitor is required between VCC and GND to meet the specified IEC-ESD level.
- (2) For optimized IEC ESD performance for DYY package, the recommendation is to have series resistor (≥ 50Ω), on all logic inputs directly connected to power or ground, to minimize the transient currents going into or out of the logic pins.

5.4 Recommended Operating Conditions

See [Figure 8-1](#) and ⁽¹⁾

			MIN	NOM	MAX	UNIT
Supply voltage		V _{CC} = 3.3 V	3	3.3	3.6	V
		V _{CC} = 5 V	4.5	5	5.5	
V _{IH}	Driver and control high-level input voltage	DIN, FORCEOFF, FORCEON, EN	V _{CC} = 3.3 V	2		V
			V _{CC} = 5 V	2.4		
V _{IL}	Driver and control low-level input voltage	DIN, FORCEOFF, FORCEON, EN			0.8	V
V _I	Driver and control input voltage	DIN, FORCEOFF, FORCEON	0		5.5	V
V _I	Receiver input voltage		-25		25	V
T _A	Operating free-air temperature	TRSF3221EI	-40		85	°C
		TRSF3221EC	0		70	

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

5.5 Thermal Resistance Characteristics

THERMAL METRIC ⁽¹⁾		TRSF3221E				UNIT
		DB (SSOP)	PW (TSSOP)	RGT (VQFN)	DYY (SOT-23-THN)	
		16 Pins	16 Pins	16 Pins	16 Pins	
R _{θJA}	Junction-to-ambient thermal resistance	82	110.9	58.8	119.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	45.7	41.7	55.8	56.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	44.4	57.2	23.8	51.5	°C/W
ψ _{JT}	Junction-to-top characterization parameter	11.0	4.2	1.7	2.6	°C/W
ψ _{JB}	Junction-to-board characterization parameter	43.8	56.6	23.7	51.1	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	9	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see [Figure 8-1](#))

PARAMETER		TEST CONDITIONS ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
I _I	Input leakage current	FORCEOFF, FORCEON, EN		±0.01	±1	μA
I _{CC}	Supply current (T _A = 25°C)	Auto-powerdown disabled	No load, FORCEOFF and FORCEON at V _{CC}	0.3	1	mA
		Powered off	No load, FORCEOFF at GND	1	10	
		Auto-powerdown enabled	No load, FORCEOFF at V _{CC} , FORCEON at GND, All RIN are open or grounded	1	10	μA

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

5.7 Electrical Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see [Figure 8-1](#))

PARAMETER	TEST CONDITIONS ⁽¹⁾		MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH} High-level output voltage	DOOUT at R _L = 3 kΩ to GND, DIN = GND		5	5.4		V
V _{OL} Low-level output voltage	DOOUT at R _L = 3 kΩ to GND, DIN = V _{CC}		-5	-5.4		V
I _{IH} High-level input current	V _I = V _{CC}			±0.01	±1	μA
I _{IL} Low-level input current	V _I at GND			±0.01	±1	μA
I _{OS} Short-circuit output current ⁽³⁾	V _{CC} = 3.6 V,	V _O = 0 V		±35	±60	mA
	V _{CC} = 5.5 V,	V _O = 0 V		±35	±90	
r _o Output resistance	V _{CC} , V+, and V- = 0 V, V _O = ±2 V		300	10M		Ω
I _{off} Output leakage current	FORCEOFF = GND	V _O = ±12 V, V _{CC} = 3 V to 3.6 V			±25	μA
		V _O = ±10 V, V _{CC} = 4.5 V to 5.5 V			±25	

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Short-circuit durations must be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output can be shorted at a time.

5.8 Switching Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see [Figure 8-1](#))

PARAMETER	TEST CONDITIONS ⁽¹⁾		MIN	TYP ⁽²⁾	MAX	UNIT
Maximum data rate (see Figure 6-1)	R _L = 3 kΩ	C _L = 1000 pF		250		kbit/s
		C _L = 250 pF, V _{CC} = 3 V to 4.5 V		1000		
		C _L = 1000 pF, V _{CC} = 4.5 V to 5.5 V		1000		
t _{sk(p)} Pulse skew ⁽³⁾	C _L = 250 pF	R _L = 3 kΩ Figure 6-2 RGT Package		25		ns
	C _L = 150 pF to 2500 pF,	R _L = 3 kΩ to 7 kΩ, See Figure 6-2 DB or PW package		100		
SR(tr) Slew rate, transition region (see Figure 6-1)	V _{CC} = 3.3 V,	R _L = 3 kΩ to 7 kΩ, C _L = 150 pF to 1000 pF	18		150	V/μs

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

5.9 Electrical Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see [Figure 8-1](#))

PARAMETER		TEST CONDITIONS ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -1 mA	V _{CC} - 0.6 V	V _{CC} - 0.1 V		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.6	2.4	V
		V _{CC} = 5 V		1.9	2.4	
V _{IT-}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.1		V
		V _{CC} = 5 V	0.8	1.4		
V _{hys}	Input hysteresis (V _{IT+} - V _{IT-})			0.5		V
I _{off}	Output leakage current	FORCEOFF = 0 V		±0.05	±10	μA
r _i	Input resistance	V _i = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

5.10 Switching Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see [Figure 8-1](#))

PARAMETER		TEST CONDITIONS ⁽¹⁾		TYP ⁽²⁾	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF, See Figure 6-3	RGT package	100	ns
			DB or PW package	150	
t _{PHL}	Propagation delay time, high- to low-level output	C _L = 150 pF, See Figure 6-3	RGT package	125	ns
			DB or PW package	150	
t _{en}	Output enable time	C _L = 150 pF, R _L = 3 kΩ, See Figure 6-4		200	ns
t _{dis}	Output disable time	C _L = 150 pF, R _L = 3 kΩ, See Figure 6-4		200	ns
t _{sk(p)}	Pulse skew ⁽³⁾	See Figure 6-3	RGT package	25	ns
			DB or PW package	50	

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

5.11 Electrical Characteristics, Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6-5)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{T+}(\text{valid})$	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage FORCEON = GND, FORCEOFF = V_{CC}		2.7	V
$V_{T-}(\text{valid})$	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage FORCEON = GND, FORCEOFF = V_{CC}	-2.7		V
$V_{T}(\text{invalid})$	Receiver input threshold for $\overline{\text{INVALID}}$ low-level output voltage FORCEON = GND, FORCEOFF = V_{CC}	-0.3	0.3	V
V_{OH}	$\overline{\text{INVALID}}$ high-level output voltage $I_{OH} = -1 \text{ mA}$, FORCEON = GND, FORCEOFF = V_{CC}	$V_{CC} - 0.6$		V
V_{OL}	$\overline{\text{INVALID}}$ low-level output voltage $I_{OL} = 1.6 \text{ mA}$, FORCEON = GND, FORCEOFF = V_{CC}		0.4	V

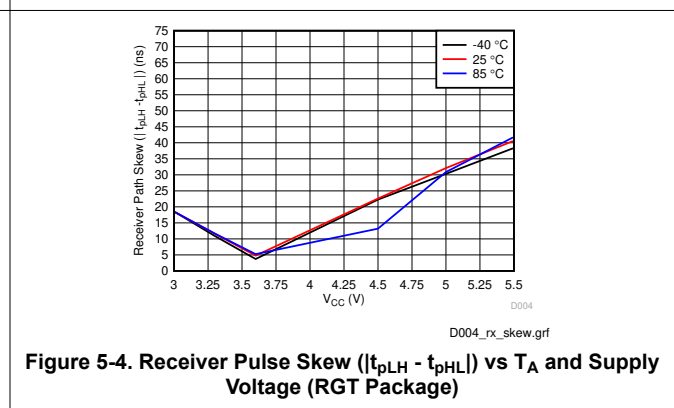
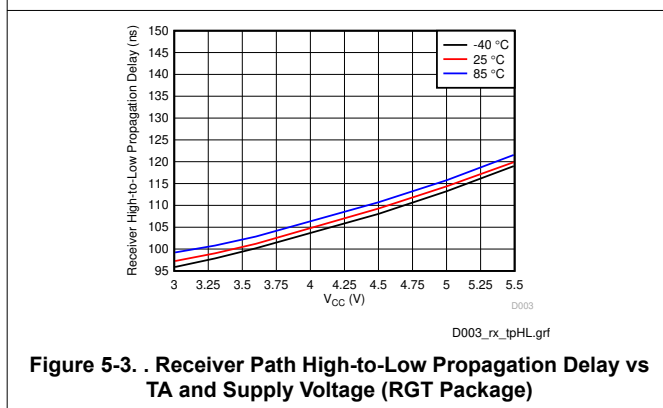
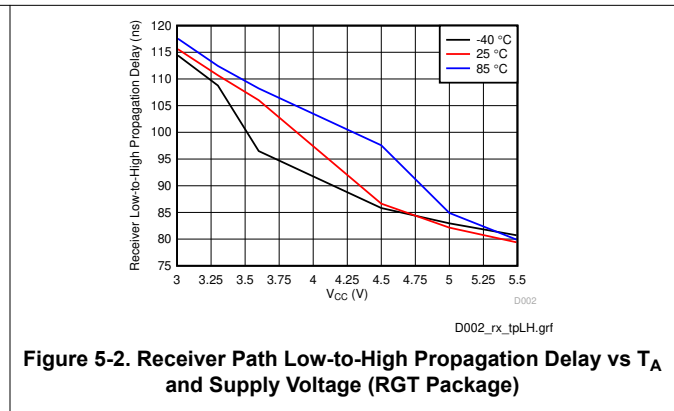
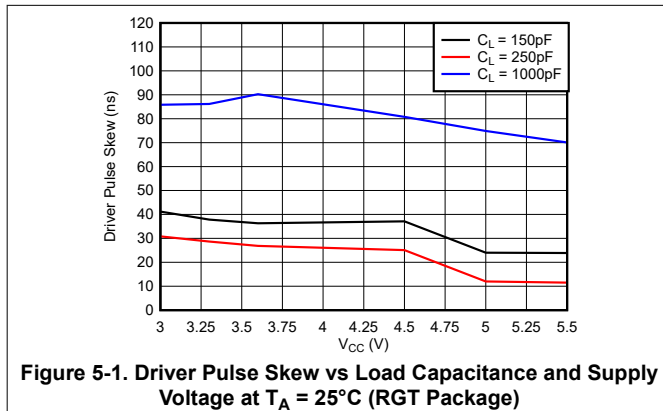
5.12 Switching Characteristics, Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6-5)

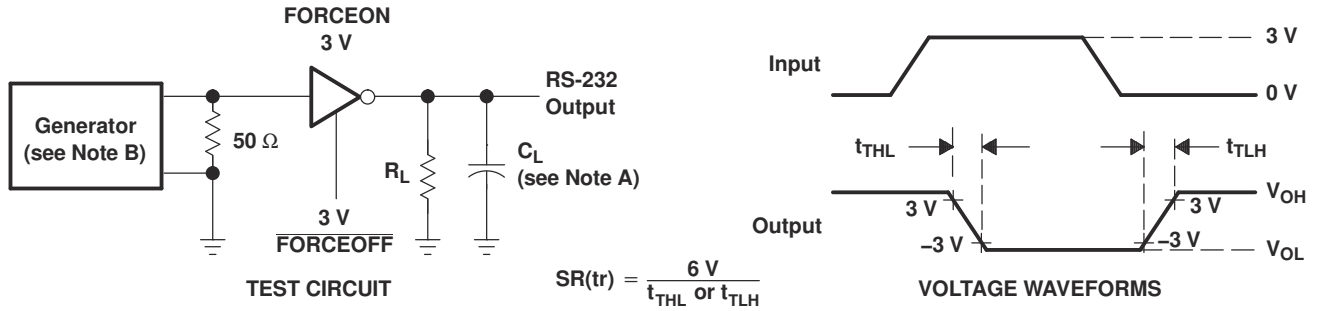
PARAMETER	TYP(1)	UNIT
t_{valid}	1	μs
t_{invalid}	30	μs
t_{en}	100	μs

(1) All typical values are at $V_{CC} = 3.3 \text{ V}$ or $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$.

5.13 Typical Characteristics

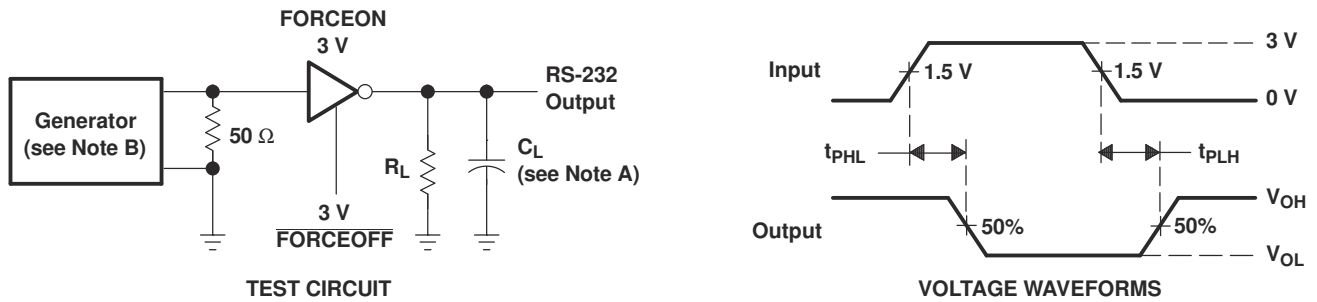


6 Parameter Measurement Information



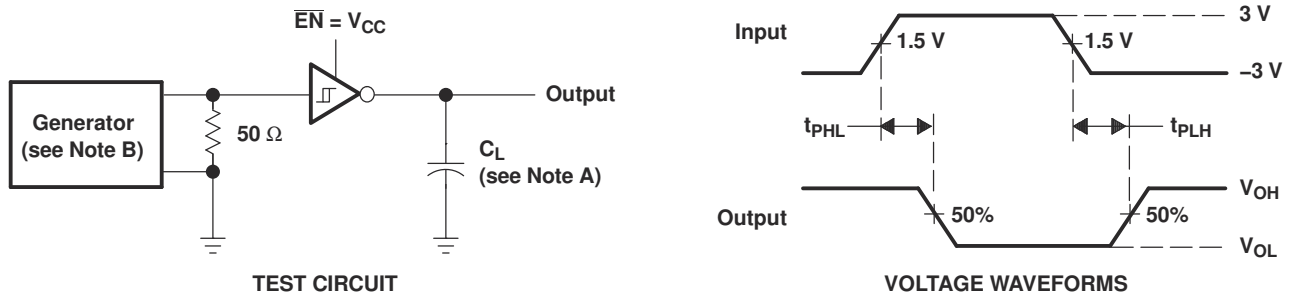
NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

Figure 6-1. Driver Slew Rate



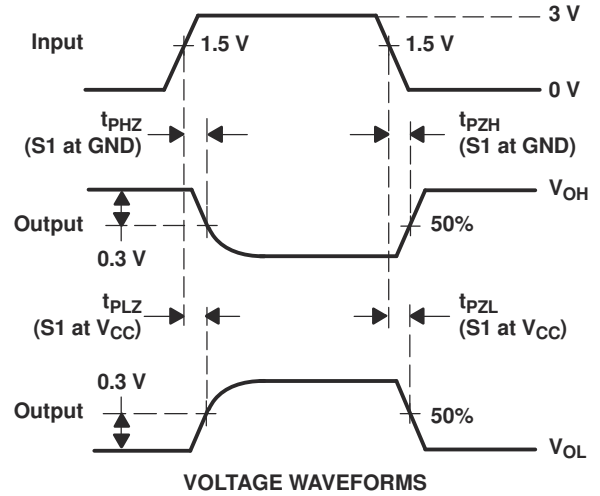
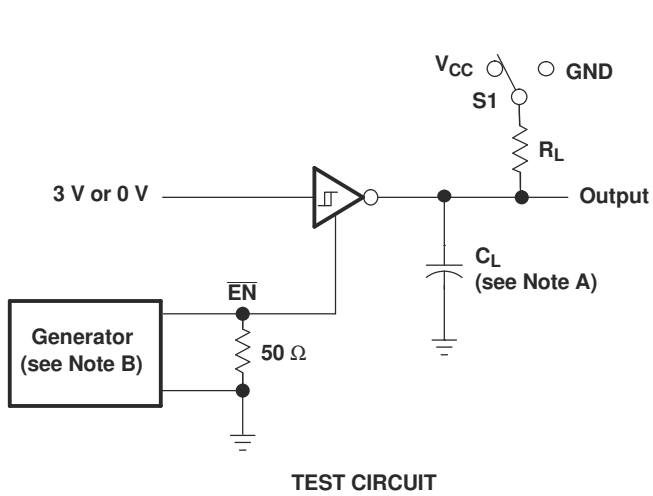
NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

Figure 6-2. Driver Pulse Skew



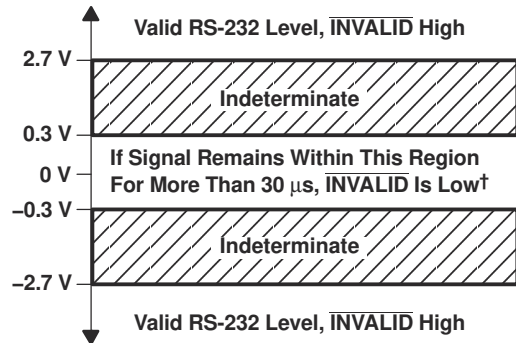
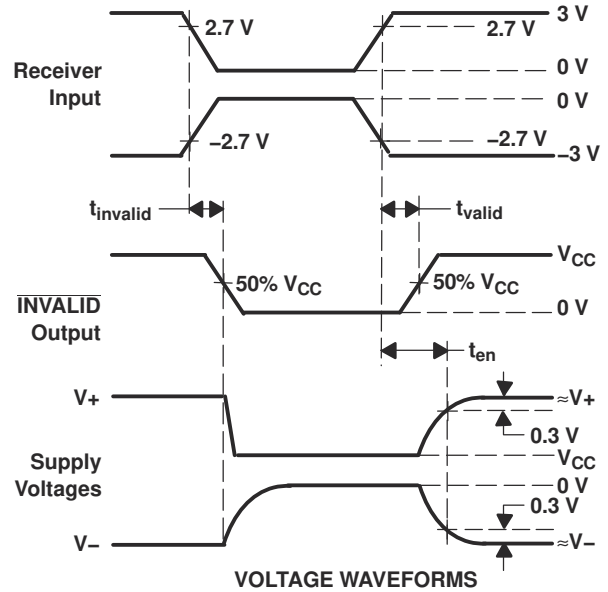
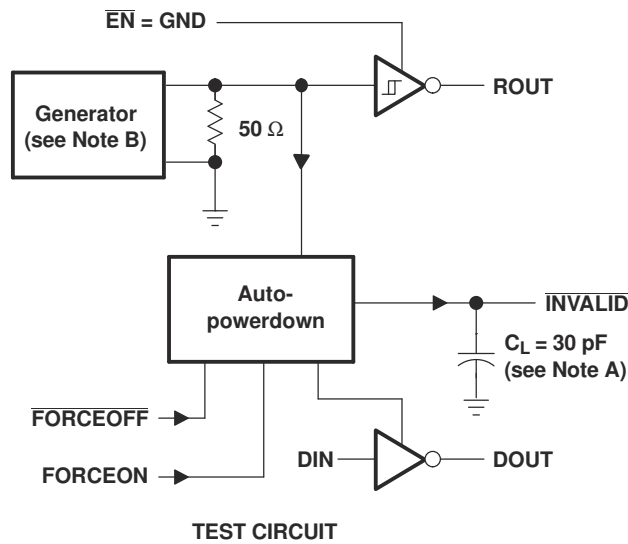
NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

Figure 6-3. Receiver Propagation Delay Times



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.
 - C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - D. t_{PZL} and t_{PZH} are the same as t_{en} .

Figure 6-4. Receiver Enable and Disable Times



† Auto-powerdown disables drivers and reduces supply current to 1 μ A.

NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 5 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 6-5. INVALID Propagation Delay Times and Driver Enabling Time

7 Detailed Description

7.1 Overview

The TRSF3221E consists of one line driver, one line receiver, and a dual charge-pump circuit with $\pm 15\text{kV}$ IEC ESD protection pin to pin (serial-port connection pins, including GND). The TRSF3221E provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3V to 5.5V supply. The TRSF3221E operates at data signaling rates up to 1Mbit/s and a driver output slew rate of $24\text{V}/\mu\text{s}$ to $150\text{V}/\mu\text{s}$.

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and $\overline{\text{FORCEOFF}}$ is high. During this mode of operation, if the TRSF3221E does not sense a valid RS-232 signal on the receiver input, the driver output is disabled. If $\overline{\text{FORCEOFF}}$ is set low and the enable ($\overline{\text{EN}}$) input is high, both the driver and receiver are shut off, and the supply current is reduced to $1\mu\text{A}$. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur. Auto-powerdown can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to the receiver input. The $\overline{\text{INVALID}}$ output notifies the user if an RS-232 signal is present at the receiver input. $\overline{\text{INVALID}}$ is high (valid data) if the receiver input voltage is greater than 2.7V or less than -2.7V , or has been between -0.3V and 0.3V for less than $30\mu\text{s}$. $\overline{\text{INVALID}}$ is low (invalid data) if the receiver input voltage is between -0.3V and 0.3V for more than $30\mu\text{s}$. Outputs are protected against shorts to ground.

7.2 Functional Block Diagram

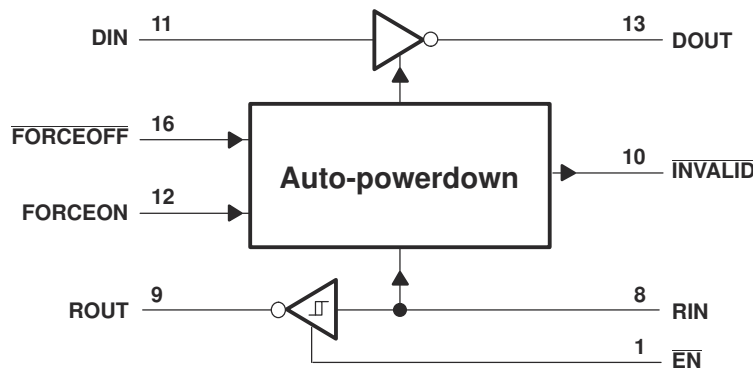


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

The power block increases, inverts, and regulates voltage at $V+$ and $V-$ pins using a charge pump that requires four external capacitors. Auto-power-down feature for driver is controlled by FORCEON and $\overline{\text{FORCEOFF}}$ inputs. Receiver is controlled by $\overline{\text{EN}}$ input. When MAX3221E is unpowered, it can be safely connected to an active remote RS-232 device.

The driver interfaces the standard logic level to RS232 voltage levels. The DIN input must be valid high or low.

The receiver interfaces RS-232 levels to standard logic levels. An open input results in a high output on ROUT. RIN input includes an internal standard RS-232 load. A logic high input on the $\overline{\text{EN}}$ pin shuts down the receiver output.

7.4 Device Functional Modes

Functional Tables, Each Driver

INPUTS ⁽¹⁾				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Each Receiver

INPUTS ⁽¹⁾			OUTPUT ROUT
RIN	\overline{EN}	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = disconnected input or connected driver off

8 Application and Implementation

Note

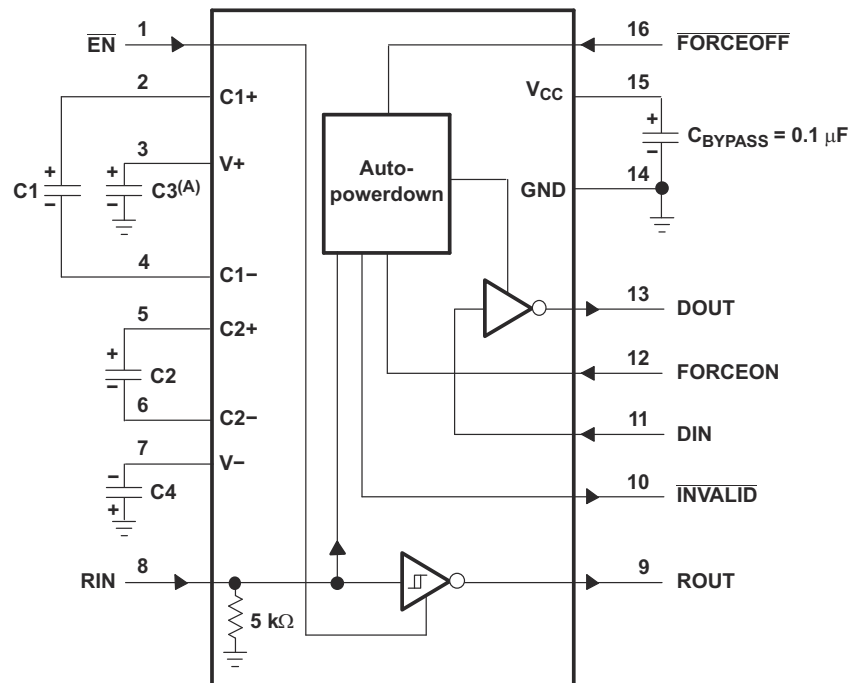
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TRSF3221E line driver and receiver is a specialized device for 3V to 5.5V RS-232 communication applications. This application is a generic implementation of this device with all required external components. For proper operation, add capacitors as shown in [Table 8-1](#).

8.1.1 Typical Application

ROUT and DIN connect to UART or general purpose logic lines. FORCEON and FORCEOFF may be connected to general purpose logic lines or tied to ground or VCC. INVALID may be connected to a general purpose logic line or left unconnected. RIN and DOUT lines connect to a RS-232 connector or cable. DIN, FORCEON, and FORCEOFF inputs must not be left unconnected.



- A. C3 can be connected to V_{CC} or GND.
- B. Resistor values shown are nominal.
- C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they must be connected as shown.

Figure 8-1. Typical Operating Circuit and Capacitor Values

Table 8-1. V_{CC} vs Capacitor Values

V_{CC}	C1	C2, C3, C4
3.3V ± 0.3V	0.1μF	0.1μF
5V ± 0.5V	0.047μF	0.33μF
3V to 5.5V	0.1μF	0.47μF

8.1.1.1 Design Requirements

- Recommended VCC is 3.3V or 5V – 3V to 5.5V is also possible
- Maximum recommended bit rate is 1Mbps
- Use capacitors as shown in [Figure 8-1](#) and [Table 8-1](#)

8.1.1.2 Detailed Design Procedure

For proper operation:

- DIN, $\overline{\text{FORCEOFF}}$ and FORCEON inputs must be connected to valid low or high logic levels
- Select capacitor values based on VCC level for best performance

ROUT and DIN connect to UART or general purpose logic lines. FORCEON and $\overline{\text{FORCEOFF}}$ may be connected general purpose logic lines or tied to ground or VCC. INVALID may be connected to a general purpose logic line or left unconnected. RIN and DOUT lines connect to a RS232 connector or cable. DIN, FORCEON, and $\overline{\text{FORCEOFF}}$ inputs must not be left unconnected.

8.1.2 Application Performance Plot

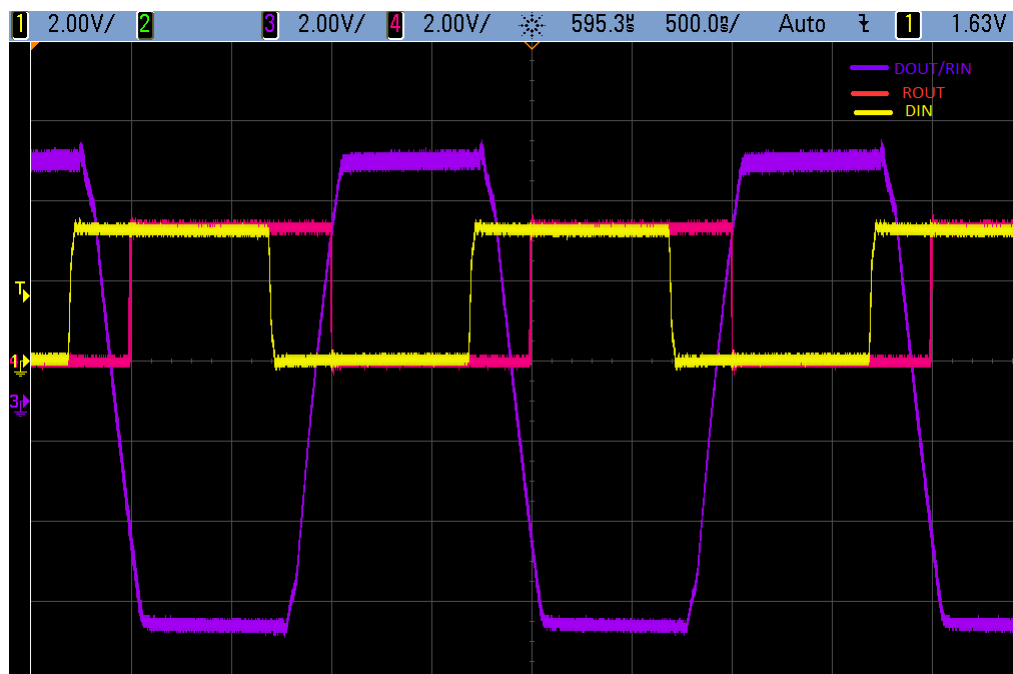


Figure 8-2. 1 Mbps Driver to Receiver Loopback Timing Waveform, VCC = 3.3 V

8.2 Power Supply Recommendations

VCC must be between 3V and 5.5V. Charge pump capacitors must be chosen using [VCC vs Capacitor Values](#).

8.3 Layout

8.3.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes, which have the fastest rise and fall times.

8.3.2 Layout Example

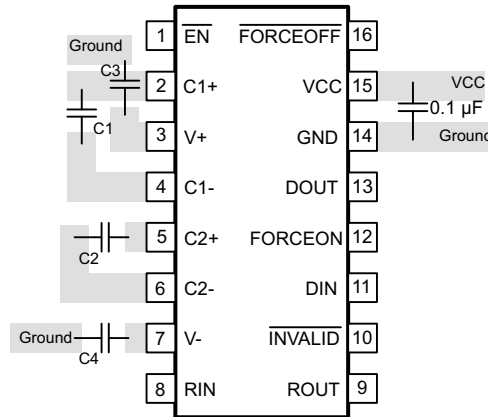


Figure 8-3. Layout Diagram

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (July 2021) to Revision C (December 2024)	Page
• Changed the <i>Device Information</i> table to the <i>Package Information</i> table.....	1
• Added the SOT-23-THN (DYY) package to the data sheet.....	1
• Added Note 2 to the <i>ESD Ratings, IEC Specifications</i>	5
<hr/>	
Changes from Revision A (May 2021) to Revision B (July 2021)	Page
• Changed the <i>Applications</i> list.....	1
• Changed the table note for the <i>ESD Ratings, IEC Specifications</i> table to make it also applicable to PW package.....	5
• Changed the thermal information for PW package.....	6
<hr/>	
Changes from Revision * (August 2007) to Revision A (May 2021)	Page
• Added Device Information table, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.....	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRSF3221ECDB	OBSOLETE	SSOP	DB	16		TBD	Call TI	Call TI	0 to 70	RT21EC	
TRSF3221ECDBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	RT21EC	Samples
TRSF3221ECPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	RT21EC	Samples
TRSF3221EIDBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT21EI	Samples
TRSF3221EIDYYR	ACTIVE	SOT-23-THIN	DYY	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT21EI	Samples
TRSF3221EIPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	RT21EI	Samples
TRSF3221EIRGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F3221	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRSF3221ECDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TRSF3221ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRSF3221EIDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TRSF3221EIDYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TRSF3221EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRSF3221EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRSF3221EIRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRSF3221ECDBR	SSOP	DB	16	2000	356.0	356.0	35.0
TRSF3221ECPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TRSF3221EIDBR	SSOP	DB	16	2000	356.0	356.0	35.0
TRSF3221EIDYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
TRSF3221EIPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TRSF3221EIPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TRSF3221EIRGTR	VQFN	RGT	16	3000	367.0	367.0	35.0

PW0016A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB0016A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

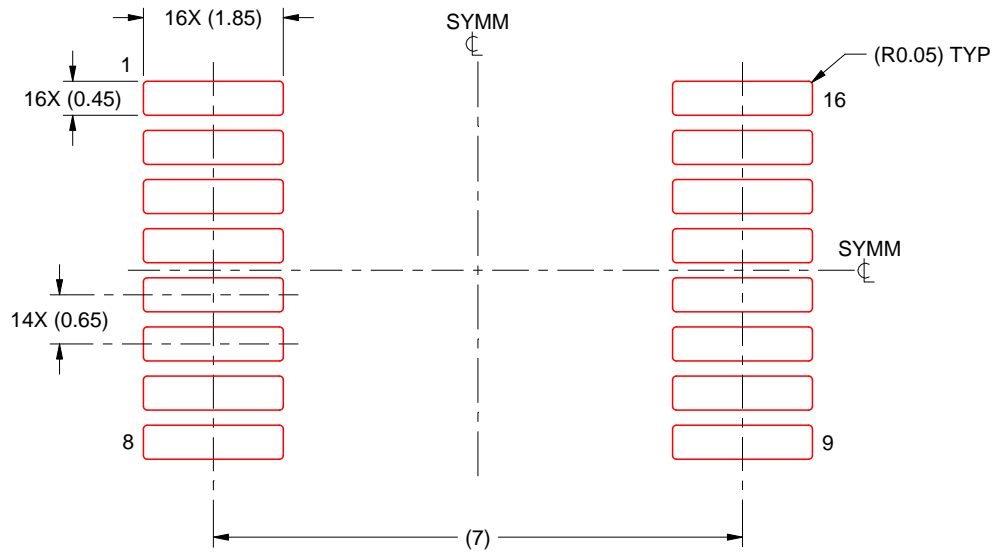
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

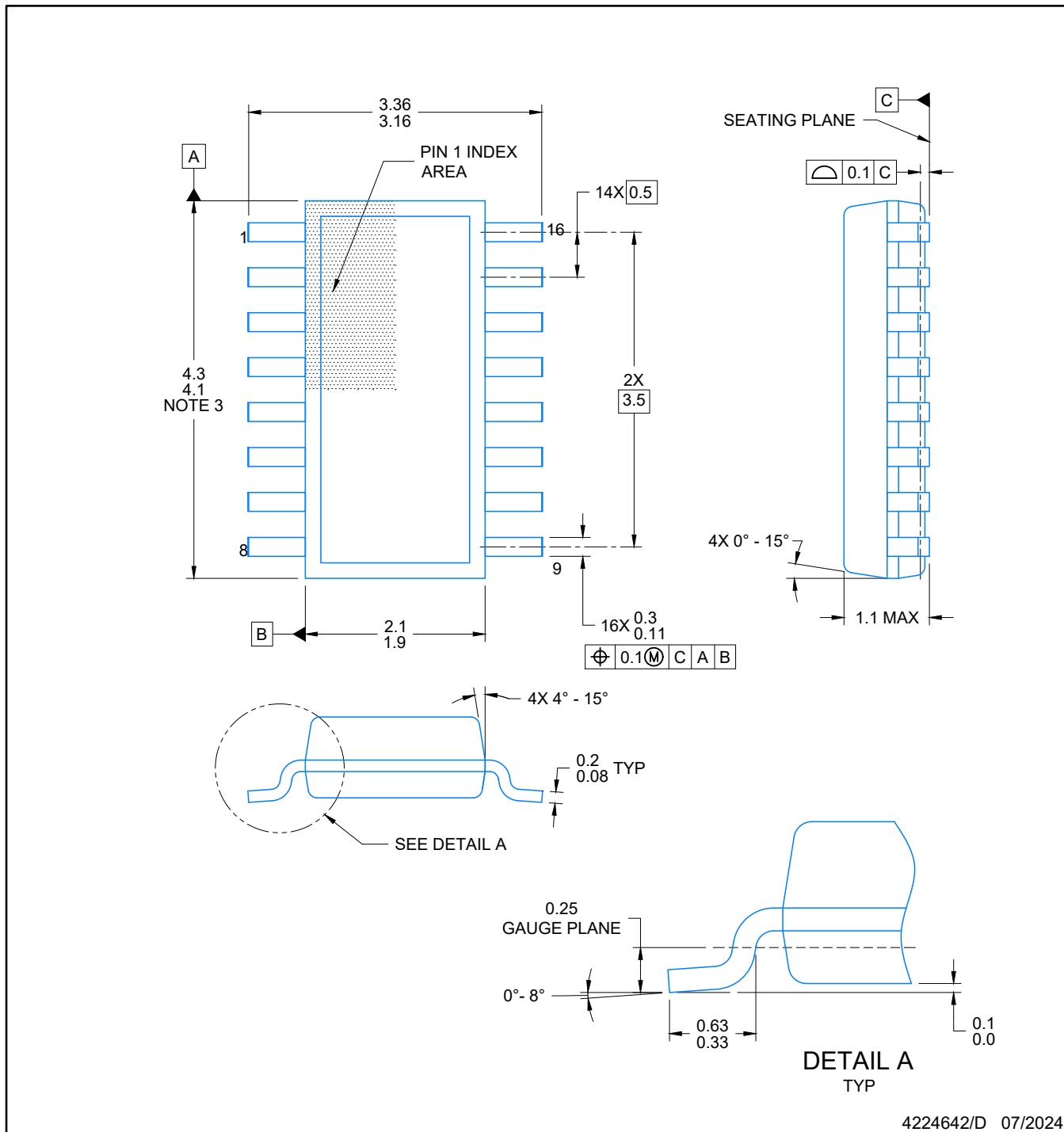


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

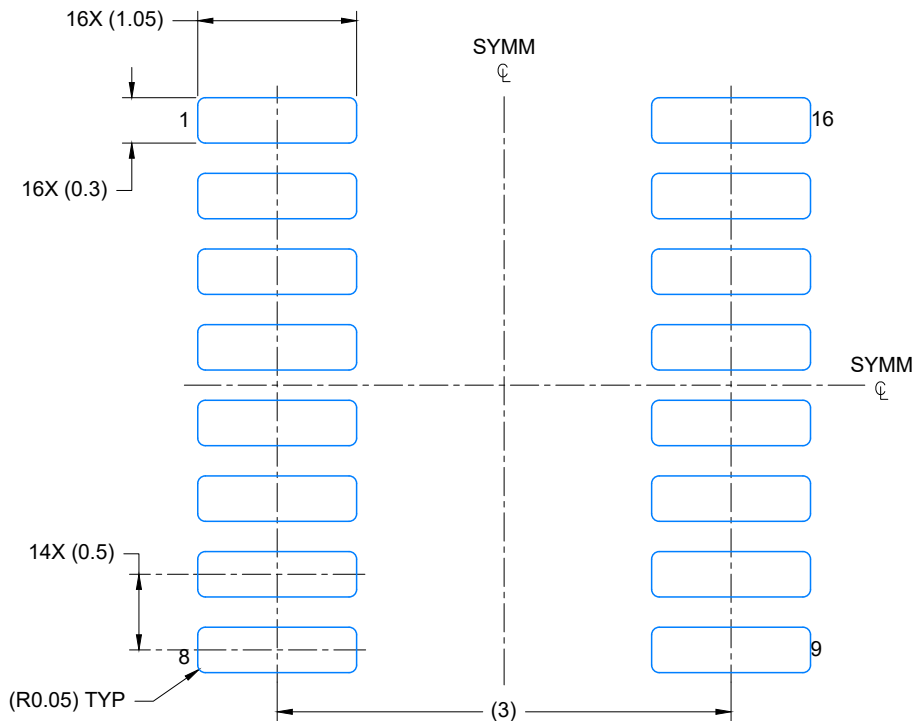
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



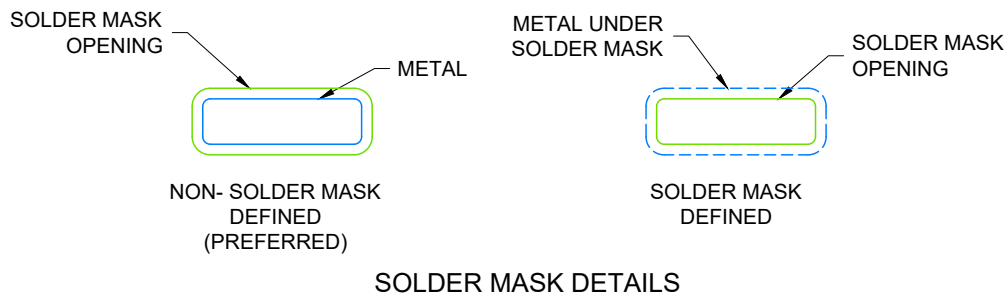
4224642/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



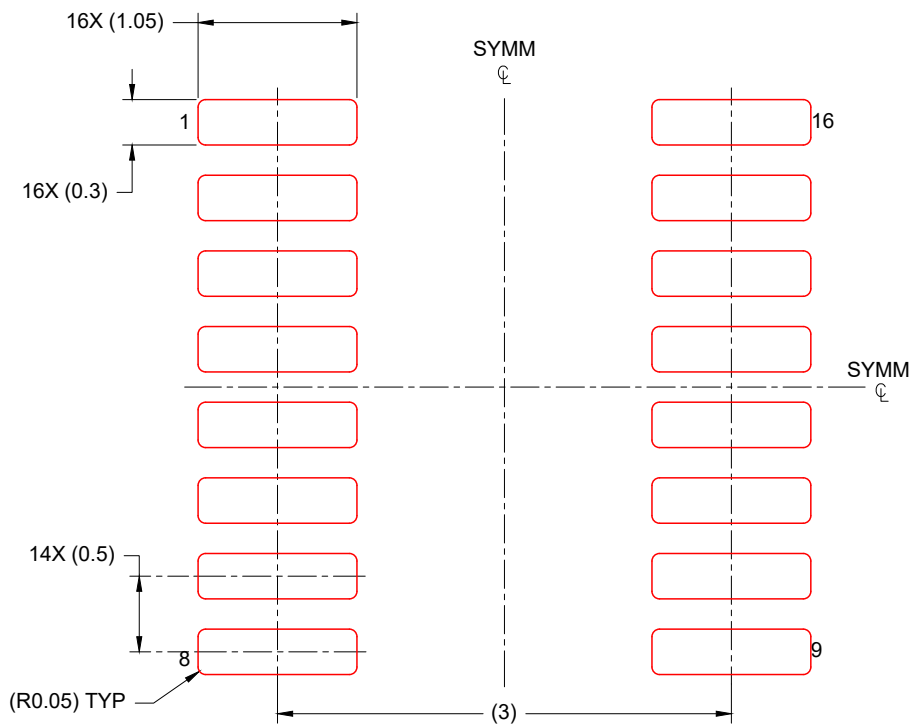
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224642/D 07/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

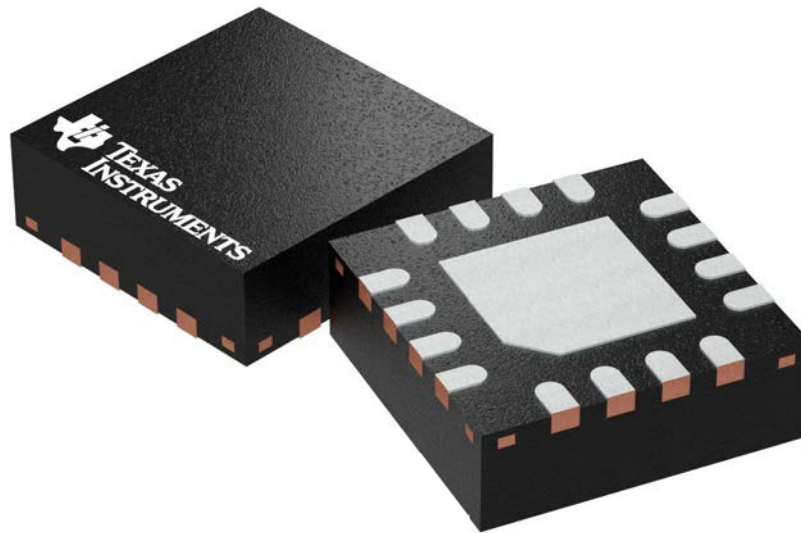
- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

RGT 16

GENERIC PACKAGE VIEW

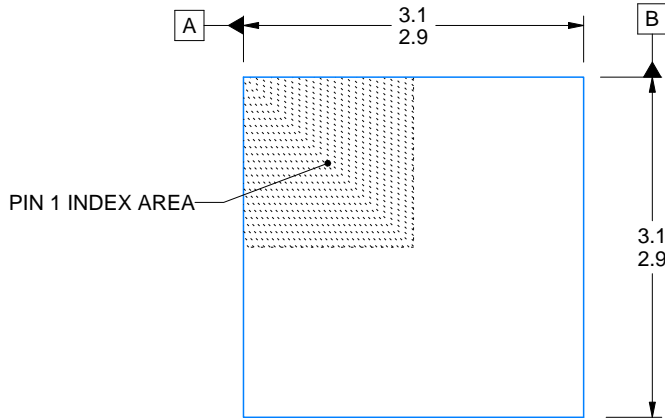
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

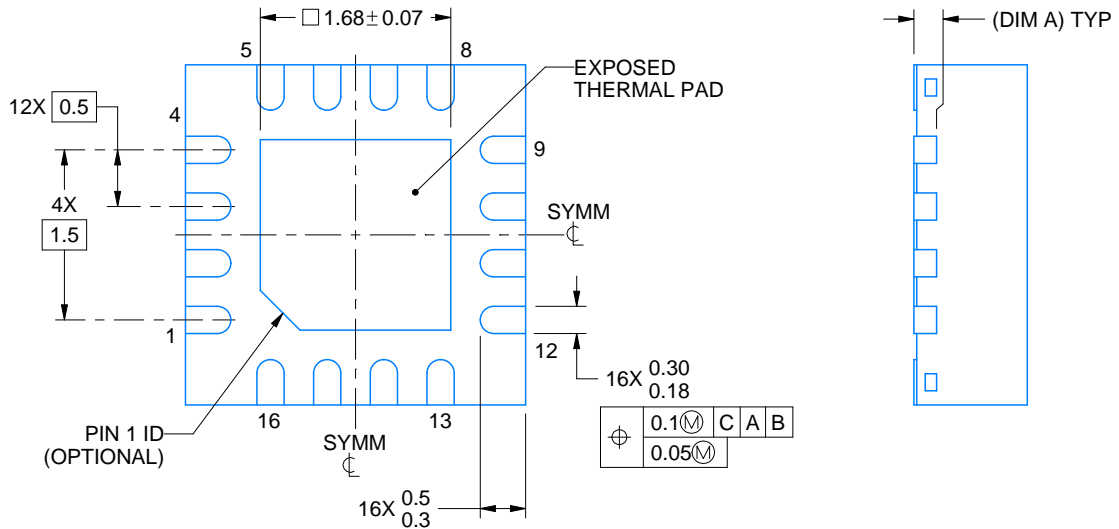


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/1



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4222419/D 04/2022

NOTES:

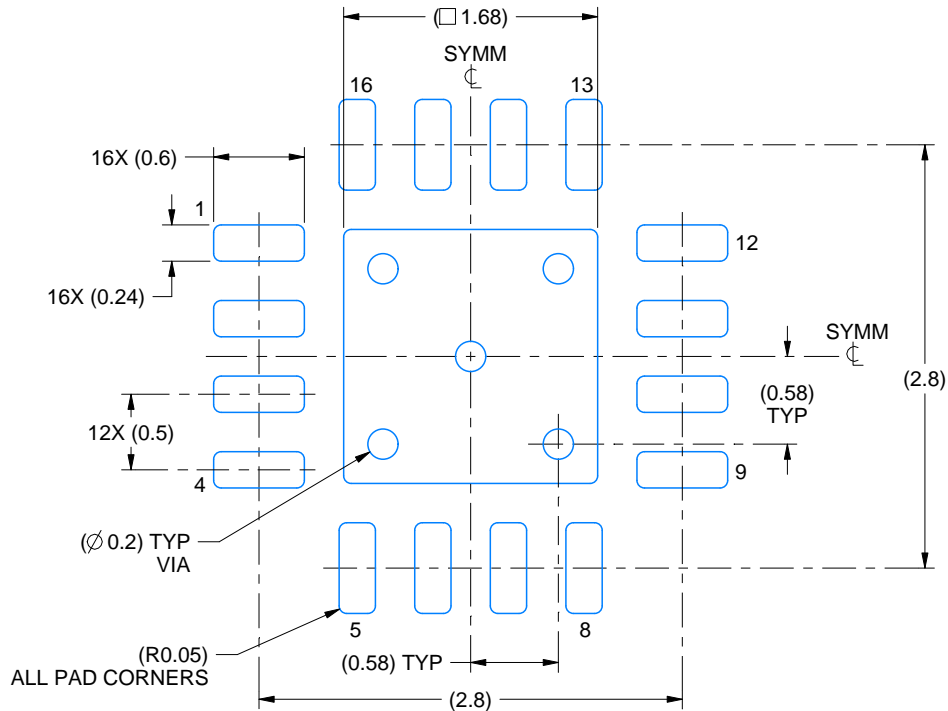
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

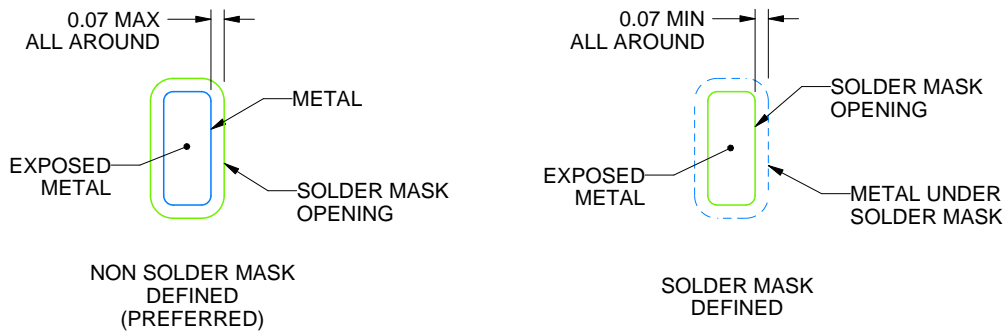
RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4222419/D 04/2022

NOTES: (continued)

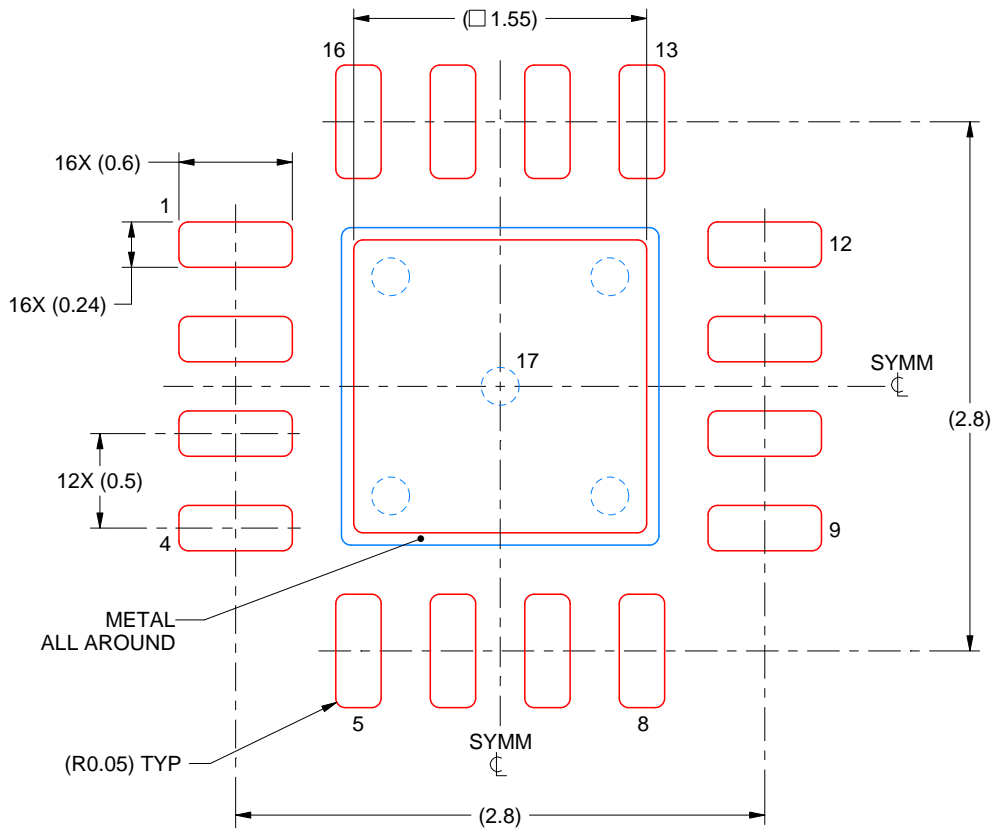
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/D 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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