TS3L110 Quad SPDT High-Bandwidth 10/100 Base-T LAN Switch
Differential 8-Channel to 4-Channel Multiplexer/Demultiplexer

1 Features

- Wide bandwidth (BW = 500 MHz typical)
- Low crosstalk (X_{TALK} = –30 dB typical)
- Bidirectional data flow with near-zero propagation delay
- Low and flat ON-state resistance (r_{on} = 4 \Omega \text{ typical}, r_{on(flat)} = 1 \Omega)
- Switching on Data I/O Ports (0 to 5 V)
- V_{CC} Operating range from 3 V to 3.6 V
- I_{off} Supports partial power-down-mode operation
- Data and control inputs have undershoot clamp diodes
- Latch-up performance exceeds 100 mA Per JESD 78, class II
- ESD Performance tested per JESD 22
  - 2000-V Human-body model (A114-B, class II)
  - 1000-V Charged-device model (C101)
- Suitable for both 10 Base-T and 100 Base-T signaling

2 Applications

- 10 and 100 Base-T signal switching

3 Description

The TS3L110 local area network (LAN) switch is a 4-bit 1-of-2 multiplexer/demultiplexer with a single switch-enable (E) input. When E is low, the switch is enabled, and the I port is connected to the Y port. When E is high, the switch is disabled, and the high-impedance state exists between the I and Y ports. The select (S) input controls the data path of the multiplexer/demultiplexer.

The TS3L110 device can be used to replace mechanical relays in LAN applications. This device has low and flat ON-state resistance (r_{on}), wide bandwidth, and low crosstalk, making it suitable for 10/100 Base-T and various other LAN applications.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current does not backflow through the device when it is powered down. The device has isolation during power off.

Device Information (1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TS3L110</td>
<td>SOIC (D) 16</td>
<td>9.90 mm x 3.91 mm</td>
</tr>
<tr>
<td></td>
<td>SSOP (DBQ) 16</td>
<td>4.90 mm x 3.90 mm</td>
</tr>
<tr>
<td></td>
<td>TVSOP (DGV) 16</td>
<td>3.60 mm x 4.40 mm</td>
</tr>
<tr>
<td></td>
<td>TSSOP (PW) 16</td>
<td>5.00 mm x 4.40 mm</td>
</tr>
<tr>
<td></td>
<td>VQFN (RGV) 16</td>
<td>4.00 mm x 4.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

To ensure the high-impedance state during power up or power down, E should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2019) to Revision B Page
• Change pin 10 to IC1, pin 11 to IC0, pin 13 to ID1, and pin 14 to ID0 in the Pin Configuration and Functions.............. 3

Changes from Original (September 2004) to Revision A Page
• Added Device Information table, ESD Ratings table, Thermal Information table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section...... 1
5 Pin Configuration and Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>Select input</td>
</tr>
<tr>
<td>IA0</td>
<td>Data I/Os</td>
</tr>
<tr>
<td>IA1</td>
<td>Data I/Os</td>
</tr>
<tr>
<td>YA</td>
<td>Data I/Os</td>
</tr>
<tr>
<td>IB0</td>
<td>Data I/Os</td>
</tr>
<tr>
<td>IB1</td>
<td>Data I/Os</td>
</tr>
<tr>
<td>YB</td>
<td>Data I/Os</td>
</tr>
<tr>
<td>GND</td>
<td>Ground (0 V) reference</td>
</tr>
<tr>
<td>YC</td>
<td>Data I/Os</td>
</tr>
<tr>
<td>IC1</td>
<td>Data I/Os</td>
</tr>
<tr>
<td>IC0</td>
<td>Data I/Os</td>
</tr>
<tr>
<td>ID</td>
<td>Data I/Os</td>
</tr>
<tr>
<td>ID0</td>
<td>Data I/Os</td>
</tr>
<tr>
<td>E</td>
<td>Enable input</td>
</tr>
<tr>
<td>VCC</td>
<td>Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD and GND.</td>
</tr>
</tbody>
</table>

Not to scale
6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CC} ) Supply voltage range</td>
<td>–0.5</td>
<td>4.6</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IN} ) Control input voltage range</td>
<td>–0.5</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IO} ) Switch I/O voltage range</td>
<td>–0.5</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>( i_{IK} ) Control input clamp current</td>
<td>( V_{IN} &lt; 0 )</td>
<td>–50</td>
<td>mA</td>
</tr>
<tr>
<td>( i_{IO} ) I/O port clamp current</td>
<td>( V_{IO} &lt; 0 )</td>
<td>–50</td>
<td>mA</td>
</tr>
<tr>
<td>( i_{IO} ) ON-state switch current</td>
<td>( \pm 128 )</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Continuous current through ( V_{CC} ) or GND</td>
<td>( \pm 100 )</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( \theta_{JA} ) Package thermal impedance</td>
<td>(D package)</td>
<td>73</td>
<td>°C/W</td>
</tr>
<tr>
<td>(DBQ package)</td>
<td>90</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(DGV package)</td>
<td>120</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(PW package)</td>
<td>108</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(RGY package)</td>
<td>39</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_{stg} ) Storage temperature range</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground, unless otherwise specified.

(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(4) \( I_{I} \) and \( I_{O} \) are used to denote specific conditions for \( V_{IO} \).

(5) \( I_{I} \) and \( I_{O} \) are used to denote specific conditions for \( V_{IO} \).

(6) The package thermal impedance is calculated in accordance with JESD 51-7.

(7) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{(ESD)} ) Electrostatic discharge</td>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001</td>
<td>±2000</td>
</tr>
<tr>
<td></td>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002</td>
<td>±1000</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CC} ) Supply voltage</td>
<td>3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IH} ) High-level control input voltage (E, S)</td>
<td>2</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IL} ) Low-level control input voltage (E, S)</td>
<td>0</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IO} ) Input/output voltage</td>
<td>0</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>( T_{A} ) Operating free-air temperature</td>
<td>–40</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) All unused control inputs of the device must be held at \( V_{CC} \) or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.
6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TS3L110</th>
<th></th>
<th>D (SOIC)</th>
<th>DBQ (SSOP)</th>
<th>DGV (TVSOP)</th>
<th>PW (TSSOP)</th>
<th>RGV (VQFN)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>16 PINS</td>
<td>16 PINS</td>
<td>16 PINS</td>
<td>16 PINS</td>
<td>16 PINS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Junction-to-ambient thermal resistance</td>
<td>92.0</td>
<td>114.5</td>
<td>139.3</td>
<td>111.5</td>
<td>50.8</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Junction-to-case (top) thermal resistance</td>
<td>52.3</td>
<td>65.5</td>
<td>57.4</td>
<td>42.0</td>
<td>48.1</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Junction-to-board thermal resistance</td>
<td>50.3</td>
<td>58.2</td>
<td>73.7</td>
<td>57.8</td>
<td>26.7</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Junction-to-top characterization parameter</td>
<td>17.3</td>
<td>15.3</td>
<td>7.2</td>
<td>4.2</td>
<td>2.1</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Junction-to-board characterization parameter</td>
<td>50.0</td>
<td>57.6</td>
<td>73.0</td>
<td>57.2</td>
<td>26.5</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>10.7</td>
<td>°C/W</td>
<td></td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

6.5 Electrical Characteristics(1)

over recommended operating free-air temperature range, \(V_{CC} = 3.3\ V \pm 0.3\ V\) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP(2)</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{IK})</td>
<td>(E, S) (V_{CC} = 3.6\ V, I_{IN} = -18\ mA)</td>
<td>-1.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(I_{IH})</td>
<td>(E, S) (V_{CC} = 3.6\ V, V_{IN} = 5.5\ V)</td>
<td>±1</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>(I_{IL})</td>
<td>(E, S) (V_{CC} = 3.6\ V, V_{IN} = \text{GND})</td>
<td>±1</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>(I_{off})</td>
<td>(V_{CC} = 0, V_{D} = 0) to (5.5\ V, V_{I} = 0)</td>
<td>1</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>(I_{CC})</td>
<td>(V_{CC} = 3.6\ V, I_{IO} = 0,) Switch ON or OFF</td>
<td>0.7</td>
<td>1.5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>(C_{in})</td>
<td>(E, S) (f = 1\ MHz, V_{IN} = 0)</td>
<td>2.5</td>
<td>3.5</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>(C_{io(\text{OFF})})</td>
<td>(I) port (V_{I} = 0, f = 1\ MHz,) Outputs open, Switch OFF</td>
<td>3.5</td>
<td>5</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(Y) port (V_{I} = 0, f = 1\ MHz,) Outputs open, Switch OFF</td>
<td>5.5</td>
<td>7</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>(C_{io(\text{ON})})</td>
<td>(I) or (Y) port (V_{I} = 0, f = 1\ MHz,) Outputs open, Switch ON</td>
<td>10.5</td>
<td>13</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>(r_{on})</td>
<td>(V_{CC} = 3\ V, 1.25\ V \leq V_{I} \leq V_{CC}, I_{O} = -10\ mA) to (-30\ mA)</td>
<td>4</td>
<td>8</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>(r_{on(flat)}(3))</td>
<td>(V_{CC} = 3\ V, V_{I} = 1.25\ V) and (V_{CC}, I_{O} = -10\ mA) to (-30\ mA)</td>
<td>1</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>(\Delta r_{on}(4))</td>
<td>(V_{CC} = 3\ V, 1.25\ V \leq V_{I} \leq V_{CC}, I_{O} = -10\ mA) to (-30\ mA)</td>
<td>0.9</td>
<td>2</td>
<td>Ω</td>
<td></td>
</tr>
</tbody>
</table>

(1) \(V_{I}, V_{O}, I_{I}, \) and \(I_{O}\) refer to I/O pins. \(V_{IN}\) refers to the control inputs.
(2) All typical values are at \(V_{CC} = 3.3\ V\) (unless otherwise noted), \(T_{A} = 25°C.\)
(3) \(r_{on(flat)}\) is the difference of \(r_{on}\) in a given channel at specified voltages.
(4) \(\Delta r_{on}\) is the difference of \(r_{on}\) in a given device.
6.6 Switching Characteristics

over recommended operating free-air temperature range, \( V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V} \), \( R_L = 200 \Omega \), \( C_L = 10 \text{ pF} \) (unless otherwise noted) (see Figure 5 and Figure 6)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>MIN</th>
<th>TYP(1)</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{pd} )</td>
<td>I or Y</td>
<td>Y or I</td>
<td>0.25</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( I_{pZH}, I_{pZL} )</td>
<td>E or S</td>
<td>I or Y</td>
<td>0.5</td>
<td>7</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( I_{PHZ}, I_{PLZ} )</td>
<td>E or S</td>
<td>I or Y</td>
<td>0.5</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{skip} )</td>
<td>I or Y</td>
<td>Y or I</td>
<td>0.1</td>
<td>0.2</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) All typical values are at \( V_{CC} = 3.3 \text{ V} \) (unless otherwise noted), \( T_A = 25^\circ \text{C} \).
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(3) Skew between opposite transitions of the same output \( |t_{PHL} - t_{PLH}| \). This parameter is not production tested.

6.7 Dynamic Characteristics

over recommended operating free-air temperature range, \( V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V} \) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>TYP(1)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( X_{TALK} )</td>
<td>( R_L = 100 \Omega ), ( f = 250 \text{ MHz} ), See Figure 7</td>
<td>–26</td>
<td>dB</td>
</tr>
<tr>
<td>( O_{IRR} )</td>
<td>( R_L = 100 \Omega ), ( f = 250 \text{ MHz} ), See Figure 8</td>
<td>–28</td>
<td>dB</td>
</tr>
<tr>
<td>BW</td>
<td>( R_L = 100 \Omega ), See Figure 6</td>
<td>500</td>
<td>MHz</td>
</tr>
</tbody>
</table>

(1) All typical values are at \( V_{CC} = 3.3 \text{ V} \) (unless otherwise noted), \( T_A = 25^\circ \text{C} \).
6.8 Typical Characteristics

Phase at 627 MHz, \(-36\) Deg
Gain \(-3\) dB at 627 MHz

Phase at 250 MHz, \(88.2\) Deg
Gain \(-28.5\) dB at 250 MHz

Phase at 250 MHz, \(137.92\) Deg
Gain \(-26\) dB at 250 MHz
7 Parameter Measurement Information

Figure 5. Test Circuit and Voltage Waveforms

A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \ \Omega$, $t_r \leq 2.5 \ ns$, $t_f \leq 2.5 \ ns$.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PLZ}$ and $t_{PHH}$ are the same as $t_{en}$.
Parameter Measurement Information (continued)

**Figure 6. Test Circuit and Voltage Waveforms**

<table>
<thead>
<tr>
<th>TEST</th>
<th>V(_{CC})</th>
<th>S1</th>
<th>R(_L)</th>
<th>(V_{IN})</th>
<th>C(_L)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{sk(p)})</td>
<td>3.3 V ± 0.3 V</td>
<td>GND</td>
<td>200 (\Omega)</td>
<td>(V_{CC}) or GND</td>
<td>10 pF</td>
</tr>
</tbody>
</table>

A. C\(_L\) includes probe and jig capacitance.

B. Switch is ON during the measurement of \(t_{sk(p)}\), that is, voltage at \(E = 0\) and \(S = V_{CC}\) or GND.

VOLTAGE WAVEFORMS
PULSE SKEW \(t_{sk(p)}\)

\[ t_{sk(p)} = t_{PHL} - t_{PLH} \]
Parameter Measurement Information (continued)

Figure 7. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when \( V_S = 0 \), \( V_E = 0 \), and \( YA \) is the input, the output is measured at \( IA_0 \). All unused analog I/O ports are left open.

HP8753ES Setup
- Average = 4
- RBW = 3 kHz
- \( V_{BIAS} = 0.35 \) V
- ST = 2 s
- \( P1 = 0 \) dBM

Note A: \( C_L \) includes probe and jig capacitance.
Parameter Measurement Information (continued)

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when \( V_S = 0 \), \( V_E = 0 \), and \( YA \) is the input, the output is measured at \( IB_0 \). All unused analog input (Y) ports are connected to GND, and output (I) ports are connected to GND through 50-Ω pulldown resistors.

HP8753ES Setup
- Average = 4
- RBW = 3 kHz
- \( V_{BIAS} = 0.35 \) V
- ST = 2 s
- P1 = 0 dBM

A. \( C_L \) includes probe and jig capacitance.

B. A 50-Ω termination resistor is needed to match the loading of the network analyzer

Figure 8. Test Circuit for Crosstalk (X\text{\_TALK})
Parameter Measurement Information (continued)

Figure 9. Test Circuit for OFF Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when \( V_S = V_{CC} \), \( V_E = 0 \), and YA is the input, the output is measured at IA\(_0\). All unused analog input (Y) ports are left open, and output (I) ports are connected to GND through 50-Ω pulldown resistors.

HP8753FS Setup
- Average = 4
- RBW = 3 kHz
- \( V_{BIAS} = 0.35 \text{ V} \)
- ST = 2 s
- P1 = 0 dBm

A. \( C_L \) includes probe and jig capacitance.
B. A 50-Ω termination resistor is needed to match the loading of the network analyzer.
8 Detailed Description

8.1 Overview
The TI TS3L110 LAN switch is a 4-bit 1-of-2 multiplexer/demultiplexer with a single switch-enable (E) input. When E is low, the switch is enabled, and the I port is connected to the Y port. When E is high, the switch is disabled, and the high-impedance state exists between the I and Y ports. The select (S) input controls the data path of the multiplexer/demultiplexer.

8.2 Functional Block Diagram

8.3 Feature Description
I\text{off} supports Partial-Power-Down Mode Operation.
The TS3L110 device ensures the signal path is high impedance state when V_{CC} = 0 V.

8.4 Device Functional Modes
The TS3L110 supports a power down mode which reduces the current consumption of the device and places all the signal paths in a high impedance state. To place the TS3L100 in power down mode, set the E pin with a logic high voltage as seen in Table 1.

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>INPUT/OUTPUT YX</th>
<th>FUNCTION</th>
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<tbody>
<tr>
<td>E</td>
<td>S</td>
<td>\text{I}_X_0</td>
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<tr>
<td>L</td>
<td>L</td>
<td>\text{I}_X_1</td>
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<tr>
<td>L</td>
<td>H</td>
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<tr>
<td>H</td>
<td>X</td>
<td>Z</td>
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</table>
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information
There are many Local Area Network (LAN) applications in which the ethernet hubs or controllers have a limited number of I/Os or need to route signals from a single ethernet PHY to multiple ethernet jacks. The TS3L110 solution can effectively expand the limited I/Os by switching between multiple Ethernet jacks to interface them to a single Ethernet PHY.

9.2 Typical Application

![Typical Application Schematic](image)

**Figure 10. Typical Application Schematic**

9.2.1 Design Requirements
Ensure that all of the signals passing through the switch are within the recommended operating ranges. To ensure proper performance, see Recommended Operating Conditions.

9.2.2 Detailed Design Procedure
The TS3L110 can be properly operated without any external components. TI recommends that the digital control pins S and E be pulled up to VCC or down to GND to avoid undesired switch positions that could result from the floating pin. Connect the exposed thermal pad to ground.
**Typical Application (continued)**

### 9.2.3 Application Curves

![Graph showing Gain and Phase vs Frequency](image)

Phase at 627 MHz, −36 Deg  
Gain −3 dB at 627 MHz

---

**Figure 11. Gain and Phase vs Frequency**

---

**10 Power Supply Recommendations**

Power to the device is supplied through the VCC pins. TI recommends placing a bypass capacitor as close to the supply pin (VCC) as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.
11 Layout

11.1 Layout Guidelines

- TI recommends keeping the high-speed signals as short as possible.
- Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.
- When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
- Do not route traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
- Avoid stubs on the high-speed signals because they cause signal reflections. If a stub is unavoidable, then the stub must be less than 200 mm.
- Route all high-speed signal traces over continuous GND planes, with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.
- Due to high-frequency signals, a printed-circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 12.
- The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

![Figure 12. Four-Layer Board Stackup](image-url)
11.2 Layout Example

Figure 13. Layout Example
12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources
TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks
E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (1)</th>
<th>Lead/Ball Finish (2)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4)</th>
<th>Samples</th>
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<td>Level-1-260C-UNLIM</td>
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<td>TK110</td>
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(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
### TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS

| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

#### REEL DIMENSIONS

- **Reel Diameter**
- **Reel Width (W1)**

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Sprocket Holes**
- **User Direction of Feed**
- **Pocket Quadrants**

*All dimensions are nominal.*

### TAPE AND REEL INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
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<th>SPQ</th>
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<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
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## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

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<td>3000</td>
<td>853.0</td>
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<td>35.0</td>
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</tbody>
</table>
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.
⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.
E. Reference JEDEC MS-012 variation AC.
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate designs.  
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.  
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 mm per side.
D. Falls within JEDEC:
   - 24/48 Pins – MO-153
   - 14/16/20/56 Pins – MO-194

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Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.
9. Board assembly site may have different recommendations for stencil design.
NOTES:  
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figures in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

⚠️ Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
⚠️ The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO-241 variation BA.
THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal wax, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

![Exposed Thermal Pad Dimensions](image_url)

**NOTE:** All linear dimensions are in millimeters.
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC–7351 is recommended for alternate designs. 
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA277, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com. 
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations. 
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
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