

## FEATURES

- Wide Bandwidth (BW = 900 MHz Typ)
- Low Crosstalk ( $X_{TALK} = -41$  dB Typ)
- Low Bit-to-Bit Skew [ $t_{sk(o)} = 0.2$  ns Max]
- Low and Flat ON-State Resistance ( $r_{on} = 4 \Omega$  Typ,  $r_{on(flat)} = 0.7 \Omega$  Typ)
- Low Input/Output Capacitance ( $C_{ON} = 10$  pF Typ)
- Rail-to-Rail Switching on Data I/O Ports (0 to 5 V)
- $V_{DD}$  Operating Range From 3 V to 3.6 V
- $I_{off}$  Supports Partial Power-Down-Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Suitable for 10-/100-/1000-Mbit Ethernet Signaling

## APPLICATIONS

- 10/100/1000 Base-T Signal Switching
- Differential (LVDS, LVPECL) Signal Switching
- Digital Video Signal Routing
- Notebook Docking Signal Routing
- Hub and Router Signal Switching

## DESCRIPTION/ORDERING INFORMATION

The TS3L301 is a 16-bit to 8-bit multiplexer/demultiplexer local area network (LAN) switch with a single select (SEL) input. The SEL input controls the data path of the multiplexer/demultiplexer.

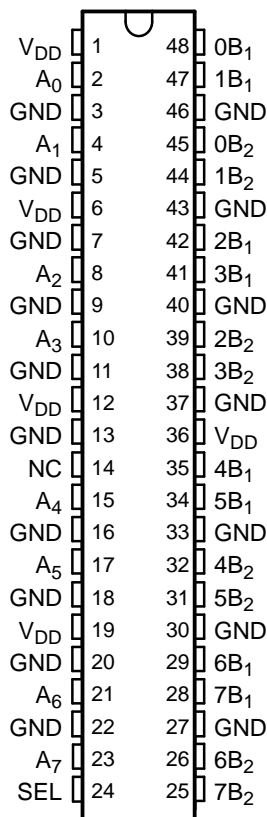
The device provides a low and flat ON-state resistance ( $r_{on}$ ) and an excellent ON-state resistance match. Low input/output capacitance, high-bandwidth, low skew, and low crosstalk among channels make this device suitable for various LAN applications, such as 10/100/1000 Base-T.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TSSOP – DGG	Tape and reel	TS3L301DGGR	TS3L301
	TVSOP – DGV	Tape and reel	TS3L301DGVR	TK301

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

DGG OR DGV PACKAGE  
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**TS3L301**  
**16-BIT TO 8-BIT SPDT GIGABIT LAN SWITCH**  
**WITH LOW AND FLAT ON-STATE RESISTANCE**

SCDS178C–NOVEMBER 2004–REVISED APRIL 2006

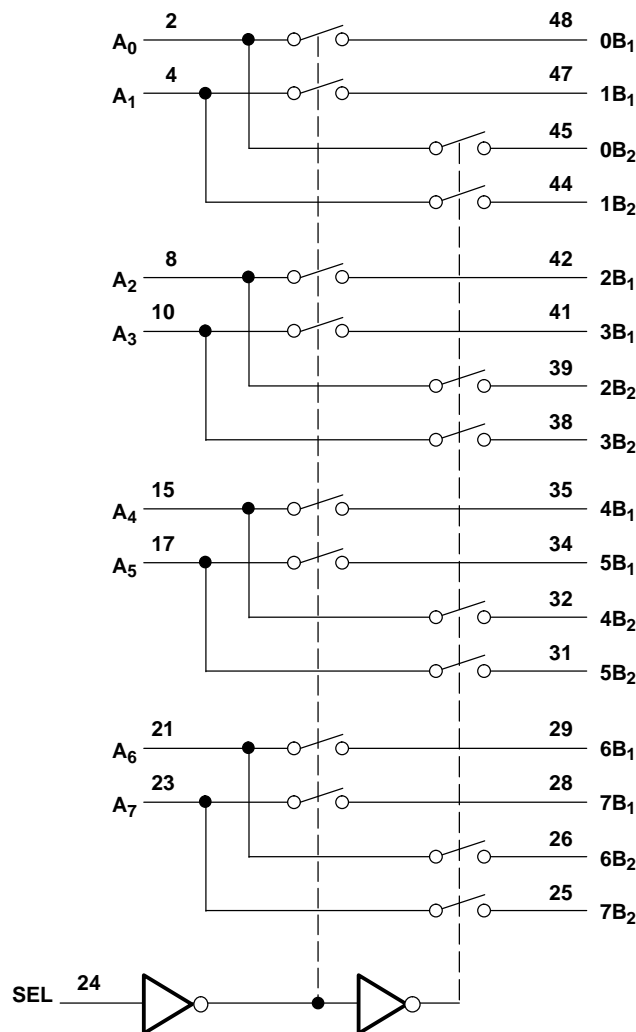
**FUNCTION TABLE**

INPUT SEL	INPUT/OUTPUT $A_n$	FUNCTION
L	$nB_1$	$A_n = nB_1$
H	$nB_2$	$A_n = nB_2$

**PIN DESCRIPTION**

NAME	DESCRIPTION
$A_n$	Data I/Os
$nB_m$	Data I/Os
SEL	Select input

**LOGIC DIAGRAM (POSITIVE LOGIC)**



### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>DD</sub>	Supply voltage range	-0.5	4.6	V
V <sub>IN</sub>	Control input voltage range <sup>(2)(3)</sup>	-0.5	7	V
V <sub>I/O</sub>	Switch I/O voltage range <sup>(2)(3)(4)</sup>	-0.5	7	V
I <sub>IK</sub>	Control input clamp current	V <sub>IN</sub> < 0	-50	mA
I <sub>I/OK</sub>	I/O port clamp current	V <sub>I/O</sub> < 0	-50	mA
I <sub>I/O</sub>	ON-state switch current <sup>(5)</sup>		±128	mA
	Continuous current through V <sub>DD</sub> or GND		±100	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(6)</sup>	DGG package	70	°C/W
		DGV package	58	
T <sub>stg</sub>	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground, unless otherwise specified.

(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(4) V<sub>I</sub> and V<sub>O</sub> are used to denote specific conditions for V<sub>I/O</sub>.

(5) I<sub>I</sub> and I<sub>O</sub> are used to denote specific conditions for I<sub>I/O</sub>.

(6) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>DD</sub>	Supply voltage	3	3.6	V
V <sub>IH</sub>	High-level control input voltage (SEL)	2	5.5	V
V <sub>IL</sub>	Low-level control input voltage (SEL)	0	0.8	V
V <sub>I/O</sub>	Input/output voltage	0	5.5	V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

(1) All unused control inputs of the device must be held at V<sub>DD</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# TS3L301

## 16-BIT TO 8-BIT SPDT GIGABIT LAN SWITCH WITH LOW AND FLAT ON-STATE RESISTANCE

SCDS178C–NOVEMBER 2004–REVISED APRIL 2006

### Electrical Characteristics

for 1000 Base-T Ethernet switching over recommended operating free-air temperature range,  $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$   
(unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP <sup>(2)</sup>	MAX	UNIT	
$V_{IK}$	SEL	$V_{DD} = 3.6 \text{ V}$ ,	$I_{IN} = -18 \text{ mA}$	-0.7	-1.2		V	
$I_{IH}$	SEL	$V_{DD} = 3.6 \text{ V}$ ,	$V_{IN} = V_{DD}$		$\pm 1$		$\mu\text{A}$	
$I_{IL}$	SEL	$V_{DD} = 3.6 \text{ V}$ ,	$V_{IN} = \text{GND}$		$\pm 1$		$\mu\text{A}$	
$I_{off}$		$V_{DD} = 0$ ,	$V_O = 0 \text{ to } 3.6 \text{ V}$ ,	$V_I = 0$		1	$\mu\text{A}$	
$I_{DD}$		$V_{DD} = 3.6 \text{ V}$ ,	$I_{I/O} = 0$ ,	Switch ON or OFF		250	600	$\mu\text{A}$
$C_{IN}$	SEL	$f = 1 \text{ MHz}$ ,	$V_{IN} = 0$		2.5	3	pF	
$C_{OFF}$	B port	$V_I = 0$ ,	$f = 1 \text{ MHz}$ ,	Outputs open,	Switch OFF	3.5	4	pF
$C_{ON}$		$V_I = 0$ ,	$f = 1 \text{ MHz}$ ,	Outputs open,	Switch ON	10	10.9	pF
$r_{on}$		$V_{DD} = 3 \text{ V}$ ,	$1.5 \text{ V} \leq V_I \leq V_{DD}$ ,	$I_O = -40 \text{ mA}$		4	8	$\Omega$
$r_{on(Flat)}$ <sup>(3)</sup>		$V_{DD} = 3 \text{ V}$ ,	$V_I = 1.5 \text{ V}$ and $V_{DD}$ ,	$I_O = -40 \text{ mA}$		0.7		$\Omega$
$\Delta r_{on}$ <sup>(4)</sup>		$V_{DD} = 3 \text{ V}$ ,	$1.5 \text{ V} \leq V_I \leq V_{DD}$ ,	$I_O = -40 \text{ mA}$		0.2	1.2	$\Omega$

- (1)  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to I/O pins.  $V_{IN}$  refers to the control inputs.  
(2) All typical values are at  $V_{DD} = 3.3 \text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .  
(3)  $r_{on(Flat)}$  is the difference of  $r_{on}$  in a given channel at specified voltages.  
(4)  $\Delta r_{on}$  is the difference of  $r_{on}$  from center ( $A_4$ ,  $A_5$ ) ports to any other port.

### Electrical Characteristics

for 10/100 Base-T Ethernet switching over recommended operating free-air temperature range,  $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$   
(unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP <sup>(2)</sup>	MAX	UNIT	
$V_{IK}$	SEL	$V_{DD} = 3.6 \text{ V}$ ,	$I_{IN} = -18 \text{ mA}$	-0.7	-1.2		V	
$I_{IH}$	SEL	$V_{DD} = 3.6 \text{ V}$ ,	$V_{IN} = V_{DD}$		$\pm 1$		$\mu\text{A}$	
$I_{IL}$	SEL	$V_{DD} = 3.6 \text{ V}$ ,	$V_{IN} = \text{GND}$		$\pm 1$		$\mu\text{A}$	
$I_{off}$		$V_{DD} = 0$ ,	$V_O = 0 \text{ to } 3.6 \text{ V}$ ,	$V_I = 0$		1	$\mu\text{A}$	
$I_{DD}$		$V_{DD} = 3.6 \text{ V}$ ,	$I_{I/O} = 0$ ,	Switch ON or OFF		250	600	$\mu\text{A}$
$C_{IN}$	SEL	$f = 1 \text{ MHz}$ ,	$V_{IN} = 0$		2.5	3	pF	
$C_{OFF}$	B port	$V_I = 0$ ,	$f = 1 \text{ MHz}$ ,	Outputs open,	Switch OFF	3.5	4	pF
$C_{ON}$		$V_I = 0$ ,	$f = 1 \text{ MHz}$ ,	Outputs open,	Switch ON	10	10.9	pF
$r_{on}$		$V_{DD} = 3 \text{ V}$ ,	$1.25 \text{ V} \leq V_I \leq V_{DD}$ ,	$I_O = -10 \text{ mA}$ to $-30 \text{ mA}$		4	8	$\Omega$
$r_{on(Flat)}$ <sup>(3)</sup>		$V_{DD} = 3 \text{ V}$ ,	$V_I = 1.25 \text{ V}$ and $V_{DD}$ ,	$I_O = -10 \text{ mA}$ to $-30 \text{ mA}$		0.7		$\Omega$
$\Delta r_{on}$ <sup>(4)</sup>		$V_{DD} = 3 \text{ V}$ ,	$1.25 \text{ V} \leq V_I \leq V_{DD}$ ,	$I_O = -10 \text{ mA}$ to $-30 \text{ mA}$		0.2	1.2	$\Omega$

- (1)  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to I/O pins.  $V_{IN}$  refers to the control inputs.  
(2) All typical values are at  $V_{DD} = 3.3 \text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .  
(3)  $r_{on(Flat)}$  is the difference of  $r_{on}$  in a given channel at specified voltages.  
(4)  $\Delta r_{on}$  is the difference of  $r_{on}$  from center ( $A_4$ ,  $A_5$ ) ports to any other port.

## Switching Characteristics

over recommended operating free-air temperature range,  $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $R_L = 200 \ \Omega$ ,  $C_L = 10 \text{ pF}$   
 (unless otherwise noted) (see Figures 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{pd}^{(2)}$	A or B	B or A		0.25		ns
$t_{PZH}$ , $t_{PZL}$	SEL	A or B	1.5		11.5	ns
$t_{PHZ}$ , $t_{PLZ}$	SEL	A or B	1		8.5	ns
$t_{sk(o)}^{(3)}$	A or B	B or A		0.1	0.2	ns
$t_{sk(p)}^{(4)}$				0.1	0.2	ns

- (1) All typical values are at  $V_{DD} = 3.3 \text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .  
 (2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).  
 (3) Output skew between center port ( $A_4$  to  $A_5$ ) to any other port  
 (4) Skew between opposite transitions of the same output in a given device  $|t_{PHL} - t_{PLH}|$

## Dynamic Characteristics

over recommended operating free-air temperature range,  $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS			TYP <sup>(1)</sup>	UNIT
$X_{TALK}$	$R_L = 100 \ \Omega$ ,	$f = 250 \text{ MHz}$ ,	See Figure 7	-41	dB
$O_{IRR}$	$R_L = 100 \ \Omega$ ,	$f = 250 \text{ MHz}$ ,	See Figure 8	-39	dB
BW	$R_L = 100 \ \Omega$ ,	See Figure 6		900	MHz

- (1) All typical values are at  $V_{DD} = 3.3 \text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

OPERATING CHARACTERISTICS

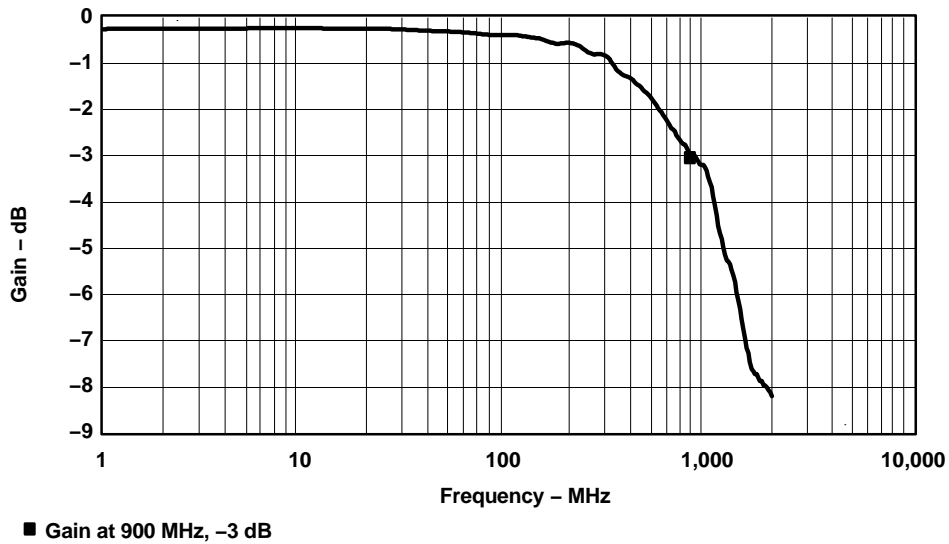


Figure 1. Gain vs Frequency

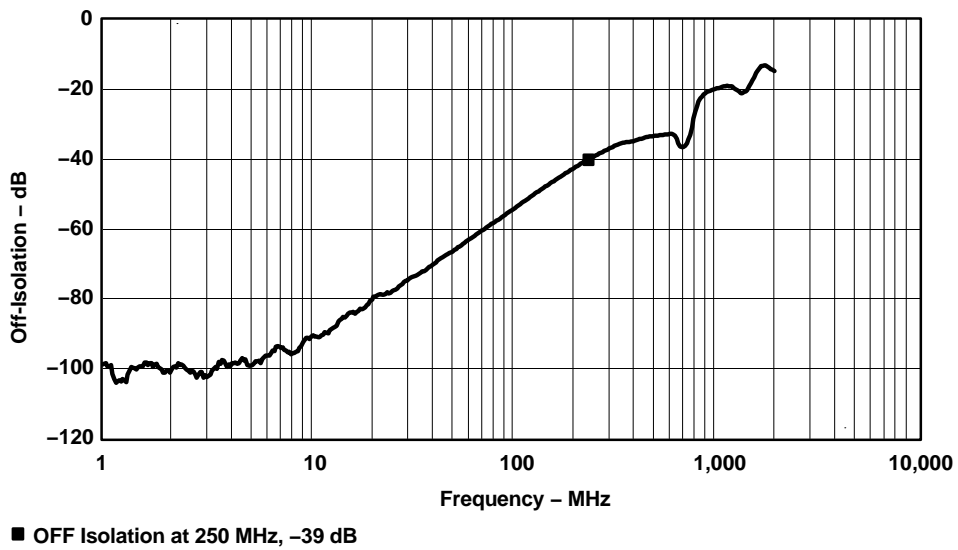


Figure 2. OFF Isolation vs Frequency

OPERATING CHARACTERISTICS (continued)

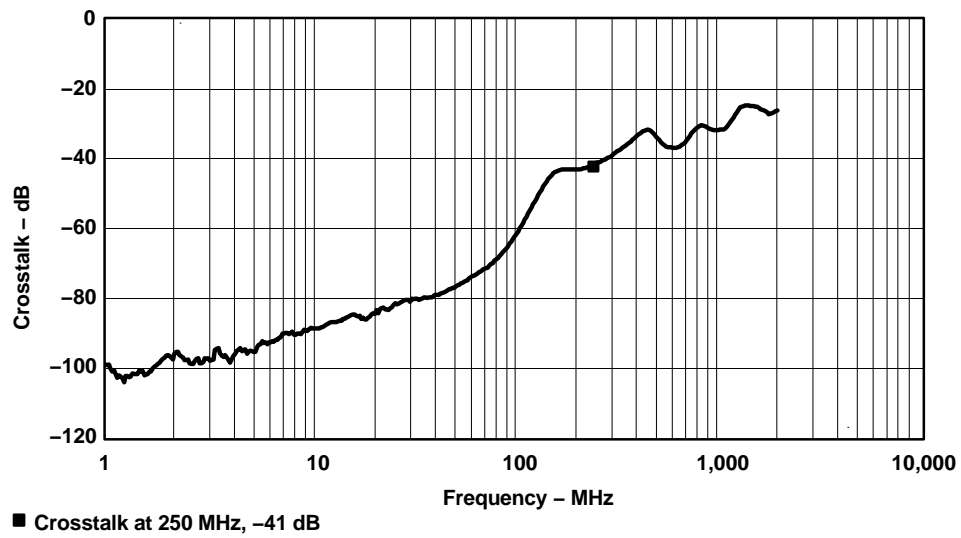
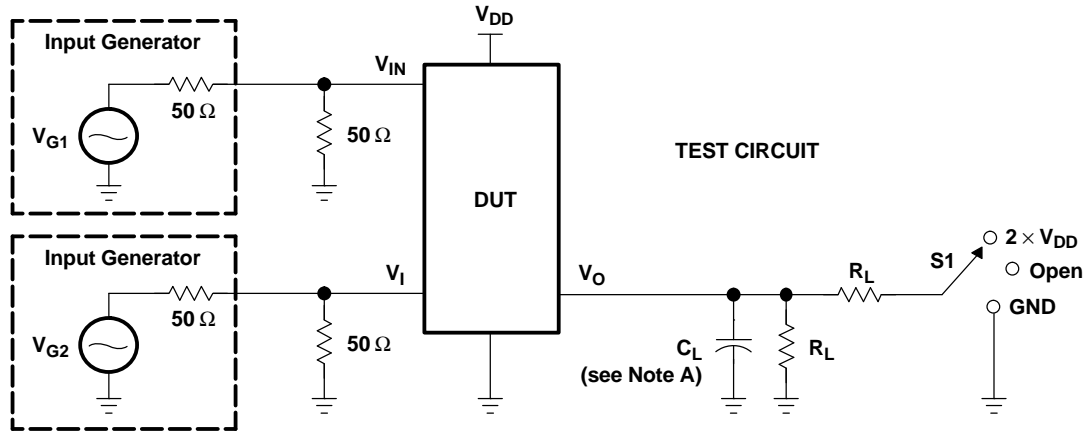
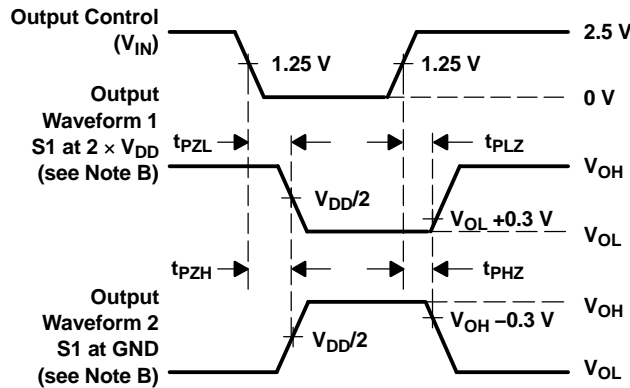


Figure 3. Crosstalk vs Frequency

**PARAMETER MEASUREMENT INFORMATION**  
**(Enable and Disable Times)**



TEST	V <sub>DD</sub>	S1	R <sub>L</sub>	V <sub>I</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>PLZ</sub> /t <sub>PZL</sub>	3.3 V ± 0.3 V	2 × V <sub>DD</sub>	200 Ω	GND	10 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	3.3 V ± 0.3 V	GND	200 Ω	V <sub>DD</sub>	10 pF	0.3 V



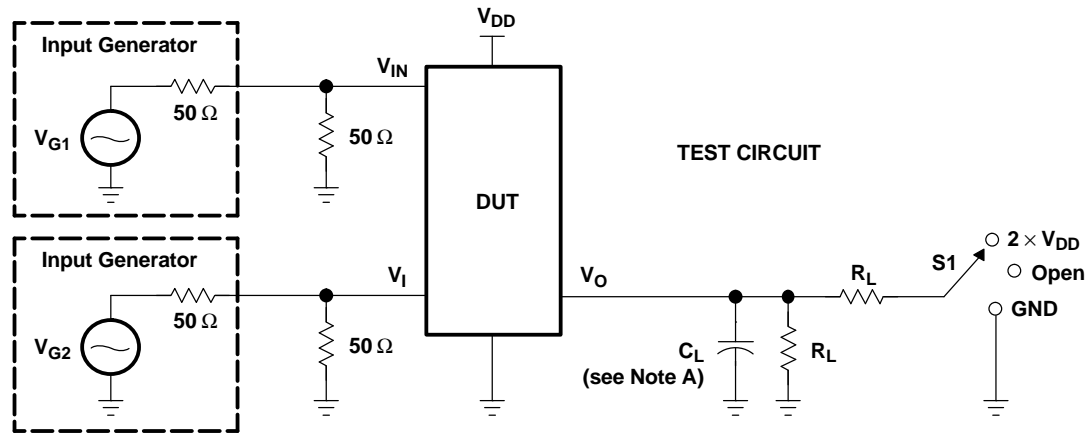
**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**

- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.  
D. The outputs are measured one at a time, with one transition per measurement.  
E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.  
F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.

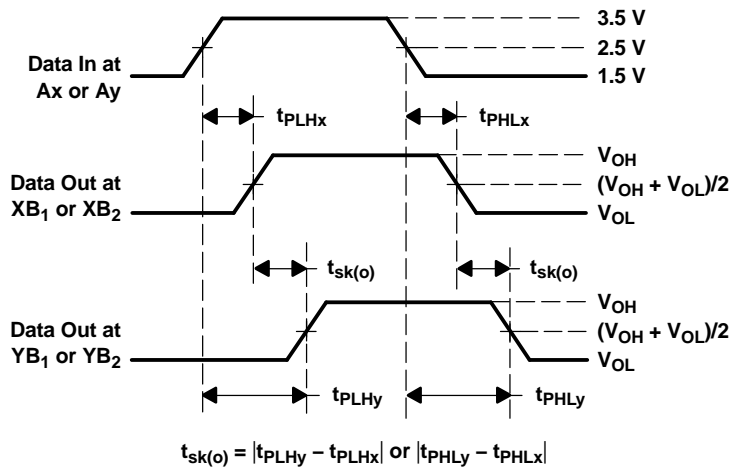
**Figure 4. Test Circuit and Voltage Waveforms**



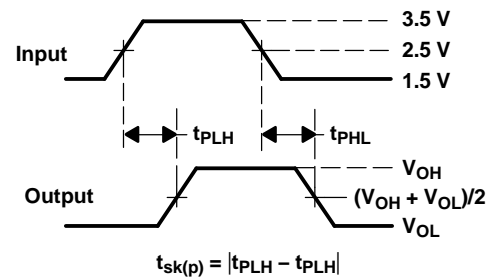
PARAMETER MEASUREMENT INFORMATION  
(Skew)



TEST	V <sub>DD</sub>	S1	R <sub>L</sub>	V <sub>I</sub>	C <sub>L</sub>
t <sub>sk(o)</sub>	3.3 V ± 0.3 V	Open	200 Ω	V <sub>DD</sub> or GND	10 pF
t <sub>sk(p)</sub>	3.3 V ± 0.3 V	Open	200 Ω	V <sub>DD</sub> or GND	10 pF



VOLTAGE WAVEFORMS  
OUTPUT SKEW [t<sub>sk(o)</sub>]

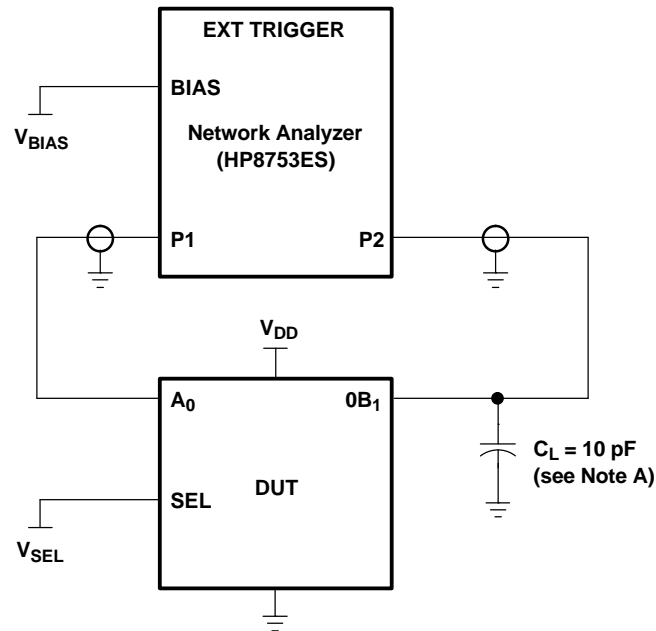


VOLTAGE WAVEFORMS  
PULSE SKEW [t<sub>sk(p)</sub>]

- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.  
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 5. Test Circuit and Voltage Waveforms

## PARAMETER MEASUREMENT INFORMATION



A.  $C_L$  includes probe and jig capacitance.

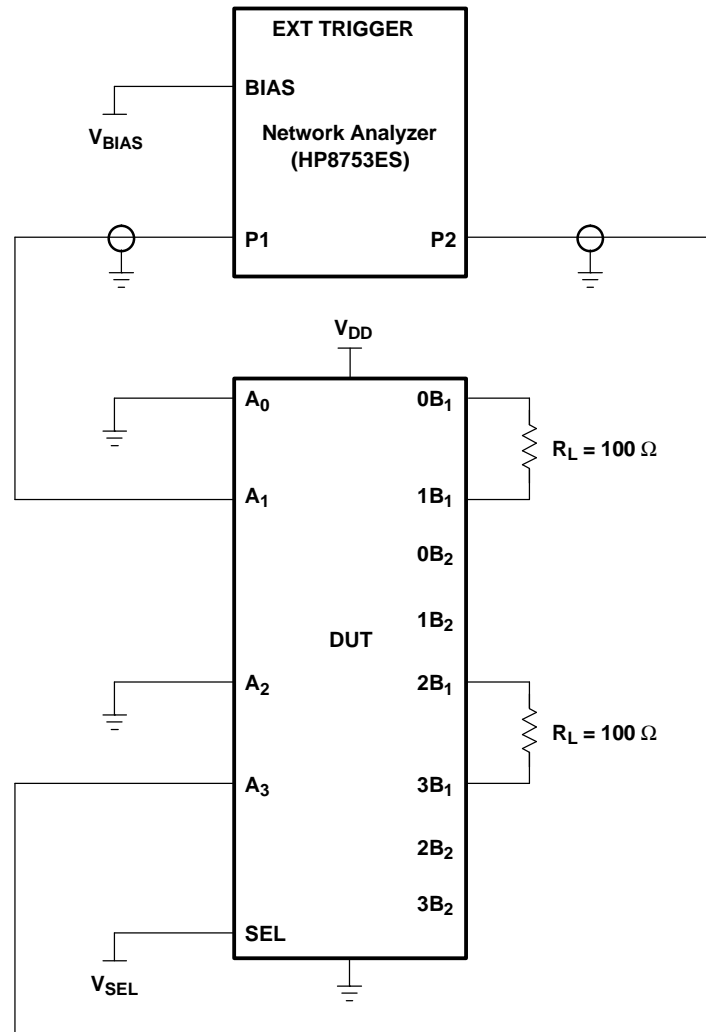
**Figure 6. Test Circuit for Frequency Response (BW)**

Frequency response is measured at the output of the ON channel. For example, when  $V_{SEL} = 0$  and  $A_0$  is the input, the output is measured at  $0B_1$ . All unused analog I/O ports are left open.

### HP8753ES Setup

Average = 4  
RBW = 3 kHz  
 $V_{BIAS} = 0.35$  V  
ST = 2 s  
P1 = 0 dBm

**PARAMETER MEASUREMENT INFORMATION (continued)**



- A.  $C_L$  includes probe and jig capacitance.
- B. A 50- $\Omega$  termination resistor is needed to match the loading of the network analyzer.

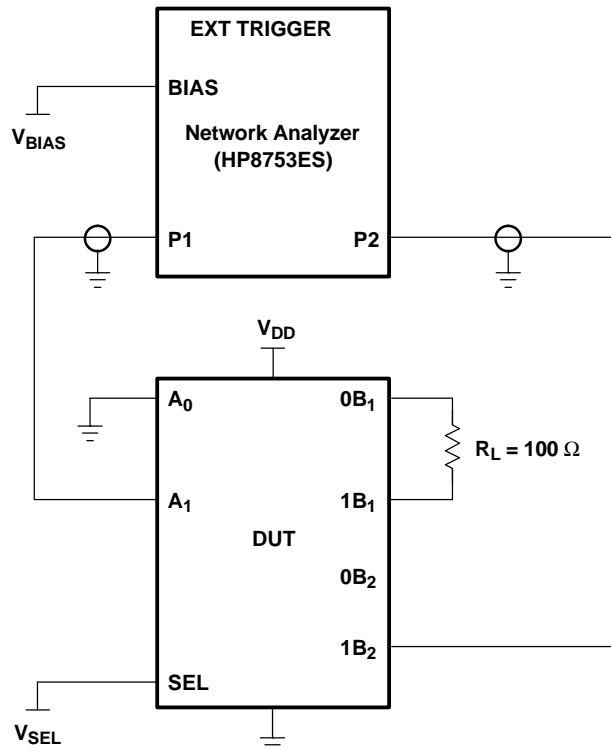
**Figure 7. Test Circuit for Crosstalk ( $X_{TALK}$ )**

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when  $V_{SEL} = 0$  and  $A_1$  is the input, the output is measured at  $A_3$ . All unused analog input (A) ports are connected to GND, and output (B) ports are left open.

**HP8753ES Setup**

Average = 4  
 RBW = 3 kHz  
 $V_{BIAS} = 0.35$  V  
 ST = 2 s  
 P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION (continued)



- A.  $C_L$  includes probe and jig capacitance.
- B. A 50- $\Omega$  termination resistor is needed to match the loading of the network analyzer.

Figure 8. Test Circuit for Off Isolation ( $O_{IRR}$ )

OFF isolation is measured at the output of the OFF channel. For example, when  $V_{SEL} = GND$  and  $A_1$  is the input, the output is measured at  $1B_2$ . All unused analog input (A) ports are connected to ground, and output (B) ports are left open.

HP8753ES Setup

Average = 4  
 RBW = 3 kHz  
 $V_{BIAS} = 0.35$  V  
 ST = 2 s  
 P1 = 0 dBm

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3L301DGG	ACTIVE	TSSOP	DGG	48	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3L301	<a href="#">Samples</a>
TS3L301DGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3L301	<a href="#">Samples</a>
TS3L301DGGRE4	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3L301	<a href="#">Samples</a>
TS3L301DGGRG4	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3L301	<a href="#">Samples</a>
TS3L301DGVR	ACTIVE	TVSOP	DGV	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TK301	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3L301DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
TS3L301DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3L301DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
TS3L301DGVR	TVSOP	DGV	48	2000	356.0	356.0	35.0



**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TS3L301DGG	DGG	TSSOP	48	40	530	11.89	3600	4.9

DGV (R-PDSO-G\*\*)

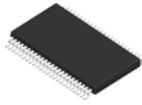
PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

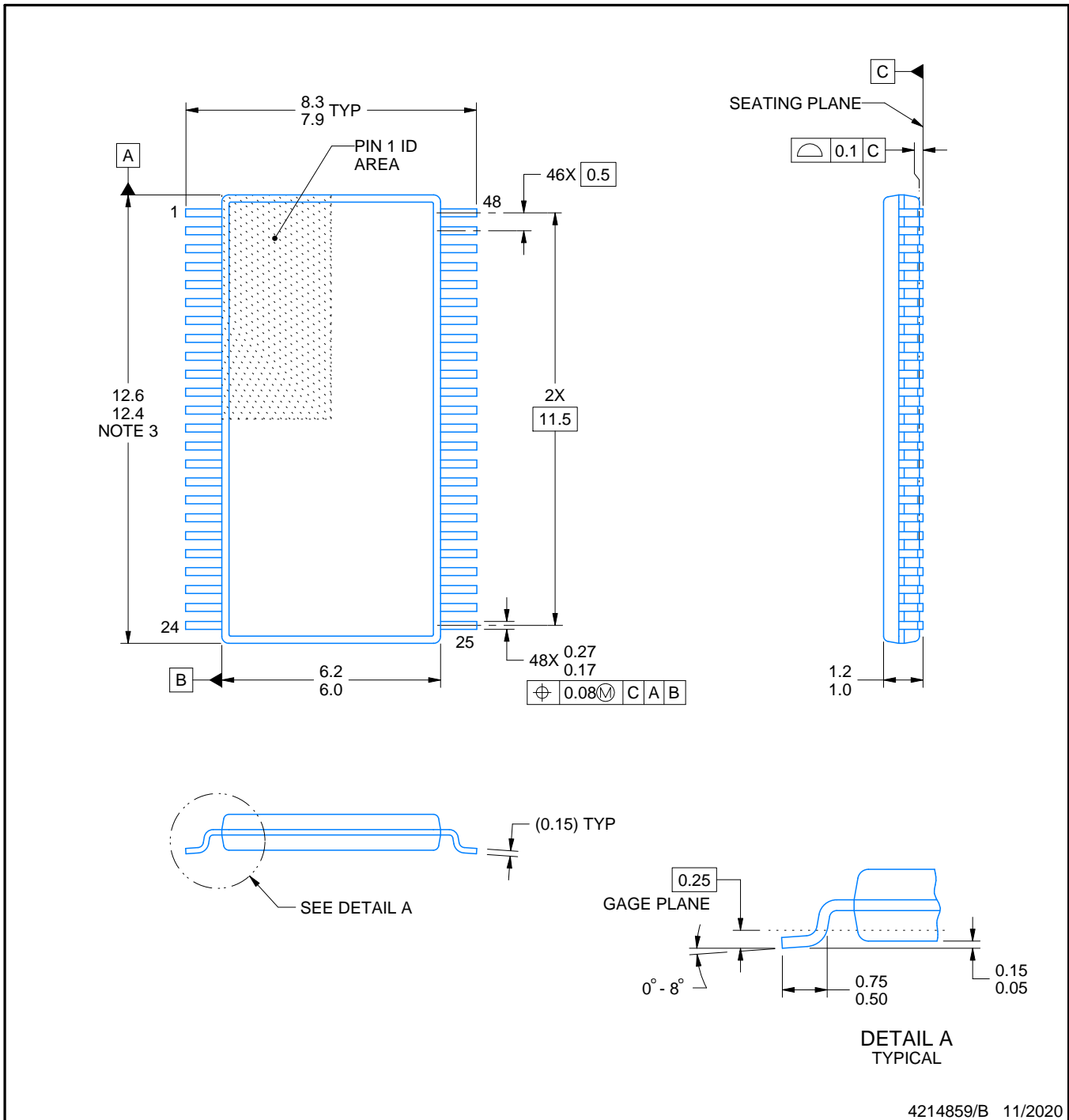


# DGG0048A

# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4214859/B 11/2020

### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated