TS3USB30 High-Speed USB 2.0 (480-MBPS)
1:2 Multiplexer/Demultiplexer Switch With Single Enable

1 Features
• \( V_{CC} \) Operation at 3 V and 4.3 V
• 1.8-V Compatible Control-Pin Inputs
• \( I_{OFF} \) Supports Partial Power-Down-Mode Operation
• \( R_{on} = 10 \, \Omega \) Maximum
• \( \Delta R_{on} < 0.35 \, \Omega \) Typical
• \( C_{io(ON)} = 7 \, pF \) Typical
• Low Power Consumption (1 \( \mu \)A Maximum)
• ESD Performance Tested Per JESD 22
  – 6000-V Human Body Model (HBM) (A114-B, Class II)
  – 1000-V Charged-Device Model (C101)
  – 250-V Machine Model (A115-A)
• –3-dB Bandwidth = 955 MHz Typical
• Packaged in 10-pin UQFN (1.4 mm × 1.8 mm)

2 Applications
• Routes Signals for USB 1.0, 1.1, and 2.0
• Mobile Industry Processor Interface (MIPI) Signal Routing

3 Description
The TS3USB30 is a high-bandwidth switch specially designed for the switching of high-speed USB 2.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os. The wide bandwidth (955 MHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

Device Information(1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TS3USB30</td>
<td>UQFN (10)</td>
<td>1.80 mm × 1.40 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (September 2010) to Revision F  Page

• Added Pin Configuration and Functions section, Handling Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section .......................................................... 1
• Removed Ordering Information table .......................................................... 1
5 Pin Configuration and Functions

Pin Functions

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>NAME</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>D1+</td>
<td>I/O</td>
<td>Data signal path</td>
</tr>
<tr>
<td>2</td>
<td>D2+</td>
<td>I/O</td>
<td>Data signal path</td>
</tr>
<tr>
<td>3</td>
<td>D+</td>
<td>I/O</td>
<td>Data signal path</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td></td>
<td>Ground</td>
</tr>
<tr>
<td>5</td>
<td>D−</td>
<td>I/O</td>
<td>Data signal path</td>
</tr>
<tr>
<td>6</td>
<td>D2−</td>
<td>I/O</td>
<td>Data signal path</td>
</tr>
<tr>
<td>7</td>
<td>D1−</td>
<td>I/O</td>
<td>Data signal path</td>
</tr>
<tr>
<td>8</td>
<td>OE</td>
<td>I</td>
<td>Bus-Switch Enable</td>
</tr>
<tr>
<td>9</td>
<td>VCC</td>
<td></td>
<td>Voltage Supply</td>
</tr>
<tr>
<td>10</td>
<td>S</td>
<td>I</td>
<td>Select Input</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{CC}}) Supply voltage</td>
<td>(-0.5)</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{IN}}) Control input voltage(^{(2)}) (\text{(V_{\text{IN}})} &lt; 0)</td>
<td>(-0.5)</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{IO}}) Signal path I/O voltage(^{(2)}) (\text{(V_{\text{IO}})} &lt; 0)</td>
<td>(-0.5) (V_{\text{CC}} + 0.3)</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(I_{\text{IK}}) Control input clamp current</td>
<td>(-50)</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>(I_{\text{I/O}}) I/O port clamp current</td>
<td>(-50)</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>(I_{\text{IO}}) ON-state switch current(^{(5)})</td>
<td>(\pm 64)</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Continuous current through (V_{\text{CC}}) or GND</td>
<td>(\pm 100)</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>(T_{\text{stg}}) Storage temperature</td>
<td>(-65) (150)</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground, unless otherwise specified.

(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(4) \(V_I\) and \(V_O\) are used to denote specific conditions for \(V_{\text{IO}}\).

(5) \(I_I\) and \(I_O\) are used to denote specific conditions for \(I_{\text{I/O}}\).

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{ESD}}) Electrostatic discharge</td>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001</td>
<td>6000</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101</td>
<td>1000</td>
<td>V</td>
</tr>
</tbody>
</table>

6.3 Recommended Operating Conditions

See \(^{(1)}\).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{CC}}) Supply voltage</td>
<td>3</td>
<td>4.3</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{IH}}) High-level control input voltage</td>
<td>(V_{\text{CC}} = 3) (V) to 3.6 (V)</td>
<td>1.3</td>
<td>(V_{\text{CC}})</td>
</tr>
<tr>
<td>(V_{\text{IL}}) Low-level control input voltage</td>
<td>(V_{\text{CC}} = 3) (V) to 3.6 (V)</td>
<td>0</td>
<td>0.5 (V_{\text{CC}})</td>
</tr>
<tr>
<td>(V_{\text{IO}}) Data input/output voltage</td>
<td>(V_{\text{CC}} = 4.3) (V)</td>
<td>0</td>
<td>0.7 (V_{\text{CC}})</td>
</tr>
<tr>
<td>(T_{\text{A}}) Operating free-air temperature</td>
<td>(-40) (85)</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

(1) All unused control inputs of the device must be held at \(V_{\text{CC}}\) or GND to ensure proper device operation. Refer to Implications of Slow or Floating CMOS Inputs (SCBA004).
6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TS3USB30 RSW (UQFN)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JA}$ Junction-to-ambient thermal resistance</td>
<td>117.6</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JC(top)}$ Junction-to-case (top) thermal resistance</td>
<td>67.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JB}$ Junction-to-board thermal resistance</td>
<td>23.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JT}$ Junction-to-top characterization parameter</td>
<td>1.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JB}$ Junction-to-board characterization parameter</td>
<td>23.2</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics (SPRA953).

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP(2)</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$ Control input clamp voltage</td>
<td>$V_{CC} = 3 , V, I_c = –18 , mA$</td>
<td>–1.2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IN}$ Control inputs</td>
<td>$V_{CC} = 4.3 , V, 0 , V$, $V_{IN} = 0 , \text{to} , 4.9 , V$</td>
<td>±1</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OZ}$ D+ and D– OFF-state leakage current (3)</td>
<td>$V_{CC} = 4.3 , V, V_D = 0 , \text{to} , 3.6 , V, V_I = 0$, Switch OFF</td>
<td>±2</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OFF}$ Powered off leakage current</td>
<td>$V_{CC} = 0 , V, V_D = 0 , \text{to} , 4.3 , V$, $V_I = 0$, $V_{IN} = V_{CC}$ or GND</td>
<td>±2</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{CC}$ Supply current</td>
<td>$V_{CC} = 4.3 , V, I_{IO} = 0$, Switch ON or OFF</td>
<td>1</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Delta I_{CC}$ (4) Control inputs</td>
<td>$V_{CC} = 4.3 , V, V_{IN} = 2.6 , V$</td>
<td>10</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{in}$ Control inputs digital input capacitance</td>
<td>$V_{CC} = 0 , V, V_{IN} = V_{CC}$ or GND</td>
<td>1</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{OS}(OFF)$ OFF-state input capacitance</td>
<td>$V_{CC} = 3.3 , V, V_{IO} = 3.3 , V$ or 0, Switch OFF</td>
<td>2</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{ON}(ON)$ ON-state input capacitance</td>
<td>$V_{CC} = 3.3 , V, V_{IO} = 3.3 , V$ or 0, Switch ON</td>
<td>7</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{ON}$ ON-state resistance (5)</td>
<td>$V_{CC} = 3 , V, V_I = 0.4, I_O = –8 , mA$</td>
<td>6</td>
<td>10 Ω</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Delta R_{ON}$ ON-state resistance match between channels</td>
<td>$V_{CC} = 3 , V, V_I = 0.4, I_O = –8 , mA$</td>
<td>0.35</td>
<td>Ω</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{ON(flat)}$ ON-state resistance flatness</td>
<td>$V_{CC} = 3 , V, V_I = 0 , \text{or} , 1 , V, I_O = –8 , mA$</td>
<td>2</td>
<td>Ω</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) $V_{IN}$ and $I_{IN}$ refer to control inputs. $V_{I}$, $V_{O}$, $I_{c}$, and $I_{O}$ refer to data pins.
(2) All typical values are at $V_{CC} = 3.3 \, V$ (unless otherwise noted), $T_A = 25°C$.
(3) For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}$ or GND.
(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

6.6 Dynamic Electrical Characteristics

over operating range, $T_A = -40°C$ to 85°C, $V_{CC} = 3.3 \, V ± 10\%$, GND = 0 V

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>TYP(1)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$X_{TALK}$ Crosstalk</td>
<td>$R_L = 50 , \Omega$, $f = 240 , MHz$, See Figure 6</td>
<td>–56</td>
<td>dB</td>
</tr>
<tr>
<td>$O_{ISO}$ OFF isolation</td>
<td>$R_L = 50 , \Omega$, $f = 240 , MHz$, See Figure 5</td>
<td>–39</td>
<td>dB</td>
</tr>
<tr>
<td>$BW$ Bandwidth (–3 dB)</td>
<td>$R_L = 50 , \Omega$, $C_L = 5 , pF$, See Figure 7</td>
<td>955</td>
<td>MHz</td>
</tr>
</tbody>
</table>

(1) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.
### 6.7 Switching Characteristics

over operating range, \( T_A = -40^\circ C \) to \( 85^\circ C \), \( V_{CC} = 3.3 \text{ V} \pm 10\% \), \( GND = 0 \text{ V} \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP(^{(1)})</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{pd} ) Propagation delay(^{(2)})(^{(3)})</td>
<td>( R_L = 50 \text{ } \Omega, C_L = 5 \text{ pF} ), See Figure 8</td>
<td>0.25</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{ON} ) Line enable time, SEL to D, nD</td>
<td>( R_L = 50 \text{ } \Omega, C_L = 5 \text{ pF} ), See Figure 4</td>
<td>30</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{OFF} ) Line disable time, SEL to D, nD</td>
<td>( R_L = 50 \text{ } \Omega, C_L = 5 \text{ pF} ), See Figure 4</td>
<td>25</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{ON} ) Line enable time, ( OE ) to D, nD</td>
<td>( R_L = 50 \text{ } \Omega, C_L = 5 \text{ pF} ), See Figure 4</td>
<td>30</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{OFF} ) Line disable time, ( OE ) to D, nD</td>
<td>( R_L = 50 \text{ } \Omega, C_L = 5 \text{ pF} ), See Figure 4</td>
<td>25</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{SK(O)} ) Output skew between center port to any other port(^{(2)})</td>
<td>( R_L = 50 \text{ } \Omega, C_L = 5 \text{ pF} ), See Figure 9</td>
<td>50</td>
<td></td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>( t_{SK(P)} ) Skew between opposite transitions of the same output ( (t_{PHL} - t_{PLH})(^{(2)})</td>
<td>( R_L = 50 \text{ } \Omega, C_L = 5 \text{ pF} ), See Figure 9</td>
<td>20</td>
<td></td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>( t_j ) Total jitter(^{(2)})</td>
<td>( R_L = 50 \text{ } \Omega, C_L = 5 \text{ pF} ), ( t_R = t_F = 500 \text{ ps at 480 Mbps (PRBS = 2}^{15} - 1))</td>
<td>20</td>
<td></td>
<td>ps</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.

\(^{(2)}\) Specified by design

\(^{(3)}\) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

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**Product Folder Links:** [TS3USB30](https://www.ti.com)
6.8 Typical Characteristics

Figure 1. Gain vs Frequency

Figure 2. OFF Isolation

Figure 3. Crosstalk
7 Parameter Measurement Information

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z₀ = 50 Ω, t<sub>r</sub> < 5 ns, t<sub>f</sub> < 5 ns.

B. C<sub>L</sub> includes probe and jig capacitance.

**Figure 4. Turn-On (t<sub>ON</sub>) and Turn-Off Time (t<sub>OFF</sub>)**

**Figure 5. OFF Isolation (O<sub>ISO</sub>)**

**Figure 6. Crosstalk (X<sub>TALK</sub>)**
Parameter Measurement Information (continued)

Network Analyzer

Source Signal

50 Ω

50 Ω

Channel ON: 1D to D
VCTRL = GND

Network Analyzer Setup
Source Power = 0 dBm
(632-mV P-P at 50-Ω load)
DC Bias = 350 mV

Figure 7. Bandwidth (BW)

Input

50% 50%

800 mV

400 mV

Output

50% 50%

VOH

VOL

tPLH

tPHL

Figure 8. Propagation Delay
Parameter Measurement Information (continued)

Figure 9. Skew Test
Parameter Measurement Information (continued)

Figure 10. ON-State Resistance ($R_{ON}$)

Figure 11. OFF-State Leakage Current

Figure 12. Capacitance
8 Detailed Description

8.1 Overview
The TS3USB30 is a high-bandwidth switch specially designed for the switching and isolating of high-speed USB 2.0 signals in systems with limited USB I/Os. The wide bandwidth (955 MHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs or from two different hosts to one corresponding output. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

8.2 Functional Block Diagram

8.3 Feature Description
The TS3USB30 has a bus-switch enable pin, OE, that can place the signal paths in high impedance. This allows the user to isolate the bus when it is not in use and consume less current.

8.4 Device Functional Modes
The device functional modes are shown in Table 1.

<table>
<thead>
<tr>
<th>S</th>
<th>OE</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>H</td>
<td>Disconnect</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>D = D1</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>D = D2</td>
</tr>
</tbody>
</table>
9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

There are many USB applications in which the USB hubs or controllers have a limited number of USB I/Os. The TS3USB30 solution can effectively expand the limited USB I/Os by switching between multiple USB buses in order to interface them to a single USB hub or controller. TS3USB221 can also be used to connect a single controller to two USB connectors or controllers.

9.2 Typical Application

![Figure 13. Application Diagram](ts3usb30.png)

9.2.1 Design Requirements

Design requirements of the USB 1.0, 1.1, and 2.0 standards should be followed. TI recommends that the digital control pins S and OE be pulled up to \( V_{CC} \) or down to GND to avoid undesired switch positions that could result from the floating pin.

9.2.2 Detailed Design Procedure

The TS3USB30 can be properly operated without any external components. However, it is recommended that unused pins should be connected to ground through a 50-\( \Omega \) resistor to prevent signal reflections back into the device.
9.2.3 Application Curves

Figure 14. Eye Pattern: 480-Mbps USB Signal With No Switch (Through Path)

Figure 15. Eye Pattern: 480-Mbps USB Signal With Switch NC Path

Figure 16. Eye Pattern: 480-Mbps USB Signal With Switch NO Path
10 Power Supply Recommendations

Power to the device is supplied through the V\textsubscript{CC} pin and should follow the USB 1.0, 1.1, and 2.0 standards. TI recommends placing a bypass capacitor as close as possible to the supply pin V\textsubscript{CC} to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

11 Layout

11.1 Layout Guidelines

Place supply bypass capacitors as close to V\textsubscript{CC} pin as possible and avoid placing the bypass caps near the D+ and D– traces.

The high speed D+ and D– traces should always be matched lengths and must be no more than 4 inches; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, the impedance of D+ and D– traces should match the cable characteristic differential impedance for optimal performance.

Route the high-speed USB signals using a minimum of vias and corners which will reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal’s transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mm.

Route all high-speed USB signal traces over continuous planes (V\textsubscript{CC} or GND), with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended: two signal layers separated by a ground and power layer. The majority of signal traces should run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimize the number of signal vias reduces EMI by reducing inductance at high frequencies. For more information on layout guidelines, see High Speed Layout Guidelines (SCAA082) and USB 2.0 Board Design and Layout Guidelines (SPRAAR7).
11.2 Layout Example

Figure 17. Layout Recommendation
12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

• High Speed Layout Guidelines, SCAA082
• USB 2.0 Board Design and Layout Guidelines, SPRAAR7

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — Ti Glossary. This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TS3USB30RSWR</td>
<td>ACTIVE</td>
<td>UQFN</td>
<td>RSW</td>
<td>10</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>(L67, L60)</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substances do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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</thead>
<tbody>
<tr>
<td>TS3USB30RWR</td>
<td>UQFN</td>
<td>RSW</td>
<td>10</td>
<td>3000</td>
<td>180.0</td>
<td>9.5</td>
<td>1.6</td>
<td>2.0</td>
<td>4.0</td>
<td>4.0</td>
<td>8.0</td>
<td>Q1</td>
</tr>
<tr>
<td>TS3USB30RWR</td>
<td>UQFN</td>
<td>RSW</td>
<td>10</td>
<td>3000</td>
<td>179.0</td>
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<td>1.7</td>
<td>2.1</td>
<td>0.7</td>
<td>4.0</td>
<td>8.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.

A0: Dimension designed to accommodate the component width
B0: Dimension designed to accommodate the component length
K0: Dimension designed to accommodate the component thickness
W: Overall width of the carrier tape
P1: Pitch between successive cavity centers

Pack Materials-Page 1
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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</thead>
<tbody>
<tr>
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<td>UQFN</td>
<td>RSW</td>
<td>10</td>
<td>3000</td>
<td>184.0</td>
<td>184.0</td>
<td>19.0</td>
</tr>
<tr>
<td>TS3USB30RSWR</td>
<td>UQFN</td>
<td>RSW</td>
<td>10</td>
<td>3000</td>
<td>203.0</td>
<td>203.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-288 variation UDEE, except minimum package height.

www.ti.com
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
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