1 Features

- $V_{CC}$ Operation at 3 V and 4.3 V
- 1.8-V Compatible Control-Pin Inputs
- $I_{OFF}$ Supports Partial Power-Down Mode Operation
- $r_{on} = 10 \Omega$ Maximum
- $\Delta r_{on} < 0.35 \Omega$ Typical
- $C_{io(ON)} = 6 \text{ pF}$ Typical
- Low Power Consumption (1 $\mu$A Maximum)
- ESD Performance Tested Per JESD 22
  - 6000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
  - 250-V Machine Model (A115-A)
- Wide $-3$-dB Bandwidth = 1220 MHz Typical
- Packaged in 8-Pin TQFN (1.5 mm × 1.5 mm)

2 Applications

Bus Isolation for USB 1.0, 1.1, and 2.0

3 Description

The TS3USB31 is a 1:1 SPST high-bandwidth switch specially designed for the switching of high-speed USB 2.0 signals. This device comes in a small UQFN package for use in a handset or consumer applications, such as cell phones, digital cameras, and notebooks with hubs. The wide bandwidth (750 MHz) of this switch allows signals to pass with minimum edge and phase distortion. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TS3USB31</td>
<td>UQFN (8)</td>
<td>1.50 mm × 1.50 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision D (July 2008) to Revision E

- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ...................................................... 1
5 Pin Configuration and Functions

Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>NAME</strong></td>
<td><strong>NO.</strong></td>
<td><strong>DESCRIPTION</strong></td>
</tr>
<tr>
<td>OE</td>
<td>1</td>
<td>I</td>
</tr>
<tr>
<td>D+</td>
<td>3</td>
<td>I/O</td>
</tr>
<tr>
<td>D–</td>
<td>5</td>
<td>I/O</td>
</tr>
<tr>
<td>HSD+</td>
<td>2</td>
<td>I/O</td>
</tr>
<tr>
<td>HSD–</td>
<td>6</td>
<td>I/O</td>
</tr>
<tr>
<td>N.C.</td>
<td>7</td>
<td>—</td>
</tr>
<tr>
<td>GND</td>
<td>4</td>
<td>—</td>
</tr>
<tr>
<td>VCC</td>
<td>8</td>
<td>I/O</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CC} ) Supply voltage</td>
<td>–0.5</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IN} ) Control input voltage (^{(2)(3)})</td>
<td>–0.5</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>( V_{I/O} ) Switch I/O voltage (^{(2)(3)(4)})</td>
<td>HSD+, HSD–</td>
<td>–0.5</td>
<td>( V_{CC} + 0.3 )</td>
</tr>
<tr>
<td></td>
<td>D+, D– when ( V_{CC} &gt; 0 )</td>
<td>–0.5</td>
<td>( V_{CC} + 0.3 )</td>
</tr>
<tr>
<td></td>
<td>D+, D– when ( V_{CC} = 0 )</td>
<td>5.25</td>
<td></td>
</tr>
<tr>
<td>( I_{IK} ) Control input clamp current</td>
<td>( V_{IN} &lt; 0 )</td>
<td>–50</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{I/O} ) I/O port clamp current</td>
<td>( V_{I/O} &lt; 0 )</td>
<td>–50</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{I/O} ) ON-state switch current (^{(5)})</td>
<td>&lt;100</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Continuous current through ( V_{CC} ) or GND</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>( T_{stg} ) Storage temperature</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) All voltages are with respect to ground, unless otherwise specified.

\(^{(3)}\) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

\(^{(4)}\) \( V_{I} \) and \( V_{O} \) are used to denote specific conditions for \( V_{I/O} \).

\(^{(5)}\) \( I_{I} \) and \( I_{O} \) are used to denote specific conditions for \( I_{I/O} \).

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>( V(ESD) ) Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (^{(1)})</td>
<td>±6000</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101 (^{(2)})</td>
<td>±1000</td>
<td>V</td>
</tr>
</tbody>
</table>

\(^{(1)}\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

\(^{(2)}\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CC} ) Supply voltage</td>
<td>3</td>
<td>4.3</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IH} ) High-level control input voltage</td>
<td>( V_{CC} = 3 , \text{V to 3.6 V} )</td>
<td>1.3</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>( V_{CC} = 4.3 , \text{V} )</td>
<td>1.7</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IL} ) Low-level control input voltage</td>
<td>( V_{CC} = 3 , \text{V to 3.6 V} )</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>( V_{CC} = 4.3 , \text{V} )</td>
<td>0.7</td>
<td>V</td>
</tr>
<tr>
<td>( V_{I/O} ) Data input/output voltage</td>
<td>0</td>
<td>( V_{CC} )</td>
<td>V</td>
</tr>
<tr>
<td>( T_{A} ) Operating free-air temperature</td>
<td>–40</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) All unused control inputs of the device must be held at \( V_{CC} \) or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs (SCBA004).
6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TS3USB31</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{JUA} Junction-to-ambient thermal resistance</td>
<td>115.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>R_{JUC(top)} Junction-to-case (top) thermal resistance</td>
<td>38.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>R_{JUB} Junction-to-board thermal resistance</td>
<td>65.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>\psi_{JT} Junction-to-top characterization parameter</td>
<td>5.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>\psi_{JB} Junction-to-board characterization parameter</td>
<td>67.9</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP(2)</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{IK} Input Clamp Voltage</td>
<td>V_{CC} = 3 V, I_{L} = –18 mA</td>
<td>–1.2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>I_{IN} Control inputs</td>
<td>V_{CC} = 4.3 V or 0V, V_{IN} = 0 to 4.3 V</td>
<td>±1</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>I_{OZ}(3)</td>
<td>V_{CC} = 4.3 V, V_{O} = 0 to 3.6 V, V_{I} = 0, Switch OFF</td>
<td>±1</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>I_{OFF} D+ and D–</td>
<td>V_{CC} = 0 V, V_{O} = 0 V to 4.3 V, V_{I} = 0, V_{IN} = V_{CC} or GND</td>
<td>±2</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>I_{CC}</td>
<td>V_{CC} = 4.3 V, I_{IO} = 0, Switch ON or OFF</td>
<td>1</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>\Delta I_{CC}(4) Control inputs</td>
<td>V_{CC} = 4.3 V, V_{IN} = 2.6 V</td>
<td>10</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>C_{in} Off-state Input/Output Capacitance</td>
<td>V_{CC} = 3.3 V, V_{IO} = 3.3 V or 0, Switch OFF</td>
<td>1</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>C_{o(ON)} On-state Input/Output Capacitance</td>
<td>V_{CC} = 3.3 V, V_{IO} = 3.3 V or 0, Switch ON</td>
<td>6</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>f_{on}(5) On-State Resistance</td>
<td>V_{CC} = 3 V, V_{I} = 0.4 V, I_{O} = –8 mA</td>
<td>6</td>
<td>10</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>\Delta r_{on} Channel Match</td>
<td>V_{CC} = 3 V, V_{I} = 0.4 V, I_{O} = –8 mA</td>
<td>0.35</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>f_{on(flat)} On-State Resistance Flatness</td>
<td>V_{CC} = 3 V, V_{I} = 0 V or 1 V, I_{O} = –8 mA</td>
<td>2</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
</tbody>
</table>

(1) V_{IN} and I_{IN} refer to control inputs. V_{i}, V_{O}, I_{L}, and I_{O} refer to data pins.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_{A} = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

6.6 Dynamic Electrical Characteristics

over operating range, T_{A} = –40°C to 85°C, V_{CC} = 3.3 V ± 10%, GND = 0 V

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>TYP(1)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>X_{TALK}</td>
<td>Crosstalk</td>
<td>R_{L} = 50 Ω, f = 240 MHz, See Figure 6</td>
<td>–53</td>
</tr>
<tr>
<td>O_{IR}</td>
<td>OFF isolation</td>
<td>R_{L} = 50 Ω, f = 240 MHz, See Figure 5</td>
<td>–30</td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth (–3 dB)</td>
<td>R_{L} = 50 Ω, C_{L} = 5 pF, See Figure 7</td>
<td>1220</td>
</tr>
</tbody>
</table>

(1) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.
6.7 Switching Characteristics

over operating range, $T_A = -40^\circ C$ to $85^\circ C$, $V_{CC} = 3.3 \text{ V} \pm 10\%$, $\text{GND} = 0 \text{ V}$

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP$^{(1)}$</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{pd}$</td>
<td>$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, See Figure 8</td>
<td>0.25</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{ON}$</td>
<td>$O\overline{E}$ to D, nD</td>
<td>30</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{OFF}$</td>
<td>$O\overline{E}$ to D, nD</td>
<td>25</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{SK(O)}$</td>
<td>$O\overline{E}$ to D, nD</td>
<td>50</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{SK(P)}$</td>
<td>$O\overline{E}$ to D, nD</td>
<td>20</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_J$</td>
<td>$O\overline{E}$ to D, nD</td>
<td>200</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

6.8 Typical Characteristics

Figure 1. Insertion Loss / Bandwidth

Figure 2. OFF Isolation
Typical Characteristics (continued)

Figure 3. Crosstalk
7 Parameter Measurement Information

Figure 4. Turnon (t_{ON}) and Turnoff Time (t_{OFF})

Figure 5. OFF Isolation (O_{IRR})

Figure 6. Crosstalk (X_{TALK})
Parameter Measurement Information (continued)

Channel ON: 1D to D
\( V(OE) = GND \)

Network Analyzer Setup
Source Power = 0 dBm
(632-mV P-P at 50-\( \Omega \) load)
DC Bias = 350 mV

Figure 7. Bandwidth (BW)

Figure 8. Propagation Delay
Parameter Measurement Information (continued)

\[ t_{SK(P)} = |t_{PHL}| - |t_{PLH}| \]

\[ t_{SK(O)} = |t_{PHL1}| - |t_{PLH2}| \]

Figure 9. Skew Test

\[ r_{on} = \frac{V_{IN} - V_{OUT} \text{ or } V_{OUT1}}{I_{IN}} \]

\[ V_{(OE)} = V_{IH} \text{ or } V_{IL} \]

Figure 10. ON-State Resistance (\( r_{on} \))
Parameter Measurement Information (continued)

OFF - State Leakage Current
Channel OFF
V(OE) = V\text{IH} or V\text{IL}

Capacitance is measured at 1D, 2D, D, and OE inputs during ON and OFF conditions

Figure 11. OFF-State Leakage Current

Figure 12. Capacitance
8 Detailed Description

8.1 Overview
The TS3USB31 is a 1:1 SPST high-bandwidth switch specially designed for the switching of high-speed USB 2.0 signals. The switch is bidirectional and offers little or no attenuation of the high-speed signals. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

8.2 Functional Block Diagram

8.3 Feature Description

8.3.1 I_{OFF} Supports Partial Power-Down Mode Operation
When $V_{CC} = 0$ V, the signal path is placed in a high impedance state which isolates the bus. This allows signals to be present on the D+/− and HSD+/− pins before the device is powered up without damaging the device.

8.4 Device Functional Modes
The TS3USB31 device has two modes that are digitally controlled by the OE pin. Setting the OE pin High isolates the signal path by a high impedance state.

<table>
<thead>
<tr>
<th>OE</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>Disconnect</td>
</tr>
<tr>
<td>L</td>
<td>D+, D− = HSD+, HSD−</td>
</tr>
</tbody>
</table>
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information
The TS3USB31 device is used to isolate a USB bus when it is not in use to prevent two different USB devices from interfering with each other.

9.2 Typical Application

9.2.1 Design Requirements
Design requirements of the USB 1.0, 1.1, and 2.0 standards should be followed. TI recommends that the digital control pin OE be pulled up to \( V_{CC} \) or down to ground to avoid undesired switch positions that could result from the floating pin.

9.2.2 Detailed Design Procedure
The TS3USB31 can be properly operated without any external components. However, it is recommended that unused pins be connected to ground through a 50-\( \Omega \) resistor to prevent signal reflections back into the device. The N.C pin should be left floating.
Typical Application (continued)

9.2.3 Application Curves

Figure 14. Eye Pattern: 480-Mbps USB Signal With No Switch (Through Path)

Figure 15. Eye Pattern: 480-Mbps USB Signal With Switch NO Path
10 Power Supply Recommendations

Power to the device is supplied through the $V_{CC}$ pin. TI recommends placing a bypass capacitor as close as possible to the supply pin $V_{CC}$ to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

This device doesn't require any power sequencing with respect to other devices in the system due to its power off isolation feature which allows signals to be present on the D+/- and HSD+/- pins before the device is powered up without damaging the device.

11 Layout

11.1 Layout Guidelines

Place supply bypass capacitors as close to $V_{CC}$ pin as possible and avoid placing the bypass caps near the D+ and D– traces.

The high-speed D+ and D– traces should always be of equal length and must be no more than 4 inches; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, the impedance of D+ and D– traces should match the cable characteristic differential impedance for optimal performance.

Route the high-speed USB signals using a minimum of vias and corners which will reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices, or IC’s that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mm.

Route all high-speed USB signal traces over continuous planes ($V_{CC}$ or GND), with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended: two signal layers separated by a ground layer and a power layer. The majority of signal traces should run on a single layer, preferably top layer. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies. For more information on layout guidelines, see High Speed Layout Guidelines (SCAA082) and USB 2.0 Board Design and Layout Guidelines (SPRAAR7).
11.2 Layout Example

Figure 16. Layout Recommendation
12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation
For related documentation see the following

- High Speed Layout Guidelines (SCAA082)
- USB 2.0 Board Design and Layout Guidelines (SPRAAR7)

12.2 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resource
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

- **TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

- **Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks
E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

⚠️ These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

**SLYZ022 — TI Glossary.**
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/ Ball material (3)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TS3USB31RSER</td>
<td>ACTIVE</td>
<td>UQFN</td>
<td>RSE</td>
<td>8</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>NIPDAUAG</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>L9</td>
</tr>
<tr>
<td>TS3USB31RSERG4</td>
<td>ACTIVE</td>
<td>UQFN</td>
<td>RSE</td>
<td>8</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>L9</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OB Solete:** TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>Dimension designed to accommodate the component width</td>
</tr>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
</tr>
</tbody>
</table>

### PACKAGE MATERIALS INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TS3USB31RSER</td>
<td>UQFN</td>
<td>RSE</td>
<td>8</td>
<td>3000</td>
<td>180.0</td>
<td>8.4</td>
<td>1.7</td>
<td>1.7</td>
<td>0.7</td>
<td>4.0</td>
<td>8.0</td>
<td>Q2</td>
</tr>
<tr>
<td>TS3USB31RSER</td>
<td>UQFN</td>
<td>RSE</td>
<td>8</td>
<td>3000</td>
<td>179.0</td>
<td>8.4</td>
<td>1.7</td>
<td>1.7</td>
<td>0.76</td>
<td>4.0</td>
<td>8.0</td>
<td>Q2</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*
# Tape and Reel Box Dimensions

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TS3USB31RSER</td>
<td>UQFN</td>
<td>RSE</td>
<td>8</td>
<td>3000</td>
<td>202.0</td>
<td>201.0</td>
<td>28.0</td>
</tr>
<tr>
<td>TS3USB31RSER</td>
<td>UQFN</td>
<td>RSE</td>
<td>8</td>
<td>3000</td>
<td>200.0</td>
<td>183.0</td>
<td>25.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
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