

# TSM24B Unidirectional Surge Protection Device in SOT-23

## 1 Features

- Robust surge protection:
  - IEC61000-4-5 (8/20  $\mu$ s): 20 A
- Low clamping voltage of 33 V (typical) at 20 A for 8/20  $\mu$ s surge current protects downstream components
- Unidirectional polarity for optimized clamping performance on single ended data lines and power rails
- 24 V working voltage for protecting signals on 12 V systems
- Low leakage current of 75 nA (maximum)
- Low I/O capacitance of 24 pF (typical)
- Integrated IEC 61000-4-2 ESD protection
  - $\pm$ 30-kV contact discharge
  - $\pm$ 30-kV air-gap discharge
- Small SOT-23 leaded package to minimize board space and allow for automatic optical inspection (AOI)

## 2 Applications

- Industrial sensors
- Controller area network (CAN)
- PLC I/O modules
- 24-V power lines or digital inputs or output lines
- [Appliances](#)
- [Medical equipment](#)
- [Motor drivers](#)

## 3 Description

The TSM24B is a part of TI's surge protection device family. The TSM24B robustly shunts up to 20 A of IEC 61000-4-5 fault current to protect systems from high power transients or lightning strikes. The TSM24B is rated to dissipate ESD strikes beyond the maximum level specified in the IEC 61000-4-2 international standard ( $\pm$ 30-kV contact,  $\pm$ 30-kV air-gap). The TSM24B clamps during a surge event, keeping system exposure below 33 V (typical) at  $I_{PP} = 20$  A.

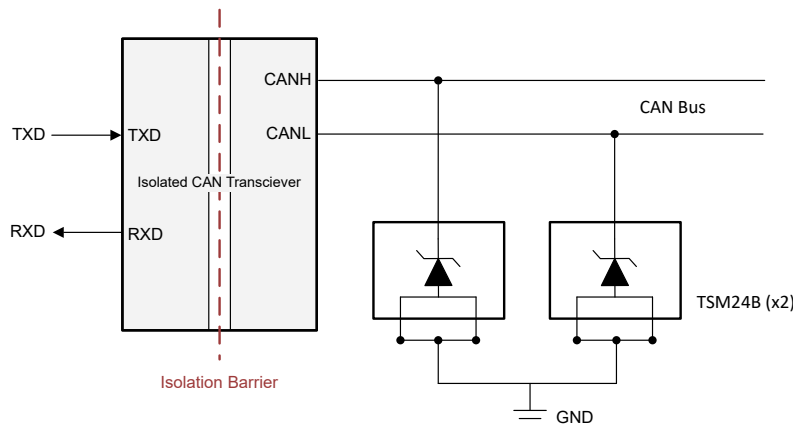
Additionally, the TSM24B is available in a small leaded SOT-23 (DBZ) package, which is reduced in size by approximately 50 percent compared to the industry standard SMA package. The device is designed to have a minimal effect on the protected line due to extremely low device leakage.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
TSM24B	DBZ (SOT-23, 3)	2.92 mm × 2.37 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



**Functional Block Diagram**



## Table of Contents

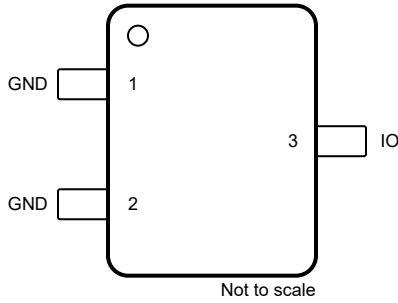
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision * (October 2023) to Revision A (October 2023)</b>	<b>Page</b>
• Changed $I_{LEAK}$ typ value from: 50 nA to: 25 nA and max value from: 100 nA to: 75 nA .....	5
• Changed $V_{BR}$ min value from: 24.8 V to: 26.5 V .....	5
• Changed $V_{CLAMP}$ typ value from: 37 V to: 33 V and deleted the max value.....	5

## 5 Pin Configuration and Functions



**Figure 5-1. DBZ Package, 3-Pin SOT-23 (Top View)**

**Table 5-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
IO	3	I/O	Surge and ESD protected IO
GND	1, 2	G	Connect to ground. To achieve the rated performance, connect pin 1 and 2 together on the PCB as close to the device as possible.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

Parameter		MIN	MAX	UNIT
P <sub>PPM</sub>	IEC 61000-4-5 Surge (t <sub>p</sub> = 8/20 μs) Peak Pulse Power at 25 °C <sup>(2)</sup>		800	W
I <sub>PPM</sub>	IEC 61000-4-5 Surge (t <sub>p</sub> = 8/20 μs) Peak Pulse Current at 25 °C <sup>(2)</sup>		20	A
T <sub>A</sub>	Operating free-air temperature	-40	125	°C
T <sub>stg</sub>	Storage temperature	-65	155	°C

- (1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Voltages are with respect to GND unless otherwise noted.

### 6.2 ESD Ratings -JEDEC Specifications

Parameter		Test Conditions	VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins <sup>(1)</sup>	±2500	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 ESD Ratings - IEC Specifications

Parameter		Test Conditions	VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air Discharge, all pins	±30000	

### 6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Input voltage	0		24	V
T <sub>A</sub>	Operating free-air temperature	-40		125	°C

### 6.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TSM24B	UNIT
		DBZ (SOT-23)	
		3 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	220.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	122.8	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	54.1	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	16.6	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	53.7	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.6 Electrical Characteristics

At  $T_A = 25^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{RWM}$	Reverse stand-off voltage	$I_{IO} < 100\text{ nA}$			24	V
$I_{LEAK}$	Leakage current at $V_{RWM}$	$V_{IO} = 24\text{ V}$ , I/O to GND		25	75	nA
$V_{BR}$	Breakdown voltage, I/O to GND <sup>(1)</sup>	$I_{IO} = 10\text{ mA}$	26.5			V
$V_{FWD}$	Forward Voltage, GND to I/O <sup>(1)</sup>	$I_{IO} = 10\text{ mA}$		0.7		V
$V_{CLAMP}$	Surge clamping voltage, $t_p = 8/20\ \mu\text{s}$ <sup>(2)</sup>	$I_{PP} = 20\text{ A}$ , I/O to GND		33		V
$V_{CLAMP}$	Surge clamping voltage, $t_p = 8/20\ \mu\text{s}$ <sup>(2)</sup>	$I_{PP} = 20\text{ A}$ , GND to I/O		6	8	V
$C_{LINE}$	Line capacitance, IO to GND	$V_{IO} = 0\text{ V}$ , $f = 1\text{ MHz}$		24	37.5	pF

- (1)  $V_{BR}$  is defined as the voltage when 10 mA is applied in the positive-going direction.  
 (2) Device stressed with 8/20  $\mu\text{s}$  exponential decay waveform according to IEC 61000-4-5.

## 6.7 Typical Characteristics

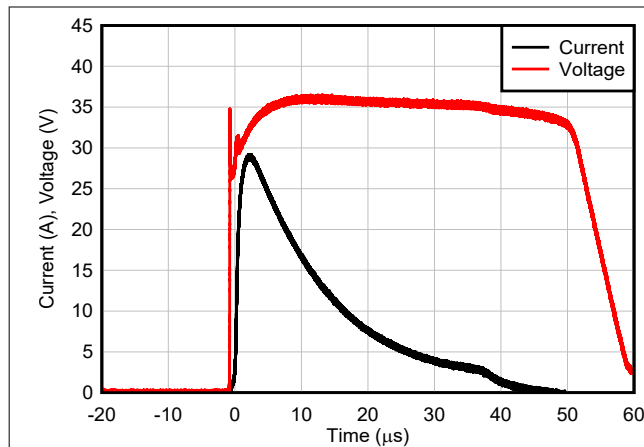


Figure 6-1. 8/20  $\mu\text{s}$  Surge Response

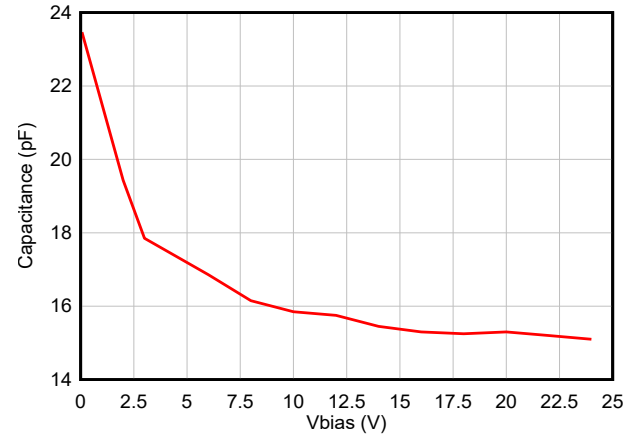


Figure 6-2. Capacitance vs Bias Voltage

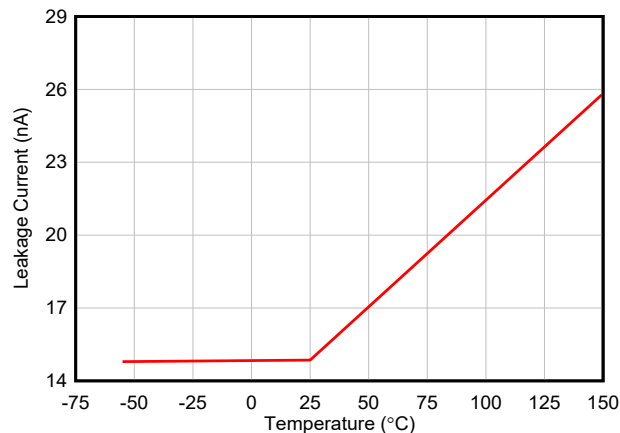


Figure 6-3. Leakage vs Temperature

## 7 Application and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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### 7.1 Application Information

The TSM24B is a diode type TVS that provides a path to ground for dissipating transient voltage spikes (such as ESD or surge) on signal lines and power lines. The device should be connected in parallel to the down stream circuitry it is protecting. As the current from the transient passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low  $R_{DYN}$  of the triggered TVS holds this voltage ( $V_{CLAMP}$ ) to a safe level for the protected IC. For more information on how to properly use this device, refer to the [ESD Packaging and Layout Guide](#).

## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [TI's IEC 61000-4-x Testing application note](#)
- Texas Instruments, [ESD Layout Guide user's guide](#)
- Texas Instruments, [ESD Protection Diodes EVM user's guide](#)
- Texas Instruments, [Generic ESD Evaluation Module user's guide](#)
- Texas Instruments, [Reading and Understanding an ESD Protection Data Sheet user's guide](#)

#### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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#### 8.4 Trademarks

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#### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSM24BDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	35H8	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

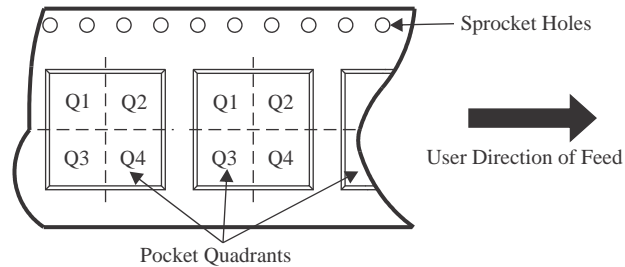
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

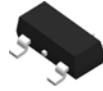
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSM24BDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSM24BDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0

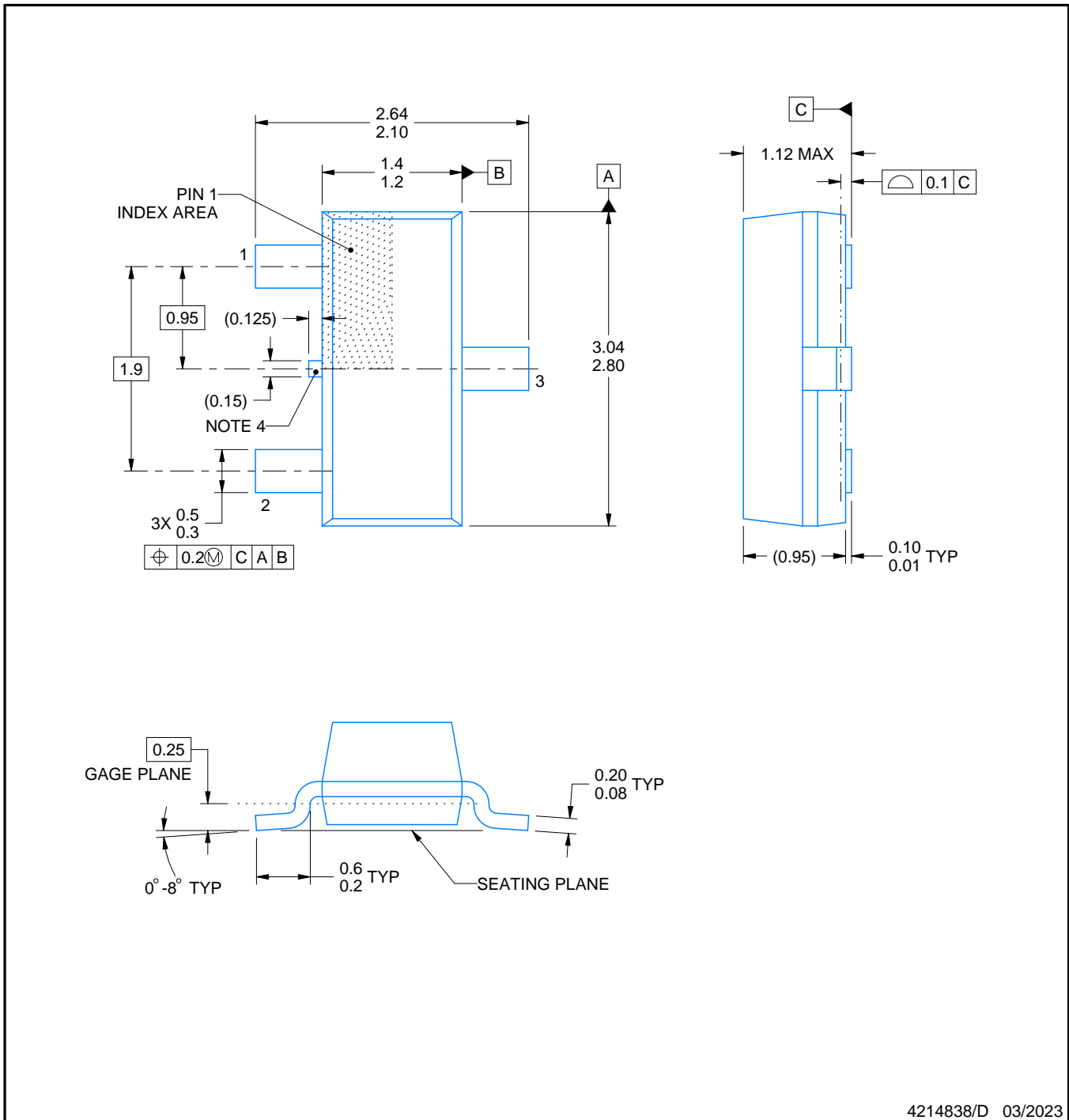
# DBZ0003A



# PACKAGE OUTLINE

## SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



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**NOTES:**

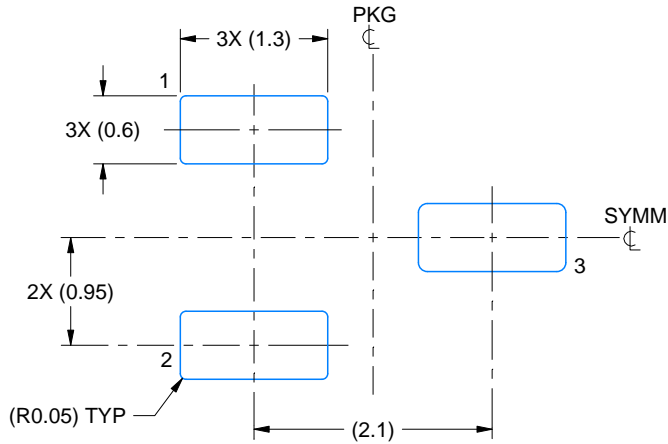
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

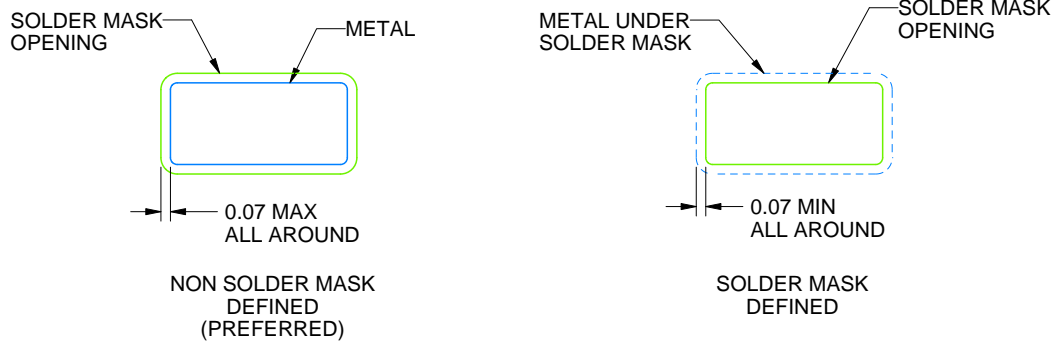
DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

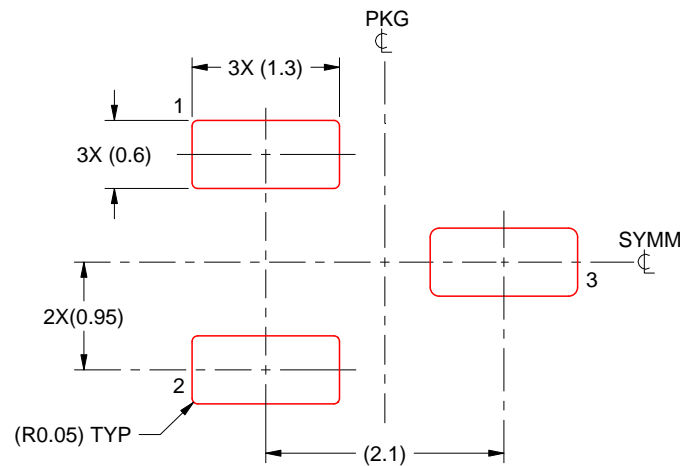
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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