TSM24CA ±24 V Low Capacitance Surge Diode for Industrial Networks in SOT-23 Package

1 Features

- Protection against 1 kV, 42 Ω IEC 61000-4-5 surges for automotive signal lines
- Robust surge protection:
  - IEC 61000-4-5 (8/20 μs): 30 A
- Low I/O Capacitance: 14 pF (typical)
- Bidirectional polarity to support positive and negative voltage swings and miswiring conditions
- Low clamping voltage of 35 V at 24 A for 8/20 μs surge current protects downstream components
- ± 24 V working voltage for protecting signals on 12-V systems
- Low leakage current of 100 nA (max)
- Integrated level 4 IEC 61000-4-2 ESD protection
  - 30-kV ESD protection (IEC 61000-4-2)
- Small SOT-23 leaded package to minimize board space and allow for automatic optical inspection (AOI)

2 Applications

- Automotive hybrid, electric and power train systems
- HEV/EV on-board charger
- EV battery charging communication
  - CHAdeMO
  - CCS
  - GB/T
- Automotive in-vehicle networks
  - Controller area network (CAN)
  - Local interconnect network (LIN)
- 24-V power lines or digital input or output lines

3 Description

The TSM24CA is low capacitance TVS diode and is part of TI’s surge protection device family. The TSM24CA robustly shunts up to 30 A of IEC 61000-4-5 (8/20 μs) fault current to protect systems from high power transients or lightning strikes. The device offers a solution to the common industrial signal line EMC requirement to survive up to 1 kV IEC 61000-4-5 open circuit voltage coupled through a 42 Ω impedance, clamping that surge at 35 V (I_{PP} = 24 A). The TSM24CA also has a very low line capacitance of 14 pF which allows it to protect common automotive communication networks like CAN from surges in EV charging applications.

Additionally, the TSM24CA is available in a small leaded SOT-23 (DBZ) package which is reduced in size by approximately 50 percent compared to the industry standard SMA package. The extremely low device leakage and capacitance provides a minimal effect on the protected line.

Package Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE(1)</th>
<th>PACKAGE SIZE(2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSM24CA</td>
<td>DBZ (SOT-23, 3)</td>
<td>2.92 mm × 2.37 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History

<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>August 2023</td>
<td>*</td>
<td>Initial Release</td>
</tr>
</tbody>
</table>
5 Pin Configuration and Functions

![DBZ Package, 3-Pin SOT-23 (Top View)](image)

Figure 5-1. DBZ Package, 3-Pin SOT-23 (Top View)

Table 5-1. Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE(1)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>IO</td>
<td>1,2</td>
<td>I/O Surge and ESD protected IO. Connect other pin to ground.</td>
</tr>
<tr>
<td>NC</td>
<td>3</td>
<td>NC Leave this pin floating for proper performance.</td>
</tr>
</tbody>
</table>

(1) I/O = Input or Output, NC = No connect
6 Specifications

6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(P_{PPM})</td>
<td>IEC 61000-4-5 Surge ((t_{p} = 8/20 \mu s)) Peak Pulse Power at 25 °C</td>
<td>1200</td>
<td>W</td>
</tr>
<tr>
<td>(I_{PPM})</td>
<td>IEC 61000-4-5 Surge ((t_{p} = 8/20 \mu s)) Peak Pulse Current at 25 °C</td>
<td>30</td>
<td>A</td>
</tr>
<tr>
<td>(T_{A})</td>
<td>Operating free-air temperature</td>
<td>–40</td>
<td>125</td>
</tr>
<tr>
<td>(T_{stg})</td>
<td>Storage temperature</td>
<td>–65</td>
<td>155</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Voltages are with respect to GND unless otherwise noted.

6.2 ESD Ratings - JEDEC Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{(ESD)})</td>
<td>Electrostatic discharge</td>
<td>±2500</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins</td>
<td>±2500</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Charged device model (CDM), per JEDEC specification JS-002, all pins</td>
<td>±1000</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{(ESD)})</td>
<td>Electrostatic discharge</td>
<td>±30000</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>IEC 61000-4-2 Contact Discharge, all pins</td>
<td>±30000</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>IEC 61000-4-2 Air Discharge, all pins</td>
<td>±30000</td>
<td>V</td>
</tr>
</tbody>
</table>

6.4 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{IN})</td>
<td>-24</td>
<td>24</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(T_{A})</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

6.5 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TSM24CA</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{θJA})</td>
<td>Junction-to-ambient thermal resistance</td>
<td>203.8</td>
</tr>
<tr>
<td>(R_{θJC(top)})</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>104.1</td>
</tr>
<tr>
<td>(R_{θJB})</td>
<td>Junction-to-board thermal resistance</td>
<td>39.4</td>
</tr>
<tr>
<td>(Ψ_{JT})</td>
<td>Junction-to-top characterization parameter</td>
<td>8.7</td>
</tr>
<tr>
<td>(Ψ_{JB})</td>
<td>Junction-to-board characterization parameter</td>
<td>38.9</td>
</tr>
<tr>
<td>(R_{θJC(bot)})</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>NA</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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Submit Document Feedback
### 6.6 Electrical Characteristics

At TA = 25°C unless otherwise noted

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{RWM}$</td>
<td>Reverse stand-off voltage</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{IO}$ &lt; 100 nA</td>
<td></td>
<td>-24</td>
<td>24</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{LEAK}$</td>
<td>Leakage current at $V_{RWM}$</td>
<td></td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>$V_{IO} = 24$ V, I/O to GND &amp; GND to I/O</td>
<td>10</td>
<td>100</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{BR}$</td>
<td>Breakdown voltage, I/O to GND &amp; GND to I/O (1)</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{IO} = 10$ mA</td>
<td></td>
<td>25.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CLAMP}$</td>
<td>Surge clamping voltage, $t_p = 8/20$ µs (3)</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{PP} = 24$ A, I/O to GND &amp; GND to I/O</td>
<td>35</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{LINE}$</td>
<td>Line capacitance, IO to GND</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$V_{IO} = 0$ V, f = 1 MHz</td>
<td></td>
<td>14</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) $V_{BR}$ is defined as the voltage obtained at 10 mA when sweeping the voltage up, before the device latches into the snapback state

(2) Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5

(3) Device stressed with IEC 61000-4-5, Type 4, 1.2/50 µs waveform
6.7 Typical Characteristics

**Figure 6-1. 8/20 µs Surge Response**

**Figure 6-2. Capacitance vs Bias Voltage**

**Figure 6-3. Leakage vs Temperature**
7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TSM24CA is a TVS diode which provides a path to ground for dissipating transient voltage spikes, such as ESD or surge, on signal lines and power lines. The device should be connected in parallel to the down stream circuitry it is protecting. As the current from the transient passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low RDYN of the triggered TVS holds this voltage (VCLAMP) to a safe level for the protected IC. For more information on how to properly use this device, refer to the ESD Packaging and Layout Guide.
8 Device and Documentation Support
8.1 Documentation Support

8.1.1 Related Documentation
For related documentation, see the following:

- Texas Instruments, *TI's IEC 61000-4-x Testing application note*
- Texas Instruments, *ESD Layout Guide user's guide*
- Texas Instruments, *ESD Protection Diodes EVM user's guide*
- Texas Instruments, *Generic ESD Evaluation Module user's guide*
- Texas Instruments, *Reading and Understanding an ESD Protection data sheet*

8.2 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources
*TI E2E™ support forums* are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Trademarks
*TI E2E™* is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary
*TI Glossary* This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/Ball material (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSM24CADBZR</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBZ</td>
<td>3</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-55 to 150</td>
<td>3SP8</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

### REEL DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component thickness
- **K0**: Overall width of the carrier tape
- **W**: Pitch between successive cavity centers

### TAPE DIMENSIONS

- **P1**: Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Q1**, **Q2**, **Q3**, **Q4**: Pocket Quadrants
- **Sprocket Holes**
- **User Direction of Feed**

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSM24CADBZR</td>
<td>SOT-23</td>
<td>DBZ</td>
<td>3</td>
<td>3000</td>
<td>180.0</td>
<td>8.4</td>
<td>2.9</td>
<td>3.35</td>
<td>1.35</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
</tbody>
</table>
## TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSM24CADBZR</td>
<td>SOT-23</td>
<td>DBZ</td>
<td>3</td>
<td>3000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.
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