TUSB211A USB 2.0 480-Mbps High-Speed Signal Conditioner

1 Features

- Wide supply voltage range: 2.3 – 6.5 V
- Ultra-low USB disconnect and shutdown power consumption
- Provides USB 2.0 high-speed signal conditioning
- Compatible with USB 2.0, OTG 2.0, and BC 1.2
- Support for low-speed, full-speed, and high-speed signaling
- Host or device agnostic
- Supports up to 5-m cable length
  - Four selectable signal EQ (edge boost along with DC boost) settings through the external pull-down resistor values
- Supports up to 10-m cable length with two TUSB211A devices
- Scalable solution – devices can be daisy chained for high loss applications
- Pin compatible with TUSB211, 212, 214, 216, and 217A (3.3 V)

2 Applications

- Laptop, desktop or docking stations
- Portable electronics
- Tablets
- Cell phones
- Televisions
- Active cable, cable extenders, backplane

3 Description

The TUSB211A is a third-generation USB 2.0 high-speed signal conditioner designed to compensate both AC loss (due to capacitive load) and DC loss (due to resistive loss) in the transmission channel.

The TUSB211A leverages a patented design to speed-up transition edges of USB 2.0 high-speed signal with an edge booster and increases static levels with a DC boost function.

In addition, the TUSB211A includes a pre-equalization function to compensate the inter-symbol interference (ISI) jitter in application with longer cable length. USB low-speed and full-speed signal characteristics are unaffected by the TUSB211A.

The TUSB211A improves signal quality without altering packet timing or adding propagation delay or latency.

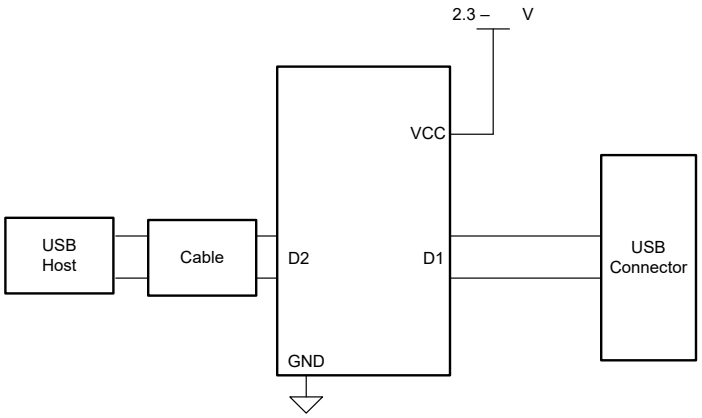
The TUSB211A helps a system to pass the USB 2.0 high-speed near end eye compliance with a cable as long as 5 meters.

The TUSB211A is compatible with USB On-The-Go (OTG) and Battery Charging (BC) protocols.

Device Information

PART NUMBER	PACKAGE(1)	OP TEMP (T_A) °C	BODY SIZE (NOM)(2)
TUSB211A	RWB (X2QFN, 12)	0 to 70	1.6 mm × 1.6 mm
TUSB211AI		-40 to 85	

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The body size (length × width) is a nominal value and does not include pins.



Simplified Schematic

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4 Revision History

DATE	REVISION	NOTES
September 2023	*	Initial Release

5 Pin Configuration and Functions

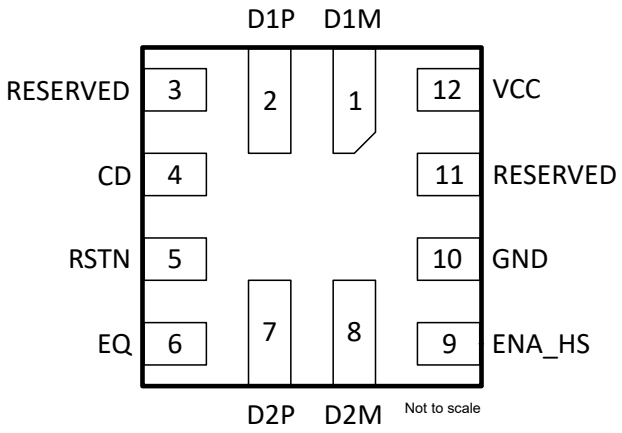


Figure 5-1. TUSB211A RWB 12-Pin X2QFN (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO.			
EQ	6	I	N/A	USB High-speed EQ select via external pull down resistor. Both edge boost and DC boost are controlled by a single pin. Sampled upon power up. Does not recognize real time adjustments. Auto selects EQ LEVEL = 3 when left floating.
RESERVED	11	I	500 kΩ PU	Reserved pin for TI test purposes. Leave floating or connect external capacitor to GND for normal operation.
ENA_HS	9	I/O	N/A	After reset: Output signal ENA_HS. Flag indicating that channel is in High-speed mode. Asserted upon: 1. Detection of USB-IF High-speed test fixture from an unconnected state followed by transmission of USB TEST_PACKET pattern. 2. Squelch detection following USB reset with a successful HS handshake [HS handshake is declared to be successful after single chirp J chirp K pair where each chirp is within 18 µs – 128 µs].
D2P	7	I/O	N/A	USB High-speed positive port.
D2M	8	I/O	N/A	USB High-speed negative port.
GND	10	P	N/A	Ground
D1M	1	I/O	N/A	USB High-speed negative port.
D1P	2	I/O	N/A	USB High-speed positive port.
RESERVED	3	I/O	500 kΩ PU 1.8 MΩ PD	Reserved pin for TI test purposes. Leave floating for normal operation.
VCC	12	P	N/A	Supply power
RSTN	5	I	500 kΩ PU 1.8 MΩ PD	Device disable/enable. Low – Device is at reset and in shutdown, and High - Normal operation. Recommend 0.1-µF external capacitor to GND to ensure clean power on reset if not driven. If the pin is driven, it must be held low until the supply voltage for the device reaches within specifications.
CD	4	O	When RSTN asserted there is a 500 kΩ PD	After reset: Output CD. Flag indicating that a USB device is attached (connection detected). Asserted from an unconnected state upon detection of DP or DM pull-up resistor. De-asserted upon detection of disconnect.

(1) I = input, O = output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage range	VCC	–0.3	7	V
Voltage range USB data	DxP, DxM	–0.3	5.5	V
Voltage range on EQ pin	EQ	-0.3	1.98	V
Voltage range other pins	RSTN	-0.3	5.5	V
Storage temperature, T_{stg}		–65	150	°C
Maximum junction temperature, $T_{J\ (max)}$			125	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (2)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (3)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.3	5	6.5	V
T_A	Operating free-air temperature (TUSB211A)	0		70	°C
	Operating free-air temperature (TUSB211AI)	–40		85	°C
T_J	Junction temperature (TUSB211A)			85	°C
	Junction temperature (TUSB211AI)			105	°C
DxP, DxM	Voltage range USB data	0		3.6	V
EQ	Voltage range EQ pin	0		1.98	V
DIGITAL	Voltage range other pins (RSTN)	0		3.6	V

6.4 Thermal Information

THERMAL METRIC (1)		RWB (X2QFN) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	137.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
POWER						
I_{ACTIVE_HS}	High Speed Active Current	USB channel = HS mode. 480 Mbps traffic. V_{CC} supply stable, with EQ = Max		22	36	mA
I_{IDLE_HS}	High Speed Idle Current	USB channel = HS mode, no traffic. V_{CC} supply stable, EQ = Max		22	36	mA
$I_{HS\_SUSPEND}$	High Speed Suspend Current	USB channel = HS Suspend mode. V_{CC} supply stable		0.75	1.4	mA
I_{FS}	Full-Speed Current	USB channel = FS mode, 12 Mbps traffic, V_{cc} supply stable		0.75	1.4	mA
$I_{DISCONN}$	Disconnect Power	Host side application. No device attachment.		0.80	1.4	mA
I_{SHUTDN}	Shutdown Power	RSTN driven low, V_{CC} supply stable		60	115	µA
CONTROL PIN LEAKAGE						
I_{LKG_FS}	Pin failsafe leakage current for RSTN	V_{CC} = 0 V, pin at $V_{IH, max}$		10	15	µA
INPUT RSTN						
V_{IH}	High level input voltage		1.5		3.6	V
V_{IL}	Low-level input voltage		0		0.5	V
I_{IH}	High level input current	V_{IH} = 3.6 V, R_{PU} enabled			±15	µA
I_{IL}	Low level input current	V_{IL} = 0V, R_{PU} enabled			±20	µA
INPUT EQ						
R_{EQ_LVL0}	External pulldown resistor for EQ Level 0				160	Ω
R_{EQ_LVL1}	External pulldown resistor for EQ Level 1		1.5	1.8	2	kΩ
R_{EQ_LVL2}	External pulldown resistor for EQ Level 2		3.4	3.6	3.96	kΩ
R_{EQ_LVL3}	External pulldown resistor for EQ Level 3 to remove upper limit for resistor value, can be left open		7.5			kΩ
OUTPUTS CD, ENA_HS						
V_{OH}	High level output voltage for CD and ENA_HS	I_O = –50 µA, VCC >= 3.0 V	2.5			V
V_{OH}	High level output voltage for CD	I_O = –25 µA, VCC = 2.3 V	1.7			V
V_{OH}	High level output voltage for ENA_HS	I_O = –25 µA, VCC = 2.3 V	1.8			V
V_{OL}	Low level output voltage for CD and ENA_HS	I_O = 50 µA			0.3	V
DxP, DxM						
C_{IO_DXX}	Capacitance to GND	Measured with VNA at 240 MHz, V_{CC} supply stable, Redriver off		2.5		pF

(1) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

6.6 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
DxP, DxM USB Signals						
F_{BR_DXX}	Bit Rate	USB channel = HS mode. 480 Mbps traffic. V_{CC} supply stable			480	Mbps
t_{R/F_DXX}	Rise/Fall time		100			ps

(1) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

6.7 Timing Requirements

		MIN	NOM	MAX	UNIT
POWER UP TIMING					
T_{RSTN_PW}	Minimum width to detect a valid RSTN signal assert when the pin is actively driven low	100			µs
T_{STABLE}	VCC must be stable before RSTN de-assertion	300			µs
T_{READY}	Maximum time needed for the device to be ready after RSTN is de-asserted.			500	µs
T_{RAMP}	V_{CC} ramp time			100	ms
T_{RAMP}	V_{CC} ramp time	0.2			ms

6.8 Typical Characteristics

The typical characteristics shown in this section apply to near-end eye measurements taken at nominal conditions. The eyes are measured with various pre-channel cable lengths applied at the input or post-channel cable lengths applied at the output of the TUSB211A as indicated.

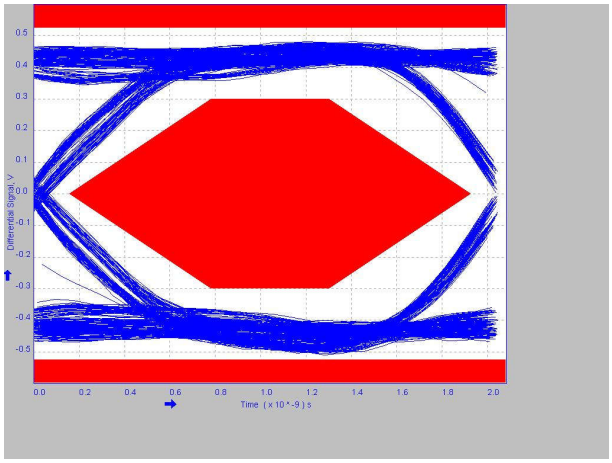


Figure 6-1. 2 Meter Pre-Channel With TUSB211A EQ=1

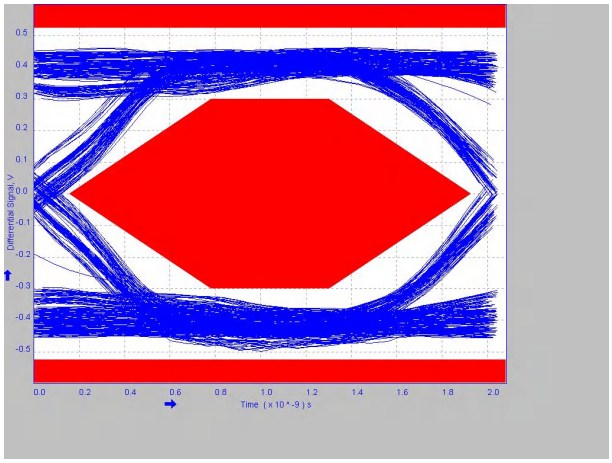


Figure 6-2. 5 Meter Pre-Channel With TUSB211A EQ=2

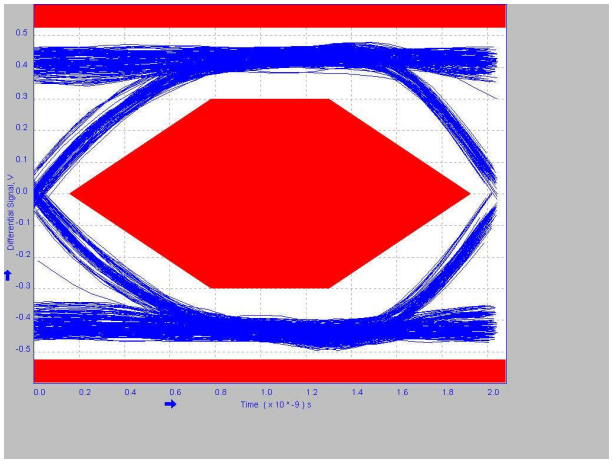


Figure 6-3. 2 Meter Post-Channel With TUSB211A EQ=1

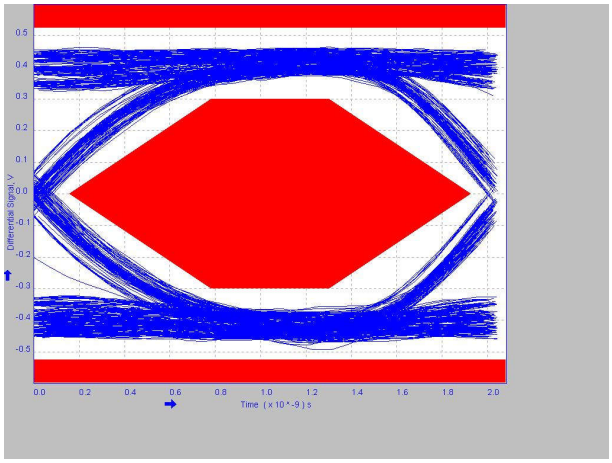


Figure 6-4. 4 Meter Post-Channel With TUSB211A EQ=2

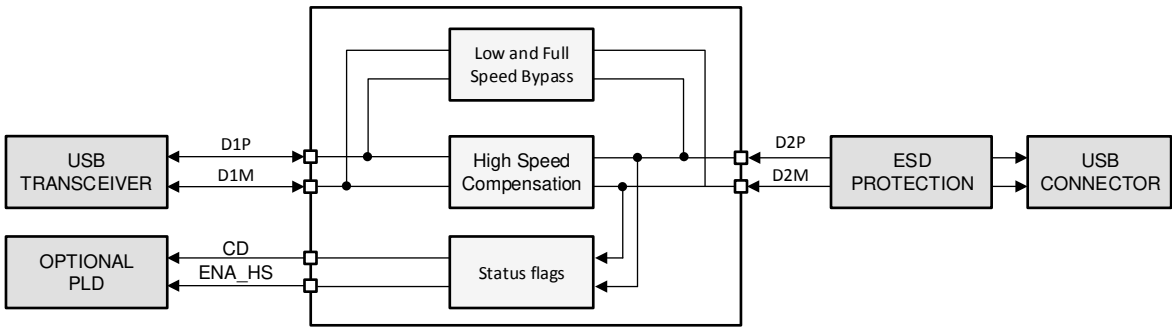
7 Detailed Description

7.1 Overview

The TUSB211A is a USB High-Speed (HS) signal conditioner designed to compensate for ISI signal loss in a transmission channel. TUSB211A has a patented design for USB Low Speed (LS) and Full Speed (FS) signals. It does not alter the signal characteristics. HS signals are compensated. The design is compatible with USB On-The-Go (OTG) and Battery Charging (BC) specifications.

Programmable signal gain through an external resistor permits fine tuning device performance to optimize signals. This helps pass USB HS electrical compliance tests at the connector. The TUSB211A allows application in series to cover longer distances, or high loss transmission paths. A maximum of 4 devices can be daisy-chained.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High-Speed EQ

The high-speed EQ (combination of edge boost and DC boost) improves the eye width for USB2.0 high-speed signals. It is direction independent and by that is compatible to OTG systems. The EQ pin is configuring the EQ strength with different values of pull down resistors to set 4 levels of EQ.

7.4 Device Functional Modes

7.4.1 Low-Speed (LS) Mode

TUSB211A automatically detects an LS connection and does not enable signal compensation. CD pin is asserted high but ENA_HS will be low.

7.4.2 Full-Speed (FS) Mode

TUSB211A automatically detects an FS connection and does not enable signal compensation. CD pin is asserted high but ENA_HS will be low.

7.4.3 High-Speed (HS) Mode

TUSB211A automatically detects an HS connection and will enable signal compensation as determined by the external pull down resistance on its EQ pin.

CD pin and ENA_HS pin are asserted high when high-speed EQ is active.

7.4.4 High-Speed Downstream Port Electrical Compliance Test Mode

TUSB211A will detect an HS compliance test fixture and enter the downstream port high-speed eye diagram test mode. CD pin will be low and ENA_HS pin is asserted high when TUSB211A is in HS eye compliance test mode.

If the RSTN pin is asserted low and de-asserted high while TUSB211A is operating in HS functional mode, then TUSB211A will transition to HS eye compliance test mode, the CD asserts low, and ENA_HS remains high. When all this occurs, signal compensation is enabled.

7.4.5 Shutdown Mode

TUSB211A can be disabled when its RSTN pin is asserted low. DP, DM traces are continuous through the device in shutdown mode. The USB channel is still fully operational, but there is neither signal compensation, nor any indication from the CD pin as to the status of the channel.

Table 7-1. CD and ENA_HS Pins in Different Modes

MODE	CD	ENA_HS
Low-speed	HIGH	LOW
Full-speed	HIGH	LOW
High-speed	HIGH	HIGH
High-speed downstream port electrical test	LOW	HIGH
Shutdown	LOW	LOW

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The purpose of the TUSB211A is to restore the signal integrity of a USB High-speed channel up to the USB connector. The loss in signal quality stems from reduced channel bandwidth due to high loss PCB trace and other components that contribute a capacitive load. This can cause the channel to fail the USB near end eye mask. Proper use of the TUSB211A can help to pass this eye mask.

A secondary purpose is to use the CD pin of the TUSB211A to control other blocks on the customer platform, if so desired.

8.2 Typical Application

A typical application for TUSB211A is shown in Figure 8-1. In this setup, D2P and D2M face the USB connector while D1P and D1M face the USB host. The orientation may be reversed [that is, D2 faces transceiver and D1 faces connector].

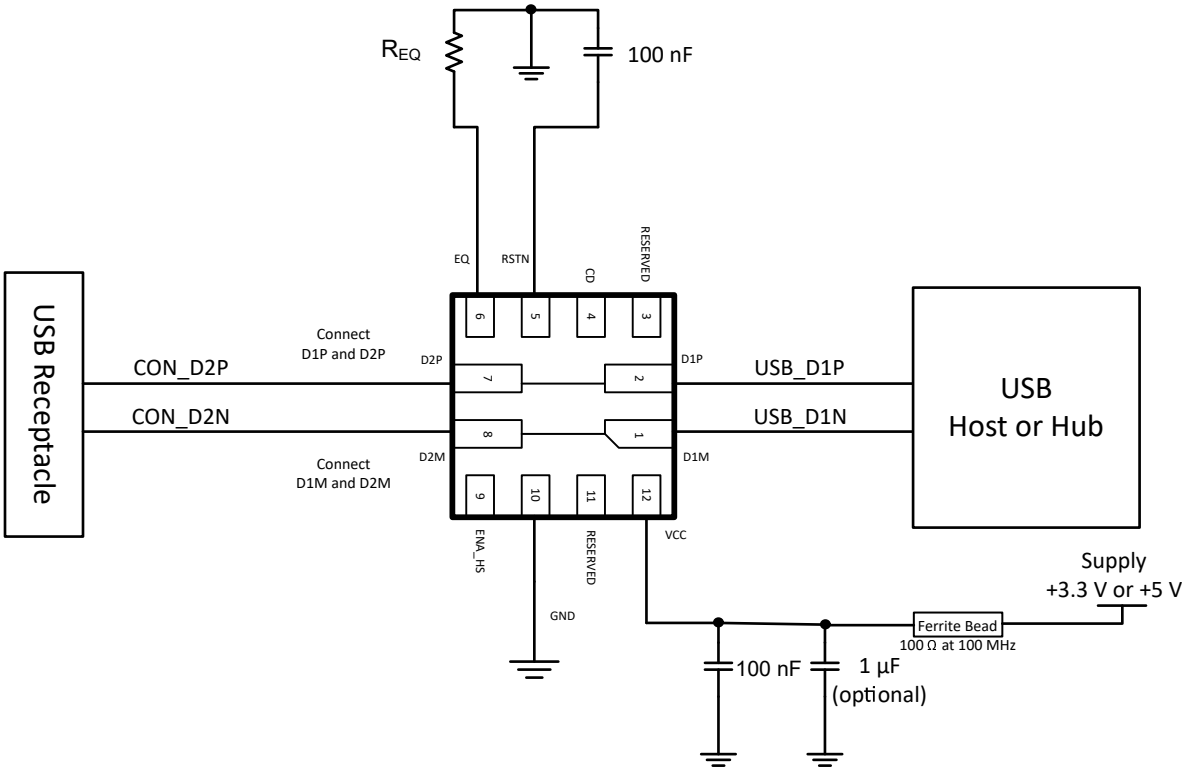


Figure 8-1. TUSB211A Reference Schematic

8.2.1 Design Requirements

TUSB211A requires a valid reset signal as described in the *Power Supply Recommendations* section. The capacitor at RSTN pin is not required if a micro controller drives the RSTN pin according to recommendations.

For this design example, use the parameters provided in Table 8-1.

Table 8-1. Design Parameters for 3.3-V Supply With Low to Medium Loss System

PARAMETER			VALUE(1)
V_{CC}			3.3 V ±10%
I^2C support required in system (Yes/No)			No
Edge and DC Boost	R_{EQ}	EQ Level	EQ Level 0: R_{EQ} = 0-Ω
	0-Ω	0	
	1.8 kΩ ±1%	1	
	3.6 kΩ ±1%	2	
	Do Not Install (DNI)	3	

(1) These parameters are starting values for a low to medium loss system. Further tuning might be required based on specific host or device as well as cable length and loss profile. These settings are not specific to a 3.3-V supply system and could be applicable to 5-V supply system as well.

8.2.2 Detailed Design Procedure

The ideal EQ setting is dependent upon the signal chain loss characteristics of the target platform. The recommendation is to start with EQ Level 0, and then increment to EQ Level 1, and so on.

For the TUSB211A to recognize any change to the EQ setting, the RSTN pin must be toggled. This is because the EQ pin is latched on power up and the pin is ignored thereafter.

Placement of the device is also dependent on the application goal. Table 8-2 describes TI recommendations.

Table 8-2. Platform Placement Guideline

PLATFORM GOAL	SUGGESTED TUSB211A PLACEMENT
Pass USB Near End Mask at the receptacle	Close to measurement point (connector)
Pass USB Far End Eye Mask at the plug	Close to USB PHY
Cascade multiple TUSB211As to improve device enumeration	Midway between each USB interconnect

Table 8-3. Table of Recommended Settings

EQ settings(1) for channel loss	
Pre-channel cable length (Between USB PHY and TUSB211A)	**EQ**
0-3 meter	Level 0
2-5 meter	Level 1
Post-channel cable length (Between TUSB211A and inter-connect)	**EQ**
0-2 meter	Level 0
1-4 meter	Level 1

(1) These parameters are starting values for different cable lengths. Further tuning might be required based on specific host or device as well as cable length and loss profile.

8.2.2.1 Test Procedure to Construct USB High-Speed Eye Diagram

Note

USB-IF certification tests for High-speed eye masks require the *mandated use* of the USB-IF developed test fixtures. These test fixtures do not require the use of oscilloscope probes. Instead they use SMA cables. More information can be found at the USB-IF Compliance Updates Page. It is located under the *Electrical Specifications* section, ID 86 dated March 2013.

The following procedure must be followed before using any oscilloscope compliance software to construct a USB High-speed Eye Mask:

8.2.2.1.1 For a Host Side Application

1. Configure the TUSB211A to the desired EQ setting.
2. Power on (or toggle the RSTN pin if already powered on) the TUSB211A.
3. Using SMA cables, connect the oscilloscope and the USB-IF host-side test fixture to the TUSB211A.
4. Enable the host to transmit USB TEST_PACKET.
5. Execute the oscilloscope USB compliance software.
6. Repeat the above steps to re-test TUSB211A with a different EQ setting (must reset to change).

8.2.2.1.2 For a Device Side Application

1. Configure the TUSB211A to the desired EQ setting.
2. Power on (or toggle the RSTN pin if already powered on) the TUSB211A.
3. Connect a USB host, the USB-IF device-side test fixture, and USB device to the TUSB211A. Ensure that the USB-IF device test fixture is configured to the ‘INIT’ position.
4. Allow the host to enumerate the device.
5. Enable the device to transmit USB TEST_PACKET.
6. Using SMA cables, connect the oscilloscope to the USB-IF device-side test fixture and ensure that the device-side test fixture is configured to the ‘TEST’ position.
7. Execute the oscilloscope USB compliance software.
8. Repeat the above steps to re-test TUSB211A with a different EQ setting (must reset to change).

8.2.3 Application Curves

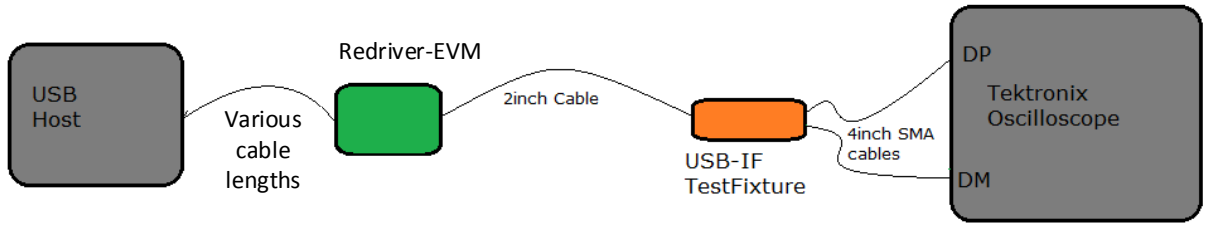


Figure 8-2. Near End Eye Measurement Set-Up With Pre-Channel Cable

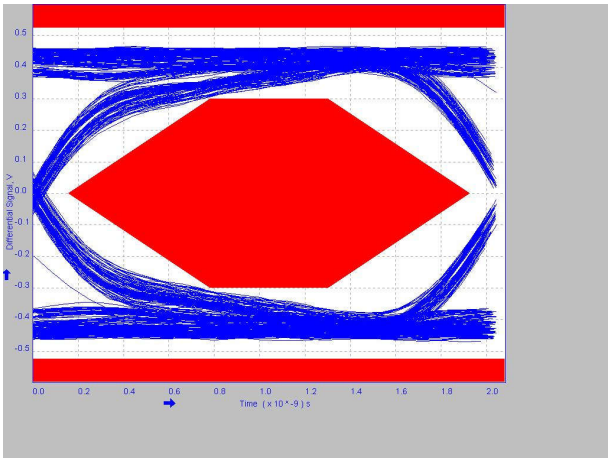


Figure 8-3. 2 Meter Pre-Channel Without TUSB211A

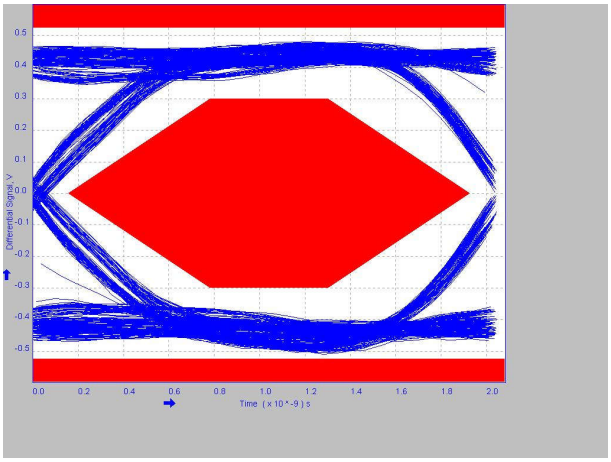


Figure 8-4. 2 Meter Pre-Channel With TUSB211A EQ=1

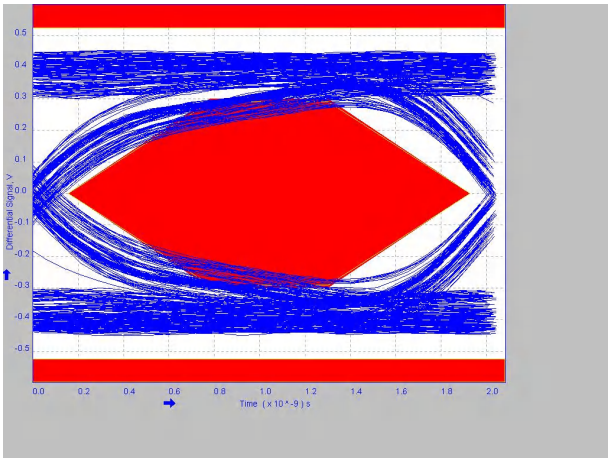


Figure 8-5. 5 Meter Without TUSB211A

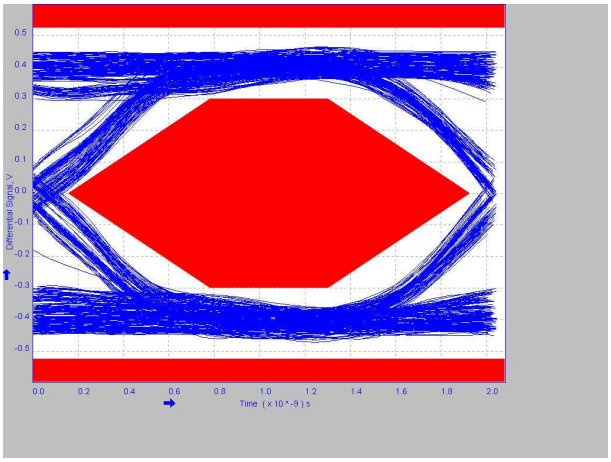


Figure 8-6. 5 Meter Pre-Channel With TUSB211A EQ=1

8.2.3 Application Curves (continued)

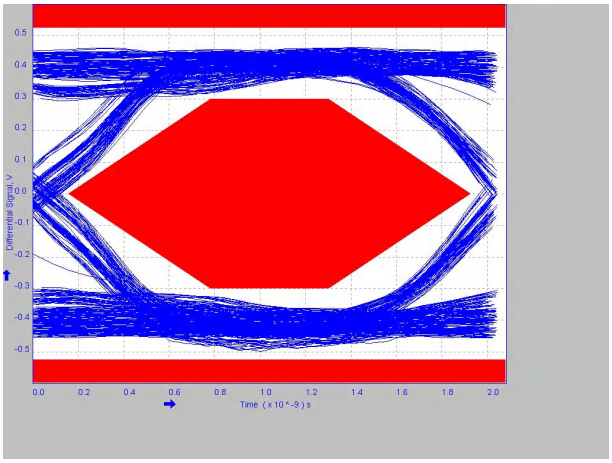


Figure 8-7. 5 Meter Pre-Channel With TUSB211A EQ=2

8.2.3 Application Curves

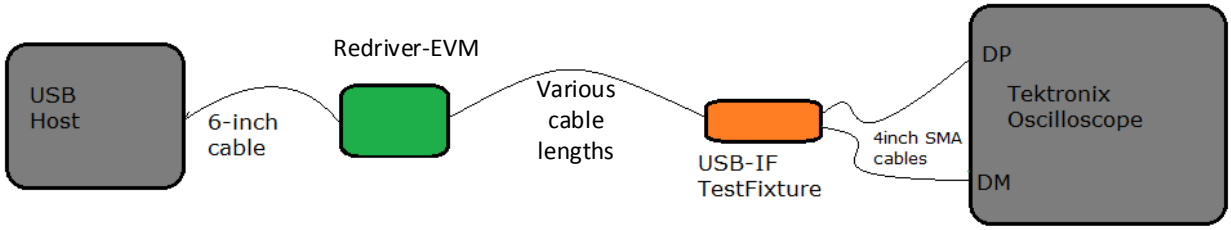


Figure 8-8. Near End Eye Measurement Set-Up With Post-Channel Cable

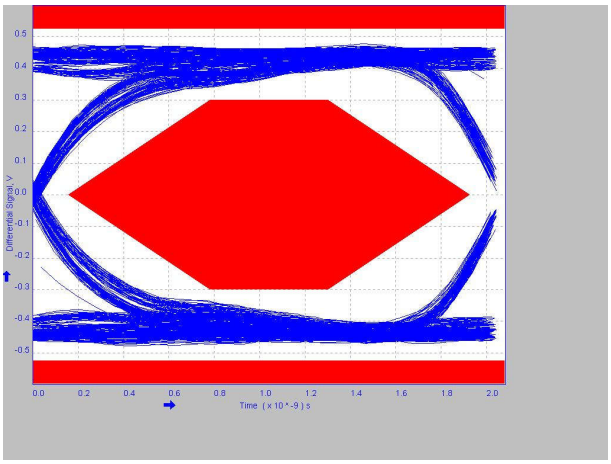


Figure 8-9. 1 Meter Post-Channel Without TUSB211A

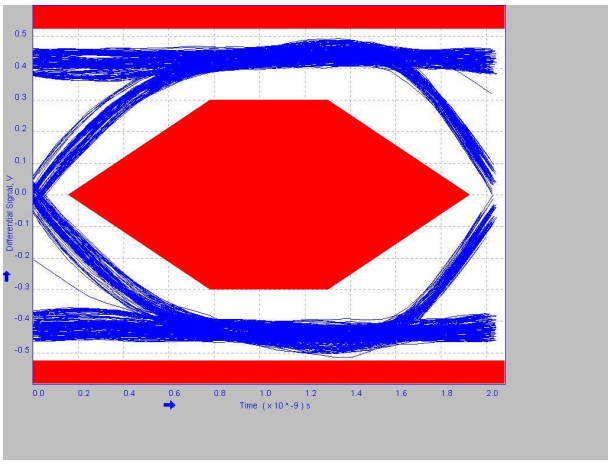


Figure 8-10. 1 Meter Post-Channel With TUSB211A EQ=0

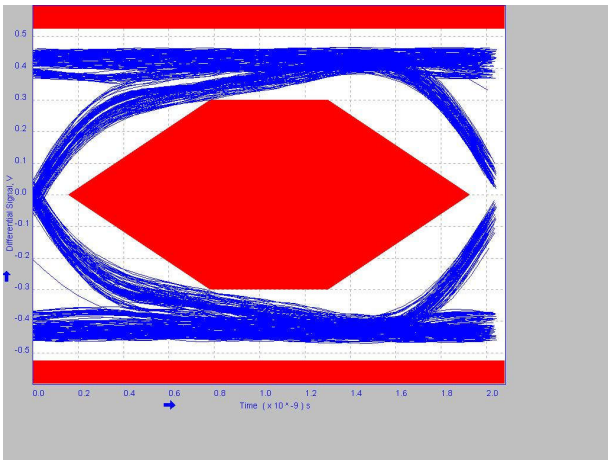


Figure 8-11. 2 Meter Post-Channel Without TUSB211A

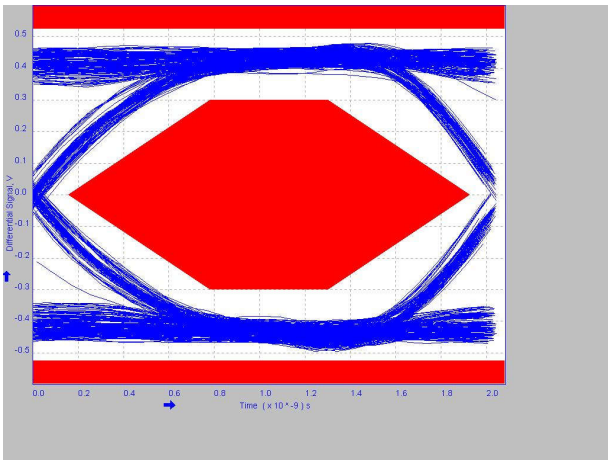


Figure 8-12. 2 Meter Post-Channel With TUSB211A EQ=1

8.2.3 Application Curves (continued)

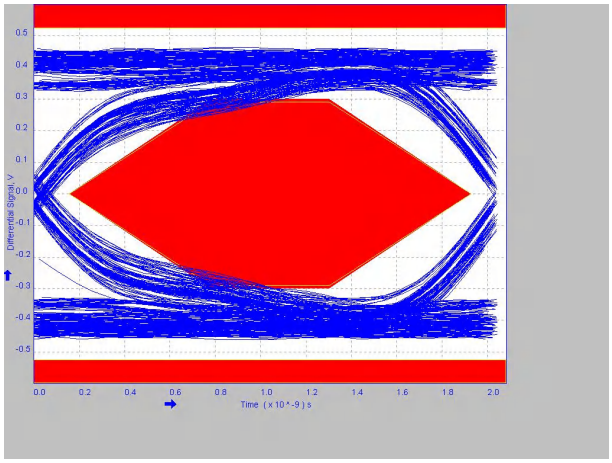


Figure 8-13. 4 Meter Post-Channel Without TUSB211A

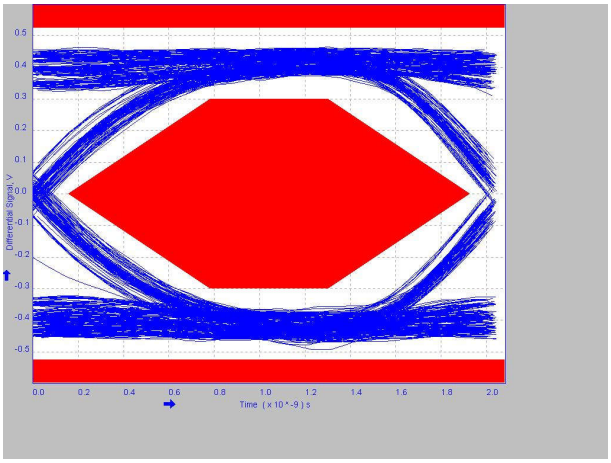


Figure 8-14. 4 Meter Post-Channel With TUSB211A EQ=2

8.3 Power Supply Recommendations

On power up, the interaction of the RSTN pin and power on ramp could result in digital circuits not being set correctly. The device should not be enabled until the power on ramp has settled to the minimum recommended supply voltage or higher for a correct power on reset of the digital circuitry. If RSTN cannot be held low by microcontroller or other circuitry until the power on ramp has settled, then an external capacitor from the RSTN pin to GND is required to hold the device in the low power reset state.

The RC time constant should be larger than five times of the power on ramp time (0 to V_{CC}). With a typical internal pullup resistance of 500 kΩ, the recommended minimum external capacitance is calculated as:

$$[Ramp\ Time\ \times\ 5]\ \div\ [500\ k\Omega] \quad (1)$$

8.4 Layout

8.4.1 Layout Guidelines

Although the land pattern has matched trace width to pad width, optimal impedance control is based on the user's own PCB stack-up. The recommendation is to maintain 90 Ω differential routing underneath the device.

8.4.2 Layout Example

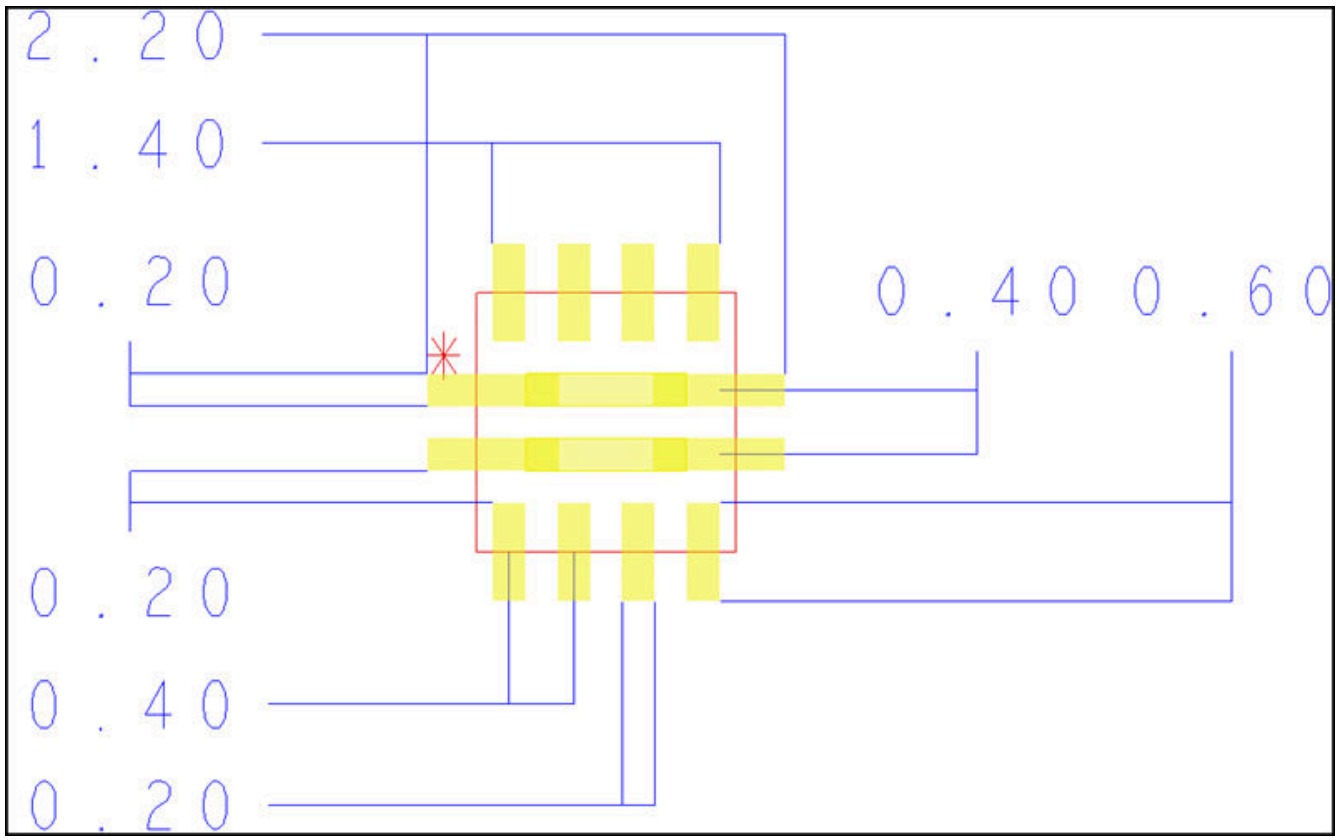


Figure 8-15. DP and DM Routing Underneath Device Package

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

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All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB211AIRWBR	ACTIVE	X2QFN	RWB	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1A	Samples
TUSB211ARWBR	ACTIVE	X2QFN	RWB	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	1A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

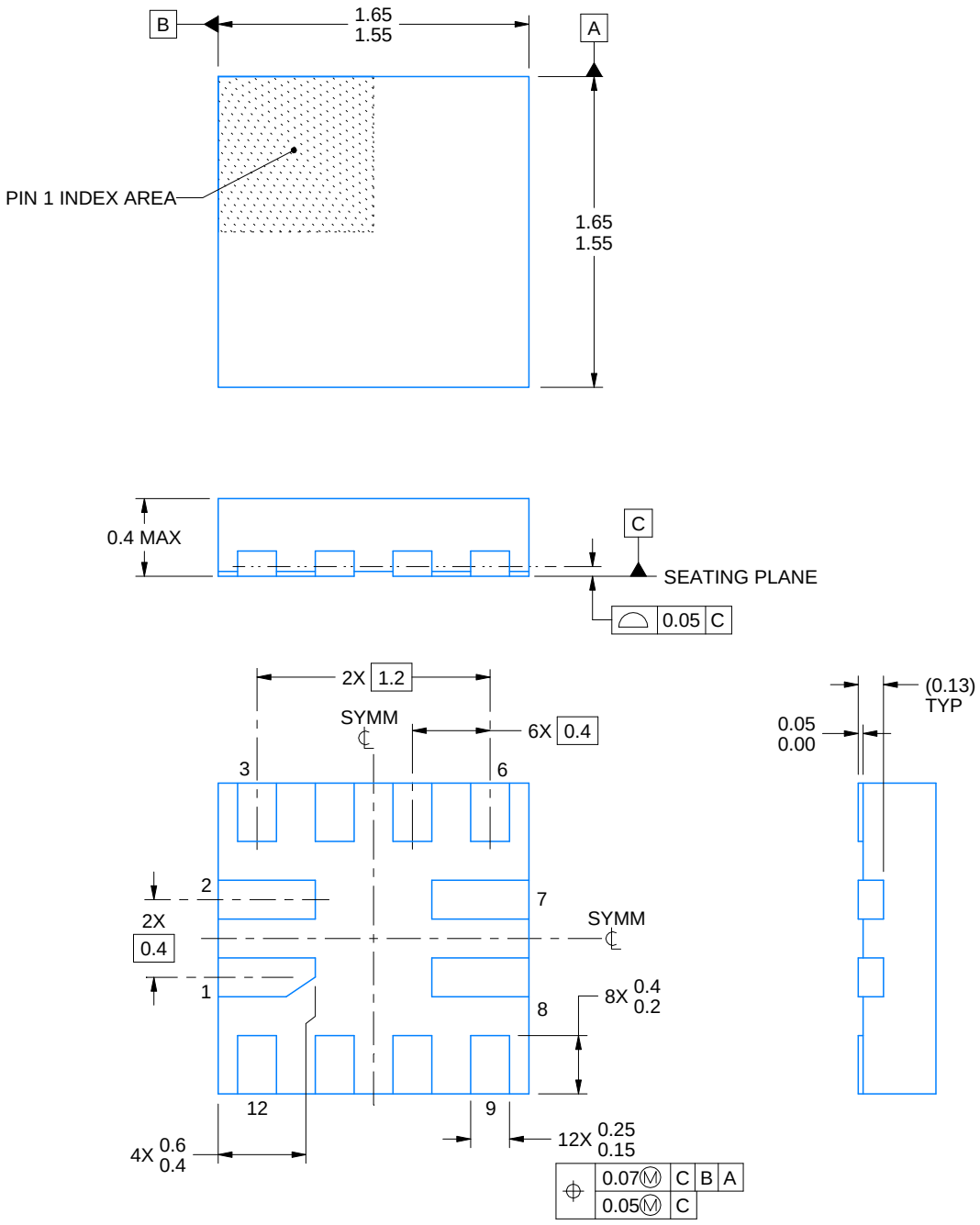
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

RWB0012A

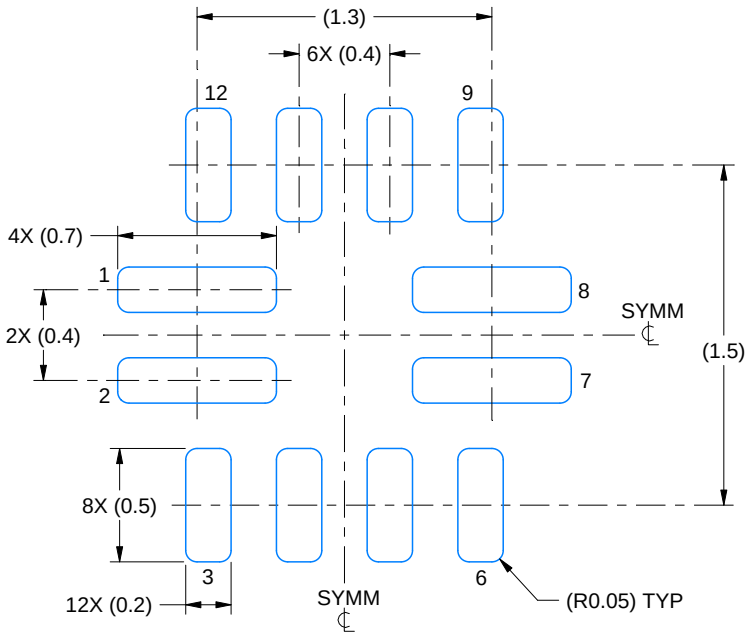
X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

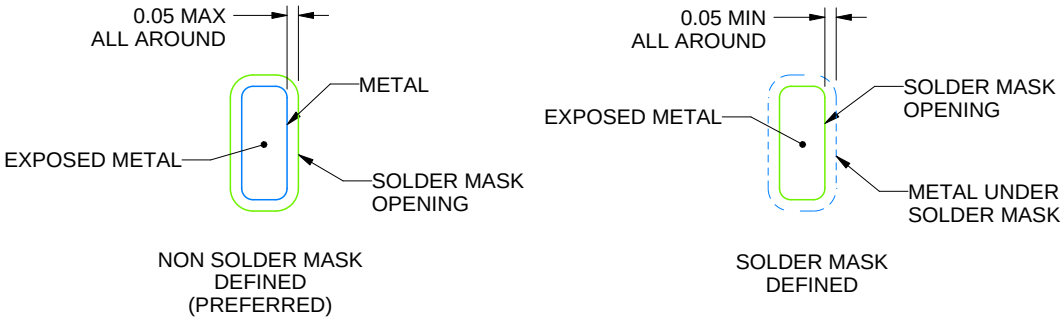


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS

4221631/B 07/2017

NOTES: (continued)

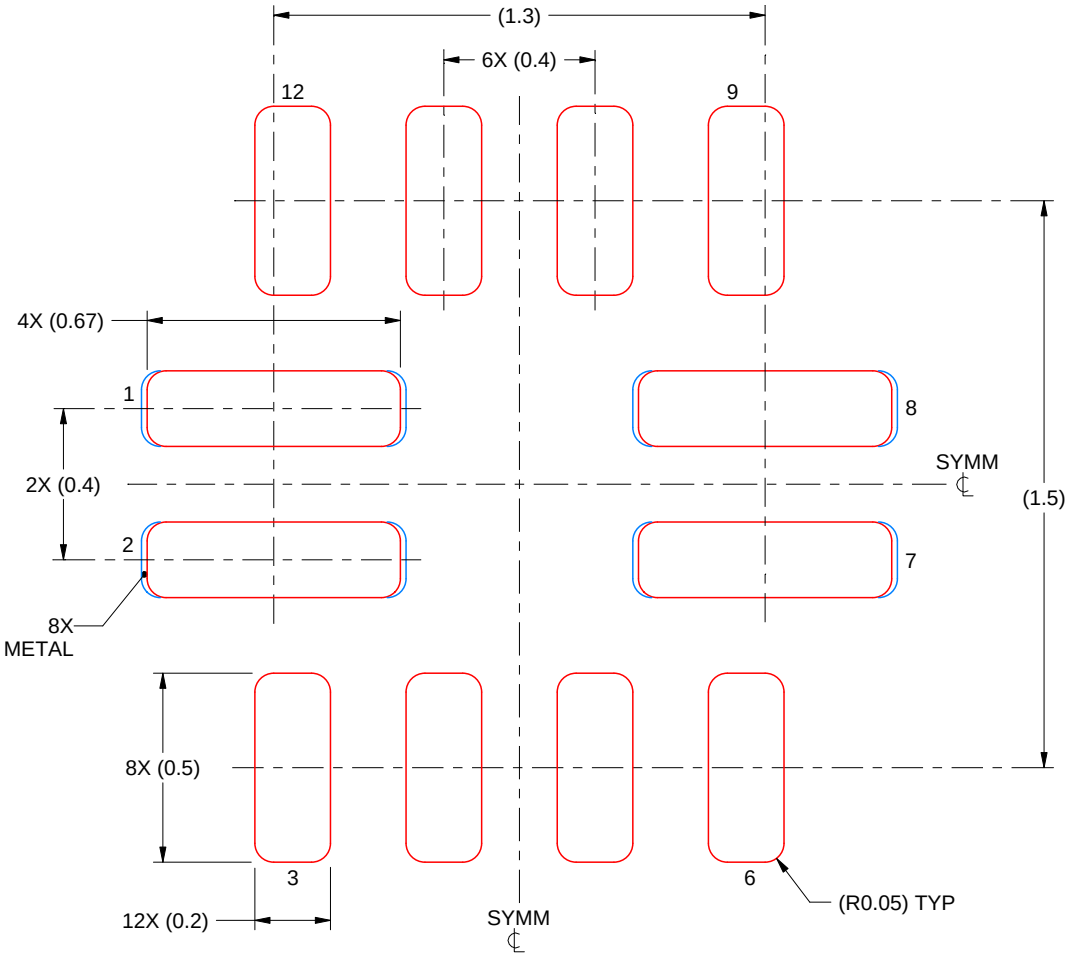
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RWB0012A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PADS 1,2,7 & 8
96% PRINTED SOLDER COVERAGE BY AREA
SCALE:50X

4221631/B 07/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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