TUSB5461-Q1 Automotive DisplayPort™ Alt Mode Over USB Type-C® Source 8.1Gbps Linear Redriver Crosspoint Switch

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature: –40°C to 105°C, T_A
- USB Type-C® crosspoint switch supporting
  - USB 3.2 + 2 DisplayPort™ Lanes
  - 4 DisplayPort™ Lanes
- USB 3.2 x1 up to 5Gbps
- VESA® DisplayPort™ 2.1 up to 8.1Gbps
- Supports D_DFP pin assignments C, D, and E
- Choice between adaptive or fixed equalization for USB DFP receivers.
- Linear and limited redriver supported on UFP transmitter
- Limited redriver option offers both TX voltage swing and TX equalization control
  - 4 levels of TX voltage swing from 800mVpp up to 1100mVpp
  - TX pre-shoot and de-emphasis
- Ultra-low-power architecture
- Up to 12dB equalization at 2.5GHz
- Transparent to DisplayPort™ link training
- Configuration through GPIO or I^2C
- Hot-plug capable
- 5mm × 7mm, 0.5mm pitch VQFN package

2 Applications

- Rear seat entertainment
- Automotive head unit
- Automotive infotainment and cluster

3 Description

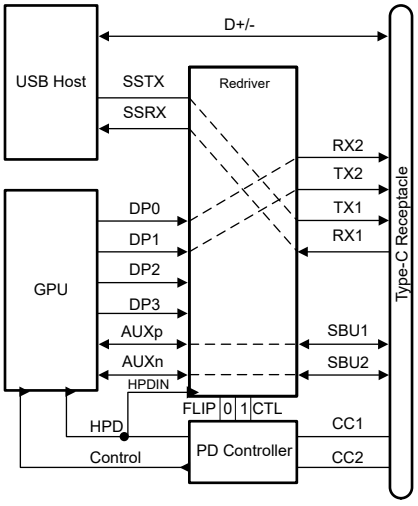
The TUSB5461-Q1 is a VESA® DisplayPort™ Alt Mode over USB Type-C® redriving switch that supports USB 3.2 data rates up to 5Gbps and DisplayPort™ 2.1 up to 8.1Gbps for downstream facing port (host). The device is used for configurations C, D, and E from the VESA® DisplayPort™ Alt Mode over USB Type-C® standard. This protocol-agnostic linear redriver is also capable of supporting other USB Type-C® Alt Mode interfaces such as HDMI® Alt Mode.

The TUSB5461-Q1 also incorporates an adaptive receiver equalization (AEQ) feature that can automatically find the best ISI compensation setting between the USB device and the TUSB5461-Q1. The AEQ finds the best setting to help improve the interoperability between a USB host and USB device. The TUSB5461-Q1 operates on a single 3.3V supply and comes in an Automotive Grade 2 temperature range.

Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)
TUSB5461-Q1	RGF (VQFN, 40)	5mm × 7mm

(1) For all available packages, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Pin Configuration and Functions

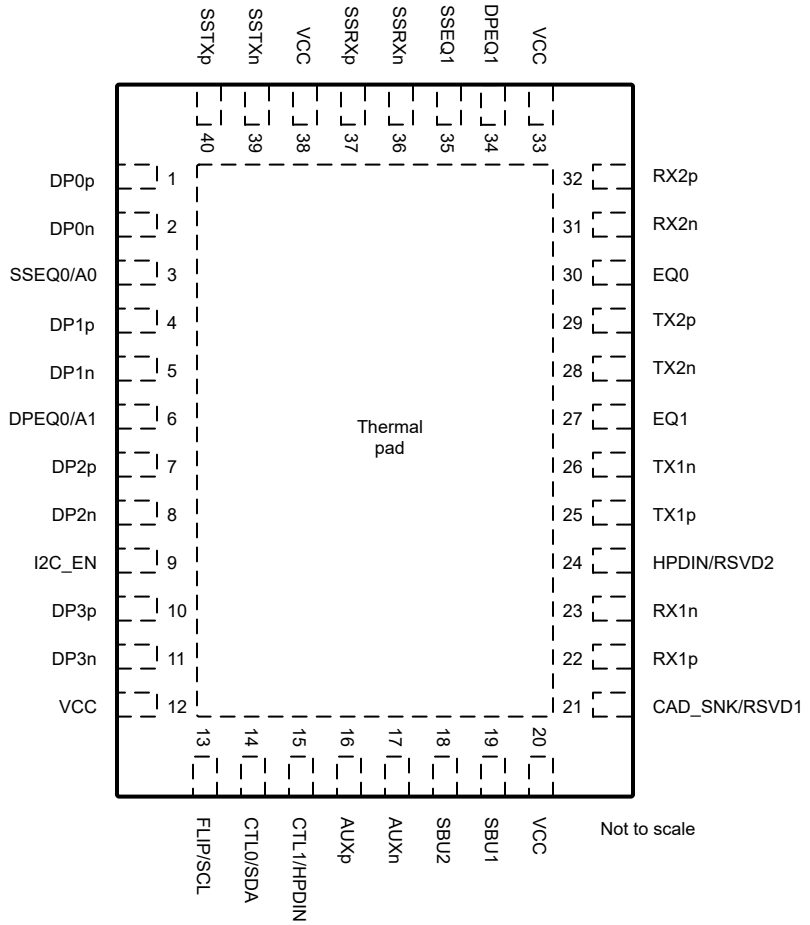


Figure 4-1. TUSB5461-Q1 RGF Package, 40-Pin VQFN (Top View)

Table 4-1. TUSB5461-Q1 Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DP0p	1	Diff I	DP Differential positive input for DisplayPort Lane 0.
DP0n	2	Diff I	DP Differential negative input for DisplayPort Lane 0.
DP1p	4	Diff I	DP Differential positive input for DisplayPort Lane 1.
DP1n	5	Diff I	DP Differential negative input for DisplayPort Lane 1.
DP2p	7	Diff I	DP Differential positive input for DisplayPort Lane 2.
DP2n	8	Diff I	DP Differential negative input for DisplayPort Lane 2.
DP3p	10	Diff I	DP Differential positive input for DisplayPort Lane 3.
DP3n	11	Diff I	DP Differential negative input for DisplayPort Lane 3.
RX1n	23	Diff I/O	Differential negative output for DisplayPort or differential negative input for USB3.2 Downstream Facing port.
RX1p	22	Diff I/O	Differential positive output for DisplayPort or differential positive input for USB3.2 Downstream Facing port.
TX1n	26	Diff O	Differential negative output for DisplayPort or USB3.2 downstream facing port.
TX1p	25	Diff O	Differential positive output for DisplayPort or USB 3.2 downstream facing port.
TX2p	29	Diff O	Differential positive output for DisplayPort or USB 3.2 downstream facing port.
TX2n	28	Diff O	Differential negative output for DisplayPort or USB 3.2 downstream facing port.
RX2p	32	Diff I/O	Differential positive output for DisplayPort or differential positive input for USB3.2 Downstream Facing port.

Table 4-1. TUSB5461-Q1 Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
RX2n	31	Diff I/O	Differential negative output for DisplayPort or differential negative input for USB3.2 Downstream Facing port.
SSTXp	40	Diff I	Differential positive input for USB3.2 upstream facing port.
SSTXn	39	Diff I	Differential negative input for USB3.2 upstream facing port.
SSRXp	37	Diff O	Differential positive output for USB3.2 upstream facing port.
SSRXn	36	Diff O	Differential negative output for USB3.2 upstream facing port.
EQ1	27	4 Level I	This pin along with EQ0 sets the USB receiver equalizer gain for downstream facing RX1 and RX2 when USB used. Refer to Table 6-7 for details on the equalization setting.
EQ0	30	4 Level I	This pin along with EQ1 sets the USB receiver equalizer gain for downstream facing RX1 and RX2 when USB used. Refer to Table 6-7 for details on the equalization setting.
CAD_SNK/RSVD1(1)	21	I/O (PD)	When I2C_EN ! = 0, this pin is reserved. Leave open if not used. When I2C_EN = 0 , this pin is CAD_SNK (L = AUX snoop enabled and H = AUX snoop disabled with all lanes active).
HPDIN/RSVD2(1)	24	I/O (PD)	When I2C_EN ! = 0, this pin is reserved. Leave open if not used. When I2C_EN = 0, this pin is an input for Hot Plug Detect received from DisplayPort sink. When HPDIN is Low for greater than 2ms, all DisplayPort lanes are disabled while the AUX-to-SBU switch remains closed.
I2C_EN	9	4 Level I	I^2C Programming Mode or GPIO Programming Select. 0 = GPIO mode (I^2C disabled) with adaptive EQ disabled. R = TI Test Mode (I^2C enabled at 3.3V) F = I^2C enabled at 1.8V when EQ0 = "0" and EQ1 = "0". Otherwise, GPIO mode (I^2C disabled) with adaptive EQ enabled. 1 = I^2C enabled at 3.3V.
SBU1	19	I/O, CMOS	SBU1. TI recommends to DC-couple this pin to the SBU1 pin on the Type-C receptacle. A 2MΩ resistor to GND is also recommended.
SBU2	18	I/O, CMOS	SBU2. TI recommends to DC-couple this pin to the SBU2 pin on the Type-C receptacle. A 2MΩ resistor to GND is also recommended.
AUXp	16	I/O, CMOS	AUXp. DisplayPort AUX positive I/O connected to the DisplayPort source through a AC-coupling capacitor. In addition to AC-coupling capacitor, this pin also requires a 100K resistor to GND. This pin along with AUXN is used by the TUSB5461-Q1 for AUX snooping and is routed to SBU1/2 based on the orientation of the Type-C.
AUXn	17	I/O, CMOS	AUXn. DisplayPort AUX negative I/O connected to the DisplayPort source through a AC-coupling capacitor. In addition to AC- coupling capacitor, this pin also requires a 100K resistor to VCC (3.3V). This pin along with AUXP is used by the TUSB5461-Q1 for AUX snooping and is routed to SBU1/2 based on the orientation of the Type-C.
DPEQ1	34	4 Level I	DisplayPort Receiver EQ. Along with DPEQ0, this pin selects the DisplayPort receiver equalization gain. Refer to Table 6-9 for details on the equalization settings.
DPEQ0/A1	6	4 Level I	DisplayPort Receiver EQ. Along with DPEQ1, this pin selects the DisplayPort receiver equalization gain. When I2C_EN is not ‘0’, this pin also sets the TUSB5461-Q1 I^2C address. Refer to Table 6-9 for details on the equalization settings.
SSEQ1	35	4 Level I	Along with SSEQ0, sets the USB receiver equalizer gain for upstream facing SSTXP/N. Refer to Table 6-8 for details on the equalization settings.
SSEQ0/A0	3	4 Level I	Along with SSEQ1, sets the USB receiver equalizer gain for upstream facing SSTXP/N. When I2C_EN is not ‘0’, this pin also sets the TUSB5461-Q1 I^2C address. Refer to Table 6-8 for details on the equalization settings.
FLIP/SCL	13	2 Level I	When I2C_EN=’0’ this is Flip control pin, otherwise this pin is I^2C clock. When used for I^2C clock, pull up the pin to the VCC I^2C supply of the I^2C controller.
CTL0/SDA	14	2 Level I	When I2C_EN=’0’ this is a USB3 Switch control pin, otherwise this pin is I^2C data. When used for I^2C data, pull up the pin to the VCC I^2C supply of the I^2C controller.
CTL1/HPDIN	15	2 Level I (Failsafe) (PD)	DP Alt mode Switch Control Pin. When I2C_EN = ‘0’, this pin enables or disables DisplayPort functionality. Otherwise, when I2C_EN is not "0", DisplayPort functionality is enabled and disabled through I^2C registers. L = DisplayPort Disabled. H = DisplayPort Enabled. When I2C_EN is not "0" this pin is an input for Hot Plug Detect received from DisplayPort sink. When this HPDIN is Low for greater than 2ms, all DisplayPort lanes are disabled and AUX-to-SBU switch remains closed.
VCC	12, 20, 33, 38	P	3.3V Power Supply
Thermal Pad		G	Ground

(1) Not a fail-safe I/O. Actively driving pin high while VCC is removed results in leakage voltage on VCC pins.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	V_{CC}	–0.3	4	V
Voltage range at any input or output pin	Differential voltage between positive and negative inputs	–2.5	2.5	V
	Voltage at differential inputs	–0.5	4	V
	CMOS Inputs	–0.5	4	V
Maximum junction temperature, T_J		–40	125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1), all pins	±2000	V
		Charged-device model (CDM), per AEQ Q100-011, all pins	±1500	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Main power supply	3.0	3.3	3.6	V
	Main supply ramp requirement	0.1		50	ms
$V_{(I2C)}$	Supply that external resistors are pulled up to on SDA and SCL	1.7		3.6	V
$V_{(PSN)}$	Supply noise on V_{CC} pins (less than 4MHz)			100	mV
T_A	Operating free-air temperature	–40		105	°C
T_{PCB}	PCB temperature (1mm away from the device)	–40		112	°C

5.4 Thermal Information

THERMAL METRIC(1)		Device RGF (VQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Power Supply Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{CC(ACTIVE-USB)}$	Average active power USB Only	Link in U0; EQ control pins = NC; PRBS7 pattern ; V_{ID} = 1000mV_{PP} ; LINR_L3; CTL1 = L; CTL0 = H		270		mW

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{CC(ACTIVE-USB-DP1)}$	Average active power USB + 2 Lane DP	Link in U0; EQ control pins = NC; PRBS7 pattern ; V_{ID} = 1000mV$_{PP}$; LINR_L3; CTL1 = H; CTL0 = H		520		mW
$P_{CC(ACTIVE--4DP)}$	Average active power 4 Lane DP Only	Four active DP lanes operating at 8.1Gbps; PRBS7 pattern; CTL1 = H; CTL0 = L; LINR_L3;		500		mW
$P_{CC(NC-USB)}$	Average power with no connection	No USB3 device is connected to TXP/TXN; CTL1 = L; CTL0 = H;		1.7		mW
$P_{CC(U2U3)}$	Average power in U2/U3	Link in U2 or U3; USB Mode Only; CTL1 = L; CTL0 = H;		2.0		mW
$P_{CC(HPDLOW--4DP)}$	Power 4 Lane DP Only when HPDIN = L	CTL1 = H; CTL0 = L; HPDIN = L;		0.475		mW
$P_{CC(DISABLED-I2C)}$	Device disabled power in I^{2}C Mode	I2C_EN != 0; HPDIN = L; CTLSEL = 0x0;		0.122		mW
$P_{CC(DISABLED)}$	Device disabled power	CTL1 = L; CTL0 = L; I2C_EN = 0; HPDIN = L;		0.110		mW

5.6 Control I/O DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4-level Inputs						
I_{IH}	High level input current	V_{CC} = 3.6V; V_{IN} = 3.6V	20		60	µA
I_{IL}	Low level input current	V_{CC} = 3.6V; V_{IN} = 0V	–100		-40	µA
4-Level V_{TH}	Threshold 0 / R	V_{CC} = 3.3V		0.55		V
4-Level V_{TH}	Threshold R/ Float	V_{CC} = 3.3V		1.65		V
4-Level V_{TH}	Threshold Float / 1	V_{CC} = 3.3V		2.7		V
R_{PU}	Internal pullup resistance			48		kΩ
R_{PD}	Internal pulldown resistance			98		kΩ
2-State CMOS Input (CTL0, CTL1, FLIP). CTL0 and FLIP are Failsafe.						
V_{IH}	High-level input voltage	V_{CC} = 3.0V	2		3.6	V
V_{IL}	Low-level input voltage	V_{CC} = 3.6V	0		0.8	V
R_{PD}	Internal pulldown resistance for HPDIN, CADSNK		300	500	600	kΩ
R_{PD}	Internal pulldown resistance for CTL1		300	400	600	kΩ
I_{IH_CTL1}	High-level input current for CTL1	V_{IN} = 3.6V	–12		12	µA
I_{IL_CTL1}	Low-level input current for CTL1	V_{IN} = GND, V_{CC} = 3.6V	–1		1	µA
$I_{IH\_HPD\_CAD}$	High-level input current for HPDIN, CADSNK	V_{IN} = 3.6V	–11		11	µA
$I_{IL\_HPD\_CAD}$	Low-level input current for HPDIN, CADSNK	V_{IN} = GND, V_{CC} = 3.6V	–1		1	µA
$I_{IH\_CTL0\_FLIP}$	High-level input current for CTL0 and FLIP	V_{IN} = 3.6V; I2C_EN = 0	–1		2	µA
$I_{IL\_CTL0\_FLIP}$	Low-level input current for CTL0 and FLIP	V_{IN} = GND, V_{CC} = 3.6V; I2C_EN = 0;	–1		1	µA
I^{2}C Control Pins (SCL, SDA)						
V_{IH_3p3V}	High-level input voltage when configured for 3.3V I^{2}C level	I2C_EN = 1	2.0		3.6	V
V_{IL_3p3V}	Low-level input voltage when configured for 3.3V I^{2}C level	I2C_EN = 1	0		0.8	V
V_{IH_1p8V}	High-level input voltage when configured for 1.8V I^{2}C level	I2C_EN = F	1.2			V
V_{IL_1p8V}	Low-level input voltage when configured for 1.8V I^{2}C level	I2C_EN = F	0		0.6	V
V_{OL}	Low-level output voltage	I2C_EN = 0; I_{OL} = 6mA	0		0.4	V
I_{OL}	Low-level output current	I2C_EN = 0; V_{OL} = 0.4V	20			mA
$I_{I(I2C)}$	Input current	0.1 × $V_{(I2C)}$ < Input voltage < 3.3V	–1		1	µA

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{I(I2C)}$	Input capacitance				10	pF
$C_{(I2C\_FM+\_BUS)}$	I^2C bus capacitance for FM+ (1MHz)				150	pF
$C_{(I2C\_FM\_BUS)}$	I^2C bus capacitance for FM (400kHz)				150	pF
$R_{(EXT\_I2C\_FM+)}$	External resistors on both SDA and SCL when operating at FM+ (1MHz)	$C_{(I2C\_FM+\_BUS)}$ = 150pF	620	820	910	Ω
$R_{(EXT\_I2C\_FM)}$	External resistors on both SDA and SCL when operating at FM (400kHz)	$C_{(I2C\_FM\_BUS)}$ = 150pF	620	1500	2200	Ω

5.7 USB and DP Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
USB Gen 2 Differential Receiver (RX1p/n, RX2p/n, SSTXp/n)						
$V_{(RX-DIFF-PP)}$	Input differential peak-peak voltage swing linear dynamic range	AC-coupled differential peak-to-peak signal measured post CTLE through a reference channel		1200		mVppd
$V_{(RX-DC-CM)}$	Common-mode voltage bias in the receiver (DC)			0		V
$V_{RX\_CM-INST}$	Maximum instantaneous RX DC common-mode voltage change for following operating states: OFF to ON, Disabled to Disconnect, U3 to Disconnect.	Measured at non-redriver side of AC-coupling capacitor with 200kΩ load.	–500		1000	mV
$V_{RX\_CM-INST}$	Maximum instantaneous RX DC common-mode voltage change for following operating states: Disconnect to U0, U0 to U3, U3 to U0.	Measured at non-redriver side of AC-coupling capacitor with 50Ω load.	–300		1000	mV
$R_{(RX-DIFF-DC)}$	Differential input impedance (DC)	Present after a USB3 device is detected on TXP/TXN	72	90	120	Ω
$R_{(RX-CM-DC)}$	Receiver DC common-mode impedance	Present after a USB3 device is detected on TXP/TXN	18		30	Ω
$Z_{(RX-HIGH-IMP-DC-POS)}$	Common-mode input impedance with termination disabled (DC)	Present when no USB3 device is detected on TXP/TXN. Measured over the range of 0V to 500mV with respect to GND.	25			kΩ
$V_{(SIGNAL-DET-DIFF-PP)}$	Input differential peak-to-peak signal detect assert level	At 5Gbps, no input loss, PRBS7 pattern		80		mVppd
$V_{(RX-IDLE-DET-DIFF-PP)}$	Input differential peak-to-peak signal detect deassert level	At 5Gbps, no input loss, PRBS7 pattern		60		mVppd
$V_{(RX-LFPS-DET-DIFF-PP)}$	Low frequency periodic signaling (LFPS) detect threshold	VCC = 3.3V; 25°C ≤ T_A ≤ 105°C; Tested at 25MHz and 300mVppd VIN; Below the minimum is squelched	100		300	mVppd
$V_{(RX-CM-AC-P)}$	Peak RX AC common-mode voltage	Measured at package pin			150	mVppd
$R_{L(RX-DIFF)}$	Differential return loss	50MHz to 1.25GHz at 90Ω;		–19		dB
$R_{L(RX-DIFF)}$	Differential return loss	2.5GHz at 90Ω;		–15		dB
$R_{L(RX-CM)}$	Common-mode return loss	50MHz to 2.5GHz at 90Ω;		–10		dB
E_{Q_SSTX0}	SSTX Receiver equalization at 100MHz	FLIPSEL = 0; SSEQ_SEL = 0;		1.8		dB
E_{Q_SSTX0}	SSTX Receiver equalization at 100MHz	FLIPSEL = 1; SSEQ_SEL = 0;		2.1		dB
E_{Q_SSTX15}	SSTX Receiver equalization at 100MHz	FLIPSEL = 0; SSEQ_SEL = 15;		3.6		dB
E_{Q_SSTX15}	SSTX Receiver equalization at 100MHz	FLIPSEL = 1; SSEQ_SEL = 15;		4.0		dB
E_{Q_SSTX15}	SSTX Receiver equalization at 2.5GHz	FLIPSEL = 0; SSEQ_SEL = 15;		12.0		dB
E_{Q_SSTX15}	SSTX Receiver equalization at 2.5GHz	FLIPSEL = 1; SSEQ_SEL = 15;		12.2		dB
E_{Q_RX0}	RX1 Receiver equalization at 100MHz	FLIPSEL = 0; EQ1_SEL = 0;		1.7		dB
E_{Q_RX15}	RX1 Receiver equalization at 100MHz	FLIPSEL = 0; EQ1_SEL = 15;		3.5		dB
E_{Q_RX15}	RX1 Receiver equalization at 2.5GHz	FLIPSEL = 0; EQ1_SEL = 15;		11.6		dB
E_{Q_RX0}	RX2 Receiver equalization at 100MHz	FLIPSEL = 1; EQ2_SEL = 0;		2.0		dB
E_{Q_RX15}	RX2 Receiver equalization at 100MHz	FLIPSEL = 1; EQ2_SEL = 15;		3.8		dB
E_{Q_RX15}	RX2 Receiver equalization at 2.5GHz	FLIPSEL = 1; EQ2_SEL = 15;		11.4		dB
$C_{AC-USB1}$	Required external AC-coupling capacitor on SSTX		75		265	nF
$C_{AC-USB2}$	Optional external AC-coupling capacitor on RX1 and RX2.		297		363	nF
USB Gen 2 Differential Transmitter (TX1p/n, TX2p/n, SSRXp/n)						
$V_{TX(DIFF-PP)}$	Transmitter dynamic differential voltage swing range.			1200		mVppd
$V_{TX(RCV-DETECT)}$	Amount of voltage change allowed during receiver detection	At T_A = 25°C;			600	mV

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{TX-CM-INST}$	Max Instantaneous TX DC common-mode voltage change under following operating states: OFF to ON, ON to OFF, Disabled to Disconnect, U3 to Disconnect.	Measured single-ended at non-redriver side of AC-coupling capacitor with 200kΩ load.	–500		1000	mV
$V_{TX-CM-INST}$	Max Instantaneous TX DC common-mode voltage change under following operating states: Disconnect to U0, U0 to U2/U3, U2/U3 to U0.	Measured single-ended at non-redriver side of AC-coupling capacitor with 50Ω load.	–300		1000	mV
$V_{TX(CM-IDLE-DELTA)}$	Transmitter idle common-mode voltage change while in U2/U3 and not actively transmitting LFPS		–300		600	mV
$V_{TX(DC-CM)}$	Common-mode voltage bias in the transmitter (DC)		0.5		1.1	V
$V_{TX(CM-AC-PP-ACTIVE)}$	Tx AC common-mode voltage active	Max mismatch from Txp + Txn for both time and amplitude			100	mVpp
$V_{TX(IDLE-DIFF-AC-PP)}$	AC electrical idle differential peak-to-peak output voltage	At package pins after high-pass filter (HPF) to remove DC component; HPF = 1/LPF; No AC or DC signals are applied at RX terminals;	0		10	mV
$V_{TX(IDLE-DIFF-DC)}$	DC electrical idle differential output voltage	At package pins after low-pass filter (LPF) to remove AC component; LPF = 1/HPF; No AC or DC signals are applied at RX terminals;	0		14	mV
$V_{TX(CM-DC-ACTIVE-IDLE-DELTA)}$	Absolute DC common-mode voltage between U1 and U0	At package pin			200	mV
$R_{TX(DIFF)}$	Differential impedance of the driver		72	90	120	Ω
$R_{TX(CM)}$	Common-mode impedance of the driver	Measured with respect to AC ground over 0V to 500mV	18		30	Ω
$V_{SSRX-LIMITED-VODL0}$	SSRX differential peak-to-peak voltage when configured for limited redriver and LINR_L0	TX_PRESHOOT_EN = 0; TX_DEEMPHASIS_EN = 0;		725		mVppd
$V_{SSRX-LIMITED-VODL1}$	SSRX differential peak-to-peak voltage when configured for limited redriver and LINR_L1	TX_PRESHOOT_EN = 0; TX_DEEMPHASIS_EN = 0;		850		mVppd
$V_{SSRX-LIMITED-VODL2}$	SSRX differential peak-to-peak voltage when configured for limited redriver and LINR_L2	TX_PRESHOOT_EN = 0; TX_DEEMPHASIS_EN = 0;		1000		mVppd
$V_{SSRX-LIMITED-VODL3}$	SSRX differential peak-to-peak voltage when configured for limited redriver and LINR_L3	TX_PRESHOOT_EN = 0; TX_DEEMPHASIS_EN = 0;		1100		mVppd
$V_{SSRX-DE-RATIO0}$	SSRX de-emphasis when configured for limited redriver and de-emphasis enabled.	TX_PRESHOOT_EN = 0; TX_DEEMPHASIS_EN = 1; TX_DEEPHASIS = 2'b00; USB_SSRX_VOD = 2'b00 (LINR_L3);		–1.5		dB
$V_{SSRX-DE-RATIO1}$	SSRX de-emphasis when configured for limited redriver and de-emphasis enabled.	TX_PRESHOOT_EN = 0; TX_DEEMPHASIS_EN = 1; TX_DEEPHASIS = 2'b01; USB_SSRX_VOD = 2'b00 (LINR_L3);		–2.1		dB
$V_{SSRX-DE-RATIO2}$	SSRX de-emphasis when configured for limited redriver and de-emphasis enabled.	TX_PRESHOOT_EN = 0; TX_DEEMPHASIS_EN = 1; TX_DEEPHASIS = 2'b10; USB_SSRX_VOD = 2'b00 (LINR_L3);		–3.2		dB
$V_{SSRX-DE-RATIO3}$	SSRX de-emphasis when configured for limited redriver and de-emphasis enabled.	TX_PRESHOOT_EN = 0; TX_DEEMPHASIS_EN = 1; TX_DEEPHASIS = 2'b11; USB_SSRX_VOD = 2'b00 (LINR_L3);		–3.8		dB
$V_{SSRX-PRESH-RATIO0}$	SSRX pre-shoot level when configured for limited redriver and pre-shoot enabled.	TX_PRESHOOT_EN = 1; TX_DEEMPHASIS_EN = 0; TX_PRESHOOT = 2'b00; USB_SSRX_VOD = 2'b00 (LINR_L3);		1.5		dB

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{SSRX-PRESH-RATIO1}$	SSRX pre-shoot level when configured for limited redriver and pre-shoot enabled.	TX_PRESHOOT_EN = 1; TX_DEEMPHASIS_EN = 0; TX_PRESHOOT = 2'b01; USB_SSRX_VOD = 2'b00 (LINR_L3);		2.0		dB
$V_{SSRX-PRESH-RATIO2}$	SSRX pre-shoot level when configured for limited redriver and pre-shoot enabled.	TX_PRESHOOT_EN = 1; TX_DEEMPHASIS_EN = 0; TX_PRESHOOT = 2'b10; USB_SSRX_VOD = 2'b00 (LINR_L3);		2.3		dB
$V_{SSRX-PRESH-RATIO3}$	SSRX pre-shoot level when configured for limited redriver and pre-shoot enabled.	TX_PRESHOOT_EN = 1; TX_DEEMPHASIS_EN = 0; TX_PRESHOOT = 2'b11; USB_SSRX_VOD = 2'b00 (LINR_L3);		2.8		dB
$I_{TX(SHORT)}$	TX short circuit current	TX± shorted to GND			40	mA
$R_{LTX(DIFF)}$	Differential return loss	50MHz to 1.25GHz at 90Ω		–20		dB
$R_{LTX(DIFF)}$	Differential return loss	2.5GHz at 90Ω		–20		dB
$R_{LTX(CM)}$	Common-mode return loss	50MHz to 2.5GHz at 90Ω		–8.5		dB
$C_{TX-AC(COUPLING)}$	External required AC-coupling capacitor		75		265	nF
AC Characteristics						
Crosstalk	Differential crosstalk between TX and RX signal pairs	At 2.5GHz; EQ = 0;		–40		dB
$CP_{LF-LINRL0}$	Low-frequency –1dB compression point at LINR_L0 setting.	At 100MHz, 200mVpp < V_{ID} < 1200mVpp, EQ = 0		750		mVppd
$CP_{HF-LINRL0}$	High-frequency –1dB compression point at LINR_L0 setting.	At 2.5GHz, 200mVpp < V_{ID} < 1200mVpp, EQ = 0		725		mVppd
$CP_{HF-LINRL0}$	High-frequency –1dB compression point at LINR_L0 setting.	At 5GHz, 200mVpp < V_{ID} < 1200mVpp, EQ = 0		675		mVppd
$CP_{LF-LINRL1}$	Low-frequency –1dB compression point at LINR_L1 setting.	At 100MHz, 200mVpp < V_{ID} < 1200mVpp, EQ = 0		850		mVppd
$CP_{HF-LINRL1}$	High-frequency –1dB compression point at LINR_L1 setting.	At 2.5GHz, 200mVpp < V_{ID} < 1200mVpp, EQ = 0		825		mVppd
$CP_{HF-LINRL1}$	High-frequency –1dB compression point at LINR_L1 setting.	At 5GHz, 200mVpp < V_{ID} < 1200mVpp, EQ = 0		740		mVppd
$CP_{LF-LINRL2}$	Low-frequency –1dB compression point at LINR_L2 setting.	At 100MHz, 200mVpp < V_{ID} < 1200mVpp, EQ = 0		975		mVppd
$CP_{HF-LINRL2}$	High-frequency –1dB compression point at LINR_L2 setting.	At 2.5GHz, 200mVpp < V_{ID} < 1200mVpp, EQ = 0		950		mVppd
$CP_{HF-LINRL2}$	High-frequency –1dB compression point at LINR_L2 setting.	At 5GHz, 200mVpp < V_{ID} < 1200mVpp, EQ = 0		800		mVppd
$CP_{LF-LINRL3}$	Low-frequency –1dB compression point at LINR_L3 setting.	At 100MHz, 200mVpp < V_{ID} < 1200mVpp, EQ = 0		1050		mVppd
$CP_{HF-LINRL3}$	High-frequency –1dB compression point at LINR_L3 setting.	At 2.5GHz, 200mVpp < V_{ID} < 1200mVpp, EQ = 0		980		mVppd
$CP_{HF-LINRL3}$	High-frequency –1dB compression point at LINR_L3 setting.	At 5GHz, 200mVpp < V_{ID} < 1200mVpp, EQ = 0		775		mVppd
t_{TX_DJ}	TX output deterministic residual jitter	VID = 1Vppd; Optimual EQ setting; 12in prechannel (SDD21 = –11.2dB at 5GHz); 1.6in post channel (SDD21 = –1.8dB at 5GHz); PRBS7; USB3 at 5Gbps		0.025		UI
t_{TX_DJ}	TX output deterministic residual jitter	VID = 0.8Vppd; Optimual EQ setting; 12in prechannel (SDD21 = –8.2dB at 5GHz); 1.6in post channel (SDD21 = –1.8dB at 5GHz); PRBS7; DP at 8.1Gbps		0.06		UI
DisplayPort Receiver (DP[3:0]p/n)						
$V_{ID(PP)}$	Peak-to-peak input differential dynamic voltage range			1400		V
V_{IC}	Input common-mode voltage		0.8	1.75	2	V

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{RX\_CM-INST}$	Maximum instantaneous RX DC common-mode voltage change under following operating states: OFF to ON, Disabled to 4DP low power, 4DP active to Disabled. (1)	Measured single-ended at non-redriver side of AC-coupling capacitor with 200kΩ load.	–1200		1000	mV
$V_{RX\_CM-INST}$	Maximum instantaneous RX DC common-mode voltage change under following operating states: Disabled to 4DP active (D0), D0 to D3, D3 to D0.	Measured single-ended at non-redriver side of AC-coupling capacitor with 50Ω load.	–500		1000	mV
d_R	Data rate				8.1	Gbps
$R_{(ti)}$	Input termination resistance		72	90	110	Ω
$C_{(AC)}$	External required AC-coupling capacitor		75		265	nF
E_{Q_DP0}	DP0 Receiver equalization at 100MHz	FLIPSEL = 0; DP0EQ_SEL = 0;		–0.2		dB
E_{Q_DP15}	DP0 Receiver equalization at 100MHz	FLIPSEL = 0; DP0EQ_SEL = 15;		2.3		dB
E_{Q_DP0}	DP0 Receiver equalization at 4.05GHz	FLIPSEL = 0; DP0EQ_SEL = 0;		0.6		dB
E_{Q_DP15}	DP0 Receiver equalization at 4.05GHz	FLIPSEL = 0; DP0EQ_SEL = 15;		14.5		dB
DisplayPort Transmitter (TX1p/n, TX2p/n, RX1p/n, RX2p/n)						
$V_{TX-CM-INST}$	Maximum instantaneous TX DC common-mode voltage change for following operating states: Disabled to 4DP active (D0), D0 to D3, D3 to D0.	Measured at non-redriver side of AC-coupling capacitor with 50Ω load.	–500		1000	mV
$V_{TX-CM-INST}$	Maximum instantaneous TX DC common-mode voltage change under following operating states: Disabled to 4DP low power, 4DP active to Disabled	Measured at non-redriver side of AC-coupling capacitor with 200kΩ load.	–1000		1000	mV
$V_{TX(DC-CM)}$	Common-mode voltage bias in the transmitter (DC)		0.6		1	V
$R_{TX(DIFF)}$	Differential impedance of the driver		72	90	120	Ω
AUXp or AUXn and SBU1 or SBU2						
R_{ON}	Output ON resistance	V_{CC} = 3.3V; V_I = 0V to 0.4V for AUXp; V_I = 2.7V to 3.6V for AUXn			6	Ω
ΔR_{ON}	ON resistance mismatch within pair	V_{CC} = 3.3V; V_I = 0V to 0.4V for AUXP; V_I = 2.7V to 3.6V for AUXN			1.0	Ω
$R_{ON(FLAT)}$	ON resistance flatness (RON max – RON min) measured at identical VCC and temperature	V_{CC} = 3.3V; V_I = 0V to 0.4V for AUXp; V_I = 2.7V to 3.6V for AUXn			1.0	Ω
$V_{(AUXP\_DC\_CM)}$	AUX Channel DC common-mode voltage for AUXp and SBU1.	V_{CC} = 3.3V;	0		0.4	V
$V_{(AUXN\_DC\_CM)}$	AUX Channel DC common-mode voltage for AUXn and SBU2	V_{CC} = 3.3V;	2.7		3.6	V

(1) Instantaneous common-mode excursions observed by GPU (DPTX) can be minimized by disabling redriver prior to disabling DPTX termination.

5.8 Timing Requirements

			MIN	NOM	MAX	UNIT
USB3.2						
$t_{IDLEEntry}$	Delay from U0 to electrical idle	Refer to Figure 6-4		10		ns
$t_{IDELExit\_U1}$	U1 exist time: break in electrical idle to the transmission of LFPS	Refer to Figure 6-4		6		ns
$t_{IDLEExit\_U2U3}$	U2/U3 exit time: break in electrical idle to transmission of LFPS	Refer to Figure 6-4		10		µs
t_{RXDET_INTVL}	RX detect interval while in Disconnect				12	ms
$t_{IDLEExit\_DISC}$	Disconnect Exit Time			10		µs
t_{Exit_SHTDN}	Shutdown Exit Time			1		ms
$t_{AEQ\_FULL\_DONE}$	Maximum time to obtain optimum EQ setting when operating in Full AEQ mode.				300	µs
$t_{AEQ\_FAST\_DONE}$	Maximum time to determine appropriate EQ setting when operating in Fast AEQ mode.				60	µs

			MIN	NOM	MAX	UNIT
t_{DIFF_DLY}	Differential Propagation Delay	Refer to Figure 6-3			300	ps
t_R, t_F	Output Rise/Fall time	20%-80% of differential voltage measured 1.7 inch from the output pin; Refer to Figure 6-5.		40		ps
t_{RF_MM}	Output Rise/Fall time mismatch	20%-80% of differential voltage measured 1.7 inch from the output pin			2.6	ps
Power-up						
t_{D_PG}	$V_{CC(min)}$ to internal Power Good asserted high	Refer to Figure 6-10			27	ms
t_{CFG_SU}	CFG(1) pins setup(2)	Refer to Figure 6-10	800			µs
t_{CFG_HD}	CFG(1) pins hold	Refer to Figure 6-10	10			µs
t_{CTL_DB}	CTL[1:0] and FLIP pin debounce	Refer to Figure 6-10			16	ms

(1) Following pins comprise CFG pins: I2C_EN, EQ[1:0], SSEQ[1:0], and DPEQ[1:0].
(2) Recommend CFG pins are stable when V_{CC} is at min.

5.9 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUXp or AUXn and SBU1 or SBU2						
t_{AUX_PD}	Switch propagation delay				400	ps
$t_{AUX\_SW\_OFF}$	Switching time CTL1 to switch OFF. Not including TCTL1_DEBOUNCE.	Refer to Figure 6-7.			500	ns
$t_{AUX\_SW\_ON}$	Switching time CTL1 to switch ON	Refer to Figure 6-6.			500	ns
USB and DisplayPort Mode Transition Requirement GPIO Mode						
$t_{GP\_USB\_4DP}$	Min overlap of CTL0 and CTL1 when transitioning from USB3 only mode to 4-Lane DisplayPort mode or vice versa.	I2C_EN = 0; Refer to Figure 6-2.	4			µs
CTL1 and HPDIN						
$t_{HPDIN\_DEBOUNCE}$	CTL1 and HPDIN debounce time when transitioning from H to L.		2		10	ms
I^2C						
f_{SCL}	I^2C clock frequency				1	MHz
t_{BUF}	Bus-free time between START and STOP conditions	Refer to Figure 6-1	0.5			µs
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock pulse is generated	Refer to Figure 6-1	0.26			µs
t_{LOW}	Low period of the I^2C clock	Refer to Figure 6-1	0.5			µs
t_{HIGH}	High period of the I^2C clock	Refer to Figure 6-1	0.26			µs
t_{SUSTA}	Setup time for a repeated START condition	Refer to Figure 6-1	0.26			µs
t_{HDDAT}	Data hold time	Refer to Figure 6-1	0.008			µs
t_{SUDAT}	Data setup time	Refer to Figure 6-1	50			ns
t_R	Rise time of both SDA and SCL signals	Refer to Figure 6-1			120	ns
t_F	Fall time of both SDA and SCL signals	Refer to Figure 6-1	1.2		120	ns
t_{SUSTO}	Setup time for STOP condition	Refer to Figure 6-1	0.26			µs
C_b	Capacitive load for each bus line				150	pF

5.10 Typical Characteristics

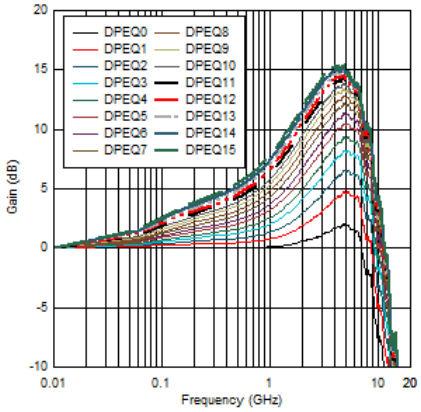


Figure 5-1. DisplayPort EQ Settings Curves

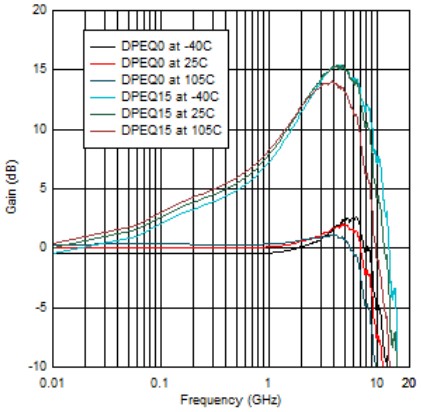


Figure 5-2. DisplayPort EQ Settings Curves Across Temperature

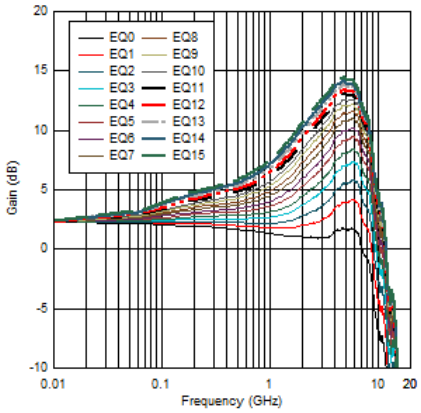


Figure 5-3. USB RX1 EQ Settings Curves

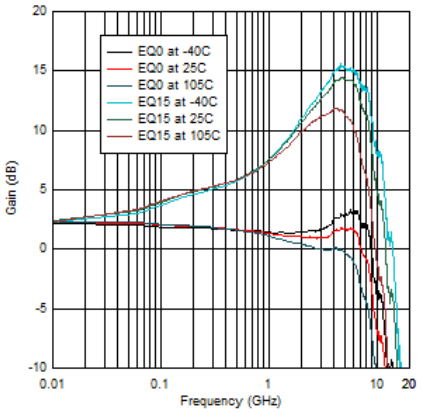


Figure 5-4. USB RX1 EQ Settings Curves Across Temperature

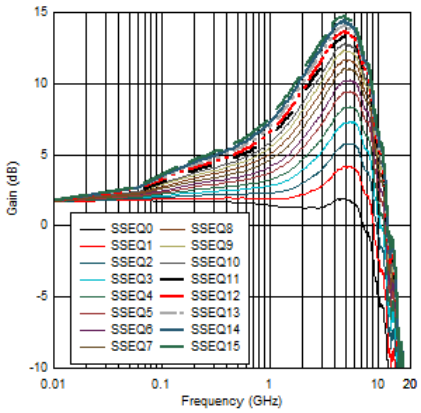


Figure 5-5. USB SSTX EQ Settings Curves

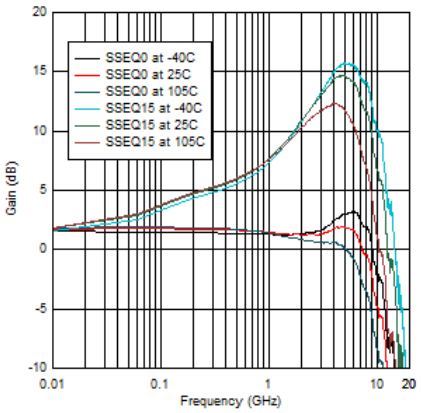


Figure 5-6. USB SSTX EQ Settings Curves Across Temperature

5.10 Typical Characteristics (continued)

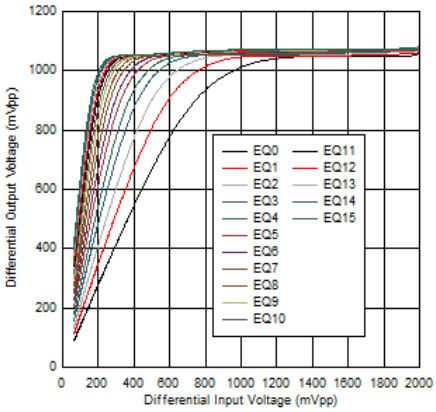


Figure 5-7. DisplayPort Linearity Curves at 4.05GHz

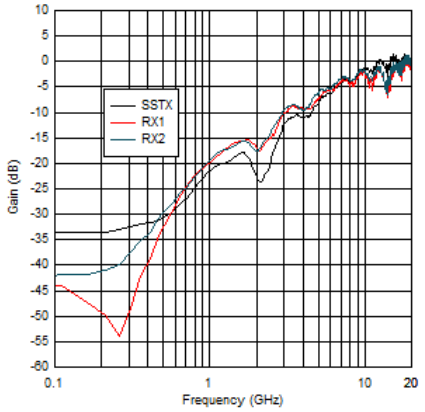


Figure 5-8. USB Input Return Loss Performance

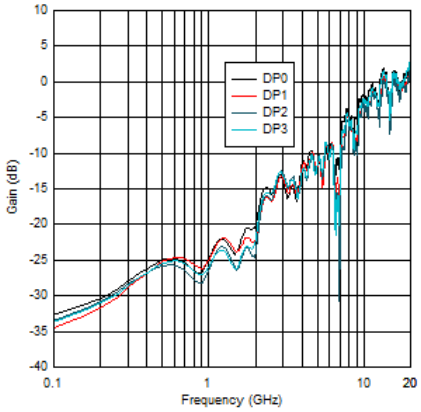


Figure 5-9. DisplayPort Input Return Loss Performance

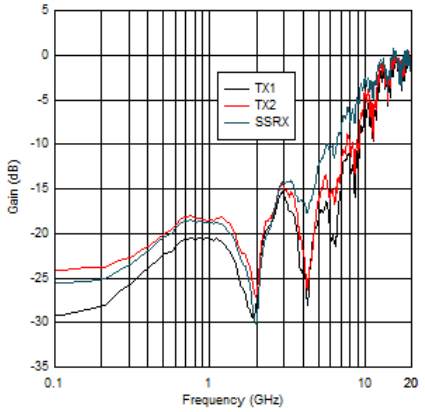


Figure 5-10. USB Output Return Loss Performance

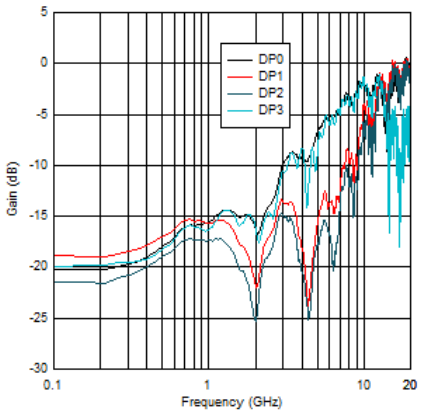


Figure 5-11. DisplayPort Output Return Loss Performance

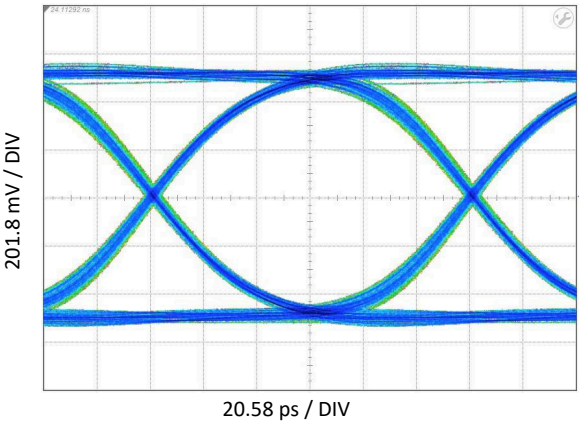


Figure 5-12. DisplayPort HBR3 Eye-Pattern Performance with 12in Input PCB Trace at 8.1Gbps

5.10 Typical Characteristics (continued)

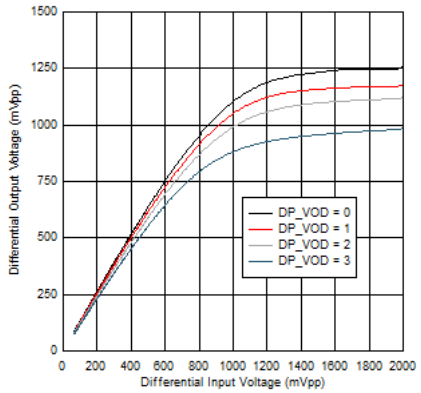


Figure 5-13. DP VOD Linearity Settings at 100MHz

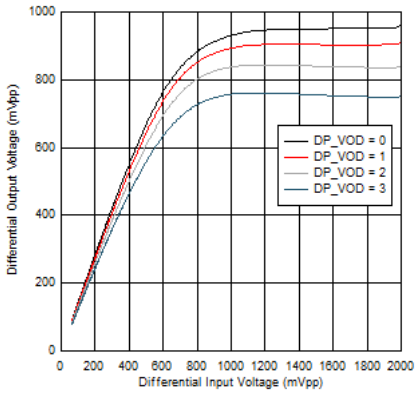


Figure 5-14. DP VOD Linearity Settings at 5GHz

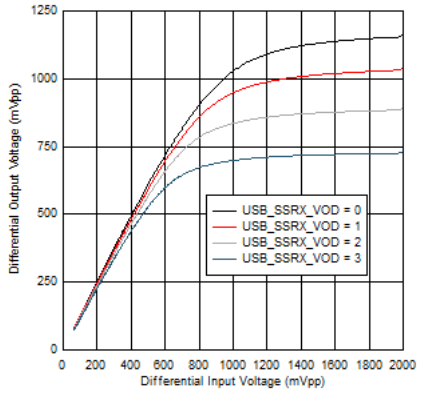


Figure 5-15. USB SSRX VOD Linearity Settings at 100MHz

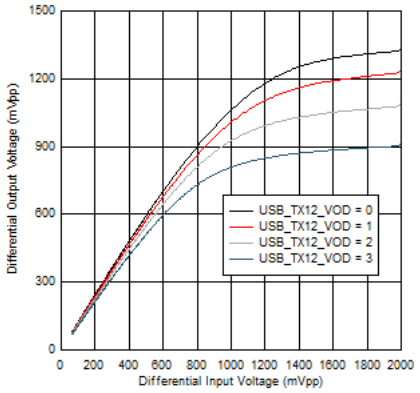


Figure 5-16. USB TX1 VOD Linearity Settings at 100MHz

Parameter Measurement Information

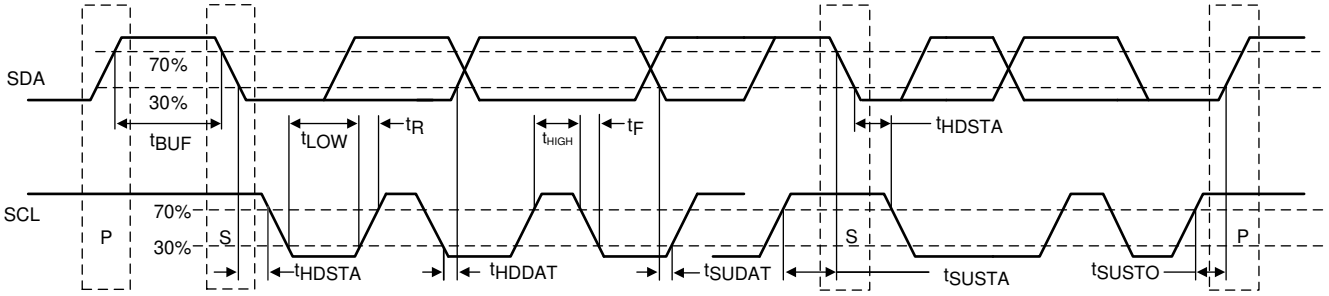


Figure 6-1. I²C Timing Diagram Definitions

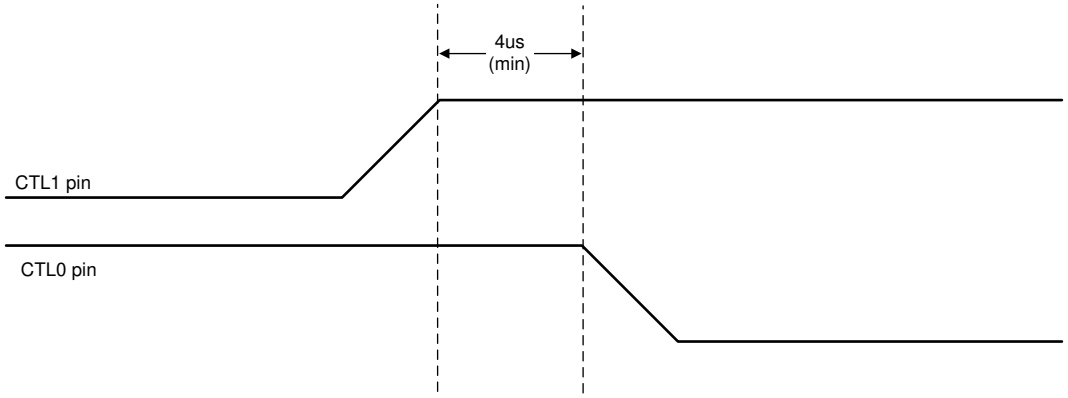


Figure 6-2. USB to 4-Lane DisplayPort in GPIO Mode

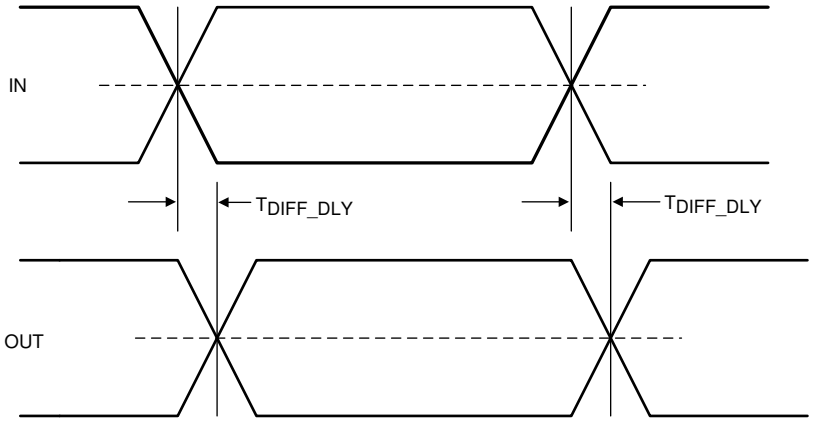


Figure 6-3. Propagation Delay

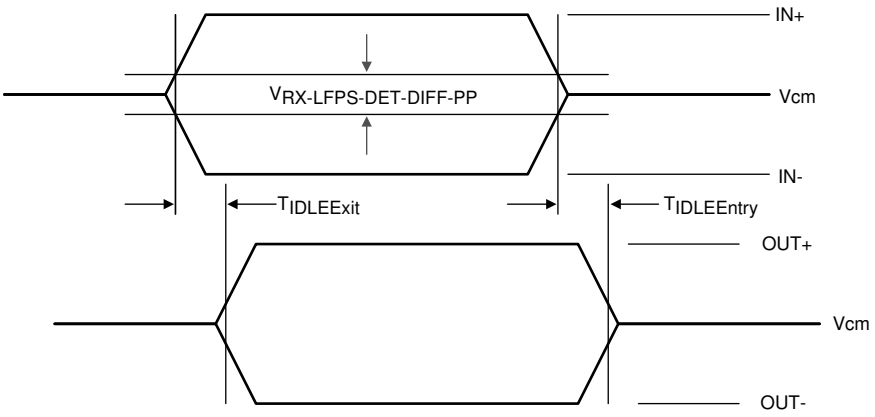


Figure 6-4. Electrical Idle Mode Exit and Entry Delay

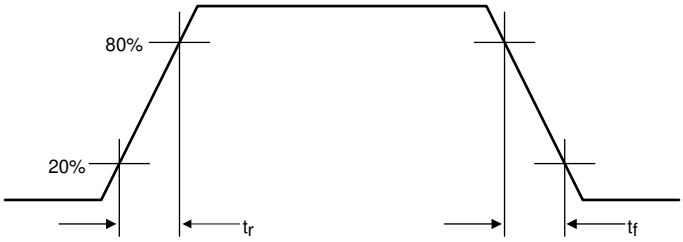


Figure 6-5. Output Rise and Fall Times

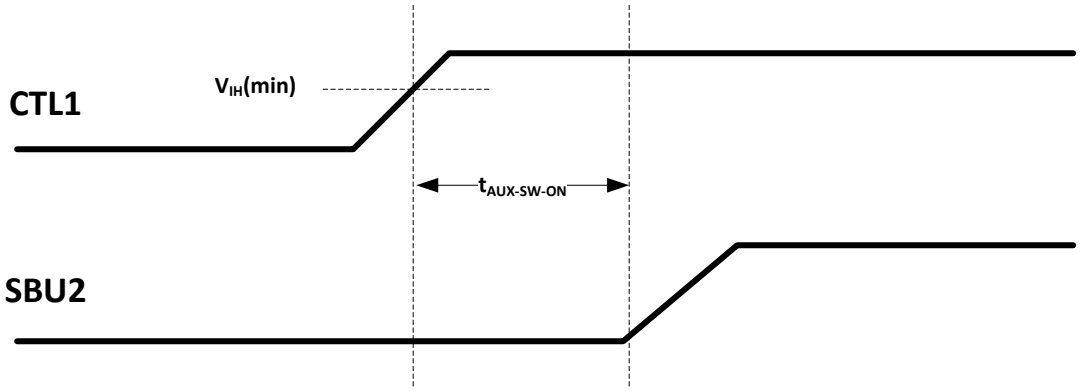


Figure 6-6. AUX to SBU Switch ON Timing Diagram

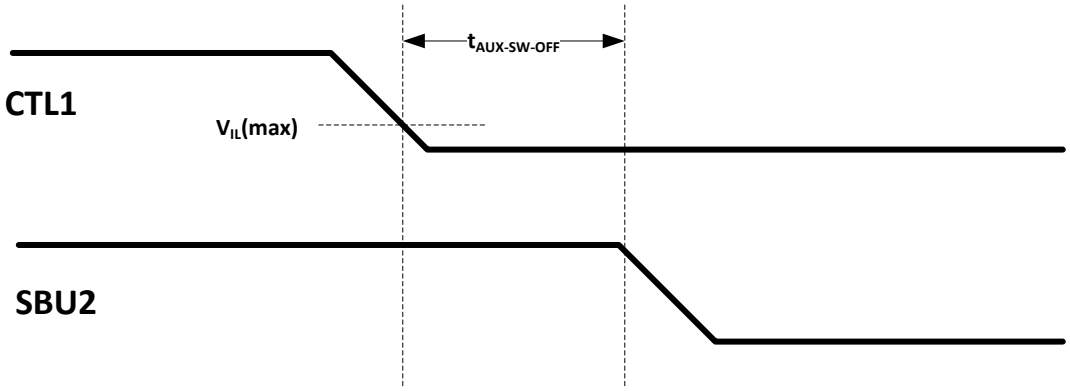


Figure 6-7. AUX to SBU Switch OFF Timing Diagram

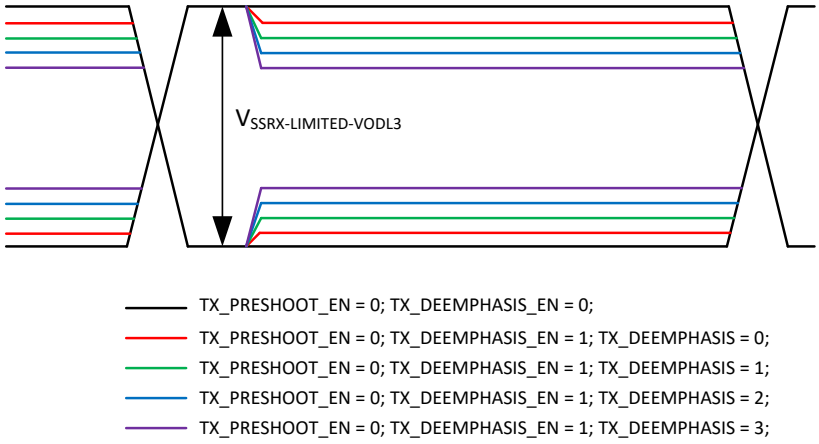


Figure 6-8. SSRX Limited De-emphasis Only

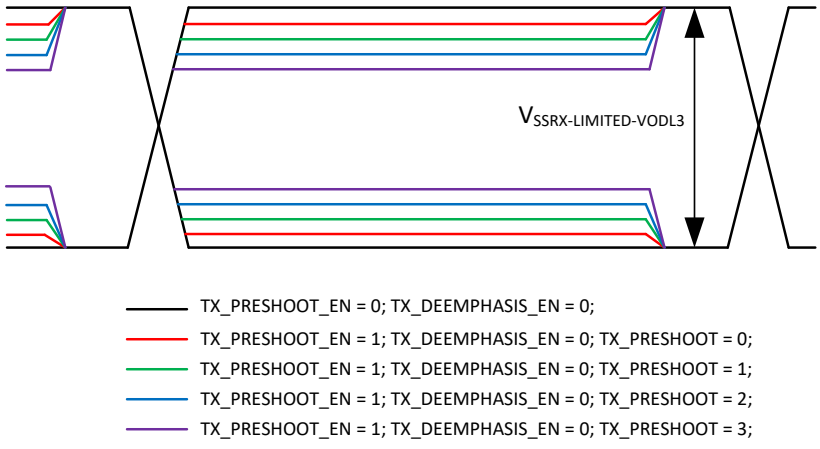


Figure 6-9. SSRX Limited Pre-Shoot Only

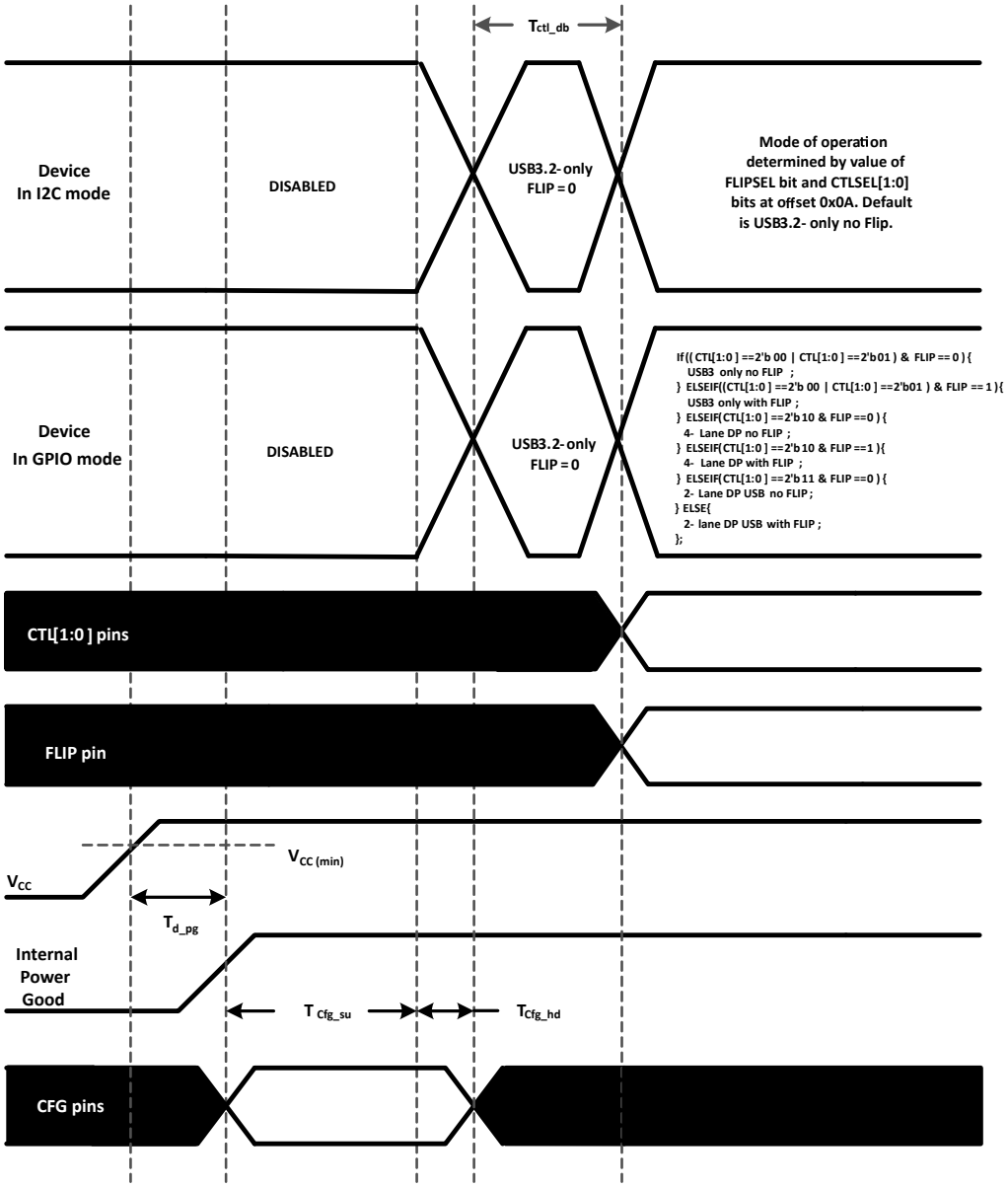


Figure 6-10. Power-On Timing

6 Detailed Description

6.1 Overview

The TUSB5461-Q1 is a VESA DisplayPort Alt Mode over USB Type-C redriving switch that supports DisplayPort data rates up to 8.1Gbps for downstream facing port. The device uses 5th generation USB redriver technology as well as an adaptive equalization feature on the DFP receivers. The device is used for DFP configurations C, D, and E from the VESA DisplayPort Alt Mode over USB Type-C.

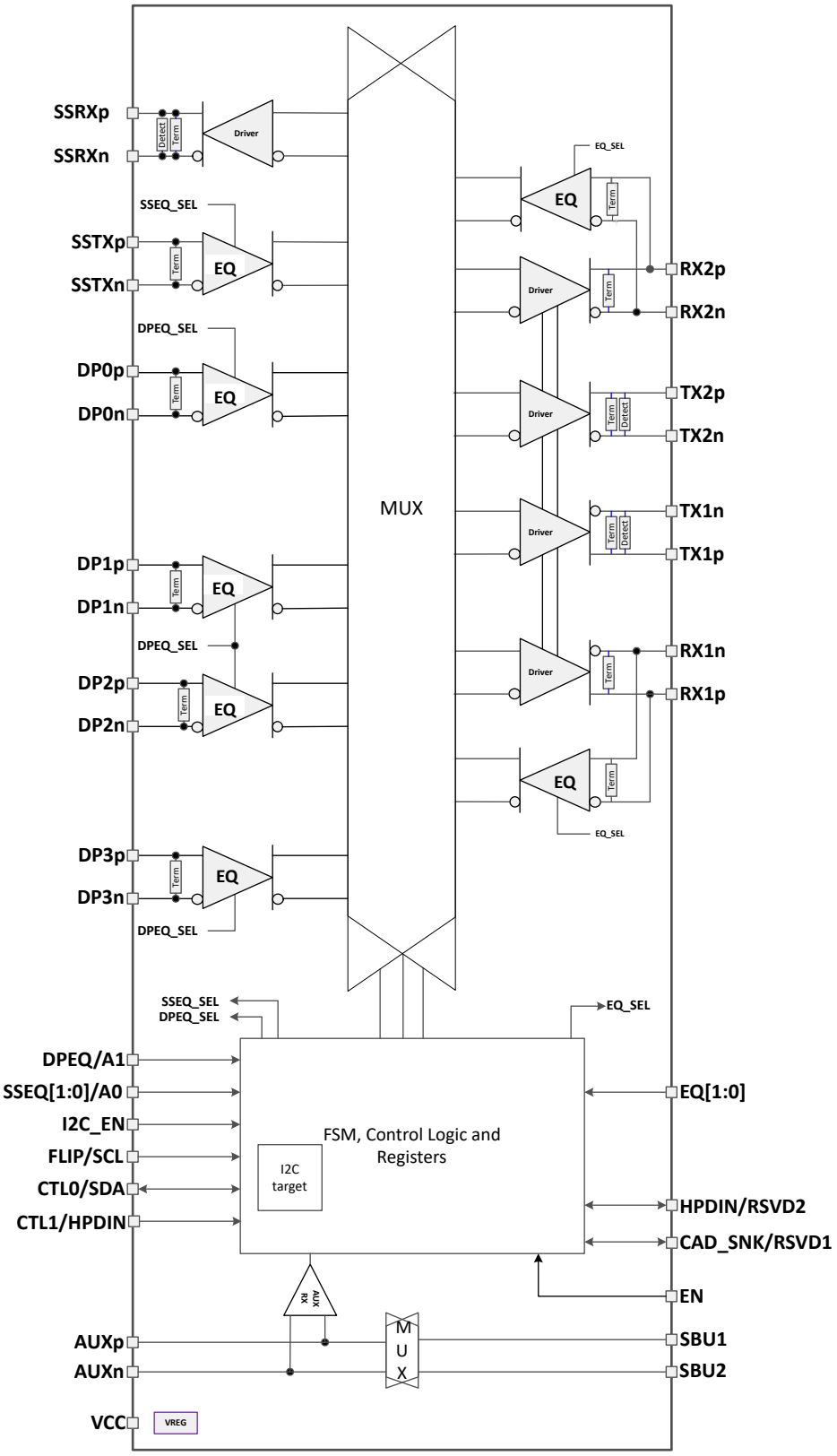
The TUSB5461-Q1 provides several levels of receive equalization to compensate for cable and board trace loss due to inter-symbol interference (ISI) when USB 3.2 or DisplayPort 2.1 signals travel across a PCB or cable. The TUSB5461-Q1 requires a 3.3V power supply and comes in an Automotive Grade 2 temperature range.

For a host application, the TUSB5461-Q1 enables the system to pass both transmitter compliance and receiver jitter tolerance tests for USB 3.2 and DisplayPort version 2.1. The redriver recovers incoming data by applying equalization that compensates for channel loss, and drives out signals with a high differential voltage. Each channel has a receiver equalizer with selectable gain settings. Set the equalization based on the amount of insertion loss before the TUSB5461-Q1 receivers. Independent equalization control for each channel can be set using EQ[1:0], SSEQ[1:0], and DPEQ[1:0] pins.

The TUSB5461-Q1 advanced state machine makes the device transparent to hosts and devices. After power up, the TUSB5461-Q1 periodically performs receiver detection on the TX pairs. If the device detects a USB 3.2 receiver, the RX termination is enabled, and the TUSB5461-Q1 is ready to redrive.

The device ultra-low-power architecture operates at a 3.3V power supply and achieves enhanced performance. The automatic LFPS de-emphasis control further enables the system to be USB3.2 compliant.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 USB 3.2

The TUSB5461-Q1 supports USB 3.2 datarates up to 5Gbps. The TUSB5461-Q1 supports all the USB defined power states (U0, U1, U2, and U3). The TUSB5461-Q1 is a linear redriver, therefore the device cannot decode USB3.2 physical layer traffic. The TUSB5461-Q1 monitors the actual physical layer conditions like receiver termination, electrical idle, LFPS, and SuperSpeed signaling rate to determine the USB power state of the USB 3.2 interface.

The TUSB5461-Q1 features an intelligent low frequency periodic signaling (LFPS) detector. The LFPS detector automatically senses the low frequency signals and disables receiver equalization functionality. When not receiving LFPS, the TUSB5461-Q1 enables receiver equalization based on the EQ[1:0] and SSEQ[1:0] pins or values programmed into EQ1_SEL, EQ2_SEL, and SSEQ_SEL registers.

6.3.2 DisplayPort

The TUSB5461-Q1 supports up to four DisplayPort lanes at datarates up to 8.1Gbps. The TUSB5461-Q1, when configured in DisplayPort mode, monitors the native AUX traffic as the flow traverses between DisplayPort source and DisplayPort sink. For the purposes of reducing power, the TUSB5461-Q1 manages the number of active DisplayPort lanes based on the content of the AUX transactions. The TUSB5461-Q1 snoops native AUX writes to the DPCD registers 0x00101 (LANE_COUNT_SET) and 0x00600 (SET_POWER_STATE) of the DisplayPort sink. The TUSB5461-Q1 disables or enables lanes based on value written to LANE_COUNT_SET. The TUSB5461-Q1 disables all lanes when SET_POWER_STATE is in the D3. Otherwise active lanes are based on value of LANE_COUNT_SET.

DisplayPort AUX snooping is enabled by default but can be disabled by changing the AUX_SNOOP_DISABLE register. When AUX snoop is disabled, management of TUSB5461-Q1 DisplayPort lanes are controlled through various configuration registers. When TUSB5461-Q1 is enabled for GPIO mode (I2C_EN = "0"), the CAD_SNK pin can be used to disable AUX snooping. When CAD_SNK pin is high, the AUX snooping functionality is disabled and all four DisplayPort lanes are active.

6.3.3 4-Level Inputs

The TUSB5461-Q1 has (I2C_EN, EQ[1:0], DPEQ[1:0], and SSEQ[1:0]) 4-level inputs pins that are used to control the equalization gain and place the TUSB5461-Q1 into different modes of operation. These 4-level inputs use a resistor divider to help set the four valid levels and provide a wider range of control settings. There are internal pullup and pulldown resistors. These resistors, together with the external resistor connection combine to achieve the desired voltage level.

Table 6-1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Tie 1 KΩ 5% to GND.
R	Tie 20 KΩ 5% to GND.
F	Float (leave pin open)
1	Tie 1 KΩ 5%to V_{CC}.

Note

All 4-level inputs are latched after rising edge of the internal reset. After t_{cfg_hd}, the internal pullup and pulldown resistors are isolated to save power.

6.3.4 Receiver Linear Equalization

The purpose of receiver equalization is to compensate for channel insertion loss and inter-symbol interference in the system before the input of the TUSB5461-Q1. The receiver overcomes these losses by attenuating the low-frequency components of the signals with respect to the high frequency components. Select the proper gain setting to match the channel insertion loss before the input of the TUSB5461-Q1 receivers. Two 4-level inputs

pins enable up to 16 possible equalization settings. USB3.2 upstream path, USB3.2 downstream path, and DisplayPort each have two 4-level inputs. The TUSB5461-Q1 also provides the flexibility of adjusting settings through I^2C registers.

The TUSB5461-Q1 implements three different equalizer features for the USB-C downstream facing port receivers (RX1 and RX2): Fixed EQ, Fast Adaptive EQ (Fast AEQ), and Full Adaptive EQ (Full AEQ). The default operation is Fixed EQ. In Fixed EQ operation, a single setting is used for all possible devices (with and without cable) inserted into the USB-C receptacle. The Fast AEQ feature can distinguish between a short channel and a long channel. A short channel represents a low loss use case of a USB 3.2 device plugged directly into USB-C receptacle without a cable. A long channel represents the high loss use case of the USB 3.2 device plugged into the receptacle through a USB cable. In Fast AEQ mode, the TUSB5461-Q1 selects between two pre-determined settings based on whether or not channel is short or long. When the TUSB5461-Q1 is configured for Full AEQ, the TUSB5461-Q1 automatically determines the best equalization setting each time a USB device is inserted into the USB-C receptacle. In Full AEQ mode, the TUSB5461-Q1 always determines the best settings regardless if the channel is short, long or somewhere in between. The Full AEQ feature is disabled by default but can be enabled through a register.

6.4 Device Functional Modes

6.4.1 Device Configuration in GPIO Mode

The TUSB5461-Q1 is in GPIO configuration when I2C_EN = “0” or when I2C_EN = "F" and !(EQ0 = "0" and EQ1 = "0"). The TUSB5461-Q1 supports the following configurations: USB 3.2 only, 2 DisplayPort lanes + USB 3.2, or 4 DisplayPort lanes (no USB 3.2). The CTL1 pin controls whether DisplayPort is enabled. The combination of CTL1 and CTL0 selects between USB 3.2 only, 2 lanes of DisplayPort, or 4 lanes of DisplayPort as detailed in Table 6-2. The AUXp or AUXn to SBU1 or SBU2 mapping is controlled based on Table 6-3.

After power-up (V_{CC} from 0V to 3.3V), the TUSB5461-Q1 defaults to USB3.2 mode. The USB PD controller upon detecting no device attached to Type-C port or USB3.2 operation not required by attached device must take TUSB5461-Q1 out of USB3.2 mode by transitioning the CTL0 pin from L to H and back to L.

Table 6-2. GPIO Configuration Control

CTL1 PIN	CTL0 PIN	FLIP PIN	TUSB5461-Q1 CONFIGURATION	VESA DisplayPort ALT MODE DFP_D CONFIGURATION
L	L	L	Power Down	—
L	L	H	Power Down	—
L	H	L	One Port USB 3.2 – No Flip	—
L	H	H	One Port USB 3.2 – With Flip	—
H	L	L	4 Lane DP – No Flip	C and E
H	L	H	4 Lane DP – With Flip	C and E
H	H	L	One Port USB 3.2 + 2 Lane DP – No Flip	D
H	H	H	One Port USB 3.2 + 2 Lane DP – With Flip	D

Table 6-3. GPIO AUXp or AUXn to SBU1 or SBU2 Mapping

CTL1 PIN	FLIP PIN	MAPPING
H	L	AUXp → SBU1 AUXn → SBU2
H	H	AUXp → SBU2 AUXn → SBU1
L > 2ms	X	Open

Table 6-4 shows the mux routing of the TUSB5461-Q1 device. This table is valid for both I^2C and GPIO configuration modes.

Table 6-4. INPUT to OUTPUT Mapping

CTL1 PIN	CTL0 PIN	FLIP PIN	FROM	TO
			INPUT PIN	OUTPUT PIN
L	L	L	NA	NA
L	L	H	NA	NA
L	H	L	RX1P	SSRXP
			RX1N	SSRXN
			SSTXP	TX1P
			SSTXN	TX1N
L	H	H	RX2P	SSRXP
			RX2N	SSRXN
			SSTXP	TX2P
			SSTXN	TX2P
H	L	L	DP0P	RX2P
			DP0N	RX2N
			DP1P	TX2P
			DP1N	TX2N
			DP2P	TX1P
			DP2N	TX1N
			DP3P	RX1P
			DP3N	RX1N
H	L	H	DP0P	RX1P
			DP0N	RX1N
			DP1P	TX1P
			DP1N	TX1N
			DP2P	TX2P
			DP2N	TX2N
			DP3P	RX2P
			DP3N	RX2N
H	H	L	RX1P	SSRXP
			RX1N	SSRXN
			SSTXP	TX1P
			SSTXN	TX1N
			DP0P	RX2P
			DP0N	RX2N
			DP1P	TX2P
			DP1N	TX2N
H	H	H	RX2P	SSRXP
			RX2N	SSRXN
			SSTXP	TX2P
			SSTXN	TX2N
			DP0P	RX1P
			DP0N	RX1N
			DP1P	TX1P
			DP1N	TX1N

6.4.2 Device Configuration In I²C Mode

The TUSB5461-Q1 is in I²C mode when I2C_EN is not equal to “0” or when I2C_EN = "F" and EQ0 = "0" and EQ1 = "0". The same configurations defined in GPIO mode are also available in I²C mode. The TUSB5461-Q1 USB3.2 and DisplayPort configuration is controlled based on Table 6-5. The AUXp or AUXn to SBU1 or SBU2 mapping control is based on Table 6-6.

Table 6-5. I²C Configuration Control

REGISTERS			TUSB5461-Q1 CONFIGURATION	VESA DisplayPort ALT MODE DFP_D CONFIGURATION
CTLSEL1	CTLSEL0	FLIPSEL		
0	0	0	Power Down	—
0	0	1	Power Down	—
0	1	0	One Port USB 3.2 - No Flip	—
0	1	1	One Port USB 3.2 – With Flip	—
1	0	0	4 Lane DP - No Flip	C and E
1	0	1	4 Lane DP – With Flip	C and E
1	1	0	One Port USB 3.2 + 2 Lane DP- No Flip	D
1	1	1	One Port USB 3.2 + 2 Lane DP– With Flip	D

Table 6-6. I²C AUXp or AUXn to SBU1 or SBU2 Mapping

REGISTERS				MAPPING
AUX_SBU_OVR1	AUX_SBU_OVR0	CTLSEL1	FLIPSEL	
0	0	1	0	AUXp → SBU1 AUXn → SBU2
0	0	1	1	AUXp → SBU2 AUXn → SBU1
0	0	0	X	Open
0	1	X	X	AUXp → SBU1 AUXn → SBU2
1	0	X	X	AUXp → SBU2 AUXn → SBU1
1	1	X	X	Open

6.4.3 DisplayPort Mode

The TUSB5461-Q1 supports up to four DisplayPort lanes at datarates up to 8.1Gbps. TUSB5461-Q1 can be enabled for DisplayPort through GPIO control or through I²C register control. When I2C_EN is ‘0’, DisplayPort is controlled based on Table 6-2. When not in GPIO mode, enable of DisplayPort functionality is controlled through I²C registers.

6.4.4 Linear EQ Configuration

Each of the TUSB5461-Q1 receiver lanes has individual controls for receiver equalization. The receiver equalization gain value can be controlled either through I^2C registers or through GPIOs. Table 6-7 details the gain value for each available combination when the TUSB5461-Q1 is in GPIO mode. These same options are also available in I^2C mode by updating registers DP0EQ_SEL, DP1EQ_SEL, DP2EQ_SEL, DP3EQ_SEL, EQ1_SEL, EQ2_SEL, and SSEQ_SEL.

Table 6-7. USB Downstream Facing Port Receiver (RX1 and RX2 Pins) Equalization Control

Register(s): EQ1_SEL or EQ2_SEL Equalization Setting #	EQ1 PIN Level	EQ0 PIN Level	EQ Gain at 2.5 GHz minus Gain at 100MHz (dB)
0	0	0	-1.0
1	0	R	0.0
2	0	F	0.9
3	0	1	1.8
4	R	0	2.6
5	R	R	3.4
6	R	F	4.0
7	R	1	4.6
8	F	0	5.2
9	F	R	5.7
10	F	F	6.1
11	F	1	6.5
12	1	0	6.8
13	1	R	7.1
14	1	F	7.5
15	1	1	7.8

Table 6-8. USB Upstream Facing Port Receiver (SSTX Pins) Equalization Control

Register(s): SSEQ_SEL Equalization Setting #	SSEQ1 PIN LEVEL	SSEQ0 PIN LEVEL	EQ Gain at 2.5GHz minus Gain at 100MHz (dB)
0	0	0	-0.5
1	0	R	0.6
2	0	F	1.5
3	0	1	2.5
4	R	0	3.2
5	R	R	4.0
6	R	F	4.6
7	R	1	5.2
8	F	0	5.7
9	F	R	6.3
10	F	F	6.6
11	F	1	7.1
12	1	0	7.4
13	1	R	7.8
14	1	F	8.0
15	1	1	8.4

Table 6-9. DisplayPort Receiver (DP[3:0] Pins) Equalization Control

Register(s): DP0EQ_SEL, DP1EQ_SEL, DP2EQ_SEL, or DP3EQ_SEL Equalization Setting #	DPEQ1 PIN LEVEL	DPEQ0 PIN LEVEL	EQ Gain at 2.7/4.05/5GHz minus Gain at 100MHz (dB)
0	0	0	0.4/0.8/0.83
1	0	R	2.0/3.1/3.4
2	0	F	3.0/4.6/5.0
3	0	1	4.2/6.0/6.5
4	R	0	5.0/7.0/7.5
5	R	R	6.0/8.0/8.4
6	R	F	6.5/8.7/9.1
7	R	1	7.2/9.4/9.8
8	F	0	7.8/10.0/10.3
9	F	R	8.3/10.4/10.7
10	F	F	8.7/10.7/10.9
11	F	1	9.1/11.1/11.2
12	1	0	9.4/11.3/11.3
13	1	R	9.7/11.5/11.5
14	1	F	10.0/11.7/11.6
15	1	1	10.2/11.8/11.7

6.4.5 Linearity VOD

The TUSB5461-Q1 provides four different linearity VOD settings. All four settings are available in I^2C mode through register control. In GPIO mode, the linearity VOD is fixed at LINR_L3.

Note

TX1 and TX2 is shared between DP and USB modes. For the case in which the TX_SWING_DFP setting is different between USB-only (CTLSEL = 2'b01) and 4-lane DP (CTLSEL = 2'b10), the external PD controller must write the appropriate values for DP and USB into TX_SWING_DFP register. TI recommends to change these registers before entering the USB or DP mode. Keep in mind that when CTLSEL = 2'b11 (DP+USB) the setting written to TX_SWING_DFP applies to both USB and DP. Therefore when CTLSEL = 2'b11 the PD controller can write the highest common setting. For example, if the setting used for 4-lane DP (CTLSEL = 2'b10) is LINR_L2 and the setting for USB-only (CTLSEL = 2'b01) is LINR_L1, then the PD controller can set TX_SWING_DFP to LINR_L2 when CTLSEL = 2'b10.

6.4.6 VOD Modes

The TUSB5461-Q1 provides two modes for VOD (voltage output differential) control: Linearity VOD and Limited VOD. The TUSB5461-Q1 defaults linearity VOD mode but can be changed to limited VOD mode through the I^2C register.

6.4.6.1 Linearity VOD

Linearity VOD defines the linearity range of the TUSB5461-Q1. When the TUSB5461-Q1 is in linear VOD mode, the output VOD is a linear function of the input VID. For example, if the signal at TUSB5461-Q1 input (VID) is at 600mVpp then the TUSB5461-Q1 output VOD is approximately 600mVpp. The linear VOD mode is the only mode available for the downstream paths (DisplayPort and USB). The upstream path (USB only) supports both linear and limited VOD. Linearity VOD mode is the default operation of the TUSB5461-Q1. The TUSB5461-Q1 provides four different linearity VOD settings. All four settings are available in I^2C mode through register control.

6.4.6.2 Limited VOD

Limited VOD mode is used to set the actual VOD level and is used when the TUSB5461-Q1 is configured in limited redriver mode. In this mode the VOD is no longer a linear function of the input VID. For example, if the signal at TUSB5461-Q1 input (VID) is at 600mVpp then the TUSB5461-Q1 output VOD is approximately 1000mVpp (assuming LINR_L3 is selected). The limited redriver mode is only supported in the upstream direction (RX1 → SSRX and RX2 → SSRX). The downstream paths always operate in linear redriver mode. Limited redriver mode can be enabled by I^2C register. This mode is not supported in GPIO mode. The TUSB5461-Q1 provides four different limited VOD settings. All four settings are available through register control.

6.4.7 Transmit Equalization

The TUSB5461-Q1 in limited redriver mode offers both SSRX transmitter pre-shoot and de-emphasis controls. The TUSB5461-Q1 offers four pre-shoot levels and four de-emphasis levels. These levels can be changed by modifying I^2C registers. Pre-shoot is enabled when SSRX_LIMIT_ENABLE bit = 1 and TX_PRESHOOT_EN bit= 1. De-emphasis is enabled when SSRX_LIMIT_ENABLE bit = 1 and TX_DEEPHASIS_EN = 1.

6.4.8 USB3.2 Modes

The TUSB5461-Q1 monitors the physical layer conditions like receiver termination, electrical idle, LFPS, and SuperSpeed signaling rate to determine the state of the USB3.2 interface. Depending on the state of the USB 3.2 interface, the TUSB5461-Q1 can be in one of four primary modes of operation when USB 3.2 is enabled (CTL0 = H or CTLSEL0 = 1b1): Disconnect, U2/U3, U1, and U0.

The disconnect mode is the state in which TUSB5461-Q1 has not detected far-end termination on both upstream facing port (UFP) or downstream facing port (DFP). The disconnect mode is the lowest power mode of each of the four modes. The TUSB5461-Q1 remains in this mode until far-end receiver termination is detected on both UFP and DFP. The TUSB5461-Q1 immediately exits this mode and enters U0 after far-end termination is detected.

When in U0 mode, the TUSB5461-Q1 redrives all traffic received on UFP and DFP. U0 is the highest power mode of all USB3.2 modes. The TUSB5461-Q1 remains in U0 mode until electrical idle occurs on both UFP and DFP. Upon detecting electrical idle, the TUSB5461-Q1 immediately transitions to U1.

The U1 mode is the intermediate mode between U0 mode and U2/U3 mode. In U1 mode, the TUSB5461-Q1 UFP and DFP receiver termination remains enabled. The UFP and DFP transmitter DC common-mode voltage is maintained. The power consumption in U1 is similar to power consumption of U0.

Next to the disconnect mode, the U2/U3 mode is next lowest power state. While in this mode, the TUSB5461-Q1 periodically performs far-end receiver detection. Anytime the far-end receiver termination is not detected on either UFP or DFP, the TUSB5461-Q1 leaves the U2/U3 mode and transitions to the disconnect mode. The device also monitors for a valid LFPS. Upon detection of a valid LFPS, the TUSB5461-Q1 immediately transitions to the U0 mode. In U2/U3 mode, the TUSB5461-Q1 receiver terminations remain enabled but the TX DC common-mode voltage is not maintained.

6.4.9 Downstream Facing Port Adaptive Equalization

The TUSB5461-Q1 implements an adaptive equalizer (AEQ) function for the USB-C downstream facing port receivers (RX1 and RX2). The purpose of the adaptive equalizer function is determine the best EQ value such that output jitter is minimized. The TUSB5461-Q1 provides two modes of adaptive equalization: Fast AEQ and Full AEQ. The selection between Fast and Full AEQ is determined by a register. The AEQ feature is disabled by default but can enabled through a register. The Full adaptive equalization feature is supported in GPIO mode when I2C_EN pin = "F" and !(EQ0 pin = "0" and EQ1 = "0").

Note

The AEQ feature is NOT supported on SSTX receiver and the DP[3:0] receivers. These receivers only support fixed EQ.

TI recommends to configure TUSB5461-Q1 for I^{2}C mode when using adaptive EQ features as this provides the most flexibility.

6.4.9.1 Fast Adaptive Equalization in I^{2}C Mode

The Fast AEQ mode is used to distinguish two channels (short channel and a long channel) and choose the appropriate receiver equalization setting for that channel. Fast AEQ only distinguishes between two choices, therefore the AEQ time is a lot shorter than Full AEQ mode, which minimizes impact to USB link training.

When Fast AEQ is enabled and channel is determined to be short, the TUSB5461-Q1 uses the value programmed into the EQx_SEL, where x = 1 or 2. If the TUSB5461-Q1 determines channel is not short, the TUSB5461-Q1 switches to the EQ value programmed into the LONG_EQx register, where x = 1 or 2. During initial system evaluation, TI recommends to perform both short and long channel USB3.2 RX JTOL testing and program EQx_SEL and LONG_EQx to the value which produced the best results for each channel configuration.

The TUSB5461-Q1 determines short and long based on the estimate eye height. The value programmed into FASTAEQ_LIMITS register determine the eye height limits. Software can change the defaults of this register to lower or raise the limits.

Note

EQ_OVERRIDE field must be set for values programmed into EQx_SEL and LONG_EQx to be used.

TI recommends to change the FASTAEQ_LIMITS register from the default value to 0x2 (80mV).

6.4.9.2 Full Adaptive Equalization

The Full AEQ mode attempts to find the best equalization value for RX1 and RX2 receivers by starting at the lowest EQ value and sweeping through all EQ combinations up to the value programmed into FULLAEQ_UPPER_EQ field. The default is to sweep through all sixteen EQ values (zero to fifteen). The number of EQ combinations can be reduced by programming FULLAEQ_UPPER_EQ register. The TUSB5461-Q1 also provides the ability to add or subtract some over/under equalization to compensate for channel in front of the TUSB5461-Q1 by programming OVER_EQ_CTRL field to a non-zero value. If OVER_EQ_SIGN = 0, the TUSB5461-Q1 adds the value programmed into OVER_EQ_CTRL to the EQ value determined by the full adaptation. If OVER_EQ_SIGN = 1, the TUSB5461-Q1 subtracts the value programmed into OVER_EQ_CTRL from the EQ value determined by the full adaptation. For example, if full adaptation determines the best equalization value to be 4 and OVER_EQ_CTRL is 2 and OVER_EQ_SIGN = 0, the EQ setting used by the TUSB5461-Q1 is 6. The TUSB5461-Q1 hardware always limits the sum of OVER_EQ_CTRL and the determined optimal EQ from full adaptation to be less than or equal to 15.

6.4.9.3 Full Adaptive Equalization in GPIO Mode (I2C_EN = "F")

The Full AEQ feature is supported in GPIO mode when the following condition is true: I2C_EN == "F" && !(EQ0 == "0" && EQ1 == "0"). When the TUSB5461-Q1 is configured for Full AEQ in GPIO mode, the TUSB5461-Q1 operates in linear redriver mode.

6.5 Programming

6.5.1 Transition Between Modes

The TUSB5461-Q1 allows for transitioning between any mode (USB-only to 4DP, 4DP to USB+2DP, and so forth). The USB-C standard requires transitioning to the USB Safe State before entering to or exiting from an Alternate Mode. The USB Safe State defines an electrical state for the SBU1/2 and SSTX/SSRX for DFPs, UFPs, and Active Cables when transitioning between USB and an Alternate Mode. Therefore before entering to or exiting from four lane DP mode, TI recommends to first enter the Disable state (CTLSEL = 2'b00 or (CTL0 pin = 0 and CTL1 pin = 0)).

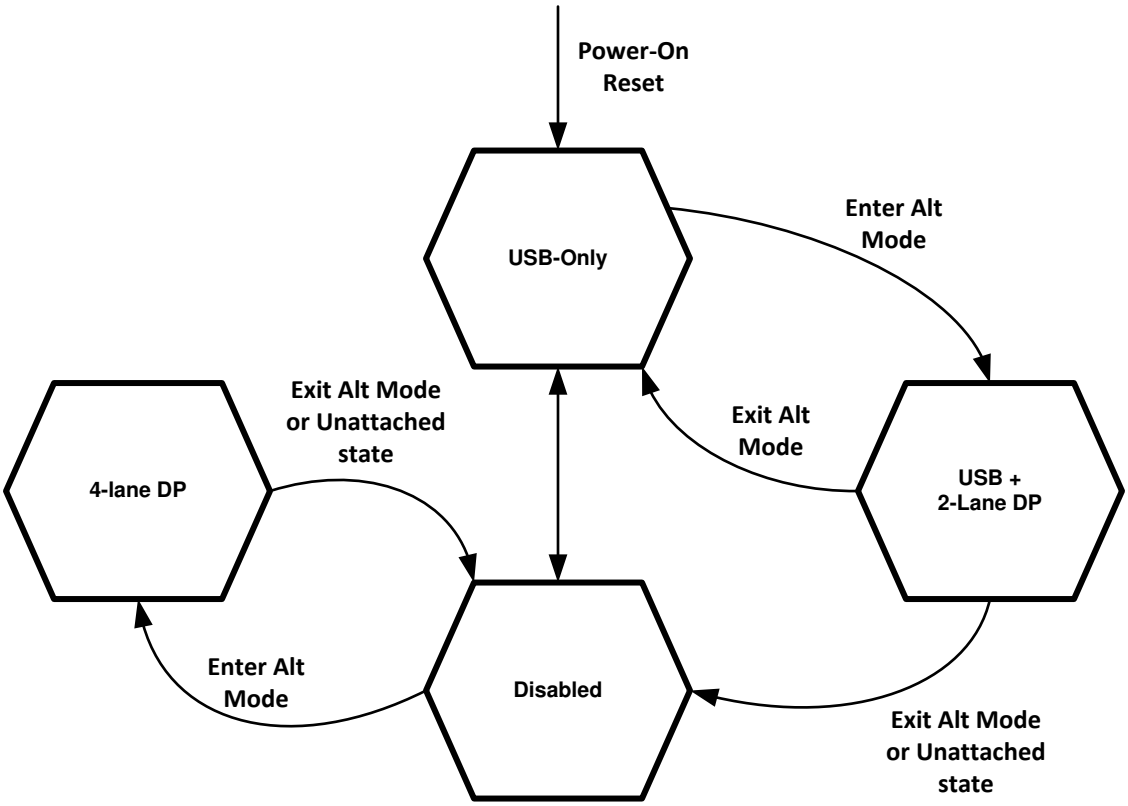


Figure 6-1. Recommended Mode Transitions

6.5.2 Pseudocode Examples

6.5.2.1 Fast AEQ With Linear Redriver Mode

```
// (address, data)
// Initial power-on configuration.
(0x0A, 0x11), // EQ_OVERRIDE and USB3.1 default.
(0x1C, 0x81), // Fast AEQ enable
(0x10, 0x55), // DP lanes 0 and 1 EQ
(0x11, 0x55), // DP lanes 2 and 2 EQ
(0x1D, 0x10), // FASTAEQ_LIMITS to 80mV
(0x1E, 0x55), // USB-C Rx1/Rx2 Long channel EQ.
(0x20, 0x00), // USB-C Rx1/Rx2 Short channel EQ.
(0x21, 0x05), // SSTX receiver EQ.
```

```
// Controls when selecting between USB and DP modes.
If (USBonly_normal)
{ (0x0A,0x11); }
Else if (USBonly_flip)
```

```
{ (0x0A, 0x15); }
Else if (Dponly_normal)
{ (0x0A, 0x12); }
Else if (Dponly_flip)
{ (0x0A, 0x16); }
Else if (DPUSB_normal)
{ (0x0A, 0x13); }
Else if (DPUSB_flip)
{ (0x0A,0x17); }
Else // Nothing connected to Type-C
{ (0x0A, 0x10); }
```

6.5.2.2 Fast AEQ With Limited Redriver Mode

```
// (address, data)
// Initial power-on configuration.
(0x0A, 0x91), // EQ_OVERRIDE and USB3.1 default.
(0x0B, 0x24), // Pre-shoot and De-emphasis control
(0x1C, 0x81), // Fast AEQ enable
(0x10, 0x55), // DP lanes 0 and 1 EQ
(0x11, 0x55), // DP lanes 2 and 2 EQ
(0x1D, 0x10), // FASTAEQ_LIMITS to 80mV
(0x1E, 0x55), // USB-C Rx1/Rx2 Long channel EQ.
(0x20, 0x00), // USB-C Rx1/Rx2 Short channel EQ.
(0x21, 0x05), // SSTX receiver EQ.
(0x32, 0x40), // VOD Control.
```

```
// Controls when selecting between USB and DP modes.
If (USBonly_normal)
{ (0x0A,0x91); }
Else if (USBonly_flip)
{ (0x0A, 0x95); }
Else if (Dponly_normal)
{ (0x0A, 0x92); }
Else if (Dponly_flip)
{ (0x0A, 0x96); }
Else if (DPUSB_normal)
{ (0x0A, 0x93); }
Else if (DPUSB_flip)
{ (0x0A,0x97); }
Else // Nothing connected to Type-C
{ (0x0A, 0x90); }
```

6.5.2.3 Full AEQ With Linear Redriver Mode

```
// (address, data)
// Initial power-on configuration.
(0x0A, 0x11), // EQ_OVERRIDE and USB3.1 default.
(0x1C, 0x83), //Full AEQ enable
(0x10, 0x55), // DP lanes 0 and 1 EQ
(0x11, 0x55), // DP lanes 2 and 2 EQ
(0x20, 0x11), // USB-C Rx1/Rx2 EQ. Not used in Full AEQ
(0x21, 0x05), // SSTX receiver EQ.
```

```
// Controls when selecting between USB and DP modes.
If (USBonly_normal)
{ (0x0A,0x11); }
Else if (USBonly_flip)
{ (0x0A, 0x15); }
Else if (Dponly_normal)
{ (0x0A, 0x12); }
Else if (Dponly_flip)
{ (0x0A, 0x16); }
Else if (DPUSB_normal)
{ (0x0A, 0x13); }
Else if (DPUSB_flip)
{ (0x0A,0x17); }
```

```
Else // Nothing connected to Type-C
{ (0x0A, 0x10); }
```

6.5.2.4 Full AEQ With Limited Redriver Mode

```
// (address, data)
// Initial power-on configuration.
(0x0A, 0x91), // Limited Redriver, EQ_OVERRIDE and USB3.1 default.
(0x0B, 0x24), // Pre-shoot and De-emphasis control
(0x1C, 0x83), //Full AEQ enable
(0x10, 0x55), // DP lanes 0 and 1 EQ
(0x11, 0x55), // DP lanes 2 and 2 EQ
(0x20, 0x11), // USB-C Rx1/Rx2 EQ. Not used in Full AEQ
(0x21, 0x05), // SSTX receiver EQ.
(0x32, 0x40), // VOD Control.
```

```
// Controls when selecting between USB and DP modes.
If (USBonly_normal)
{ (0x0A,0x91); }
Else if (USBonly_flip)
{ (0x0A, 0x95); }
Else if (Dponly_normal)
{ (0x0A, 0x92); }
Else if (Dponly_flip)
{ (0x0A, 0x96); }
Else if (DPUSB_normal)
{ (0x0A, 0x93); }
Else if (DPUSB_flip)
{ (0x0A,0x97); }
Else // Nothing connected to Type-C
{ (0x0A, 0x90); }
```

6.5.3 TUSB5461-Q1 I²C Address Options

For further programmability, the TUSB5461-Q1 can be controlled using I²C. The SCL and SDA pins are used for I²C clock and I²C data, respectively.

Table 6-10. TUSB5461-Q1 I²C Target Address

DPEQ0/A1 PIN LEVEL	SSEQ0/A0 PIN LEVEL	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)
0	0	1	0	0	0	1	0	0	0/1
0	R	1	0	0	0	1	0	1	0/1
0	F	1	0	0	0	1	1	0	0/1
0	1	1	0	0	0	1	1	1	0/1
R	0	0	1	0	0	0	0	0	0/1
R	R	0	1	0	0	0	0	1	0/1
R	F	0	1	0	0	0	1	0	0/1
R	1	0	1	0	0	0	1	1	0/1
F	0	0	0	1	0	0	0	0	0/1
F	R	0	0	1	0	0	0	1	0/1
F	F	0	0	1	0	0	1	0	0/1
F	1	0	0	1	0	0	1	1	0/1
1	0	0	0	0	1	1	0	0	0/1
1	R	0	0	0	1	1	0	1	0/1
1	F	0	0	0	1	1	1	0	0/1
1	1	0	0	0	1	1	1	1	0/1

6.5.4 TUSB5461-Q1 I²C Target Behavior

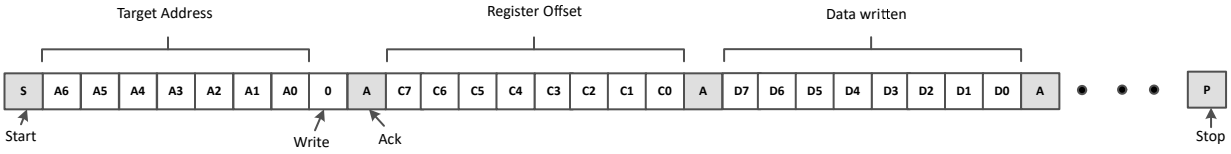


Figure 6-2. I2C Write With Data

Use the following procedure to write data to TUSB5461-Q1 I²C registers (refer to Figure 6-2):

1. The controller initiates a write operation by generating a start condition (S), followed by the TUSB5461-Q1 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB5461-Q1 acknowledges the address cycle.
3. The controller presents the register offset within TUSB5461-Q1 to be written, consisting of one byte of data, MSB-first.
4. The TUSB5461-Q1 acknowledges the sub-address cycle.
5. The controller presents the first byte of data to be written to the I²C register.
6. The TUSB5461-Q1 acknowledges the byte transfer
7. The controller can continue to present additional bytes of data to be written, where each byte transfer is complete after an acknowledge from the TUSB5461-Q1.
8. The controller terminates the write operation by generating a stop condition (P).

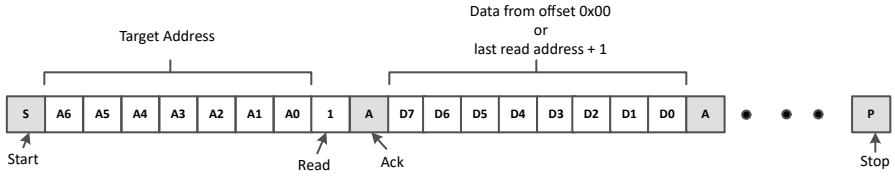


Figure 6-3. I2C Read Without Repeated Start

Use the following procedure to read the TUSB5461-Q1 I²C registers without a repeated Start (refer Figure 6-3).

1. The controller initiates a read operation by generating a start condition (S), followed by the TUSB5461-Q1 7-bit address and a zero-value “W/R” bit to indicate a read cycle.
2. The TUSB5461-Q1 acknowledges the 7-bit address cycle.
3. Following the acknowledge the controller continues sending clock.
4. The TUSB5461-Q1 transmit the contents of the memory registers MSB-first starting at register 00h or last read register offset+1. If a write to the I²C register occurred prior to the read, then the TUSB5461-Q1 shall start at the register offset specified in the write.
5. The TUSB5461-Q1 waits for either an acknowledge (ACK) or a not-acknowledge (NACK) from the controller after each byte transfer; the I²C controller acknowledges reception of each data byte transfer.
6. If an ACK is received, the TUSB5461-Q1 transmits the next byte of data as long as the controller provides the clock. If a NAK is received, the TUSB5461-Q1 stops providing data and waits for a stop condition (P).
7. The controller terminates the write operation by generating a stop condition (P).

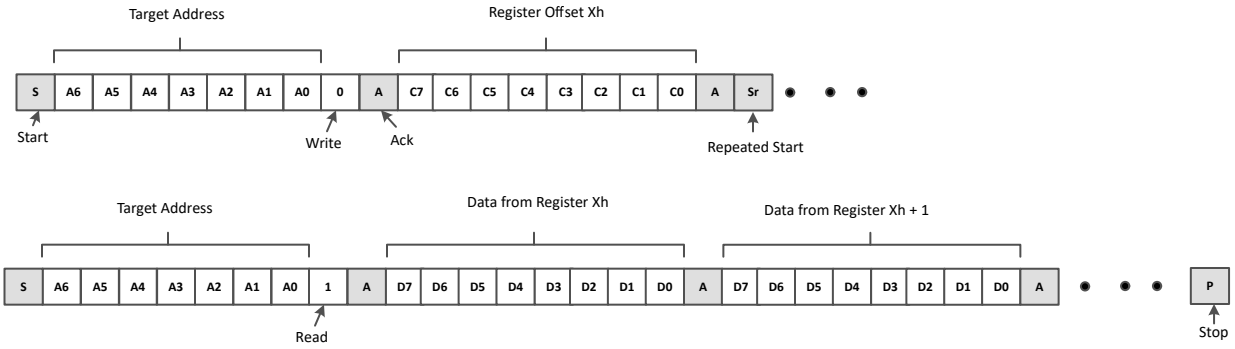


Figure 6-4. I2C Read With Repeated Start

Use the following procedure to read the TUSB5461-Q1 I^{2}C registers with a repeated Start (refer Figure 6-4).

1. The controller initiates a read operation by generating a start condition (S), followed by the TUSB5461-Q1 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB5461-Q1 acknowledges the 7-bit address cycle.
3. The controller presents the register offset within TUSB5461-Q1 to be written, consisting of one byte of data, MSB-first.
4. The TUSB5461-Q1 acknowledges the register offset cycle.
5. The controller presents a repeated start condition (Sr).
6. The controller initiates a read operation by generating a start condition (S), followed by the TUSB5461-Q1 7-bit address and a one-value “W/R” bit to indicate a read cycle.
7. The TUSB5461-Q1 acknowledges the 7-bit address cycle.
8. The TUSB5461-Q1 transmit the contents of the memory registers MSB-first starting at the register offset.
9. The TUSB5461-Q1 shall wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the controller after each byte transfer; the I^{2}C controller acknowledges reception of each data byte transfer.
10. If an ACK is received, the TUSB5461-Q1 transmits the next byte of data as long as the controller provides the clock. If a NAK is received, the TUSB5461-Q1 stops providing data and waits for a stop condition (P).
11. The controller terminates the read operation by generating a stop condition (P).

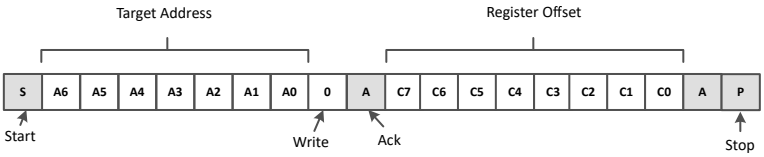


Figure 6-5. I2C Write Without Data

Use the following procedure to set a starting sub-address for I^{2}C reads (refer to Figure 6-5).

1. The controller initiates a write operation by generating a start condition (S), followed by the TUSB5461-Q1 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB5461-Q1 acknowledges the address cycle.
3. The controller presents the register offset within TUSB5461-Q1 to be written, consisting of one byte of data, MSB-first.
4. The TUSB5461-Q1 acknowledges the register offset cycle.
5. The controller terminates the write operation by generating a stop condition (P).

Note

After initial power-up, if no register offset is included for the read procedure (refer to Figure 6-3), then reads start at register offset 00h and continue byte by byte through the registers until the I^{2}C controller terminates the read operation. During a read operation, the TUSB5461-Q1 auto-increments the I^{2}C internal register address of the last byte transferred independent of whether or not an ACK was received from the I^{2}C controller.

7 Register Maps

7.1 TUSB5461-Q1 Registers

Table 7-1 lists the TUSB5461-Q1 registers. All register offset addresses not listed in Table 7-1 should be considered as reserved locations and the register contents should not be modified.

Table 7-1. TUSB5461-Q1 Registers

Offset	Acronym	Register Name	Section
0xA	General_1	General Register	Go
0xB	TXEQ_CTRL	TX EQ Control	Go
0x10	DP01EQ_SEL	DisplayPort Lane 0 and 1 EQ Control	Go
0x11	DP23EQ_SEL	DisplayPort Lane 2 and 3 EQ Control	Go
0x12	DisplayPort_1	AUX Snoop Status	Go
0x13	DisplayPort_2	DP Lane Enable/Disable Control	Go
0x1C	AEQ_CONTROL1	AEQ Controls	Go
0x1D	AEQ_CONTROL2	AEQ Controls	Go
0x1E	AEQ_LONG	AEQ setting for Long channel	Go
0x20	USBC_EQ	EQ control for RX1 and RX2 receivers	Go
0x21	SS_EQ	EQ Control for SSTX receiver	Go
0x22	USB3_MISC	Misc USB3 Controls	Go
0x24	USB_STATUS	USB state machine status	Go
0x32	VOD_CTRL	VOD Linearity and AEQ Controls	Go
0x3B	AEQ_STATUS	Full and Fast AEQ status	Go

Complex bit access types are encoded to fit into small table cells. Table 7-2 shows the codes that are used for access types in this section.

Table 7-2. TUSB5461-Q1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
WS	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.1.1 General_1 Register (Offset = 0xA) [reset = 0x1]

General_1 is shown in Table 7-3.

Return to the Summary Table.

This register is used to select between USB and DisplayPort modes as well as selecting the orientation of the MUX. Software can set the EQ_OVERRIDE ti use the EQ registers instead of pins.

Table 7-3. General_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SSRX_LIMIT_ENABLE	R/W	0x0	Limited redriver mode enable for SSRX transmitter. 0x0 = Linear Redriver 0x1 = Limited Redriver
6	RESERVED	R	0x0	Reserved
5	SWAP_HPDIN	R/W	0x0	Controls which pin HPDIN is derived from. 0x0 = HPDIN is in default location 0x1 = HPDIN location is swapped (PIN 15 to PIN 24, or PIN 24 to PIN 15).
4	EQ_OVERRIDE	R/W	0x0	This field allows software to use EQ settings from registers instead of value sampled from pins. 0x0 = EQ settings based on sampled state of EQ pins. 0x1 = EQ settings based on programmed value of each of the EQ registers.
3	HPDIN_OVERRIDE	R/W	0x0	Overrides HPDIN pin state. 0x0 = HPD_IN based on HPD_IN pin. 0x1 = HPD_IN high.
2	FLIP_SEL	R/W	0x0	This field controls the orientation. 0x0 = Normal Orientation 0x1 = Flip orientation.
1-0	CTLSEL	R/W	0x1	Controls the DP and USB modes. 0x0 = Disabled. All RX and TX for USB3 and DisplayPort are disabled. 0x1 = USB3 only enabled. 0x2 = Four Lanes of DisplayPort enabled. 0x3 = USB3 and Two DisplayPort Lanes.

7.1.2 TXEQ_CTRL Register (Offset = 0xB) [reset = 0x6C]

TXEQ_CTRL is shown in Table 7-4.

Return to the Summary Table.

This register controls the pre-shoot and de-emphasis levels for SSRX when limited redriver mode is enabled.

Table 7-4. TXEQ_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	TX_PRESHOOT	R/W	0x1	SSRX TX pre-shoot level (pre-cursor). 0x0 = 1.5dB 0x1 = 2dB 0x2 = 2.3dB 0x3 = 2.8dB

Table 7-4. TXEQ_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TX_PRESHOOT_EN	R/W	0x1	SSRX TX pre-shoot (pre-cursor) enabled. Valid only when SSRX_LIMIT_ENABLE = 1. 0x0 = Disabled (0dB) 0x1 = Enabled
4-3	TX_DEEPHASIS	R/W	0x1	SSRX TX de-emphasis level (post-cursor) 0x0 = -1.5dB 0x1 = -2.1dB 0x2 = -3.2dB 0x3 = -3.8dB
2	TX_DEEPHASIS_EN	R/W	0x1	SSRX TX de-emphasis (post-cursor) enable. Valid only when SSRX_LIMIT_ENABLE = 1. 0x0 = Disabled (0dB) 0x1 = Enabled
1-0	RESERVED	R	0x0	Reserved

7.1.3 DP01EQ_SEL Register (Offset = 0x10) [reset = 0x0]

DP01EQ_SEL is shown in Table 7-5.

Return to the Summary Table.

This register controls the receiver equalization setting for the DisplayPort receivers 0 and 1.

Table 7-5. DP01EQ_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DP1EQ_SEL	RH/W	0x0	Field selects EQ for DP lane 1 pins. When EQ_OVERRIDE = 0b, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1b, software can change the EQ setting for DP Lane 1 based on value written to this field.
3-0	DP0EQ_SEL	RH/W	0x0	Field selects EQ for DP lane 0 pins. When EQ_OVERRIDE = 0b, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1b, software can change the EQ setting for DP Lane 0 based on value written to this field.

7.1.4 DP23EQ_SEL Register (Offset = 0x11) [reset = 0x0]

DP23EQ_SEL is shown in Table 7-6.

Return to the Summary Table.

This register controls the receiver equalization setting for the DisplayPort receivers 2 and 3.

Table 7-6. DP23EQ_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DP3EQ_SEL	RH/W	0x0	Field selects EQ for DP lane 3 pins. When EQ_OVERRIDE = 0b, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1b, software can change the EQ setting for DP Lane 3 based on value written to this field.

Table 7-6. DP23EQ_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	DP2EQ_SEL	RH/W	0x0	Field selects EQ for DP lane 2 pins. When EQ_OVERRIDE = 0b, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1b, software can change the EQ setting for DP Lane 2 based on value written to this field.

7.1.5 DisplayPort_1 Register (Offset = 0x12) [reset = 0x0]

DisplayPort_1 is shown in Table 7-7.

Return to the Summary Table.

This register provides status of AUX snooping when AUX Snooping is enabled.

Table 7-7. DisplayPort_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6-5	SET_POWER_STATE	RH	0x0	This field represents the snooped value of the AUX write to DPCD address 0x00600. When AUX_SNOOP_DISABLE = 0b, the enable/disable of DP lanes based on the snooped value. When AUX_SNOOP_DISABLE = 1b, then DP lane enable/disable are determined by state of DPx_DISABLE registers, where x = 0, 1, 2, or 3. This field is reset to 0h by hardware when CTLSEL1 changes from a 1b to a 0b.
4-0	LANE_COUNT_SET	RH	0x0	This field represents the snooped value of AUX write to DPCD address 0x00101 register. When AUX_SNOOP_DISABLE = 0b, DP lanes enabled specified by the snoop value. Unused DP lanes are disabled to save power. When AUX_SNOOP_DISABLE = 1b, then DP lanes enable/disable are determined by DPx_DISABLE registers, where x = 0, 1, 2, or 3. This field is reset to 0h by hardware when CTLSEL1 changes from a 1b to a 0b.

7.1.6 DisplayPort_2 Register (Offset = 0x13) [reset = 0x0]

DisplayPort_2 is shown in Table 7-8.

Return to the Summary Table.

This register provides controls for enabling and disabling AUX snooping and individual DP lanes.

Table 7-8. DisplayPort_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	AUX_SNOOP_DISABLE	R/W	0x0	Controls whether DP lanes are enabled based on AUX snooped value or registers. 0x0 = AUX snoop enabled. 0x1 = AUX snoop disabled. DP lanes are controlled by registers.
6	RESERVED	R	0x0	Reserved

Table 7-8. DisplayPort_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	AUX_SBU_OVR	R/W	0x0	This field overrides the AUXP/N to SBU1/2 connect and disconnect based on CTL1 and FLIP. Changing this field to 01b or 10b allows traffic to pass through AUX to SBU regardless of the state of CTLSEL1 and FLIPSEL register. 0x0 = AUX to SBU connection determined by CTLSEL1 and FLIPSEL 0x1 = AUXP -> SBU1 and AUXN -> SBU2 0x2 = AUXP -> SBU2 and AUXN -> SBU1 0x3 = AUX to SBU open.
3	DP3_DISABLE	R/W	0x0	When AUX_SNOOP_DISABLE = 1b, this field can be used to enable or disable DP lane 3. When AUX_SNOOP_DISABLE = 0b, changes to this field has no effect on lane 3 functionality. 0x0 = DP Lane 3 enabled. 0x1 = DP Lane 3 disabled.
2	DP2_DISABLE	R/W	0x0	When AUX_SNOOP_DISABLE = 1b, this field can be used to enable or disable DP lane 2. When AUX_SNOOP_DISABLE = 0b, changes to this field has no effect on lane 2 functionality. 0x0 = DP Lane 2 enabled. 0x1 = DP Lane 2 disabled.
1	DP1_DISABLE	R/W	0x0	When AUX_SNOOP_DISABLE = 1b, this field can be used to enable or disable DP lane 1. When AUX_SNOOP_DISABLE = 0b, changes to this field has no effect on lane 1 functionality. 0x0 = DP Lane 1 enabled. 0x1 = DP Lane 1 disabled.
0	DP0_DISABLE	R/W	0x0	When AUX_SNOOP_DISABLE = 1b, this field can be used to enable or disable DP lane 0. When AUX_SNOOP_DISABLE = 0b, changes to this field has no effect on lane 0 functionality. 0x0 = DP Lane 0 enabled. 0x1 = DP Lane 0 disabled.

7.1.7 AEQ_CONTROL1 Register (Offset = 0x1C) [reset = 0x80]

AEQ_CONTROL1 is shown in Table 7-9.

Return to the Summary Table.

This register is used to enable adaptive EQ and select between Fast and Full adaptive EQ.

Table 7-9. AEQ_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FULLAEQ_UPPER_EQ	R/W	0x8	Maximum EQ value to check for full AEQ mode

Table 7-9. AEQ_CONTROL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	USB3_U1_DISABLE	R/W	0x0	This field when set causes entry to U3 instead of U1 when electrical idle is detected. 0x0 = U1 entry after electrical idle. 0x1 = U3 entry after electrical idle.
2-1	AEQ_MODE	R/W	0x0	Selects between Fast and 2 Full Adaption modes 0x0 = Fast AEQ. 0x1 = Full AEQ with hits counted at mideye for every EQ. 0x2 = Fast AEQ. 0x3 = Full AEQ with hits counted at mideye only for EQ equal 0.
0	AEQ_EN	R/W	0x0	Controls whether or not adaptive EQ for USB downstream facing port is enabled. 0x0 = AEQ disabled 0x1 = AEQ enabled

7.1.8 AEQ_CONTROL2 Register (Offset = 0x1D) [reset = 0x10]

AEQ_CONTROL2 is shown in Table 7-10.

Return to the Summary Table.

This register allows for controls for the Fast AEQ limits as well as adding or reducing final EQ value used by the Full AEQ function.

Table 7-10. AEQ_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OVER_EQ_SIGN	R/W	0x0	Selects the sign for OVER_EQ_CTRL field. 0x0 = positive 0x1 = negative
6	RESERVED	R	0x0	Reserved
5-3	FASTAEQ_LIMITS	R/W	0x2	Selects the upper/lower limits of DAC for determining short vs long channel. 0x0 = +/- 0mV 0x1 = +/- 40mV 0x2 = +/- 80mV 0x3 = +/- 120mV 0x4 = +/- 160mV 0x5 = +/- 200mV 0x6 = +/- 240mV 0x7 = +/- 280mV

Table 7-10. AEQ_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	OVER_EQ_CTRL	R/W	0x0	This field increases or decreases the AEQ by value programmed into this field. For example, full AEQ value is 6 and this field is programmed to 2 and OVER_EQ_SIGN = 0, then EQ value used is 8. This field is only used in Full AEQ mode. 0x0 = 0 or -8 0x1 = 1 or -7 0x2 = 2 or -6 0x3 = 3 or -5 0x4 = 4 or -4 0x5 = 5 or -3 0x6 = 6 or -2 0x7 = 7 or -1

7.1.9 AEQ_LONG Register (Offset = 0x1E) [reset = 0x77]

AEQ_LONG is shown in Table 7-11.

Return to the Summary Table.

This register is used to program the EQ used for long channel setting when Fast AEQ is enabled.

Table 7-11. AEQ_LONG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LONG_EQ2	R/W	0x7	When AEQ_EN = 1 and AEQ_MODE = x0, selects EQ setting for USB downstream facing port1 (RX2) when long channel is detected. Value programmed into this field can provide best Rx JTOL results for long channel configuration.
3-0	LONG_EQ1	R/W	0x7	When AEQ_EN = 1 and AEQ_MODE = x0, selects EQ setting for USB downstream facing port2 (RX1) when long channel is detected. Value programmed into this field can provide best Rx JTOL results for long channel configuration.

7.1.10 USBC_EQ Register (Offset = 0x20) [reset = 0x0]

USBC_EQ is shown in Table 7-12.

Return to the Summary Table.

This register controls the receiver equalization setting for the DFP (RX1 and RX2).

Table 7-12. USBC_EQ Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	EQ2_SEL	RH/W	0x0	If AEQ_EN = 0, this field selects EQ for USB3.1 RX2 receiver which faces the USB-C receptacle. When EQ_OVERRIDE = 0b, this field reflects the sampled state of EQ[1:0] pins. When EQ_OVERRIDE = 1b, software can change the EQ setting for RX2p/n pins based on value written to this field. When AEQ_EN = 1 and AEQ_MODE = x0, selects EQ setting for USB downstream facing port1 (RX2) when short channel is detected. Value programmed into this field can provide best Rx JTOL results for short channel configuration.
3-0	EQ1_SEL	RH/W	0x0	If AEQ_EN = 0, this field selects EQ for USB3.1 RX1 receiver which faces the USB-C receptacle. When EQ_OVERRIDE = 0b, this field reflects the sampled state of EQ[1:0] pins. When EQ_OVERRIDE = 1b, software can change the EQ setting for RX1p/n pins based on value written to this field. When AEQ_EN = 1 and AEQ_MODE = x0, selects EQ setting for USB downstream facing port1 (RX1) when short channel is detected. Value programmed into this field can provide best Rx JTOL results for short channel configuration.

7.1.11 SS_EQ Register (Offset = 0x21) [reset = 0x0]

SS_EQ is shown in Table 7-13.

Return to the Summary Table.

This register controls the receiver equalization setting for the UFP (SSTX).

Table 7-13. SS_EQ Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3-0	SSEQ_SEL	RH/W	0x0	This field selects EQ for USB3.1 SSTX receiver which faces the USB host. When EQ_OVERRIDE = 0b, this field reflects the sampled state of SSEQ[1:0] pins. When EQ_OVERRIDE = 1b, software can change the EQ setting for SSTXp/n pins based on value written to this field.

7.1.12 USB3_MISC Register (Offset = 0x22) [reset = 0x44]

USB3_MISC is shown in Table 7-14.

Return to the Summary Table.

Table 7-14. USB3_MISC Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RXD_START_TERM	R/W	0x0	Termination setting at start of RX detection following warm reset and at entry to SS.Inactive. 0x0 = Maintain termination. Same as tusb1046 0x1 = Turn off termination. Avoid compliance failures due to race between local and remote rxd in case of disconnect. If connection remains next state was polling regardless.

Table 7-14. USB3_MISC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	LFPS_EQ	R/W	0x1	Controls whether settings of EQ based on EQ1_SEL, EQ2_SEL, and SSEQ_SEL applies to received LFPS signal. 0x0 = EQ set to zero when receiving LFPS 0x1 = EQ set by the related registers when receiving LFPS.
5	U2U3_LFPS_DEBOUNCE	R/W	0x0	Controls whether or not incoming LFPS is debounced or not. 0x0 = No debounce of LFPS before U2/U3 exit. 0x1 = 200us debounce of LFPS before U2/U3 exit.
4	DISABLE_U2U3_RXDET	R/W	0x0	Controls whether or not Rx.Detect is performed in U2/U3 state. 0x0 = Rx.Detect in U2/U3 enabled. 0x1 = Rx.Detect in U2/U3 disabled.
3-2	DFP_RXDET_INTERVAL	R/W	0x1	This field controls the Rx.Detect interval for the downstream facing port (TX1P/N and TX2P/N). 0x0 = Reserved 0x1 = 6ms 0x2 = 36ms 0x3 = 84ms
1	DIS_WARM_RESET_RXD	R/W	0x0	Disables receiver detection following warm reset if device starts polling during warm reset. 0x0 = whether receiver detection is done following warm reset depends on other settings. 0x1 = if USB FSM detects that device started polling during warm reset, receiver detection is not performed.
0	USB_COMPLIANCE_CTRL	R/W	0x0	Controls whether compliance mode detection is determined by FSM or disabled 0x0 = Compliance mode determined by FSM. 0x1 = Compliance mode disabled.

7.1.13 USB_STATUS Register (Offset = 0x24) [reset = 0x41]

USB_STATUS is shown in Table 7-15.

Return to the Summary Table.

Table 7-15. USB_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	USB_FASTAEQ_STAT	RH	0x0	When AEQ_EN = 1 and AEQ_MODE = x0, this status field indicates whether short or long EQ setting is used. When AEQ_EN = 0, this field defaults to 0h. 0x0 = Short channel EQ used. 0x1 = Long channel EQ used.

Table 7-15. USB_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	USB_AEQDONE_STAT	RH	0x1	This field is low while AEQ is active and high when AEQ is done. The bit is valid when U0_STAT and AEQ_EN = 1 or when FORCE_AEQ_EN = 1 and HW has reset FORCE_AEQ back to 0. 0x0 = AEQ is running 0x1 = AEQ is done
5	AEQ_HC_OVERFLOW	RH	0x0	13-bit AEQ hit counter overflow status
4	RESERVED	R	0x0	Reserved
3	CM_ACTIVE	RH	0x0	Compliance mode status. 0x0 = Not in USB3 compliance mode. 0x1 = In USB3 compliance mode.
2	U0_STAT	RH	0x0	U0 Status. Set if the device enters U0 state.
1	U2U3_STAT	RH	0x0	U2/U3 Status. Set if the device enters U2/U3 state.
0	DISC_STAT	RH	0x1	Disconnect Status. Set if the device enters Disconnect state.

7.1.14 VOD_CTRL Register (Offset = 0x32) [reset = 0x40]

VOD_CTRL is shown in Table 7-16.

Return to the Summary Table.

This register controls the transmitters output linearity range for both UFP and DFP. When device is configured for limited redriver (SSRX_LIMIT_ENABLE field is set), USB_SSRX_VOD controls the VOD level for SSRX limited driver.

Table 7-16. VOD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	LFPS_TX12_VOD	R/W	0x1	VOD linearity control for TX1 or TX2 when LFPS is being transmitted. 0x0 = LINR_L3 (highest) 0x1 = LINR_L2 0x2 = LINR_L1 0x3 = LINR_L0 (lowest)
5-4	DP_VOD	R/W	0x0	VOD linearity control for DP paths. 0x0 = LINR_L3 (highest) 0x1 = LINR_L2 0x2 = LINR_L1 0x3 = LINR_L0 (lowest)

Table 7-16. VOD_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	USB_TX12_VOD	R/W	0x0	VOD linearity control for USB downstream facing ports (TX1 and TX2). 0x0 = LINR_L3 (highest) 0x1 = LINR_L2 0x2 = LINR_L1 0x3 = LINR_L0 (lowest)
1-0	USB_SSRX_VOD	R/W	0x0	VOD linearity control for USB upstream facing port (SSRX). When SSRX_LIMIT_ENABLE = 1, then this field controls the limited VOD for SSRX. 0x0 = LINR_L3 (highest) 0x1 = LINR_L2 0x2 = LINR_L1 0x3 = LINR_L0 (lowest)

7.1.15 AEQ_STATUS Register (Offset = 0x3B) [reset = 0x0]

AEQ_STATUS is shown in Table 7-17.

Return to the Summary Table.

This register provides the status of AEQ function.

Table 7-17. AEQ_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4	DONE_STAT	RH	0x0	This flag is set after DAC wait timer expires.
3-0	AEQ_STAT	RH	0x0	Optimal EQ determined by FSM after the completion of Full AEQ. This field also indicates the EQ used for Fast AEQ. This field also includes the value programmed into OVER_EQ_CTRL field.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TUSB5461-Q1 is a linear redriver designed specifically to compensation for intersymbol interference (ISI) jitter caused by signal attenuation through a passive medium like PCB traces and cables. The TUSB5461-Q1 has four independent DisplayPort 2.1 inputs, one upstream facing USB 3.2 input, and two downstream facing USB 3.2 inputs, therefore the device can be optimized to correct ISI on all those seven inputs through 16 different equalization choices. Placing the TUSB5461-Q1 between a USB3.2 Host/DisplayPort 2.1 GPU and a USB3.2 Type-C receptacle can correct signal integrity issues resulting in a more robust system.

8.2 Typical Application

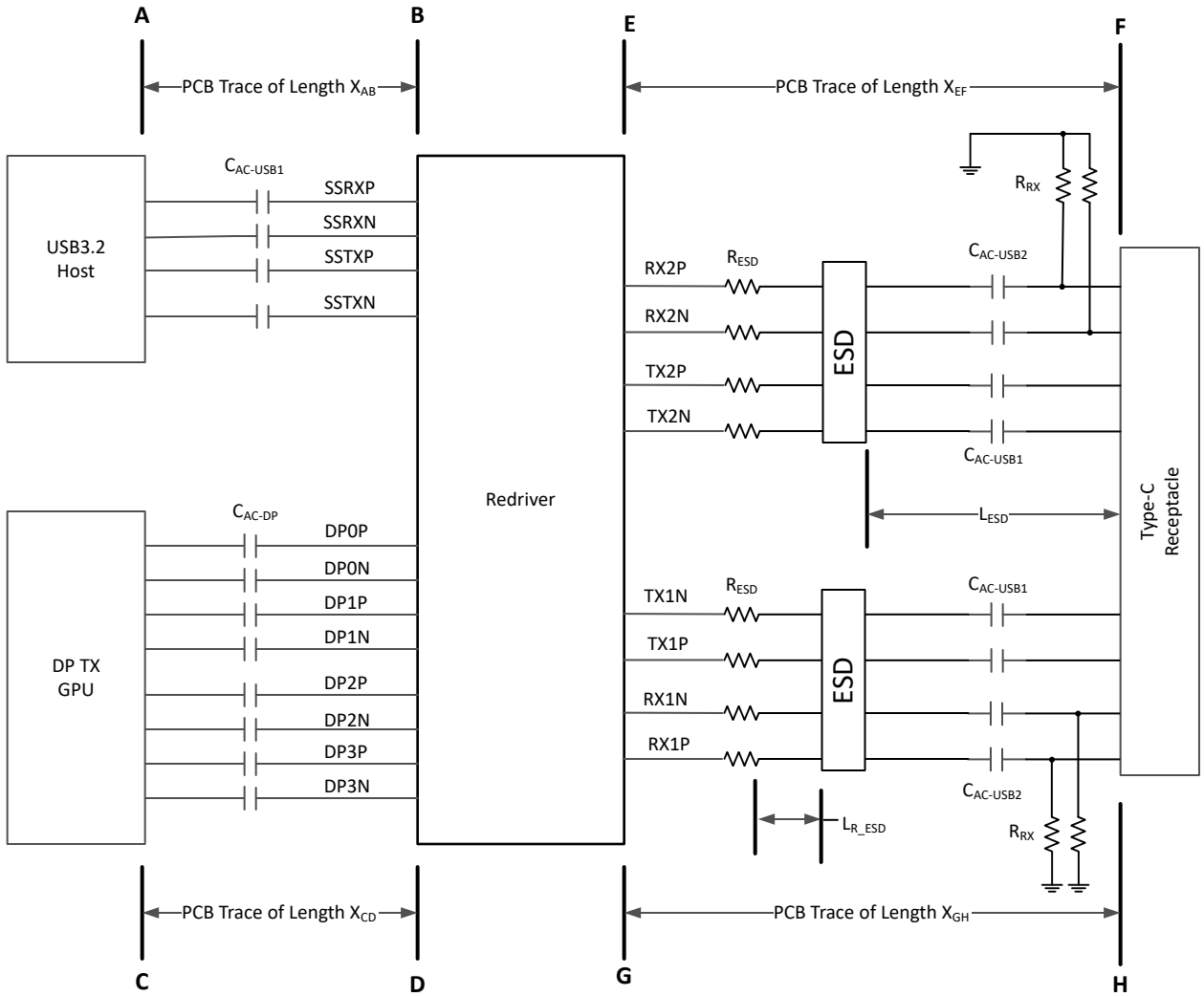


Figure 8-1. TUSB5461-Q1 in a Host Application

8.2.1 Design Requirements

For this design example, use the parameters shown in Table 8-1.

Table 8-1. Design Parameters

PARAMETER	VALUE
USB3 pre-channel A to B PCB trace length, X_{AB}. Refer to Figure 8-1.	2 inches ≤ X_{AB} ≤ 12 inches – [MAX (X_{EF} or X_{GH})]
DP pre-channel C to D PCB trace length, X_{CD}. Refer to Figure 8-1.	2 inches ≤ X_{CD} ≤ 12 inches – [MAX (X_{EF} or X_{GH})]
USB and DP post channel E to F PCB trace length, X_{EF}. Refer to Figure 8-1.	up to 4 inches
USB and DP post channel G to H PCB trace length, X_{GH}. Refer to Figure 8-1.	up to 4 inches
Maximum distance of ESD component from the USB-C receptacle, L_{ESD}	0.5 inches
Maximum distance of series resistor (R_{ESD}) from ESD component, L_{R_ESD}.	0.25 inches
$C_{AC-USB1}$ AC-coupling capacitor (75nF to 265nF)	220nF
$C_{AC-USB2}$ AC-coupling capacitor (297nF to 363nF)	Options: • 330nF AC-couple capacitor with R_{RX} resistor • 330nF AC-couple capacitor without R_{RX} resistor
Optional R_{RX} resistor (220kΩ ±5%)	220kΩ
C_{AC-DP} AC-coupling capacitor (75nF to 265nF)	220nF
R_{ESD} (0Ω to 2.2Ω)	1Ω
V_{CC} supply (3V to 3.6V)	3.3V
I^2C Mode or GPIO Mode	I^2C Mode. (I2C_EN pin != "0")
1.8V or 3.3V I^2C Interface	3.3V I^2C. Pull up the I2C_EN pin to 3.3V with a 1KΩ resistor.

8.2.2 Detailed Design Procedure

Figure 8-2 shows a typical usage of the TUSB5461-Q1 device. The device can be controlled either through the GPIO pins or through the I^2C interface. In the example shown below, a Type-C PD controller is used to configure the device through the I^2C interface. When configured for I^2C mode, pins 29 and 32 can be left unconnected. In I^2C mode, the equalization settings for each receiver can be independently controlled through I^2C registers. For this reason, all of the equalization pins (EQ[1:0], SSEQ[1:0], and DPEQ[1:0]) can be left unconnected. If these pins are left unconnected, the TUSB5461-Q1 7-bit I^2C target address is 0x12 because both DPEQ0/A1 and SSEQ0/A0 are at pin level "F". If a different I^2C target address is desired, set the DPEQ0/A1 and SSEQ0/A0 pins to a level which produces the desired I^2C target address.

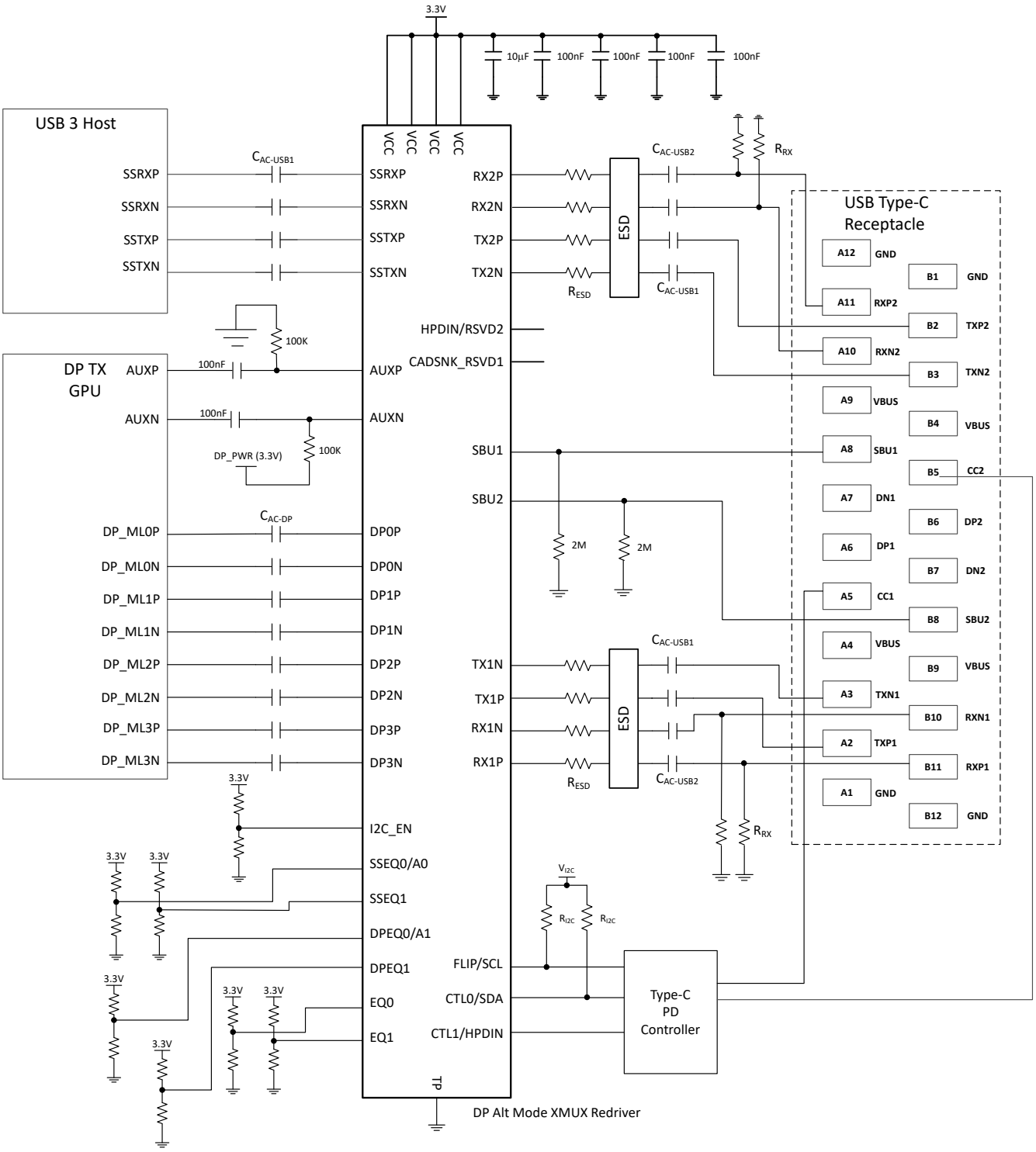


Figure 8-2. Application Circuit

8.2.2.1 USB and DP Upstream Facing Port (USB Host / DP GPU to USB-C Receptacle) Configuration

Configuring the TUSB5461-Q1 for the USB and DP downstream direction involves understanding the insertion loss (SDD21) of the pre-channel (X_{AB} and X_{CD}). Set the DPEQ[1:0] pins and SSEQ[1:0] pins or SSEQ_SEL and DPEQx_SEL registers to the level of the pre-channel insertion loss at 2.5GHz. TI recommends using insertion loss at 2.5GHz of approximately –0.5dB per inch for FR4 trace. Following this recommendation, if the

pre-channel for USB (X_{AB}) is 8 inches, program the SSEQ to –4dB. If the pre-channel insertion loss for DP (X_{CD}) is 10 inches, then program DPEQ to –5dB. Refer to Table 6-8 for USB SSEQ settings and to Table 6-9 for DP EQ settings.

8.2.2.2 USB Downstream Facing Port (USB-C Receptacle to USB Host) Configuration

8.2.2.2.1 Fixed Equalization

In Fixed EQ operation, a single EQ setting is used for all possible devices inserted into the USB-C receptacle (with or without USB cable). TI recommends to set the TUSB5461-Q1 EQ[1:0] pins if GPIO mode, or EQ1_SEL and EQ2_SEL if I^2C mode to approximately 4db to 5dB greater than loss of the post channel (MIN(X_{EF}, X_{GH})). For example, if post channel is 0.5 inches, then assuming –0.5dB per inch at 2.5GHz, program the EQ1_SEL and EQ2_SEL between 4.25dB to 5.25dB. TI recommends performing USB3.1 Rx JTOL long and short channel tests to optimize the setting. Depending on the USB 3.1 Host, a single EQ setting which satisfies both the long and short channel tests may not be possible. If this is the case, then TI recommends to use Fast or Full AEQ mode.

8.2.2.2.2 Fast Adaptive Equalization

Fast Adaptive EQ can distinguish between a short and long channel and select a pre-determined EQ setting based on which channel is detected. Fast AEQ is available in I^2C mode. Fast AEQ is enabled when AEQ_MODE = 0 and AEQ_EN = 1.

Program the short channel EQ settings into the EQ1_SEL and EQ2_SEL registers. TI recommends to program these registers about 1dB to 2dB more than the loss of post channel (MIN(X_{EF}, X_{GH})). For example, if post channel is 0.5 inches, then assuming –0.5dB insertion loss per inch at 2.5GHz, program the EQ1_SEL and EQ2_SEL between 1.25dB to 2.25dB. TI recommends to perform USB3.1 Rx JTOL short channel test to find the optimal short channel setting.

Program the long channel EQ settings into the LONG_EQ1 and LONG_EQ2 registers. TI recommends to program these registers about 4dB to 5dB more than the loss of post channel (MIN(X_{EF}, X_{GH})). For example, if post channel is 0.5 inches, then assuming –0.5dB per inch at 2.5GHz, program the LONG_EQ1 and LONG_EQ2 between 4.25dB to 5.25dB. TI recommends to perform USB3.1 Rx JTOL long channel test to find the optimal long channel setting.

8.2.2.2.3 Full Adaptive Equalization

In Full AEQ mode, the TUSB5461-Q1 always determines the best settings regardless of whether the channel is short, long or somewhere in between. The Full AEQ feature is disabled by default in I^2C mode. Full AEQ is enabled when AEQ_MODE = 1 and AEQ_EN = 0x1 or 0x3.

8.2.2.3 ESD Protection

It may be necessary to incorporate an ESD component to protect the TUSB5461-Q1 from electrostatic discharge (ESD). TI recommends following the ESD protection recommendations listed in Table 8-2. A clamp voltage greater than value specified in Table 8-2 may require a R_{ESD} on each differential pin. Place the ESD component near the USB connector.

Table 8-2. ESD Diodes Recommended Characteristics

Parameter	Recommendation
Breakdown voltage	≥ 3.5V for DP input pins ≥ 1.5V for non-DP input pins
I/O line capacitance	Data rates ≤ 5Gbps: ≤ 0.50pF
	Data rates > 5Gbps: ≤ 0.35pF
Delta capacitance between any P and N I/O pins	≤ 0.07pF
Clamping voltage at 8A I_{PP} IO to GND(1)	≤ 4.5V
Typical dynamic resistance	≤ 30mΩ

(1) According to IEC 61000-4-5 (8/20µs current waveform)

Table 8-3. Recommended ESD Protection Component

Manufacturer	Part Number	R_{ESD} to support IEC 61000-4-2 Contact ±8kV
Nexperia	PUSB3FR4	1Ω
Nexperia	PESD2V8Y1BSF	1Ω
Texas Instruments	TPD1E04U04DPLR	2Ω
Texas Instruments	TPD4E02B04DQAR	2Ω

8.2.3 Application Curve

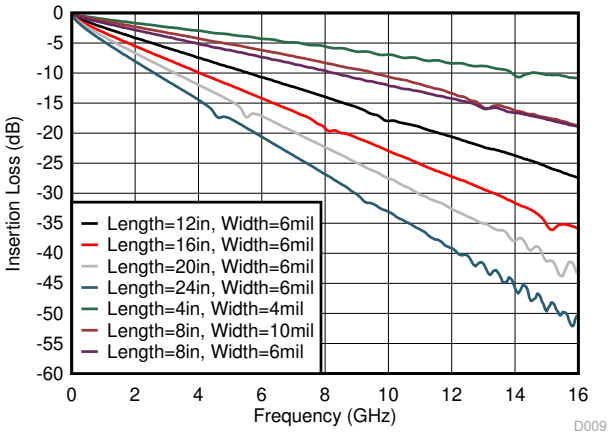


Figure 8-3. Insertion Loss of FR4 PCB Traces

8.3 System Examples

8.3.1 USB 3.1 Only

The TUSB5461-Q1 is in USB3.1 only when the CTL1 pin is low and CTL0 pin is high.

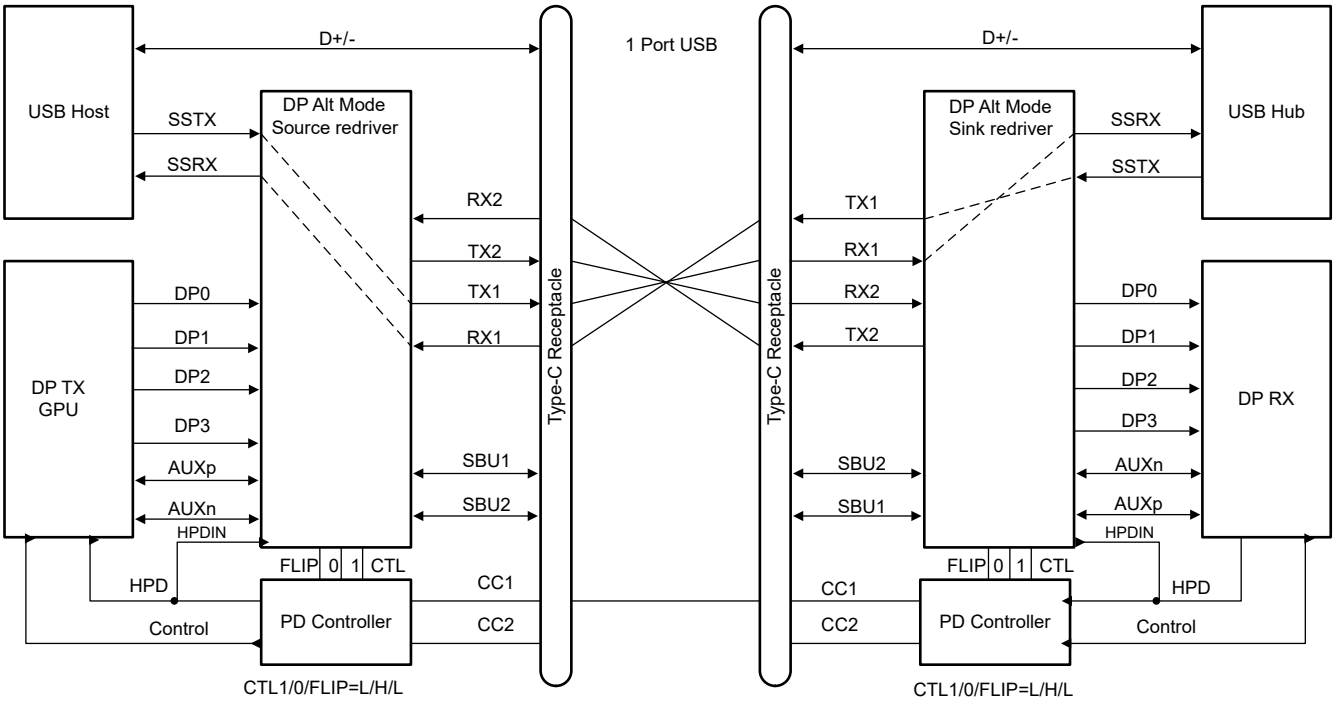


Figure 8-4. USB3.1 Only – No Flip (CTL1 = L, CTL0 = H, FLIP = L)

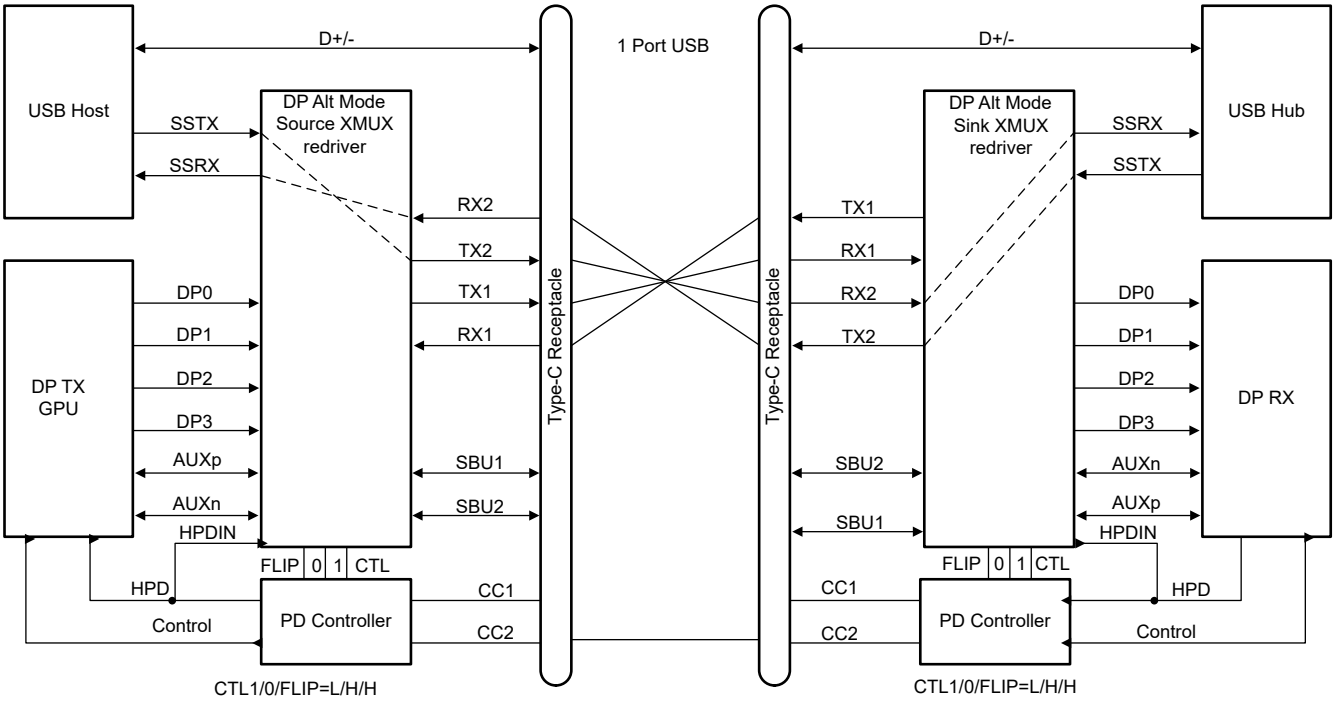


Figure 8-5. USB3.1 Only – With Flip (CTL1 = L, CTL0 = H, FLIP = H)

8.3.2 USB 3.1 and 2-Lane DisplayPort Mode

The TUSB5461-Q1 operates in USB3.1 and in two lanes of DisplayPort mode when the CTL1 pin is high and CTL0 pin is high.

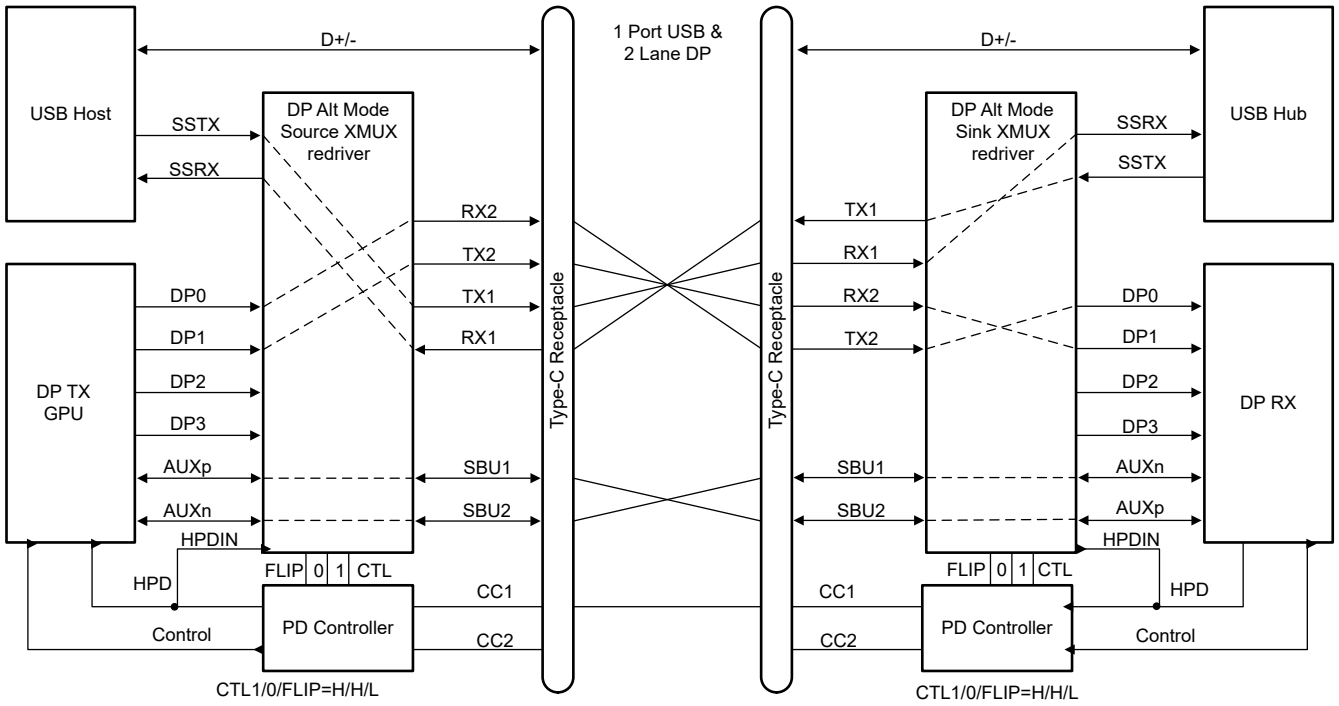


Figure 8-6. USB3.1 + 2-Lane DP – No Flip (CTL1 = H, CTL0 = H, FLIP = L)

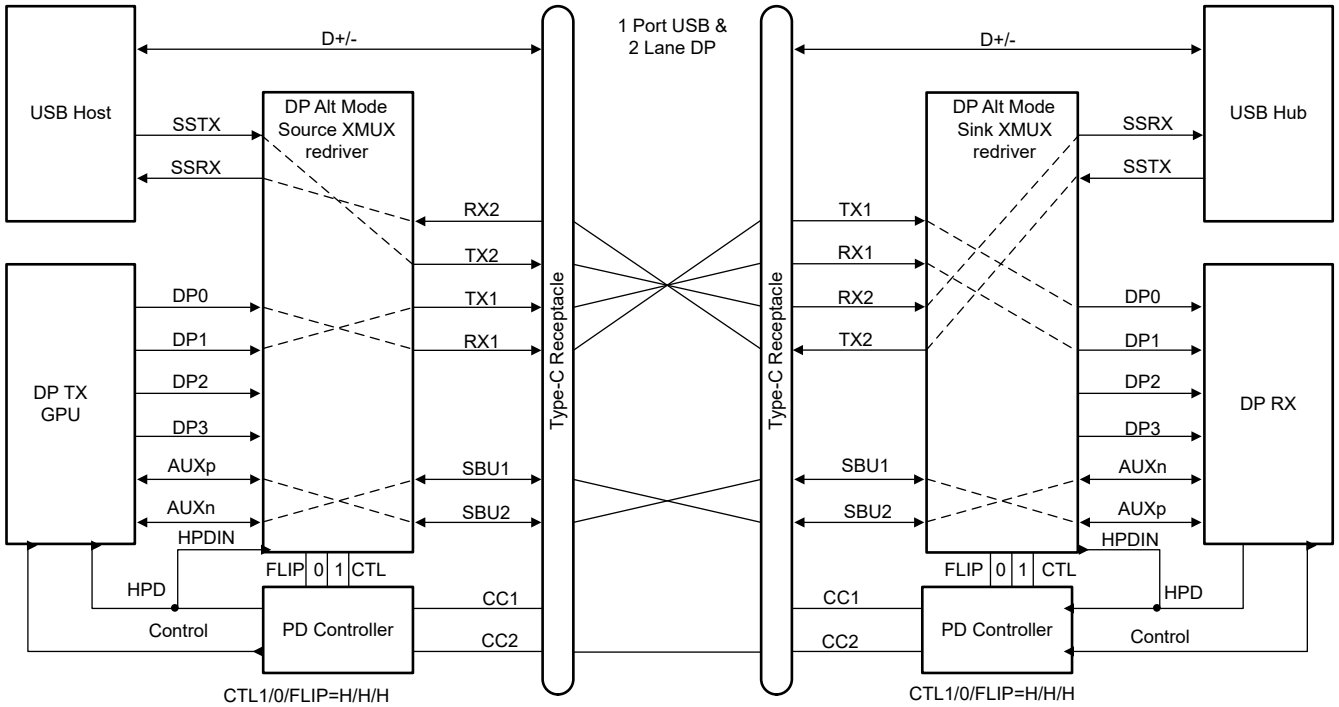


Figure 8-7. USB 3.1 + 2-Lane DP – Flip (CTL1 = H, CTL0 = H, FLIP = H)

8.3.3 DisplayPort Only

The TUSB5461-Q1 operates in four lanes of DisplayPort-only mode when the CTL1 pin is high and CTL0 pin is low.

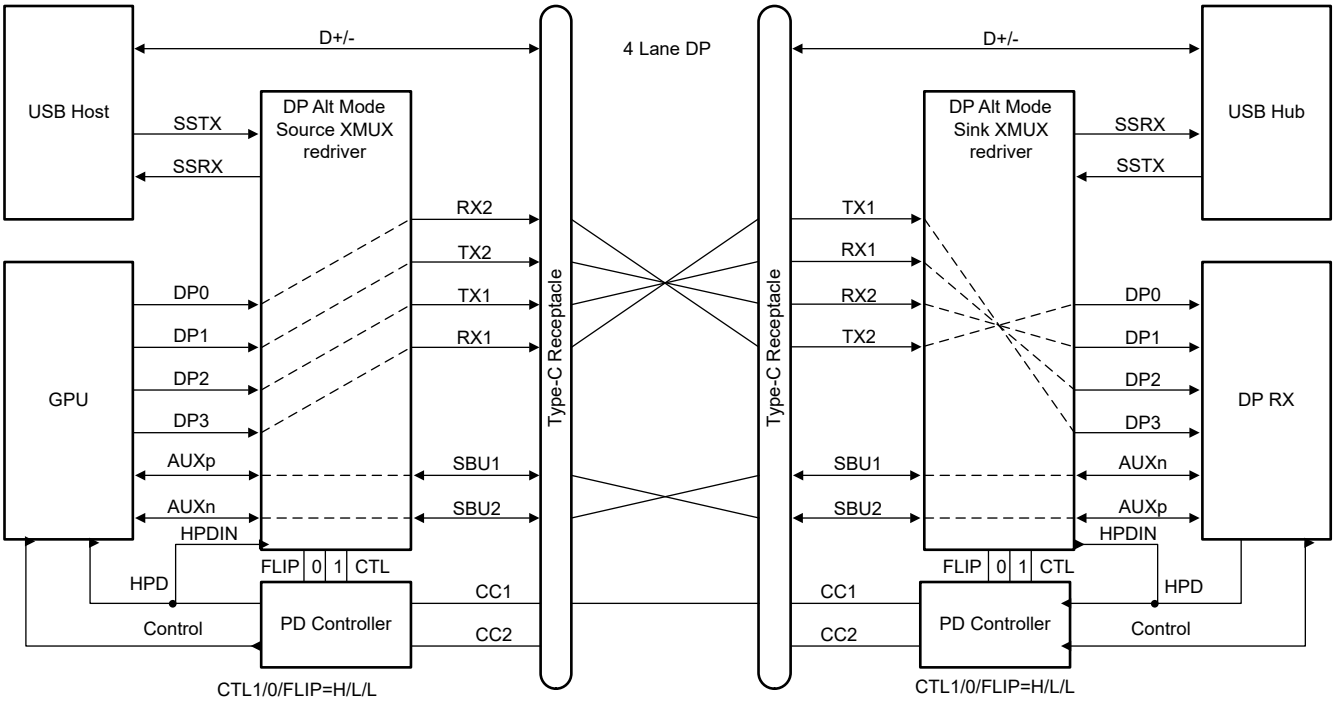


Figure 8-8. 4-Lane DP – No Flip (CTL1 = H, CTL0 = L, FLIP = L)

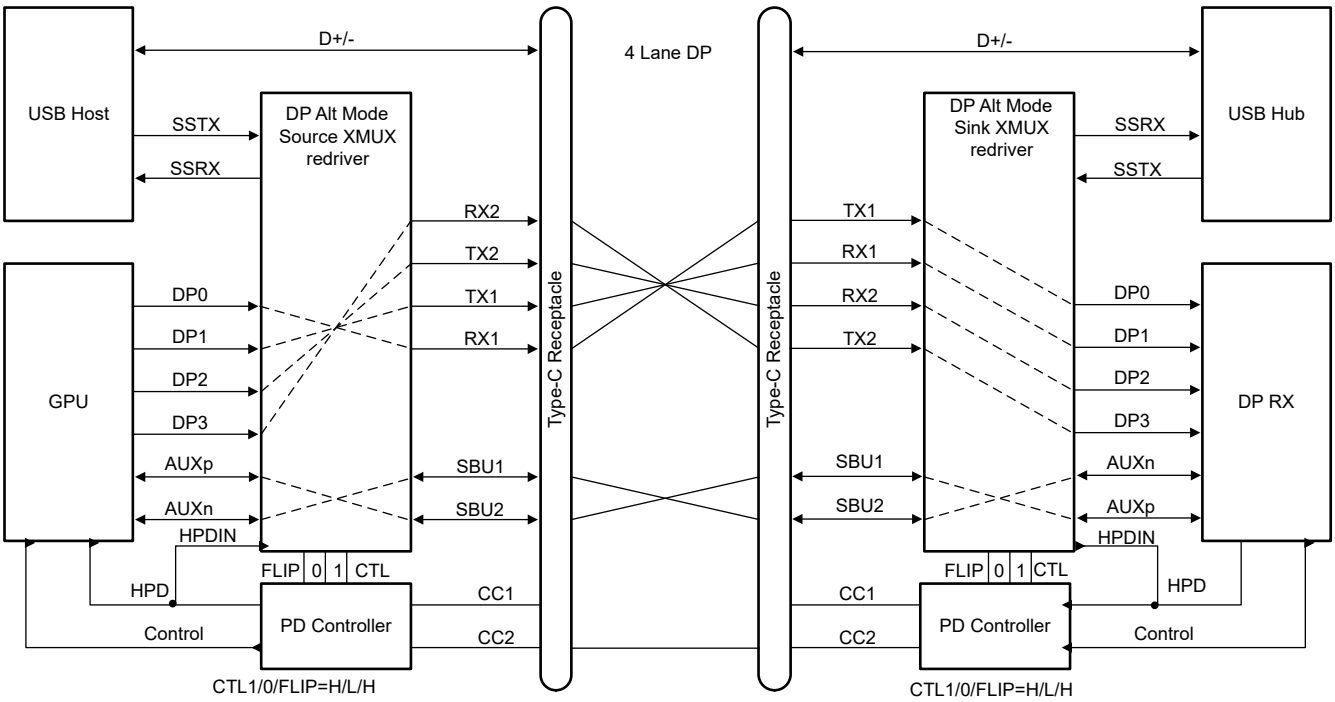


Figure 8-9. 4-Lane DP – With Flip (CTL1 = H, CTL0 = L, FLIP = H)

8.4 Power Supply Recommendations

The TUSB5461-Q1 is designed to operate with a 3.3V power supply. Do not use levels above those listed in the *Absolute Maximum Ratings* table. If using a higher voltage system power supply, a voltage regulator can be used to step down to 3.3V. Use decoupling capacitors to reduce noise and improve power supply integrity. Use a 0.1µF capacitor on each power pin.

8.5 Layout

8.5.1 Layout Guidelines

1. Route SSTXP/N, SSRXP/N, RX1P/N, RX2PN, TX1P/N, and TX2P/N pairs with controlled 90Ω differential impedance (±10%).
2. Route DP[3:0]P/N pairs with controlled 90Ω differential impedance (±10%).
3. There is no inter-pair length match requirement between SSTXP/N and SSRXP/N.
4. Keep the inter-pair matching between DP lanes (DP[3:0]) from GPU through TUSB5461-Q1 to the USB-C receptacle to less than 100 mils.
5. Keep away from other high speed signals.
6. Keep intra-pair routing (between P and N) to less than 5 mils.
7. Make sure length matching is near the location of mismatch.
8. Separate each pair by at least 3 times the signal trace width.
9. Keep the use of bends in differential traces to a minimum. When bends are used, make sure the number of left and right bends are as equal as possible and that the angle of the bend is≥ 135 degrees. This can minimize any length mismatch causes by the bends and therefore minimize the impact bends have on EMI.
10. Route all differential pairs on the same of layer.
11. Keep the number of vias to a minimum. TI recommends to keep the vias count to 2 or less.
12. Keep traces on layers adjacent to ground plane.
13. Do not route differential pairs over any plane split.
14. Remember that adding test points can cause impedance discontinuity, and therefore, negatively impact signal performance. If test points are used, place the test points in series and symmetrically. Do not place test points in a manner that can cause a stub on the differential pair.
15. TI highly recommends to have reference plane void under the SuperSpeed pins of the USB-C receptacle to minimize the capacitance effect of the receptacle.
16. TI highly recommends to have reference plane void under the AC-coupling capacitances.

8.5.2 Layout Example

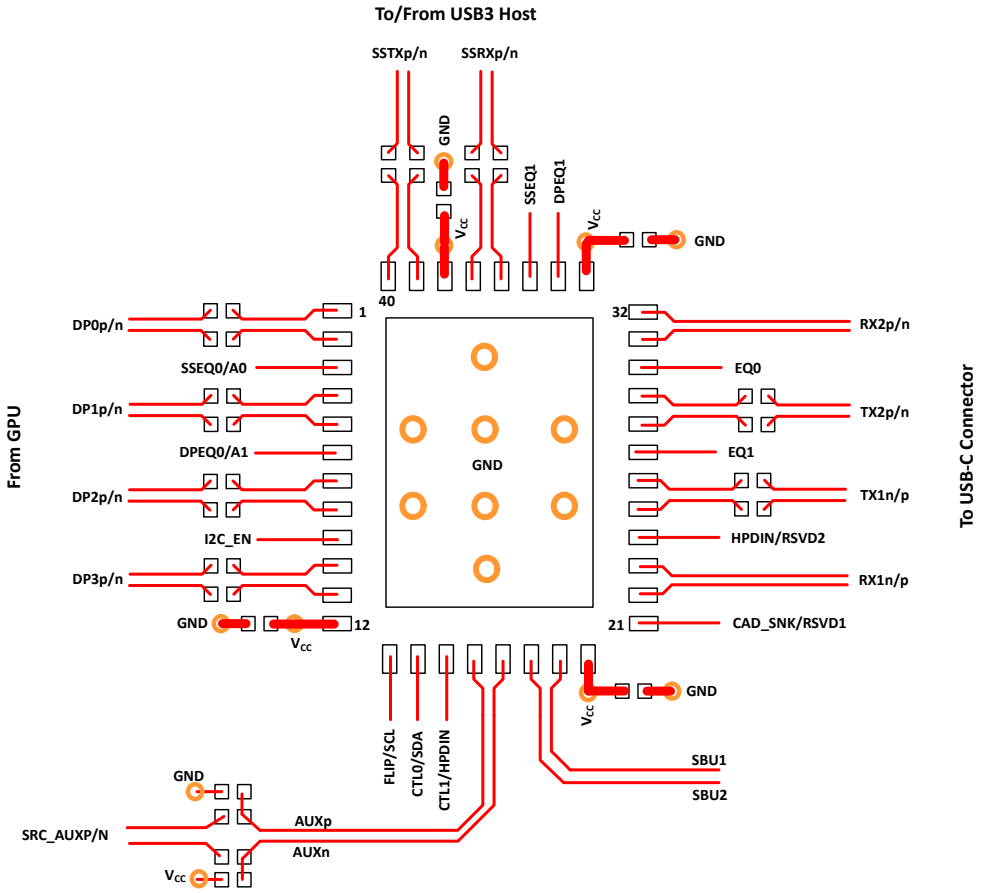


Figure 8-10. Layout Example

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

DisplayPort™ is a trademark of VESA.
TI E2E™ is a trademark of Texas Instruments.
USB Type-C® is a registered trademark of USB Implementers Forum.
VESA® is a registered trademark of Video Electronics Standards Association.
HDMI® is a registered trademark of HDMI Licensing LLC.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from Revision * (November 2024) to Revision A (February 2025)	Page
• Changed data sheet status from: Advanced Information to: Production Data	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TUSB5461RGFRQ1	Active	Production	VQFN (RGF) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	TDB461
TUSB5461RGFTQ1	Active	Production	VQFN (RGF) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	TDB461

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

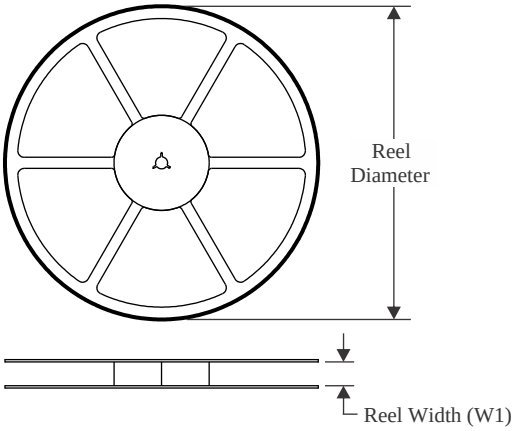
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

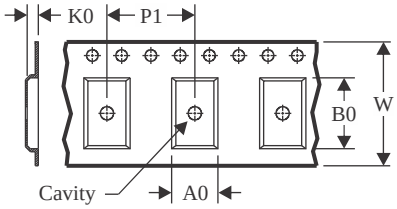
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

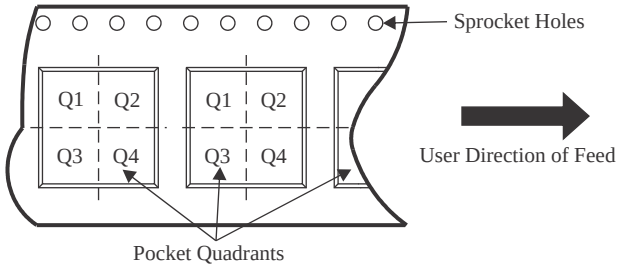


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

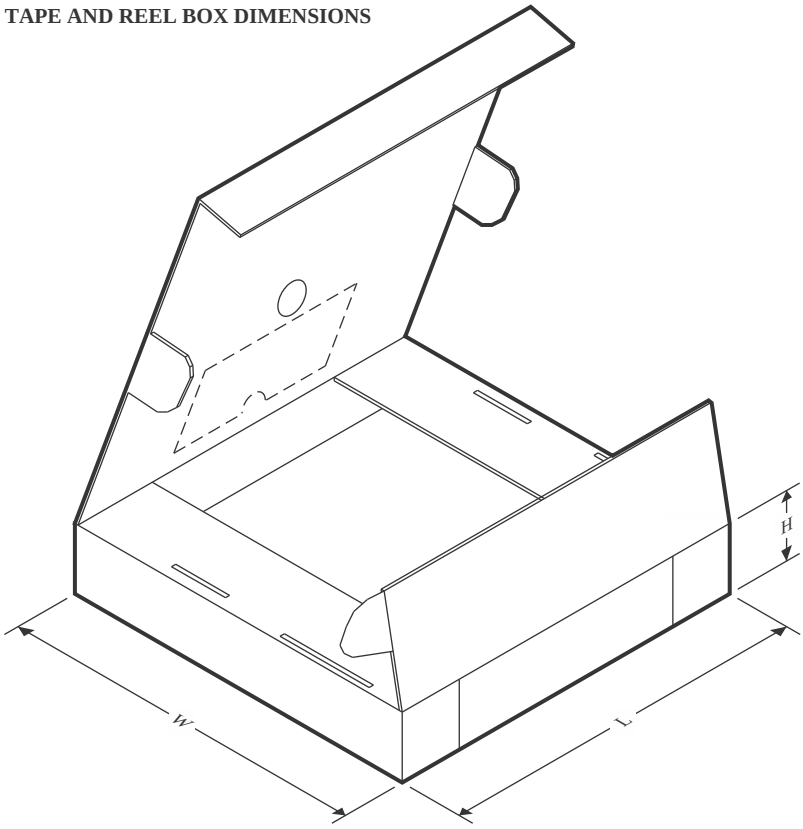
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB5461RGFRQ1	VQFN	RGF	40	3000	330.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1
TUSB5461RGFTQ1	VQFN	RGF	40	250	180.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB5461RGFRQ1	VQFN	RGF	40	3000	367.0	367.0	35.0
TUSB5461RGFTQ1	VQFN	RGF	40	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

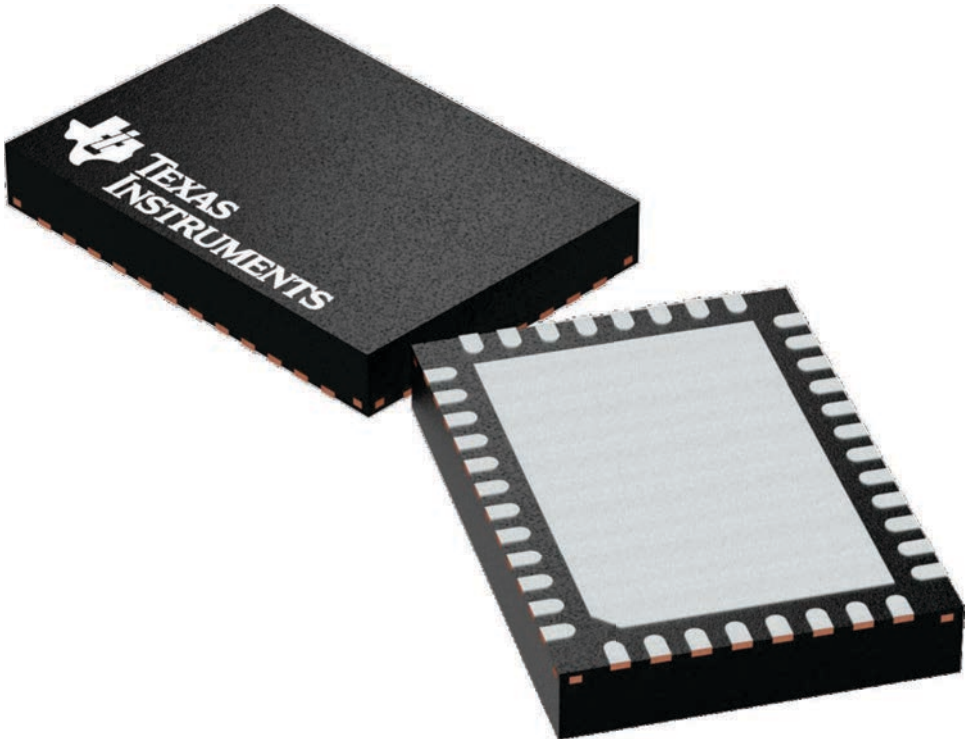
RGF 40

VQFN - 1 mm max height

5 x 7, 0.5 mm pitch

PLASTIC QUAD FLAT PACK- NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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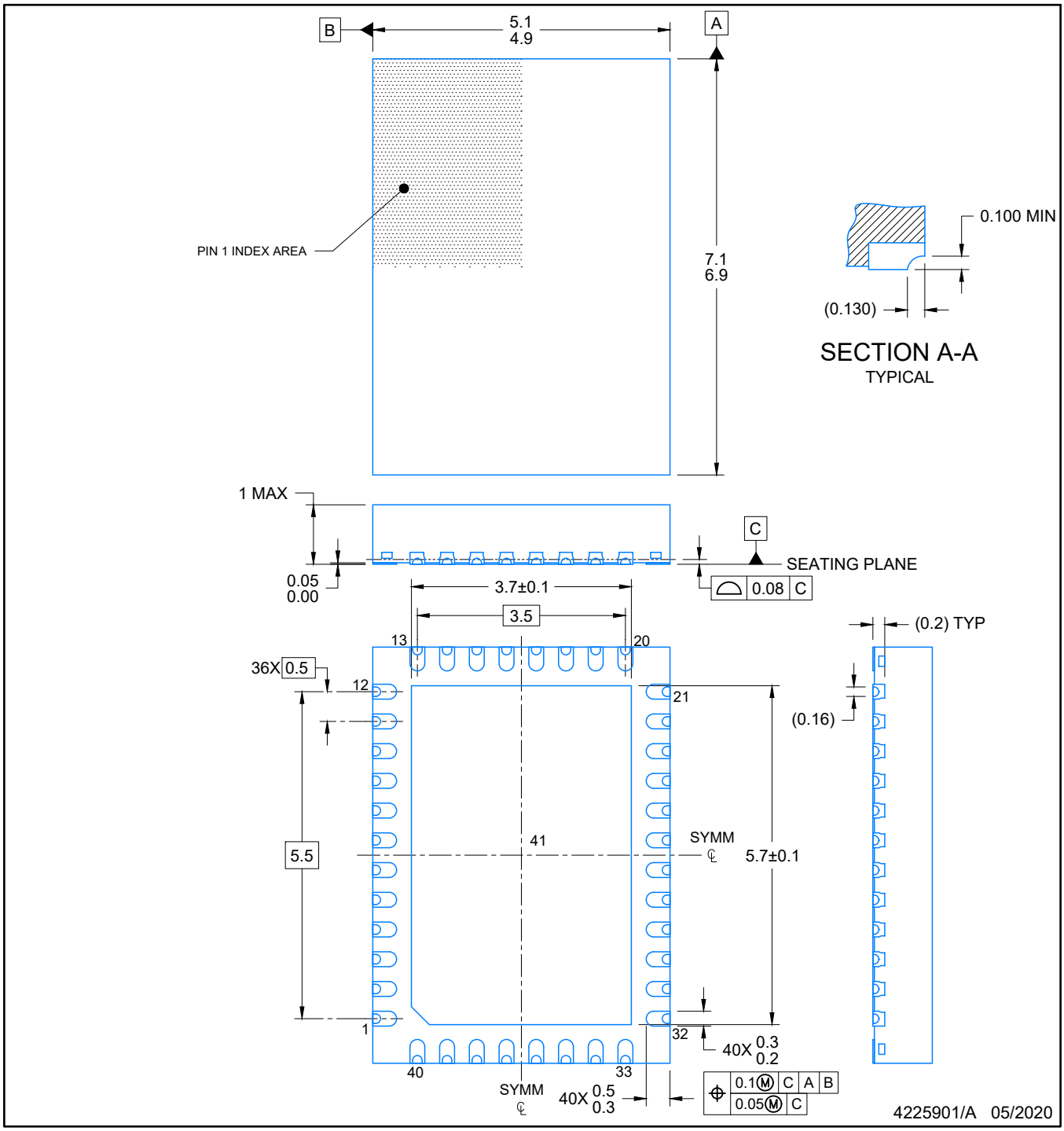
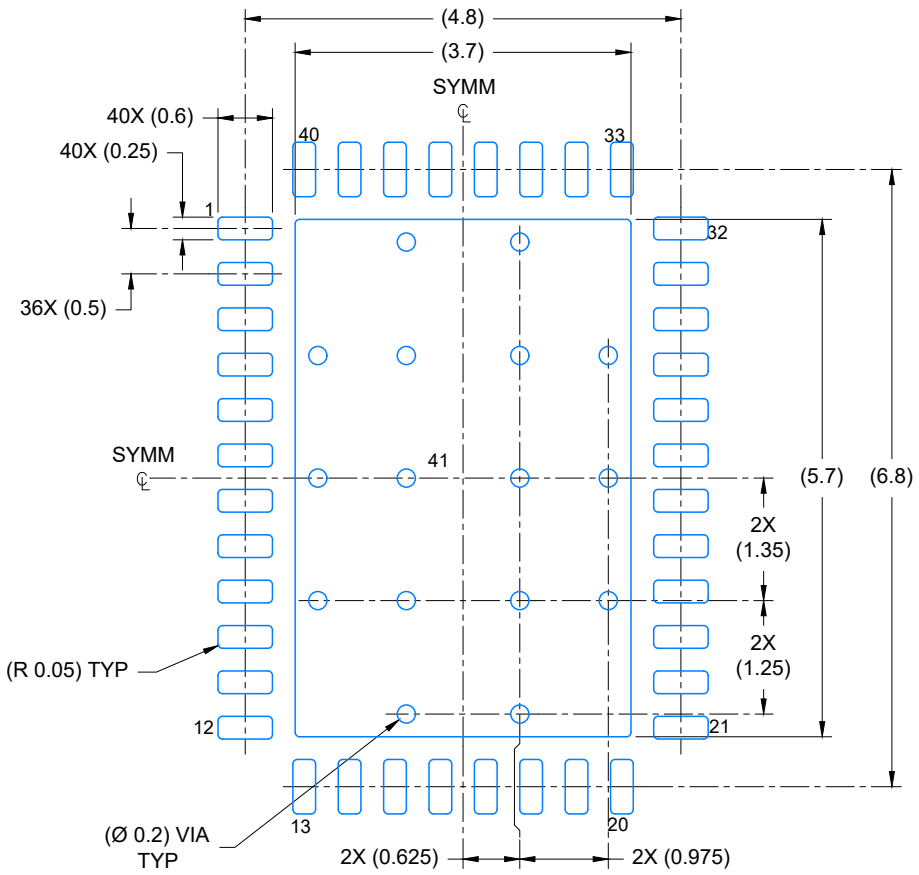
PLASTIC QUAD FLATPACK- NO LEAD

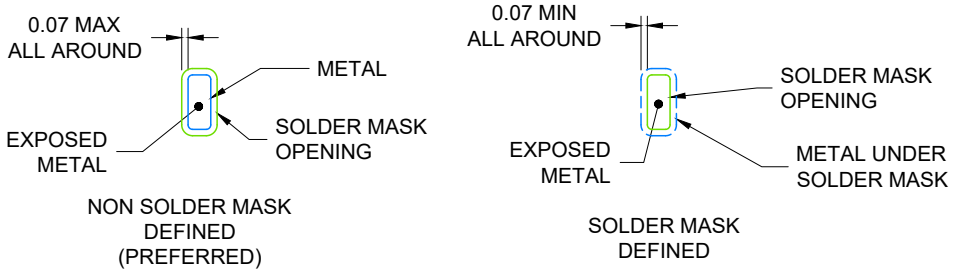


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

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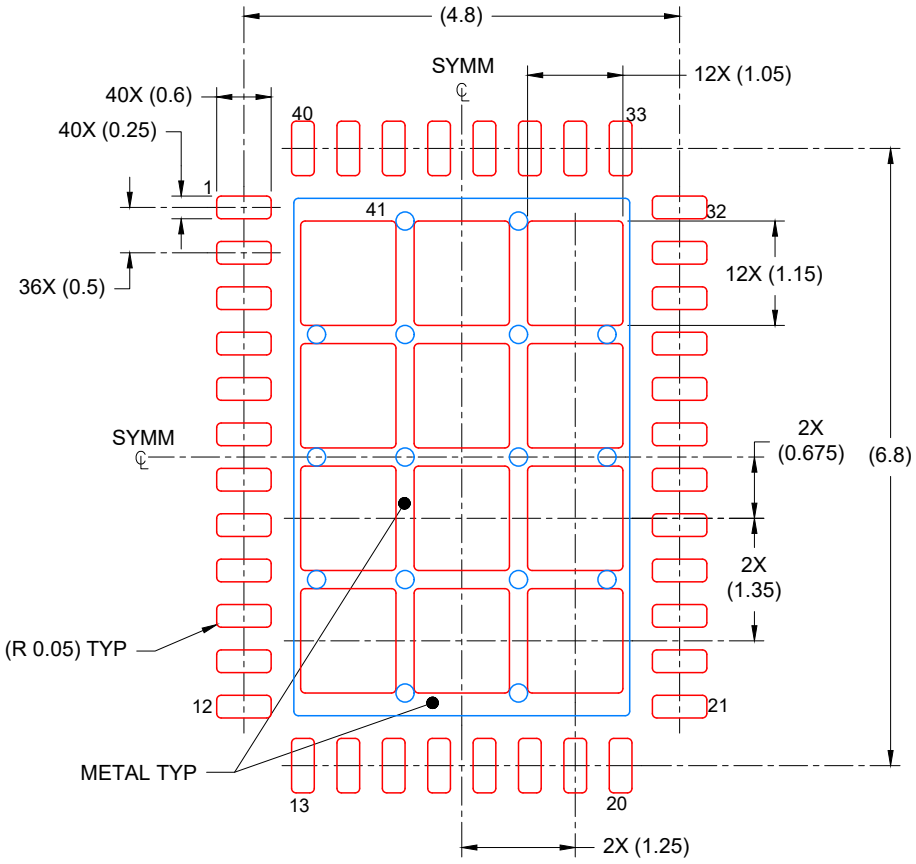
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
69% PRINTED COVERAGE BY AREA
SCALE: 12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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